A 1K SHADOW RAM FOR CIRCUMVENTION APPLICATIONS*

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Introduction

A 1K bit Shadow RAM has been developed for storage of critical data in a high transient radiation environment. The circuit includes a 1K bit (128 x 8) static RAM with two non-volatile (NV) shadows. The NV shadows are used to back-up the data in the static RAM allowing the circuit to be powered down during transient radiation without losing critical data. The following sections will describe the circuit's operation and characterization results.

Operational Description

The SA3766 Shadow RAM was designed for fabrication in a double level metal SNOS/CMOS process. A block diagram of the circuit is shown in Figure 1. The static RAM portion of the circuit operates in the standard fashion with either asynchronous or synchronous addressing (address latches are included for synchronous operation). The NV shadows cannot be accessed directly, but only through the static RAM. In addition to the static RAM and NV shadows, two single bit volatile flags with non-volatile backup are included. The flags are used to indicate which shadow should be used for recall and storage. The flag bit is bit 0 (D0) of the eight data bits (D0-D7). All the NV operations are accessed by the combination of the NV enable pin (NEB) being active and the value of the address inputs.

There are four basic NV commands; erase, store, recall, and load erase/store time. The erase and store commands initiate programming the shadow. Programming terminates when the on-chip timer times out. Erase is a preconditioning command which is required before the data can be copied into a shadow by the store command. The timer is a counter which is started at an initial count that is set by the load erase/store time commands. The erase and store times are stored in two 16-bit volatile latches so that they need to be entered only once after power-up. The static RAM can be accessed while an NV erase is executing but cannot be accessed during a store command. The NV commands can operate on either one or both shadows or one or both NV flags. The NV flags require only a store operation to change the data while the shadows require an erase followed by a store to change the data. The recall command copies the data from a shadow or NV flag back into the static RAM or volatile flag respectively.

Each bit of the non-volatile shadows consists of two SNOS transistors and two NMOS access transistors. The difference in the thresholds of two SNOS transistors determines if the bit is a one or a zero. Two SNOS transistors per bit improves

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the retention and reliability of the NV shadows. To program the SNOS transistors, a -5 volt supply is needed. The part includes a circuit to generate this voltage internally or it can be supplied externally.

Figure 1 Block Diagram

Memory Cell Design

This section will describe the structure and operation of the non-volatile (NV) Shadow RAM cell. The function of each transistor will be defined followed by a discussion of the cell's operation in its various modes. The modes are; static RAM, erase shadow, store shadow, and recall shadow. The schematic of the Shadow RAM memory cell is shown in Figure 2.

The cell consists of three memory elements: a static RAM cell and two non-volatile shadows. Eight transistors are used to form the static RAM cell instead of the usual six. Transistors MP1-MP4 and MN1-MN2 are configured as a standard static RAM cell, MN7-MN8 are included to allow the cell to be disconnected from the negative supply rail during recall operations. P-channel transistors (MP3-MP4) are used as access transistors so that the row select signal (WLB) operates at 0v - 5v logic levels. The use of P-channel access transistors also assists in equalizing the static RAM cell during the recall operation.

Transistors MP7-MP8 and MN9-MN10 function as switches controlling the transfer of data between the static RAM cell and the NV shadows. During static RAM and erase shadow operations the switches are off since no data is transferred between the static RAM and the shadows. The switches are on during the recall shadow and store shadow operations. This allows data to flow from shadow to static RAM cell during a recall and to flow the opposite direction during a store. The switch control signals (NT1, PT1) are generated by the control logic block and are tri-level signals (-5v, 0v, +5v).

Figure 2 Shadow RAM Memory Cell

Four transistors (two SNOS and two NMOS) form each of the two NV shadows: MNS1, MNS4, MN3, and MN6 are shadow 1; MNS2, MNS3, MN4, and MN5 are shadow 2. The n-channel transistors are used only during the recall operation to select which shadow is recalled. The data is stored in a shadow as a difference in threshold voltage (V_{th}) between the two SNOS transistors.

During static RAM operation the latch transistors (MN7, MN8) are turned on and the negative rail voltage (VSS1) is at 0 volts. The cell functions as a standard six transistor static RAM cell, with the row selected by the word line signal (WLB) and the column selected from the various bit-lines (BL, BLB) by the column circuit.

Test Results

Harris Semiconductor provided foundry service for the Shadow RAM in their H2SNOS process for design validation purposes. Electrical characterization and total dose radiation testing of these parts has been completed, transient radiation testing is in progress and will be completed in February, 1991.

Electrical characterization verified that the design was completely functional. The characteristics of the part are summarized below. The read access time of the static RAM was designed conservatively to ensure functionality of the first silicon. Future work will be directed at reducing this time, mainly through the reduction of the pre-charge time.

The circuit was designed to operate with a 1ms erase pulse and a 100 μ s store pulse. Since these erase/store cycles degrade the retention of the NV shadows, one of the characteristics measured is the retention after cycling. The design goal was for 24 hour retention at 125°C after 1e7 store/erase cycles. The current tester has limited the characterization to 1e4 cycles. After 1e4 cycles, the part has retained data for greater than 48 hours at 150°C. Another tester will be used to increase the cycling to the 1e7 level to verify that the design goals were achieved.

Electrical Characteristics

Parameter	Typical Value	Units
Read Access	125	nS
Iddq (active)	300	uA
Iddq (standby)	25	uA
IIL/IIH	<10	nA
IOL (@ 0.5v)	3.2	mA
IOH (@ 4.5v)	-2.5	mA
IOZ (@ 2.5v)	<20	nA
Endurance	>1e4	Cycles
Retention	>48	Hours (@ 150°C, 1e4 cycles)

Total dose radiation testing of the circuit has been completed using a Co-60 source at a dose rate of 100 rad(Si)/s. The initial dose was 300K rad(Si) with additional steps of 100K rad(Si) to a total of 1.2M Rad(Si). One of the two shadows was used to store data throughout the irradiation without re-programming, while the second shadow had various patterns programmed in and recalled at each irradiation step. This verified both data retention and the functionality of the circuit through the 1.2M rad(Si) radiation level.

Transient radiation testing was performed on the LINAC at White Sands Missile Range. The design goals were for a logic upset level of greater than 5e8 rad(Si)/s and a NV data loss level of greater than 1e12 rad(Si)/s. The LINAC testing measured a logic upset level of >5e8 rad(Si)/s. The maximum dose rate available on the LINAC is 1e11. The NV shadows didn't lose data when exposed to this transient radiation level. Further testing is planned on another system to verify retention through the 1e12 rad(Si)/s design goal.

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