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Using a Digital Signal Processor as a Data Stream Controller in Digital Subtraction Angiography

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Abstract

High speed, flexibility, and good arithmetic abilities make digital signal processors (DSP) a good choice as input/output controllers for real time applications. The DSP can be made to pre-process data in real time to reduce data volume, to open early windows on what is being acquired and to implement local servo loops. We present an example of a DSP as an input/output controller for a digital subtraction angiographic imaging system. The DSP pre-processes the raw data, reducing data volume by a factor of two, and is potentially capable of producing real-time subtracted images for immediate display.

I. INTRODUCTION

A real time process controller for a digital subtraction angiography system not only must operate at a high speed but must be capable of very fast arithmetic operations. A brief description of digital subtraction angiography and its data system requirements is presented below in order to more fully describe the use of the DSP.

The ability to image coronary arteries using a venous injection of a contrast agent (instead of an arterial injection) by means of a digital subtraction data system has undergone extensive development. This technique was developed to utilize

the available synchrotron sources of monochromatic, intense and well collimated x-ray beams at both the Stanford Synchrotron Radiation Laboratory (SSRL) and the National Synchrotron Light Source (NSLS) [1,2]. The collaboration of many scientists and physicians—from institutions including Stanford University, SSRL, NSLS, University of Tennessee, Lawrence Berkeley Laboratory (LBL) and others—has contributed to the development of x-ray beam optics to satisfy the medical requirements of the imaging systems. Many-element Si(Li) diode arrays have been developed by the Silicon Detector Group [3], and the detection data system [4] was developed by the Electronics Instrumentation Group; both groups are at LBL.

II. IMAGING SYSTEM DESCRIPTION

The imaging procedure requires two x-ray beams of slightly different energies to acquire two simultaneous images at either side of the iodine K edge at 33.17 keV. The absorption of x-rays increases by a factor of 6 across this edge. The logarithmic difference of the two images produces an image which is very sensitive to the iodine contrast agent (venous injection) and minimally sensitive to intervening tissue and bone. A schematic layout of the imaging system is shown in Fig. 1.

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Fig. 1 Schematic layout of imaging system

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Fig. 2 Typical recent 600 element angiogram

A pair of fan x-ray beams, 125 mm wide and 0.5 mm high, cross at the patient and diverge into a 600 element, dual-row Si(Li) detector which has a center-to-center spacing of 0.5 mm. Following an injection of contrast agent, an image is obtained

by moving the patient across the x-ray beam in a vertical stepping chair. For a typical imaging procedure around 35 ml of contrast agent is injected at an injection rate of 12 ml/s. A series of frames is then taken by moving the patient up and down at a chair speed of 12 cm/s. The exposure time for each line of the image is 4 msec. Therefore, a complete 250 line image requires 1 second to acquire. An additional 1 second is taken between frames to reverse the chair motion.

In 1989 the experimental equipment, a 600 element detector and data system were moved from SSRL and installed at NSLS as part of a new dedicated medical imaging suite. After several studies and improvements to the monochromator crystals, images similar to the one shown in Fig. 2 can be acquired at NSLS.

Images obtained so far clearly show that large portions of both the left anterior and the right coronary arteries can be visualized with this method. However, some additional improvement in image quality is desired before large groups of patients are studied. To this end, a 1200 element 0.25 mm square Si(Li) diode detector has been fabricated by the Silicon Detector Group at LBL. The 1200 element, 2 ms/line detector data system is nearing completion.

Fig. 3b Reciprocal counting technique timing diagram

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Fig. 3a Current-to-digital data circuit

III. DETECTOR DATA SYSTEM DESCRIPTION

The current in each of the 1200 Si(Li) detector diodes is proportional to the incident x-ray flux. The detector circuit must possess very high linearity and good resolution. Also, it must not degrade the diode current signal-to-noise ratio. In addition, digital data for each diode must be collected while data from the previous image line is transferred to the DSP during each 2 ms interval. This is accomplished by the use of 1200 input circuits. A typical one is shown in Fig. 3a.

The noise contribution of the input amplifiers is small when compared to the thermal noise due to the approximately 70 kilo-ohms inter-element surface impedance of the detector diode.

A large dynamic range is required since the incident x-ray flux is reduced dramatically when the beam traverses a bone. The three FET switches can be independently set for each pair of the 1200 diodes by the computer control system. In this manner, full scale current may be varied from 40 to 5000 nA. Additionally, the effect of diode bias current and input amplifier offset may be minimized by a computer controlled offset for each circuit.

Very high linearity and good resolution are required since the image intensity is determined by the logarithmic difference of the x-ray induced current between corresponding pairs of detector diodes. Voltage-to-frequency converters with less than 0.01% maximum non-linearity, 500 kHz full scale, are used to provide very high linearity [6]. The reciprocal counting technique is used to achieve resolution of 1 part in 40,000. See the digital timing diagram shown in Fig. 3b.

This technique and the circuitry have been previously described [4]. Both the M and V counters have tri-state output buffers to enable data collection while data from a previously acquired image line is transferred.

The 1200 current-to-digital data circuits have been designed and fabricated to fit on 100 printed circuit cards, 12 circuits to each card. The printed circuit cards have been designed to fit into commercially available VME extra deep D size modules (367 by 400 mm) and utilize the standard VME backplane.

Fig 4 Digital data gathering system, showing major subsystems and data flows

Each Si(Li) detector diode is connected to an input amplifier by up to 12 meters of twisted pair cabling, 12 per card, via the 26 pin front panel connector.

IV. DIGITAL DATA GATHERING SYSTEM

The digital data gathering system comprises four functional parts, interconnected as shown in Fig. 4. They are:

- 1) The beam-patient-detector array (see Fig. 1) whose output is current from each of the 1200 detector diodes.
- 2) Current-to-digital data circuits which convert the 1200 detector currents into M and V counts, which are converted to 16-bit digital image intensity values by the DSP for each scan line. The hardware can individually set gain and offsets for each circuit. In order to measure and calibrate system performance, an adjustable calibration current can be applied to every circuit input simultaneously.
- 3) The digital signal processor and a digital interface to provide phase-locked timing control and an addressing tree for selecting individual input circuits.
- 4) Lastly, of course, output pixel data files must be provided for the imaging software to produce interpretable pictorial results.

Components of the digital data gathering system are shown in Fig. 5.

Fig. 5 Digital data gathering system components

The DSP processor is an AT&T DSP32C, 50 MHz, 32 bit processor board in an AT host computer [7]. The cable connection to the DSP interface may be up to 4 meters long. A commercially defined digital protocol, the DSPLINK [7], which is capable of up to 10 megabyte per second data transfers is used. Each current-to-digital data circuit has a

unique hardware address. Addresses are decoded and asserted by the DSP interface. A DSP read of each address will gate V or M data back from each of the sub-racks via the DSP interface. A DSP write to each circuit address will load individual 8-bit offset current adjustment DACs and set individual gains for each of the 1200 input circuits.

In addition, other addresses are assigned to several global system functions. One such global function is the calibrate current source. A 16 bit data word written into this address is loaded into a 16-bit DAC located on the first sub-rack interface card. The DAC output is distributed to all sub-racks and every input as a calibration test current. Timing and control signals, including the scan-line timing gate (Fig. 3b), are generated by a phase-locked clock synchronized to the 60 Hz power line, and originate in the DSP interface.

Note that while there are five individual data returns from the sub-racks, the DSP interface sends control signals to all of the five sub-racks in parallel. Each sub-rack responds to two addresses, one unique and one common for all of the sub-racks. Consequently, each input circuit may be uniquely addressed to set up individual circuit gains and offsets. The common sub-rack address permits the simultaneous selection of one circuit in each sub-rack. Current data from each sub-rack is simultaneously asserted onto the five returning data cables. Therefore, in order to collect one line of data (1200 pixels), only 480 addresses need be asserted. Sixteen-bit data from the five sub-racks may be read two words at a time by a single 32-bit DSP read instruction. Each pair of the 2400 counter values (two per pixel) is put into a memory array in the DSP for further processing. For example, the DSP processor program divides and normalizes incoming data, but is also capable of additional operations such as real time image subtraction, which will produce a fast preliminary image for help in system setup.

The DSP-based controller is the current implementation of what was originally a hard-wired controller for the 600 element detector, and is much more flexible than the previous controller. If a new angiography system with a different-sized detector or with different electronics becomes available, the DSP can readily be made to adapt by simply updating its software, thus avoiding any controller hardware redesign.

This system is the first one of its kind that we have designed. As such, use of the DSP expedites testing components of the system as it is being built and assembled. For example, each circuit generates two counts, the ratio of which is a value proportional to detector current. To localize a fault, knowing which count is in error can eliminate half the suspects. The DSP, unlike the previous hard-wired controller, makes this information readily available. As another example of the utility and power of the DSP controller, the hardware delay time that occurs between addressing an input circuit and reading its data value was marginally short. The problem was readily fixed by simply adding two NOPs to the DSP code.

A primitive software package was developed to facilitate debugging this system. It contains operator callable functions such as initialize system, set system parameters (gains,

offsets, chair step rate, and calibrate current), or select an input circuit to read raw or computed data.

Many of these primitives will be used by the operational system software to acquire image data synchronized with the vertical stepping chair. In addition to these primitive functions, a few meta-functions have been developed. One such meta-function scans each circuit output to determine its output at extreme values of offset. Then each circuit offset is computed and set to produce a similar output data value for all the circuits. The offset data file for each circuit is written to a disk file which may then be used by the operational software to download offsets into the digital data gathering system.

V. CONCLUSIONS AND FUTURE CONSIDERATIONS

The use of a DSP processor as a programmable input/output controller for a real time application has been described above. The demonstrated utility and power of this technique has enabled us to build, test and debug a 1200 element system for less than 1.5 times the cost of our previous 600 element system.

Not only is the DSP capable of adjusting to permutations of the present system, it may be used to control a diverse array of other systems. For example, we use it to control a tunneling microscope, an atomic force microscope, and have proposed its use as a controller for a 128 channel data-readout chip in an x-ray fluorescence system. The same device could be an in-line real-time data autocorrelator in a system detecting the fluorescence of single molecules.

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