RADIAN
CORPORATION

MASTER

DART II DOCUMENTATION

VOLUME III

APPENDICES

1 OCTOBER 1979

DOCUMENT 098A0069-001, Revision -

250 2484

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APPENDIX A

ADJUSTMENT AND CALIBRATION PROCEDURES

1. Power Supply Adjustment Procedure
2. ADC Calibration Procedure
3. Analog Multiplexer Calibration Procedure

POWER SUPPLY ADJUSTMENT PROCEDURE

CAUTION

Use extreme caution while performing maintenance on or near the power supply. Exposed 117 VAC is present on the power interconnect board. Batteries are high current, sealed lead acid type. Care should be taken to avoid shorting their terminals. Disconnect the batteries by unplugging P44 and P45 if the DART is to be deliberately left without an AC power source for more than eight hours.

- I. Five volt power supply EMA-5/6 CC voltage and overvoltage protection adjustment:
 - A. Equipment required.
 1. DC Voltmeter, Accuracy $\pm 3\%$.
 2. Insulated alignment tool.
 - B. Connect the DC voltmeter to the power supply output terminals. Adjust the voltage adjustment potentiometer so that the meter reads 5.4 volts.
 - C. Overvoltage protector adjustment. Under normal circumstances the overvoltage protector should not require adjustment; however, if adjustment is required, the procedure is as follows:
 1. Turn the AC power off.
 2. Unplug P36 from the power interconnect board.
 3. Connect the DC voltmeter to the output terminals of the power supply.
 4. Adjust the overvoltage adjustment potentiometer fully clockwise.
 5. Turn the AC power on.

6. Adjust the voltage adjustment potentiometer on the power supply for a reading of 6.5 volts.
 7. Slowly adjust the overvoltage potentiometer counterclockwise until the output of the power supply suddenly drops to zero.
 8. Turn the AC power off.
 9. Adjust the voltage adjustment potentiometer on the power supply counterclockwise.
 10. Turn the AC power on. If the output reads zero, repeat steps 8 and 9. If power supply appears to be operating correctly, slowly adjust the voltage upward until the overvoltage protector trips. It should trip between 6.2 and 6.5 volts. If it fails to trip correctly, repeat steps 6 through 10. Turn the AC power off.
 11. Adjust the voltage adjustment potentiometer of the power supply counterclockwise. Turn the AC power on. Adjust the power supply voltage potentiometer for an output of 5.4 volts. Turn the AC power off. Reconnect P36 to the power interconnect board.
- II. Fifteen volt power supply ETA-12/15B voltage and over-voltage protector adjustment:
- A. Equipment Required.
 1. DC voltmeter, Accuracy $\pm 3\%$
 2. Insulated alignment tool.
 - B. Connect the DC voltmeter to the power supply output terminals. Adjust the voltage adjustment potentiometer until the meter reads 15.0 volts. Repeat the procedure for the negative supply.
 - C. Overvoltage protector adjustment:

1. Turn the AC power off.
2. Unplug P38 from the power interconnect board.
3. Connect the DC voltmeter to the power supply terminals.
4. Adjust the overvoltage adjustment potentiometer fully clockwise.
5. Turn the AC power on.
6. Adjust the voltage adjustment potentiometer on the power supply for a reading of 17.0 volts.
7. Slowly adjust the overvoltage potentiometer counterclockwise until the output of the power supply suddenly drops to zero.
8. Turn the AC power off.
9. Adjust the voltage adjustment potentiometer on power supply counterclockwise.
10. Turn the AC power on. If the power supply reads zero, repeat steps 8 and 9. If the power supply appears to be operating correctly, slowly adjust the voltage upward until the overvoltage protector trips. It should trip between 16.7 and 17.0 volts. If it fails to trip correctly, repeat steps 7 through 10. Turn the AC power off.
11. Adjust the voltage adjustment potentiometer of the power supply counterclockwise. Turn the AC power on. Adjust the power supply voltage potentiometer for an output of 15.0 volts. Repeat steps 6 through 11 for the negative supply.
12. Reconnect P38 to the power interconnect board.

III. Twenty-four volt power supply EMA-18/24B.

A. Equipment Required:

1. DC voltmeter, Accuracy $\pm 3\%$

2. Insulated alignment tool.

- B. Connect the DC voltmeter to the power supply output terminals. Adjust the voltage adjustment potentiometer so that the meter reads 24.0 volts.

ADC CALIBRATION PROCEDURE

A. Equipment Required:

1. Adjustable DC voltage reference source with the following specifications:
 - a. Maximum output voltage of +10.0000 volts with a resolution of one hundred microvolts.
 - b. Accuracy of 0.1% of setting
2. Test leads.

B. Procedure:

1. Remove the ADC board from the DART. Disconnect the jumper connecting pins 2 and 12 of U1.
2. Connect low side of the voltage source of U1 Pin 8. Connect high side of the voltage source to U1 pin 12.
3. Place the ADC board on an extender board in the ADC board position.
4. Allow the equipment to warm up for 15 minutes.
5. Set the front panel gain switch to the one hundred millivolt position.
6. Set the output of the voltage source to -9.9951 volts.
7. Adjust zero adjustment potentiometer, R12, for a reading of -2.047 on front panel display.
8. Set the output of the voltage source to 9.9902 volts.

9. Adjust the gain adjustment potentiometer, R13, for a reading of 2.046 on front panel display.
10. Repeat steps 6 through 9.
11. Remove the leads from the voltage source and short them together. The front panel display should read 0.00±1 count.
12. Remove the ADC board and extender card. Disconnect the test leads from U1 pins 8 and 12. Reconnect the jumper between U2 pins 2 and 12.
13. Place the ADC board back in the unit.

ANALOG MULTIPLEXER CALIBRATION PROCEDURE

A. Equipment Required:

1. DC voltage source with the following specifications:
 - a. Maximum output voltage of ± 10.0000 volts with a resolution of one hundred microvolts.
 - b. Accuracy of 0.1% of setting.
2. Test leads.
3. Calibrated ADC board.

B. Procedure:

1. Allow the equipment to warm up 15 minutes.
2. Connect the voltage source output to any pair of analog inputs on the DART II back panel, observing polarity markings. Set thumbwheel channel select switches to correspond to the channel to which the voltage source is connected.
3. Set the gain select switch to the ± 10 volt position. Use the calibration table to perform the adjustments on the analog multiplexer card. Repeat the adjustments, if necessary, until the unit falls within limits specified in the calibration table.
4. Check the tracking on each voltage range at several points between zero and one hundred percent overrange, with the exception of the 10 volt range which does not have the overrange capability. Check tracking on the ± 10 volt range up to ± 10 volts.

If all of the ranges do not track correctly, check the calibration of the ADC board. If a particular range does not track correctly, repeat the zero and span adjustments for that range.

ANALOG MULTIPLEXER CALIBRATION TABLE

GAIN SELECT SWITCH SETTING	VOLTAGE SOURCE OUTPUT		ADJUSTMENT BEING PERFORMED	POTENTIOMETER	FRONT PANEL DISPLAY LIMITS
10 V	0.00	V	10 V Zero	R56	-0.01 +0.01
10 V	10.00	V	10 V Span	R51	+9.99 +10.01
5 V	0.000	V	5 V Zero	R50	-0.005 +0.005
5 V	5.000	V	5 V Span	R45	+4.995 +5.005
1 V	0.000	V	1 V Zero	R44	-0.001 +0.001
1 V	1.000	V	1 V Span	R39	+0.999 +1.001
100 MV	0.000	V	100 MV Zero	R38	-0.0001 +0.0001
100 MV	0.1000	V	100 MV Span	R33	+0.0999 +0.1001
10 MV	0.00000	V	10 MV Zero	R32	-0.00001 +0.00001
10 MV	0.01000	V	10 MV Span	R27	+0.00999 +0.01001

A-10

APPENDIX B

MOTHER BOARD SIGNATURE LIST

Drawing 500D3269-001

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	-	RELEASED PER DAN 333	11 MAR 79	WDAK

PORT F P			
J3A			
50	FPSTRB-	33	GND
49		32	PWRES-
48	BREAD	31	
47		30	
46	BD7-	29	BD6-
45	BD5-	28	BD4-
44	BD3-	27	BD2-
43	BD1-	26	BD0-
42		25	
41		24	
40		23	FPSTDEC-
39	FPNEM-	22	FPROMD-
38	BVMA02-	21	FPURW-
37	FPWRT-	20	FPHALT-
36	BKCLK-	19	B02-
35		18	B1-
34	B15	17	B0-
		16	BAG-
		15	BA7-
		14	BA2-
		13	BA3-
		12	BA4-
		11	BA5-
		10	BA6-
		9	BA7-
		8	BA8-
		7	BA9-
		6	BA10-
		5	BA11-
		4	BA12-
		3	BA13-
		2	BA14-
		1	BA15-

FRONT

J9A		J9A	
50	49	50	49
48	47	48	47
46	45	46	45
44	43	44	43
42	41	42	41
40	39	40	39
38	37	38	37
36	35	36	35
34	33	34	33
32	31	32	31
30	29	30	29
28	27	28	27
26	25	26	25
24	23	24	23
22	21	22	21
20	19	20	19
18	17	18	17
16	15	16	15
14	13	14	13
12	11	12	11
10	9	10	9
8	7	8	7
6	5	6	5
4	3	4	3
2	1	2	1

J7A	
34 201	33 208
32 104	31 202
30 102	29 204
28 108	21
26 101	25
24 FPA2	23
22 MPKCLH	21
20 FPA1	19
18 MS1	11
16 MSQ	15
14 STBR	13
12 MS2	11 TSET
10 FPA0	9 SETMIN
8	7 SETMIN
6	5 SETHRS
4	3 SETDAY
2 END	1

ADC, TH WH SWITCH					
ISA					
7	TW21-	8	TW20-	9	GND
4	TW10-	5	TW11-	6	TW12-
1	TW02-	2	TW00-	3	TW01-

ADC DISP		
150A		
7 SIOV-	8 SIOV+	9 FPST
4 55V-	5 55V+	6 FPCLN
1 SIOV-	2 FPCLN	3 FP5GN-

DVC4FLPY TO EP			
J55A			
7 PCL-	8 GND	9 #5	
4 PLS-	5	6 FLPY5-	
1 FLPYON-	2 TTYON-	3 TTY5-	

ADC DISF PWR	
J52A	
1	+5
2	GND
3	GND

SIC TO STATUS LTS					
J56A					
1	583-	8	587-	4	15
4	582-	5	580-	6	586-
1	581-	2	584-	3	585-

J47A	
1	45
2	GND
3	GND

156A 4	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	
156A 7	PARTS LIST				
156A-2	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE		CONTRACT NO		RADIAN CORPORATION P.O. BOX 5000/JENKINS TEXAS 75260
156A-3	FRACTIONS DECIMALS ANGLES + = 020 XX = 010 ± 30° XXX = 005		APPROVALS DATE		
156A 6	MATERIAL		DRAWN <i>John Smith</i> 7/20/77 CHECKED <i>R.C. Brown</i> 7/20/77 <i>W. Kautz</i> 7/20/77		
156A 8	FINISH				MOTHER BOARD WIRE LIST
182D0317	750A0042			SIZE D	CODE IDENT NO 29913
NEXT ASSY	USED ON			DRAWING NO 500D3269-C01	
APPLICATION		DO NOT SCALE DRAWING		SCALE NONE	
				SHEET 1 OF 2	

APPENDIX C
SCHEMATIC DIAGRAMS

Schematic Diagrams

<u>Title</u>	<u>Drawing No.</u>
CPU	500D3201-001
Memory-16KX8	500D3205-001
APU	500C3209-001
Async. Interface	500C3213-001
P.S. Interconnect	500C3217-001
Floppy Disk Cont.	500D3225-001
Status Input Cont.	500D3229-001
Device Controller	500D3233-001
Battery Clock	500D3241-001
Battery Clock Display	500D3245-001
A/D Converter	500C3249-001
Analog Multiplexer	500D3253-001
A/D Display	500D3257-001
A/D Display Logic	500D3261-001
Busy/Done	500B3265-001
Mag. Tape Interface	500D3273-001
I/O Controller	500D3277-001
ROM/RAM	500D3301-001
Analog MPX.Exp.	500D3306-001
Front Panel	500C3349-001
Bus terminator	500A3352-001

REVISIONS		DATE	APPROVED
ZONE	STR		
RELEASED PER DRN 333		11 MAY 78	720K

CH20-CH37		CH00-CH17	
J20A & J18A	J21A & J19A	J21A & J19A	J21A & J19A
34 CH37- 35 CH37+	34 CH17- 35 CH17+	34 CH17- 35 CH17+	34 CH17- 35 CH17+
32 CH36- 33 CH36+	32 CH16- 33 CH16+	32 CH16- 33 CH16+	32 CH16- 33 CH16+
30 CH35- 31 CH35+	30 CH15- 31 CH15+	30 CH15- 31 CH15+	30 CH15- 31 CH15+
28 CH34- 29 CH34+	28 CH14- 29 CH14+	28 CH14- 29 CH14+	28 CH14- 29 CH14+
26 CH33- 27 CH33+	26 CH13- 27 CH13+	26 CH13- 27 CH13+	26 CH13- 27 CH13+
24 CH32- 25 CH32+	24 CH12- 25 CH12+	24 CH12- 25 CH12+	24 CH12- 25 CH12+
22 CH31- 23 CH31+	22 CH11- 23 CH11+	22 CH11- 23 CH11+	22 CH11- 23 CH11+
20 CH30- 21 CH30+	20 CH10- 21 CH10+	20 CH10- 21 CH10+	20 CH10- 21 CH10+
18 CH29- 19 CH29+	18 CH09- 19 CH09+	18 CH09- 19 CH09+	18 CH09- 19 CH09+
16 CH28- 17 CH28+	16 CH08- 17 CH08+	16 CH08- 17 CH08+	16 CH08- 17 CH08+
14 CH27- 15 CH27+	14 CH07- 15 CH07+	14 CH07- 15 CH07+	14 CH07- 15 CH07+
12 CH26- 13 CH26+	12 CH06- 13 CH06+	12 CH06- 13 CH06+	12 CH06- 13 CH06+
10 CH25- 11 CH25+	10 CH05- 11 CH05+	10 CH05- 11 CH05+	10 CH05- 11 CH05+
8 CH24- 9 CH24+	8 CH04- 9 CH04+	8 CH04- 9 CH04+	8 CH04- 9 CH04+
6 CH23- 7 CH23+	6 CH03- 7 CH03+	6 CH03- 7 CH03+	6 CH03- 7 CH03+
4 CH22- 5 CH22+	4 CH02- 5 CH02+	4 CH02- 5 CH02+	4 CH02- 5 CH02+
2 AG	2 AG	2 AG	2 AG

PWR		E1REF		BP PWR	
J22A	J23A	J22A	J23A	J24A	J24A
1 RFTX1	1 RNFALL-	1 RFTX1	1 RNFALL-	1 GND	1 GND
2 RFTX2	2 EXTPLS	2 RFTX2	2 EXTPLS	2 GND	2 GND
3 GND	3 GND	3 GND	3 GND	3 +5	3 +5
				4 +5	4 +5
				5 -15	5 -15

PWR		J22A		J23A	
7 AG	8 GND	7 AG	8 GND	9 GND	9 GND
4 GND	5 -15	4 GND	5 -15	6 +5	6 +5
1 +5	2 +5	1 +5	2 +5	3 +24	3 +24

J22A		J23A	
1 AG	2 GND	1 AG	2 GND
3 GND	4 -15	3 GND	4 -15
5 +5	6 +5	5 +5	6 +5
7 +24	8 +24	7 +24	8 +24

REAR HALF		PARTS LIST	
QTY	CODE	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS DECIMALS ANGLES .XX ± .010 .XX ± .005 .XX ± .005			
DRAWN		APPROVALS	DATE
CHECKED		DATE	DATE
TITLED		MOTHER BOARD WIRE LIST	
SIZE		CODE/IDENT NO	DRAWING NO
D 29913		50003269-001	
SCALE NONE		SHEET 2 OF 2

REVISIONS			
DATE	DESCRIPTION	DATE	APPROVED
20 APR 79	RELEASED PER DRN 333		
20 MAY 79	A - REVISED PER E.O. 2227

QTY REQD		CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	
				PARTS LIST	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .020 ± .010 ± 30° ± .005 ± .005				CONTRACT NO.
APPROVALS	
				DATE	
				DRAWN	
				CHECKED	
				DATE	
				DESIGNED	
				DATE	
782C0300				750A0042	
NEXT ASSY				USED ON	
APPLICATION				DO NOT SCALE DRAWING	
				RADIANT CORPORATION 1000 604/AVTH, TEL: 617/884	
				DIAG, SCHEM, CPU	
SIZE				CODE IDENT NO. DRAWING NO.	
D				29913 50003201-001	
SCALE				SHEET 2 OF 2

D

C

B

A

500C3209-001

B

A

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
-	-	RELEASED PER DRN 333	20 APR 79	71AR
A	-	REVISED PER E OI 2401	10 SEP 79	71AR

QTY REQD		CODE IDENT		PART OR IDENTIFYING NO		NOMENCLATURE OR DESCRIPTION	
PARTS LIST							
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES # ± .020 XX = .010 ± 30" XXX = .005				CONTRACT NO			
				APPROVALS			
MATERIAL				DRAWN		DATE	
				CHECKED		DATE	
FINISH				DATE		DATE	
				DATE		DATE	
DO NOT SCALE DRAWING				SCALE			

RADIAN CORPORATION P.O. BOX 9848/AUSTIN TEXAS 78766		
DIA. SCHEM., ASYNCHRONOUS INTERFACE		
SIZE	CODE IDENT NO	DRAWING NO
C	29913	500C3213-001
SHEET 1 OF 3		

RADIAN CORPORATION
P.O. BOX 9948/AUSTIN TEXAS 78768

DIA. SCHEM., ASYNCHRONOUS
INTERFACE

29913 500C3213-001

D
C
B
A

110 BAUD OPERATION REQUIRES BOTH 110 AND 150 SWITCHES TO BE CLOSED

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		RELEASED PER DRN. 333	18 APR 79	REU
A		REVISED PER E.O. 2401	10 SEP 79	714K

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION
PARTS LIST			
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE:		CONTRACT NO.	
FRACTIONS	DECIMALS	ANGLES	
- .020	XX = ± .010	± 30'	
	XXX = ± .005		
MATERIAL		APPROVALS	
FINISH		DATE	
782CD303		SCOTT COLEMAN 6 APR 79	
750A0042		18 APR 79	
NEXT ASSY		USED ON	
APPLICATION		DO NOT SCALE DRAWING	
		RADIANT CORPORATION P.O. BOX 9848/MUSTIN, TEXAS 75708	
		DIAG. SCHEM., ASYNCHRONOUS INTERFACE	
SIZE	CODE IDENT NO.	DRAWING NO.	
C	29913	500C3213-001	
SCALE		SHEET 2 OF 3	

D
C
B
A

500C3213-001

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	-	RELEASED PER DRN 333	18 APR 79	
A		REVISED PER E.O. 2401	10 SEP 79	W.D.K.

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	
PARTS LIST			RADIANT CORPORATION P.O. BOX 2048/AUSTIN TEXAS 78768	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES = ± .020 XX = ± .010 = 30° XXX = ± .005		CONTRACT NO		DIAG SCHEM ASYNCHRONOUS INTERFACE
MATERIAL		APPROVALS	DATE	
FINISH		DRAWN <i>DJ Barnes</i>	4-6-79	
		CHECKED <i>DJ Barnes</i>	18 APR 79	
782C0303 750A0042				SIZE CODE IDENT NO DRAWING NO
NEXT ASSY USED ON				C 29913 500C3213-001
APPLICATION		DO NOT SCALE DRAWING		SCALE SHEET 3 OF 3

REVISIONS				
ZONE	LTB	DESCRIPTION	DATE	APPROVED
-	-	RELEASED PER DSN 333	22 APR 79	ADD
A	-	REVISED PER E.O. 2403	10 SEP 79	HOK

QTY REQD		CODE IDENT		PART OR IDENTIFYING NO		NOMENCLATURE OR DESCRIPTION		
PARTS LIST								
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES ± .020 .001 ± .010 ± .005				CONTRACT NO		RADIAN CORPORATION P O BOX 9999 WILSON TEXAS 75070		
MATERIAL				APPROVALS				DATE
FINISH				DRAWN <i>[Signature]</i>				4-12-79
				CHECKED <i>[Signature]</i>				2-2-80
				DATE				2-2-80
DO NOT SCALE DRAWING				SIZE		CODE IDENT NO	DRAWING NO	
				D		29913	500D3233-001	
				SCALE		SHEET 1 of 2		

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
		RELEASED PER DRN 333	20 APR 79	DRN
A		REVISED PER E.O. 2403	10 SEP 79	BAK

QTY	CODE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION
PARTS LIST			
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES FRACTIONS DECIMALS ANGLES " = .000 .001 = .001 .002 = .002 .003 = .003			
CONTRACT NO.		RADIANT CORPORATION P.O. BOX 1000, MOUNTAIN VIEW, TEXAS 75080	
APPROVALS		DATE	
DESIGNED BY: [Signature]		20 APR 79	
CHECKED BY: [Signature]		20 APR 79	
MATERIAL		SCALE	
FINISH		SCALE	
APPLICATION		DO NOT SCALE DRAWING	
NEXT ASSY USED ON		SCALE	
782C0308 750A0042		D 29913 50003233-001	
SHEET 2 OF 2		SHEET 2 OF 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
-	-	RELEASED PER DRN 333	10 APR 79	700
A	-	REVISED PER E.O. 2404	18 SEP 79	700

QTY	CODE	PART OR IDENTIFYING NO	DESCRIPTION
PARTS LIST			
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .000 ± .010 30 30K 000			
MATERIAL		CONTRACT NO.	DATE
FINISH		APPROVALS	DATE
NEXT ASSY USED ON		CHECKED BY	DATE
APPLICATION		DO NOT SCALE DRAWING	
RADIAN CORPORATION P.O. BOX 6049, LITTLE ROCK, AR 72206			
DIAG. SCHEM., BATTERY OPERATED CLOCK			
SIZE	CODE IDENT NO	DRAWING NO	
D	29913	500D3241-001	
SCALE		SHEET 3 OF 3

QTY REQD		CODE IDENT	PART OR IDENTIFYING NO		NOMENCLATURE OR DESCRIPTION		
					PARTS LIST		
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES = ± .020 .001 ± .010 ± 30 XXX ± .005			CONTRACT NO 1		RADIAN CORPORATION P.O. BOX 9940/AUSTIN, TEXAS 78768		
MATERIAL			APPROVALS DESIGNED <i>[Signature]</i> DATE 17 APR 79 CHECKED <i>[Signature]</i> DATE 10 APR 79 9.2 <i>[Signature]</i> DATE 2 APR 79				
FINISH					DIAG SCHEM. BATTERY CLOCK DISPLAY		
782C03H		750A0042		SAC D		CODE/IDENT NO 29913	DRAWING NO 500D3245-001
NEXT ASSY		USED ON		SCALE —		SHEET OF	
APPLICATION		DO NOT SCALE DRAWING					

500C3249-001 REV. -

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
-	-	RELEASED PER DRN 1333	2 MAR 79	RCB
A	A	REVISED PER E.O. 2234	17 MAY 79	RCB
B	B	REVISED PER E.O. 2234	2 OCT 79	RCB

* 1% METAL FILM
ETCH FROM PIN 22-AS SHORT AS
POSSIBLE

- NOTES 1 FILTER CAPACITOR ON EACH OF THE VOLTAGES
SHOULD BE LOCATED PHYSICALLY CLOSE TO A/D
2 IN APPLICATIONS WHERE SAMPLE-HOLD (U1)
IS NOT REQUIRED, DELETE R6, R7, R14, U1 AND
AND C9; JUMPER PINS 2 AND 7 ON THE
SOCKET FOR U1.

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION
PARTS LIST			
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES = ± 020 .XX = ± 010 ± 30° XXX = ± 005		CONTRACT NO	
MATERIAL		APPROVALS DATE	
FINISH		DRAWN <i>John Samford</i> DEC 6, 78	
		CHECKED <i>John Samford</i> 2 MAR 79	
		APPROVED <i>D. L. Patton</i> 02 MAR 79	
782C0312 75NAD042		SIZE CODE IDENT NO DRAWING NO	
NEXT ASSY USED ON		C 29913 500C3249-001	
APPLICATION		SCALE NONE SHEET 1 OF 2	
DO NOT SCALE DRAWING

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE
—	—	RELEASED PER ORN 333	20 APR 79
A	—	REVISED PER L.O. 2236	12 JUN 79
B	—	REVISED PER E.O. 2299	166 8 79

RESISTOR VALUES DEPENDENT ON REQUIREMENT

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	
PARTS LIST				
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE			CONTRACT NO.	
FRACTIONS DECIMALS ANGLES			APPROVALS DATE	
X ± .020 KK ± .010 ° ± 30°			DRAWN 10/16/79	
MATERIAL			CHECKED 10/16/79	
FINISH			DATE 10/16/79	
DO NOT SCALE DRAWING			SIZE CODE IDENT NO DRAWING NO	
			D 29913 500D3253-001	
			SCALE -/- SHEET 1 of 2	
RADIANT CORPORATION P O BOX 8948/MIAMI TEL:305/363-1000				
DIAG SCHEM ANALOG MULTIPLEXER				

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE
-	-	RELEASED PER DRN 333	10 APR 79
A	-	REVISED PER E.O. 2256	12 JUN 79
B	-	REVISED PER E.O. 2299	18 FEB 79

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CONTRACT NO		DATE	
78RC0313		10 APR 79	
750A0042		12 JUN 79	
NEXT ASST		USED ON	
RADIANT CORPORATION		P.O. BOX 1048/1050 TOLSON, MD	
DIAG SCHEM, ANALOG MULTIPLEXER		50003253-001	
SCALE		SHEET 2 OF 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
		RELEASED PER DRN 333	18 APR 79	REU

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION
PARTS LIST			
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .020 .XX ± .010 ± 30° XXX ± .005		CONTRACT NO.	
MATERIAL		APPROVALS	DATE
FINISH		CHECKED	18 APR 79
DO NOT SCALE DRAWING		DRAWN	18 APR 79
782B0315 750A0042		RADIANT CORPORATION P.O. BOX 9946 AUSTIN, TEXAS 78766	
NEXT ASSY USED ON		D/AG. SCHEM., A/D DISPLAY	
APPLICATION		SIZE	CODE IDENT NO.
		C	29913
		DRAWING NO. 500C3257-001	
		SCALE	SHEET / OF

500C3257-001

REVISIONS			
REV	DATE	DESCRIPTION	APPROVED
1	18 APR 79	RELEASED PER ORN 333	RJB

QTY	REQD	CODE	IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION
PARTS LIST					
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE					
FRACTIONS DECIMALS ANGLES					
= ± .020 = ± .010 ± 30° XXX = .005					
MATERIAL					
FINISH					
DO NOT SCALE DRAWING					
CONTRACT NO					
APPROVALS					
DATE					
DRAWN					
CHECKED					
DATE					
DATE					
RADIANT CORPORATION					
P O BOX 8048 DALLAS TEXAS 75218					
DIAG. SCHEM.					
A/D DISPLAY LOGIC					
SIZE CODE IDENT NO DRAWING NO					
D 29913 50003261-001					
SCALE					
SHEET OF					

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REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	-	RELEASED PER DRN. 333	2 MAR 79	1894

1. ALL LOGIC 74LS SERIES
NOTES UNLESS OTHERWISE SPECIFIED.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES = ± 0.20 XX = ± 0.10 ± 30° XXX = ± 0.05		CONTRACT NO.		RADIAN CORPORATION P.O. BOX 9948/AUSTIN, TEXAS/78766	
MATERIAL		APPROVALS			
782B0316		DRAWN J. BRUDER		DATE 4-10-78	
NEXT ASSY		CHECKED <i>DE Wainy</i>		DATE 2 MAR 79	
USED ON		DO NOT SCALE DRAWING		DRAWING NO. 5008 3265-001	
APPLICATION		SCALE NONE		SHEET 1 OF 1

REVISIONS			
REV	DATE	DESCRIPTION	APPROVED
1	18 APR 78	RELEASED PER DRN 393	REW

EDGE CONNECTOR PINOUTS SECTION A THRU D

QTY	CODE	PART OR IDENTIFYING NO	DESCRIPTION OR DESCRIPTION
PARTS LIST			
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ±.020 ±.010 ±.010 ±.005 ±.005 ±.005			
MATERIAL		CONTRACT NO.	
FINISH		APPROVALS DATE	
NEXT ASSY USED ON		DRAWN BY DATE	
APPLICATION		CHECKED BY DATE	
DO NOT SCALE DRAWING		SCALE	
702C(03)19-001 750A0042-001		RADIANT CORPORATION P.O. BOX 3084/AMTMA, TEXAS 75064	
SHEET 1 OF 2		SCHEMATIC DIAGRAM, I/O BOARD	
D 29913		DRAWING NO. 500D3277-001	

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE
-	-	RELEASED PER DRN. 933	18 APR 79

ONE OF FOUR IDENTICAL SECTIONS (A,B,C AND D)

EXAMPLE: SECTION A CONFIGURED AS 8 INPUTS

PARTS LIST FOR
SECTION A = INPUTS
UX2-10K SIP RESISTORS
ARRAY
UX3-270Ω DIP RESISTORS
ARRAY
UX5-TID 12G DIODE
ARRAY
UX6-OMIT
UX4-74LS273
UX1-OMIT
UX7-74LS244
RA1 THRU RA9-OMIT
CRA1-OMIT
QA1-OMIT
JA1-INPUT

EXAMPLE SECTION A CONFIGURED AS 8 OUTPUTS

PARTS LIST FOR
SECTION A = OUTPUTS
UX2,UX3,UX5-OMIT
UX6-33Ω DIP RESISTOR
ARRAY
UX4-74LS273
UX1-SEE NOTE 1
UX7-74LS240
RA1 THRU RA9-10Ω 1/4W 5%
RA9,CRA1,QA1-SEE NOTE 1
JA1-OUTPUT

1 UX1 MAY BE ONE OF TWO SPRAGUE PART NUMBERS. IF ULN-2803 IS USED RX9, QX1, AND CRX1 CAN BE OMITTED. IF ULM 2803 IS USED RX9, QX1, AND CRX1 MUST BE INSTALLED. IF ULM 2803 IS USED IT SHOULD BE INSTALLED SUCH THAT PIN 4 ON THE IC CORRESPONDS TO PIN 2 ON THE PCB.

NOTES:

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION
PARTS LIST			
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES ± .020 ± .010 ± .005 ± 30°			
MATERIAL			
FINISH			
NEXT ASSY USED ON			
APPLICATION			
DO NOT SCALE DRAWING			
CONTRACT NO			
APPROVALS			
DATE			
DRAWN BY			
CHECKED BY			
DATE			
DATE			
RADIANT CORPORATION			
P.O. BOX 9944, AUSTIN, TEXAS 78768			
SCHEMATIC DIAGRAM			
I/O BOARD			
SIZE CODE IDENT NO DRAWING NO			
D 29913 50003277-001			
SCALE			
SHEET 2 OF 2			

REV	DATE	APPROVED
1	1984-07-29	ADD

RELEASED PER ORN 393

DATE 1984-07-29

APPROVED

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REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	-	RELEASED PER DRN 333	12/26/74	ASD
	A	REVISED PER EO 2311	30/05/79	ASD
	B	REVISED PER EO 2325	12/07/77	ASD

QTY REQD	CODE IDENT	PART OR IDENTIFYING #	NOMENCLATURE OR DESCRIPTION		PARTS LIST	
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE			CONTRACT NO.		RADIAN CORPORATION P.O. BOX 2045/MARTIN TEL#873288	
FRACTIONS DECIMALS ANGLES			APPROVALS DATE		SCHEMATIC DIAGRAM ANALOG MPX EXP	
$\pm$.020 $\times$ $\pm$.010 $\pm$ 30° $\times$ $\pm$.005			DESIGN <i>[Signature]</i> <i>1 MAY 79</i> CHECKED BY <i>[Signature]</i> <i>20 APR 79</i> <i>5012 [Signature]</i>			
MATERIAL						
FINISH			SIZE		CODE IDENT NO	DRAWING NO
			D		29913	500D3306-001
DO NOT SCALE DRAWING			SCALE		SHEET OF	

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
-	-	RELEASED PER DRN 333	22 APR 79	1001
A	-	REVISED PER E.O. 2311	30 APR 79	1001
B	-	REVISED PER E.O. 2325	12 OCT 79	1001

1. RESISTOR VALUES DEPENDENT ON REQUIREMENT

NOTE

QTY	REQD	CODE	IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION
PARTS LIST					
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES X = .020 XX = .010 XXX = .005					
MATERIAL					
FINISH					
NEXT ASSY USED ON					
APPLICATION					
DO NOT SCALE DRAWING					
CONTRACT NO					
APPROVALS DATE					
DRAWN BY DATE					
CHECKED BY DATE					
RADIANT CORPORATION P.O. BOX 4444444444444444					
DIAGRAM SCHEMATIC ANALOG MPX EXP					
SIZE CODE IDENT NO DRAWING NO					
D 29913 5000 3306-001					
SCALE = SHEET 2 OF 2					

D
C
B
A

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION
PARTS LIST			
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE		CONTRACT NO	
FRACTIONS	DECIMALS	ANGLES	
= ± 0.20	XX ± 0.10	± 30'	
	XXX ± 0.05		
MATERIAL		APPROVALS	
FINISH		DATE	
500D3292 DART II		SCOTT COLEMAN 5 APR 79	
NEXT ASSY USED ON		CHECKED 12 APR 79	
APPLICATION		DO NOT SCALE DRAWING	
		DRAWING NO	
		500C3349-001	
		SHEET OF	

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE
		RELEASED PER DRN 333	18 APR 79

RADIAN CORPORATION
P O BOX 9948/AUSTIN, TEXAS 78768

DIAG. SCHEM. FRONT PANEL

SIZE C 29913 DRAWING NO 500C3349-001

100-7-EC0005

APPLICATION		REVISION			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
782C0324	750A0042	-	RELEASED PER DRN.333	2 MAR 79	<i>[Signature]</i>

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:

FRACTIONS DECIMALS ANGLES
= ± 0.20 XX = ± 0.10 $\pm 30^\circ$
XXX = ± 0.05

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS

DATE

DRAWN *[Signature]*

2-11-79

CHECKED *[Signature]*

2 MAR 79

[Signature]

02 MAR 79

RADIAN CORPORATION

P.O. BOX 9948/AUSTIN, TEXAS 78766

DIAG. SCHEM.
BUS TERMINATOR

SIZE

CODE IDENT NO.

DRAWING NO.

A

29913

500A3352-001

SCALE NONE

SHEET

OF

APPENDIX D

DEVICE SPECIFICATION SHEETS

M6800	Microprocessor
TR 1863	Asynchronous Receiver/Transmitter
AD 572	Analog-to-Digital Converter
AM 9511	Arithmetic Processing Unit
EMA 5/6 CC	5 Volt Power Supply
ETA 12/15 B	± 15 Volt Power Supply
EMA 18/24 B	24 Volt Power Supply
FD 1771	Floppy Disk Formatter/Controller
TMS 4046	Random Access Static Memory

MC6800

(0 to 70°C; L or P Suffix)

MC6800C

(-40 to 85°C; L Suffix only)

MICROPROCESSING UNIT (MPU)

The MC6800 is a monolithic 8-bit microprocessor forming the central control function for Motorola's M6800 family. Compatible with TTL, the MC6800, as with all M6800 system parts, requires only one +5.0-volt power supply, and no external TTL devices for bus interface.

The MC6800 is capable of addressing 65K bytes of memory with its 16-bit address lines. The 8-bit data bus is bidirectional as well as 3-state, making direct memory addressing and multiprocessing applications realizable.

- Eight-Bit Parallel Processing
- Bi-Directional Data Bus
- Sixteen-Bit Address Bus — 65K Bytes of Addressing
- 72 Instructions — Variable Length
- Seven Addressing Modes — Direct, Relative, Immediate, Indexed, Extended, Implied and Accumulator
- Variable Length Stack
- Vectored Restart
- Maskable Interrupt Vector
- Separate Non-Maskable Interrupt — Internal Registers Saved In Stack
- Six Internal Registers — Two Accumulators, Index Register, Program Counter, Stack Pointer and Condition Code Register
- Direct Memory Addressing (DMA) and Multiple Processor Capability
- Clock Rates as High as 1 MHz
- Simple Bus Interface Without TTL
- Halt and Single Instruction Execution Capability

MOS

(N-CHANNEL SILICON-GATE)

MICROPROCESSOR

L SUFFIX
CERAMIC PACKAGE
CASE 715

NOT SHOWN: P SUFFIX
PLASTIC PACKAGE
CASE 711

**M6800 MICROCOMPUTER FAMILY
BLOCK DIAGRAM**

**MC6800 MICROPROCESSOR
BLOCK DIAGRAM**

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0 \text{ V} \pm 5\%$, $V_{SS} = 0$, $T_A = 0 \text{ to } 70^\circ\text{C}$ unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage	Logic $\phi 1, \phi 2$	V_{IH} V_{IHC}	$V_{SS} + 2.0$ $V_{CC} - 0.3$	—	V_{CC} $V_{CC} + 0.1$	Vdc
Input Low Voltage	Logic $\phi 1, \phi 2$	V_{IL} V_{ILC}	$V_{SS} - 0.3$ $V_{SS} - 0.1$	—	$V_{SS} + 0.8$ $V_{SS} + 0.3$	Vdc
Clock Overshoot/Undershoot — Input High Level — Input Low Level		V_{OS}	$V_{CC} - 0.5$ $V_{SS} - 0.5$	—	$V_{CC} + 0.5$ $V_{SS} + 0.5$	Vdc
Input Leakage Current ($V_{in} = 0 \text{ to } 5.25 \text{ V}$, $V_{CC} = \text{max}$) ($V_{in} = 0 \text{ to } 5.25 \text{ V}$, $V_{CC} = 0.0 \text{ V}$)	Logic* $\phi 1, \phi 2$	I_{in}	— —	1.0 —	2.5 100	μA_{dc}
Three-State (Off State) Input Current ($V_{in} = 0.4 \text{ to } 2.4 \text{ V}$, $V_{CC} = \text{max}$)	D0-D7 A0-A15, R/W	I_{TSI}	— —	2.0 —	10 100	μA_{dc}
Output High Voltage ($I_{Load} = -205 \mu\text{A}_{dc}$, $V_{CC} = \text{min}$) ($I_{Load} = -145 \mu\text{A}_{dc}$, $V_{CC} = \text{min}$) ($I_{Load} = -100 \mu\text{A}_{dc}$, $V_{CC} = \text{min}$)	D0-D7 A0-A15, R/W, VMA BA	V_{OH}	$V_{SS} + 2.4$ $V_{SS} + 2.4$ $V_{SS} + 2.4$	— — —	— — —	Vdc
Output Low Voltage ($I_{Load} = 1.5 \text{ mA}_{dc}$, $V_{CC} = \text{min}$)		V_{OL}	—	—	$V_{SS} + 0.4$	Vdc
Power Dissipation		P_D	—	0.600	1.2	W
Capacitance* ($V_{in} = 0$, $T_A = 25^\circ\text{C}$, $f = 1.0 \text{ MHz}$)	$\phi 1, \phi 2$ TSC DBE D0-D7 Logic Inputs A0-A15, R/W, VMA	C_{in} C_{out}	80 — — — — —	120 — 7.0 10 6.5	160 15 10 12.5 8.5	pF
Frequency of Operation		f	0.1	—	1.0	MHz
Clock Timing (Figure 1)						
Cycle Time		t_{CYC}	1.0	—	10	μs
Clock Pulse Width (Measured at $V_{CC} - 0.3 \text{ V}$)	$\phi 1$ $\phi 2$	PW_{OH}	430 450	— —	4500 4500	ns
Total $\phi 1$ and $\phi 2$ Up Time		t_{ut}	940	—	—	ns
Rise and Fall Times (Measured between $V_{SS} + 0.3 \text{ V}$ and $V_{CC} - 0.3 \text{ V}$)	$\phi 1, \phi 2$	t_{or}, t_{of}	5.0	—	50	ns
Delay Time or Clock Separation (Measured at $V_{OV} = V_{SS} + 0.5 \text{ V}$)		t_d	0	—	9100	ns
Overshoot Duration		t_{OS}	0	—	40	ns

*Except TRQ and NM, which require 3 k Ω pullup load resistors for wire-OR capability at optimum operation.

*Capacitances are periodically sampled rather than 100% tested.

FIGURE 1 — CLOCK TIMING WAVEFORM

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	Vdc
Input Voltage	V_{in}	-0.3 to +7.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Thermal Resistance	θ_{JA}	70	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

READ/WRITE TIMING Figures 2 and 3, $f = 1.0$ MHz, Load Circuit of Figure 6.

Characteristic	Symbol	Min	Typ	Max	Unit
Address Delay	t_{AD}	—	220	300	ns
Peripheral Read Access Time $t_{acc} = t_{ut} - (t_{AD} + t_{DSR})$	t_{acc}	—	—	540	ns
Data Setup Time (Read)	t_{DSR}	100	—	—	ns
Input Data Hold Time	t_H	10	—	—	ns
Output Data Hold Time	t_H	10	25	—	ns
Address Hold Time (Address, R/W, VMA)	t_{AH}	50	75	—	ns
Enable High Time for DBE Input	t_{EH}	450	—	—	ns
Data Delay Time (Write)	t_{DDW}	—	165	225	ns
Processor Controls*					
Processor Control Setup Time	t_{PCS}	200	—	—	ns
Processor Control Rise and Fall Time	t_{PCR}, t_{PCF}	—	—	100	ns
Bus Available Delay	t_{BA}	—	—	300	ns
Three State Enable	t_{TSE}	—	—	40	ns
Three State Delay	t_{TSO}	—	—	700	ns
Data Bus Enable Down Time During $\phi 1$ Up Time (Figure 3)	t_{DBE}	150	—	—	ns
Data Bus Enable Delay (Figure 3)	t_{DBED}	300	—	—	ns
Data Bus Enable Rise and Fall Times (Figure 3)	t_{DBER}, t_{DBEF}	—	—	25	ns

*Additional information is given in Figures 12 through 16 of the Family Characteristics — see pages 17 through 20.

FIGURE 2 — READ DATA FROM MEMORY OR PERIPHERALS

FIGURE 3 - WRITE IN MEMORY OR PERIPHERALS

FIGURE 4 - TYPICAL DATA BUS OUTPUT DELAY versus CAPACITIVE LOADING

FIGURES 5 - TYPICAL READ/WRITE, VMA, AND ADDRESS OUTPUT DELAY versus CAPACITIVE LOADING

FIGURE 6 - BUS TIMING TEST LOAD

- C = 130 pF for D0-D7
 = 90 pF for A0-A15, R/W, and VMA
 = 30 pF for BA
 R = 11.7 k Ω for D0-D7
 = 16.5 k Ω for A0-A15, R/W, and VMA
 = 24 k Ω for BA

TYPICAL POWER SUPPLY CURRENT

FIGURE 7 - VARIATIONS WITH FREQUENCY

FIGURE 8 - VARIATIONS WITH TEMPERATURE

EXPANDED BLOCK DIAGRAM

MPU SIGNAL DESCRIPTION

Proper operation of the MPU requires that certain control and timing signals be provided to accomplish specific functions and that other signal lines be monitored to determine the state of the processor.

Clocks Phase One and Phase Two ($\phi 1$, $\phi 2$) — Two pins are used for a two-phase non-overlapping clock that runs at the VCC voltage level.

Address Bus (A0-A15) — Sixteen pins are used for the address bus. The outputs are three-state bus drivers capable of driving one standard TTL load and 130 pF. When the output is turned off, it is essentially an open circuit. This permits the MPU to be used in DMA applications.

Data Bus (D0-D7) — Eight pins are used for the data bus. It is bi-directional, transferring data to and from the memory and peripheral devices. It also has three-state output buffers capable of driving one standard TTL load and 130 pF.

Halt — When this input is in the low state, all activity in the machine will be halted. This input is level sensitive. In the halt mode, the machine will stop at the end of an instruction. Bus Available will be at a one level, Valid Memory Address will be at a zero, and all other three state lines will be in the three-state mode.

Transition of the **Halt** line must not occur during the last 250 ns of phase one. To insure single instruction operation, the **Halt** line must go high for one clock cycle.

Three-State Control (TSC) — This input causes all of the address lines and the Read/Write line to go into the off or high impedance state. This state will occur 700 ns after TSC = 2.0 V. The Valid Memory Address and Bus Available signals will be forced low. The data bus is not affected by TSC and has its own enable (Data Bus Enable). In DMA applications, the Three-State Control line should be brought high on the leading edge of the Phase One Clock. The $\phi 1$ clock must be held in the high state and the $\phi 2$ in the low state for this function to operate properly. The address bus will then be available for other devices to directly address memory. Since the MPU is a dynamic device, it can be held in this state for only 45 μ s or destruction of data will occur in the MPU.

Read/Write (R/W) — This TTL compatible output signals the peripherals and memory devices whether the MPU is in a Read (high) or Write (low) state. The normal standby state of this signal is Read (high). Three State Control going high will turn Read/Write to the off (high impedance) state. Also, when the processor is halted, it will be in the off state. This output is capable of driving one standard TTL load and 90 pF.

Valid Memory Address (VMA) — This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling peripheral interfaces such as the PIA and ACIA. This signal is not three-state. One standard TTL load and 90 pF may be directly driven by this active high signal.

Data Bus Enable (DBE) — This input is the three-state control signal for the MPU data bus and will enable the bus drivers when in the high state. This input is TTL compatible, however in normal operation, it would be driven by the phase two clock. During an MPU read cycle, the data bus drivers will be disabled internally. When it is desired that another device control the data bus such as in Direct Memory Access (DMA) applications, DBE should be held low.

Bus Available (BA) — The Bus Available signal will normally be in the low state, when activated, it will go to the high state indicating that the microprocessor has stopped and that the address bus is available. This will occur if the **Halt** line is in the low state or the processor is in the WAIT state as a result of the execution of a WAIT instruction. At such time, all three-state output drivers will go to their off state and other outputs to their normally inactive level. The processor is removed from the WAIT state by the occurrence of a maskable (mask bit 1 = 0) or nonmaskable interrupt. This output is capable of driving one standard TTL load and 30 pF.

Interrupt Request (IRQ) — This level sensitive input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the Condition Code Register is not set, the machine will begin an interrupt sequence. The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. Next the MPU will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur. At the end of the cycle, a 16 bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations causes the MPU to branch to an interrupt routine in memory.

The **Halt** line must be in the high state for interrupts to be serviced. Interrupts will be latched internally while **Halt** is low.

The **IRQ** has a high impedance pullup device internal to the chip, however a 3 k Ω external resistor to VCC should be used for wire OR and optimum control of interrupts.

Reset — This input is used to reset and start the MPU from a power down condition, resulting from a power failure or an initial start up of the processor. If a high level is detected on the input, this will signal the MPU to begin the restart sequence. This will start execution of a routine to initialize the processor from its reset condition. All the higher order address lines will be forced high. For the restart, the last two (FFFF, FFFF) locations in memory will be used to load the program that is addressed by the program counter. During the restart routine the interrupt mask bit is set and must be reset before the MPU can be interrupted by **IRQ**.

Figure 9 shows the initialization of the microprocessor after restart. $\overline{\text{Reset}}$ must be held low for at least eight clock periods after V_{CC} reaches 4.75 volts. If $\overline{\text{Reset}}$ goes high prior to the leading edge of ϕ_2 , on the next ϕ_1 the first restart memory vector address (FFFE) will appear on the address lines. This location should contain the higher order eight bits to be stored into the program counter. Following, the next address FFFF should contain the lower order eight bits to be stored into the program counter.

Non-Maskable Interrupt (NMI) — A low-going edge on this input requests that a non-mask-interrupt sequence be generated within the processor. As with the Interrupt Request signal, the processor will complete the current instruction that is being executed before it recognizes the NMI signal. The interrupt mask bit in the Condition Code Register has no effect on $\overline{\text{NMI}}$.

The Index Register, Program Counter, Accumulators, and Condition Code Register are stored away on the stack. At the end of the cycle, a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations causes the MPU to branch to a non-maskable interrupt routine in memory.

$\overline{\text{NMI}}$ has a high impedance pullup resistor internal to the chip, however a 3 k Ω external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

Inputs $\overline{\text{IRQ}}$ and $\overline{\text{NMI}}$ are hardware interrupt lines that are sampled during ϕ_2 and will start the interrupt routine on the ϕ_1 following the completion of an instruction.

Figure 10 is a flow chart describing the major decision paths and interrupt vectors of the microprocessor. Table 1 gives the memory map for interrupt vectors.

FIGURE 9 — INITIALIZATION OF MPU AFTER RESTART

TABLE 1 — MEMORY MAP FOR INTERRUPT VECTORS

Vector		Description
MS	LS	
FFFE	FFFF	Restart
FFFC	FFFD	Non maskable Interrupt
FFFA	FFFB	Software Interrupt
FFFB	FFFD	Interrupt Request

FIGURE 10 - MPU FLOW CHART

MPU REGISTERS

The MPU has three 16-bit registers and three 8-bit registers available for use by the programmer (Figure 11).

Program Counter — The program counter is a two byte (16-bits) register that points to the current program address.

Stack Pointer — The stack pointer is a two byte register that contains the address of the next available location in an external push-down/pop-up stack. This stack is normally a random access Read/Write memory that may

have any location (address) that is convenient. In those applications that require storage of information in the stack when power is lost, the stack must be non-volatile.

Index Register — The index register is a two byte register that is used to store data or a sixteen bit memory address for the Indexed mode of memory addressing.

Accumulators — The MPU contains two 8-bit accumulators that are used to hold operands and results from an arithmetic logic unit (ALU).

FIGURE 11 — PROGRAMMING MODEL OF THE MICROPROCESSING UNIT

FIGURE 12 — SAVING THE STATUS OF THE MICROPROCESSOR IN THE STACK

SP = Stack Pointer
 CC = Condition Codes (Also called the Processor Status Byte)
 ACCE = Accumulator B
 ACCA = Accumulator A
 IXH = Index Register, Higher Order 8 Bits
 IXL = Index Register, Lower Order 8 Bits
 PCH = Program Counter, Higher Order 8 Bits
 PCL = Program Counter, Lower Order 8 Bits

Condition Code Register — The condition code register indicates the results of an Arithmetic Logic Unit operation: Negative (N), Zero (Z), Overflow (V), Carry from bit 7 (C), and half carry from bit 3 (H). These bits of the Condition Code Register are used as testable conditions for the conditional branch instructions. Bit 4 is the interrupt mask bit (I). The unused bits of the Condition Code Register (b6 and b7) are ones.

Figure 12 shows the order of saving the microprocessor status within the stack.

MPU INSTRUCTION SET

The MC6800 has a set of 72 different instructions. Included are binary and decimal arithmetic, logical, shift, rotate, load, store, conditional or unconditional branch, interrupt and stack manipulation instructions (Tables 2 thru 6).

MPU ADDRESSING MODES

The MC6800 eight-bit microprocessing unit has seven addressing modes that can be used by a programmer, with the addressing mode a function of both the type of instruction and the coding within the instruction. A summary of the addressing modes for a particular instruction can be found in Table 7 along with the associated instruction execution time that is given in machine cycles. With a clock frequency of 1 MHz, these times would be microseconds.

Accumulator (ACCX) Addressing — In accumulator only addressing, either accumulator A or accumulator B is specified. These are one byte instructions.

Immediate Addressing — In immediate addressing, the operand is contained in the second byte of the instruction except LDS and LDX which have the operand in the second and third bytes of the instruction. The MPU addresses

this location when it fetches the immediate instruction for execution. These are two or three-byte instructions.

Direct Addressing — In direct addressing, the address of the operand is contained in the second byte of the instruction. Direct addressing allows the user to directly address the lowest 256 bytes in the machine, i.e., locations zero through 255. Enhanced execution times are achieved by storing data in these locations. In most configurations, it should be a random access memory. These are two byte instructions.

Extended Addressing — In extended addressing, the address contained in the second byte of the instruction is used as the higher eight-bits of the address of the operand. The third byte of the instruction is used as the lower eight bits of the address for the operand. This is an absolute address in memory. These are three byte instructions.

Indexed Addressing — In indexed addressing, the address contained in the second byte of the instruction is added to the index register's lowest eight bits in the MPU. The carry is then added to the higher order eight bits of the index register. This result is then used to address memory. The modified address is held in a temporary address register so there is no change to the index register. These are two-byte instructions.

Implied Addressing — In the implied addressing mode the instruction gives the address (i.e., stack pointer, index register, etc.). These are one byte instructions.

Relative Addressing — In relative addressing, the address contained in the second byte of the instruction is added to the program counter's lowest eight bits plus two. The carry or borrow is then added to the high eight bits. This allows the user to address data within a range of -125 to +129 bytes of the present instruction. These are two-byte instructions.

TABLE 2 — MICROPROCESSOR INSTRUCTION SET — ALPHABETIC SEQUENCE

ABA	Add Accumulators	CLR	Clear	PUL	Pull Data
ADC	Add with Carry	CLV	Clear Overflow	ROL	Rotate Left
ADD	Add	CMP	Compare	ROR	Rotate Right
AND	Logical And	COM	Complement	RTI	Return from Interrupt
ASL	Arithmetic Shift Left	CPX	Compare Index Register	RTS	Return from Subroutine
ASR	Arithmetic Shift Right	DAA	Decimal Adjust	SBA	Subtract Accumulators
BCC	Branch if Carry Clear	DEC	Decrement	SBC	Subtract with Carry
BCS	Branch if Carry Set	DES	Decrement Stack Pointer	SEC	Set Carry
BEQ	Branch if Equal to Zero	DEX	Decrement Index Register	SEI	Set Interrupt Mask
BGE	Branch if Greater or Equal Zero	EOR	Exclusive OR	SEV	Set Overflow
BGT	Branch if Greater than Zero	INC	Increment	STA	Store Accumulator
BHI	Branch if Higher	INS	Increment Stack Pointer	STS	Store Stack Register
BIT	Bit Test	INX	Increment Index Register	STX	Store Index Register
BLE	Branch if Less or Equal	JMP	Jump	SUB	Subtract
BLS	Branch if Lower or Same	JSR	Jump to Subroutine	SWI	Software Interrupt
BLT	Branch if Less than Zero	LDA	Load Accumulator	TAB	Transfer Accumulators
BMT	Branch if Minus	LDS	Load Stack Pointer	TAP	Transfer Accumulators to Condition Code Reg
BNE	Branch if Not Equal to Zero	LDX	Load Index Register	TBA	Transfer Accumulators
SPL	Branch if Plus	LSR	Logical Shift Right	TPA	Transfer Condition Code Reg to Accumulator
SRA	Branch Always	NEG	Negate	TST	Test
BSR	Branch to Subroutine	NOP	No Operation	TSX	Transfer Stack Pointer to Index Register
BVC	Branch if Overflow Clear	ORA	Inclusive OR Accumulator	TXS	Transfer Index Register to Stack Pointer
BVS	Branch if Overflow Set	PSH	Push Data	WAI	Wait for Interrupt
CBA	Compare Accumulators				
CLC	Clear Carry				
CLI	Clear Interrupt Mask

TABLE 3 - ACCUMULATOR AND MEMORY INSTRUCTIONS

ADDRESSING MODES										BOOLEAN/ARITHMETIC OPERATION										COND CODE REG						
OPERATIONS	MNEMONIC	IMMED		DIRECT		INDEX		EXTEND		IMPLIED		[All register labels refer to operands]										S	O	N	Z	V
		OP	~	=	OP	~	=	OP	~	=	OP	~	=	M	I	N	Z	V	C							
Add	ADD	38	2	2	38	3	2	48	5	2	88	4	3		A ← A + A											
	ADD5	08	2	2	08	3	2	18	5	2	F8	4	3		B ← A + B											
Add Accumulator	ADA												18	2	1	A ← B + A										
Add with Carry	ADCA	08	2	2	98	3	2	08	5	2	88	4	3		A ← A + C + A											
	ADC5	08	2	2	08	3	2	18	5	2	F8	4	3		B ← A + C + B											
And	ANDA	37	2	2	94	3	2	40	3	2	84	4	3		A ← A & A											
	AND5	C4	2	2	04	3	2	64	5	2	F4	4	3		B ← A & B											
Bit Test	BITA	05	2	2	95	3	2	A5	5	2	85	4	3		A ← A											
	BIT5	C5	2	2	05	3	2	E5	5	2	F5	4	3		B ← A											
Clear	CLB							4F	1	2	2F	6	3		00 ← A											
	CLRA										4F	2	1		00 ← A											
	CLRB										5F	2	1		00 ← B											
Compare	CMPA	31	2	2	91	3	2	A1	5	2	81	4	3		A ← M											
	CMP5	C1	2	2	01	3	2	E1	5	2	F1	4	3		B ← M											
Compare Accumulator	CBA												11	2	1	A ← B										
Complement 1's	COM							52	1	2	72	6	3		B ← M											
	COMA												21	2	1	A ← A										
	COMB												52	2	1	B ← B										
Complement 2's	NEG							50	1	2	70	6	3		00 ← M - M											
Increment	INCA												40	2	1	00 ← A - A										
	INCA5												50	2	1	00 ← B - B										
Decrement	DECA							6A	1	2	7A	6	3		Convert Binary Add of BCD Characters into BCD Format											
	DECA5												6A	2	1	M ← 1 - M										
Exclusive OR	EXORA	08	2	2	98	3	2	08	5	2	88	4	3		A ← 1 - A											
	EXOR5	C8	2	2	08	3	2	E8	5	2	F8	4	3		B ← 1 - B											
Increment	INCA							9C	7	2	7C	6	3		A ← M - A											
	INCA5												4C	2	1	B ← 1 - B										
Load Accumulator	LDA	06	2	2	96	3	2	A6	5	2	86	4	3		2 - 1 - B											
	LDA5	C6	2	2	06	3	2	E6	5	2	F6	4	3		M ← A											
Or Exclusive	EXORA	2A	2	2	9A	3	2	AA	5	2	8A	4	3		M ← B											
	EXOR5	CA	2	2	0A	3	2	EA	5	2	FA	4	3		A ← M - A											
Push Data	PSHA												26	4	1	B ← M - B										
	PSHB												37	4	1	A ← Msp SP - 1 - SP										
Push Data	PULA												32	4	1	B ← Msp SP - 1 - SP										
	PULB												33	4	1	SP - 1 - SP Msp - A										
Rotate Left	ROL							80	7	2	78	6	3		SP - 1 - SP Msp - B											
	ROLA												18	2	1	A										
	ROLB												58	2	1	B										
Rotate Right	ROR							66	1	2	76	6	3		A											
	RORA												46	2	1	B										
	RORB												56	2	1	B										
Shift Left Arithmetic	ASL							50	7	2	70	6	3		A											
	ASLA												48	2	1	A										
	ASLB												58	2	1	B										
Shift Right Arithmetic	ASR							57	1	2	77	6	3		A											
	ASRA												47	2	1	A										
	ASRB												57	2	1	B										
Shift Right Logical	LSR							56	7	2	76	6	3		A											
	LSRA												46	2	1	A										
	LSRB												56	2	1	B										
Store Accumulator	STAA							97	4	2	A7	6	3		A ← M											
	STAB							07	4	2	67	6	3		B ← M											
Subtract	SUBA	30	2	2	90	3	2	A0	5	2	80	4	3		A ← M - A											
	SUB5	C0	2	2	00	3	2	E0	5	2	F0	4	3		B ← M - B											
Subtract Accumulator	SBA												10	2	1	A ← B - A										
Subtract with Carry	SBCA	82	2	2	92	3	2	A2	5	2	82	4	3		A ← B - C - A											
	SBC5	C2	2	2	02	3	2	E2	5	2	F2	4	3		B ← M - C - B											
Transfer Accumulator	TAA												16	2	1	A ← B										
	TBA												17	2	1	B ← A										
Test Zero or Negative	TST							60	7	2	70	6	3		M ← 00											
	TSTA												10	2	1	A ← 00										
	TSTB												50	2	1	B ← 00										

LEGEND

- OP Operation Code (Hexadecimal)
- ~ Number of CPU Cycles
- ~ Number of Program Bytes
- ~ Arithmetic Plus
- ~ Arithmetic Minus
- ~ Boolean AND

*Sp - Contents of memory location pointed to by Stack Pointer

Note - Accumulator addressing mode instructions are included in the column for IMPLIED addressing

CONDITION CODE SYMBOLS

- M Null Carry from bit 3
- I Interrupt Mask
- N Negative Flag Set
- Z Zero Flag Set
- V Overflow, 2's complement
- C Carry from bit 7
- R Reset Always
- S Set Always
- T Test and set if true, cleared otherwise
- W Word Aligned

TABLE 4 - INDEX REGISTER AND STACK MANIPULATION INSTRUCTIONS

POINTER OPERATIONS	MNEMONIC																COND CODE REG				
		IMMED			DIRECT			INDEX			EXTND			IMPLIED							
		OP	~	=	OP	~	=	OP	~	=	OP	~	=	OP	~	=	BOOLEAN/ARITHMETIC OPERATION				
Compare Index Reg	CPX	8C	3	3	9C	4	2	AC	6	2	BC	5	3				$X_H - M, X_L - (M + 1)$	1	0	1	0
Decrement Index Reg	DEX													09	4	1	$X - 1 - X$	+	+	+	+
Decrement Stack Ptr	OES													34	4	1	$SP - 1 - SP$	+	+	+	+
Increment Index Reg	INX													08	4	1	$X + 1 - X$	+	+	+	+
Increment Stack Ptr	INS													37	4	1	$SP + 1 - SP$	+	+	+	+
Load Index Reg	LDX	CE	3	3	DE	4	2	EE	6	2	FE	5	3				$M - X_H, (M + 1) - X_L$	+	+	+	+
Load Stack Ptr	LOS	BE	3	3	9E	4	2	AE	6	2	BE	5	3				$M - SP_H, (M + 1) - SP_L$	+	+	+	+
Store Index Reg	STX				0F	5	2	EF	7	2	FF	6	3				$X_H - M, X_L - (M + 1)$	+	+	+	+
Store Stack Ptr	STS				0F	5	2	AF	7	2	BF	6	3				$SP_H - M, SP_L - (M + 1)$	+	+	+	+
Index Reg - Stack Ptr	TXS													35	4	1	$X - 1 - SP$	+	+	+	+
Stack Ptr - Index Reg	TSX													30	4	1	$SP - 1 - X$	+	+	+	+

TABLE 5 - JUMP AND BRANCH INSTRUCTIONS

OPERATIONS	MNEMONIC																COND CODE REG				
		RELATIVE			INDEX			EXTND			IMPLIED										
		OP	~	=	OP	~	=	OP	~	=	OP	~	=				BRANCH TEST				
Branch Always	BRA	20	4	2													None	+	+	+	+
Branch If Carry Clear	BCC	24	4	2													$C = 0$	+	+	+	+
Branch If Carry Set	BCS	25	4	2													$C = 1$	+	+	+	+
Branch If = Zero	BED	27	4	2													$Z = 1$	+	+	+	+
Branch If > Zero	BGE	20	4	2													$M \oplus V = 0$	+	+	+	+
Branch If > Zero	BGT	2E	4	2													$Z + (M \oplus V) = 0$	+	+	+	+
Branch If Higher	BHI	22	4	2													$C + Z = 0$	+	+	+	+
Branch If < Zero	BLE	2F	4	2													$Z + (M \oplus V) = 1$	+	+	+	+
Branch If Lower Or Same	BLS	23	4	2													$C + Z = 1$	+	+	+	+
Branch If < Zero	BLT	20	4	2													$M \oplus V = 1$	+	+	+	+
Branch If Not Equal	BNE	26	4	2													$N = 1$	+	+	+	+
Branch If Not Equal Zero	BNE	26	4	2													$Z = 0$	+	+	+	+
Branch If Overflow Clear	BVC	28	4	2													$V = 0$	+	+	+	+
Branch If Overflow Set	BVS	29	4	2													$V = 1$	+	+	+	+
Branch If Plus	BPL	2A	4	2													$N = 0$	+	+	+	+
Branch To Subroutine	BSR	30	4	2														+	+	+	+
Jump	JMP				6E	4	2	7E	3	3								+	+	+	+
Jump To Subroutine	JSR				AD	4	2	BD	3	3								+	+	+	+
No Operation	NOP										01	2	1					+	+	+	+
Return From Interrupt	RTI										38	10	1					+	+	+	+
Return From Subroutine	RTS										39	5	1					+	+	+	+
Software Interrupt	SWI										3F	12	1					+	+	+	+
Wait for Interrupt*	WAI										3E	9	1					+	+	+	+

*WAI puts Address Bus, R/W, and Data Bus in the three state mode while WDA is held low.

SPECIAL OPERATIONS

JSR JUMP TO SUBROUTINE

BSR BRANCH TO SUBROUTINE

JMP, JUMP

RTS, RETURN FROM SUBROUTINE

RTI, RETURN FROM INTERRUPT

TABLE 6 - CONDITION CODE REGISTER MANIPULATION INSTRUCTIONS

OPERATIONS	MNEMONIC	OP	IMPLIED			COND CODE REG									
			DP	~	=	BOOLEAN OPERATION		H		L		V		C	
Clear Carry	CLC	0C	2	1		0 ← C		•	•	•	•	•	•	•	R
Clear Interrupt Ack	CLI	0E	2	1		0 ← I		•	•	•	•	•	•	•	•
Clear Overflow	CLV	0A	2	1		0 ← V		•	•	•	•	•	•	•	•
Set Carry	SEC	0D	2	1		1 ← C		•	•	•	•	•	•	•	S
Set Interrupt Mask	SEI	0F	2	1		1 ← I		•	•	•	•	•	•	•	•
Set Overflow	SEV	0B	2	1		1 ← V		•	•	•	•	•	•	•	•
Accum A ← CCR	TAP	05	2	1		A ← CCR									
CCR ← Accum A	TPA	07	2	1		CCR ← A									

CONDITION CODE REGISTER NOTES (Bit set if test is true and cleared otherwise)

1 (Bit V) Test Result = 10000000?	7 (Bit N) Test Sign bit of most significant (MS) byte = 1?
2 (Bit C) Test Result = 00000000?	8 (Bit V) Test 2's complement overflow from subtraction of 16 bytes?
3 (Bit C) Test Decimal value of most significant BCD Character greater than nine?
(Not cleared if previously set)	9 (Bit N) Test Result less than zero? (Bit IS + 1)
4 (Bit V) Test Operand = 10000000 prior to execution?	10 (Bit I) Load Condition Code Register from Stack (See Special Operations)
5 (Bit V) Test Operand = 01111111 prior to execution?	11 (Bit I) Set when interrupt occurs. If previously set a Non Maskable Interrupt is required to exit the wait state
6 (Bit V) Test Set word to result of MISC after shift has occurred	12 (Bit I) Set according to the contents of Accumulator A

TABLE 7 — INSTRUCTION ADDRESSING MODES AND ASSOCIATED EXECUTION TIMES
(Times in Machine Cycles)

	(Dist Operated)	ACCK	Immediate	Direct	Extended	Indexed	Implied	Relative		(Dist Operated)	ACCK	Immediate	Direct	Extended	Indexed	Implied
ABA		+								WAC	+					
ADC	x	+	2	3	4	5	+			WAS	+			6	7	+
ADD	x	+	2	3	4	5	+			WAX	+			3	4	+
AND	x	+	2	3	4	5	+			JMP	+			3	4	+
ASL		2			6	7				JSM	+			6	7	
ASR		2			6	7				LDA	x	+	3	4	5	+
BCC								4		LDS		+	3	4	5	+
BES								4		LDS		+	3	4	5	+
BEA								4		LSR	+	+		6	7	
BGE								4		NEG	+	+		6	7	
BGT								4		NOP		+				
BHI								4		ORA	x	+	2	3	4	+
BIT	x	+	2	3	4	5	+			PSH		+				
BLE								4		PUL		+				
BLS								4		RCL	+	+		6	7	
BLT								4		ROR	+	+		6	7	
BAH								4		RTI		+			10	
BNE								4		RTS		+				
BPL								4		SBA		+			2	
BRA								4		SBC	x	+	2	3	4	+
BSR								8		SEC		+				
BVC								4		SEI		+				
BVS								4		SEV		+				
CBA							2			STA	x	+	4	5	6	+
CLC							2			STS		+	5	6	7	+
CLI							4			STX		+	5	6	7	+
CLR	2			6	7					SUB	x	+	2	3	4	+
CLV						2				SVI		+				12
CMP	x	+	2	3	4	5	+			TAB		+				2
COM		2		6	7					TAP		+				2
CPX		3	4	5	6					TBA		+				2
DAA						2				TPA		+				2
DEC	2			6	7					TST	+	+		6	7	+
DES										TSX		+				4
DEX										TSX		+				4
EOR	x	+	2	3	4	5	+			WAI		+				9

NOTE: Interrupt time is 12 cycles from the end of the instruction being executed, except following a WAI instruction. Then it is 4 cycles.

PIN ASSIGNMENT

1	VSS	Reset	40
2	HALT	TSC	39
3	Q1	NC	38
4	IRQ	O2	37
5	VMA	DBE	36
6	NMI	NC	35
7	BA	R/W	34
8	VCC	D0	33
9	A0	D1	32
10	A1	D2	31
11	A2	D3	30
12	A3	D4	29
13	A4	D5	28
14	A5	D6	27
15	A6	D7	26
16	A7	A15	25
17	A8	A14	24
18	A9	A13	23
19	A10	A12	22
20	A11	VSS	21

PACKAGE DIMENSIONS
CASE 715 02
(CERAMIC)

See Page 165 for
Plastic Package dimensions.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.86	15.62	0.585	0.615
C	2.54	4.19	0.100	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54	8.50	0.100	8.50
H	0.76	1.78	0.030	0.070
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	14.80	15.37	0.575	0.605
M	—	10 ⁰	—	10 ⁰
N	0.51	1.52	0.020	0.060

NOTE:
1 LEADS TRUE POSITIONED WITHIN
0.25 mm (0.010) DIA (AT SEATING
PLANE) AT MAX MAT L
CONDITION

SUMMARY OF CYCLE BY CYCLE OPERATION

Table 8 provides a detailed description of the information present on the Address Bus, Data Bus, Valid Memory Address line (VMA), and the Read/Write line (R/W) during each cycle for each instruction.

This information is useful in comparing actual with expected results during debug of both software and hard-

ware as the control program is executed. The information is categorized in groups according to Addressing Mode and Number of Cycles per instruction. (In general, instructions with the same Addressing Mode and Number of Cycles execute in the same manner; exceptions are indicated in the table.)

TABLE 8 - OPERATION SUMMARY

Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
IMMEDIATE						
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	2	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Operand Data
CPX LDS LDX	3	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Operand Data (High Order Byte)
		3	1	Op Code Address + 2	1	Operand Data (Low Order Byte)
DIRECT						
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	3	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand
		3	1	Address of Operand	1	Operand Data
CPX LDS LDX	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand
		3	1	Address of Operand	1	Operand Data (High Order Byte)
		4	1	Operand Address + 1	1	Operand Data (Low Order Byte)
STA	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Destination Address
		3	0	Destination Address	1	Irrelevant Data (Note 1)
		4	1	Destination Address	0	Data from Accumulator
STS STX	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand
		3	0	Address of Operand	1	Irrelevant Data (Note 1)
		4	1	Address of Operand	0	Register Data (High Order Byte)
		5	1	Address of Operand + 1	0	Register Data (Low Order Byte)
INDEXED						
JMP	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	1	Index Register Plus Offset	1	Operand Data
CPX LDS LDX	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	1	Index Register Plus Offset	1	Operand Data (High Order Byte)
		6	1	Index Register Plus Offset + 1	1	Operand Data (Low Order Byte)

TABLE 8 - OPERATION SUMMARY (Continued)

Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
INDEXED (Continued)						
STA	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	0	Index Register Plus Offset	1	Irrelevant Data (Note 1)
		6	1	Index Register Plus Offset	0	Operand Data
ASL LSR ASR NEG CLR ROL COM ROR DEC TST INC	7	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	1	Index Register Plus Offset	1	Current Operand Data
		6	0	Index Register Plus Offset	1	Irrelevant Data (Note 1)
		7	1/0 (Note 3)	Index Register Plus Offset	0	New Operand Data (Note 3)
STS STX	7	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
		5	0	Index Register Plus Offset	1	Irrelevant Data (Note 1)
		6	1	Index Register Plus Offset	0	Operand Data (High Order Byte)
		7	1	Index Register Plus Offset + 1	0	Operand Data (Low Order Byte)
JSR	8	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Offset
		3	0	Index Register	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer	0	Return Address (Low Order Byte)
		5	1	Stack Pointer - 1	0	Return Address (High Order Byte)
		6	0	Stack Pointer - 2	1	Irrelevant Data (Note 1)
		7	0	Index Register	1	Irrelevant Data (Note 1)
		8	0	Index Register Plus Offset (w/o Carry)	1	Irrelevant Data (Note 1)
EXTENDED						
JMP	3	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Jump Address (High Order Byte)
		3	1	Op Code Address + 2	1	Jump Address (Low Order Byte)
ADC EOR ADD LDA AND ORA BIT SBC CMP SUB	4	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	1	Address of Operand	1	Operand Data
CPX LDS LDX	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	1	Address of Operand	1	Operand Data (High Order Byte)
		5	1	Address of Operand + 1	1	Operand Data (Low Order Byte)
STA A STA B	5	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Destination Address (High Order Byte)
		3	1	Op Code Address + 2	1	Destination Address (Low Order Byte)
		4	0	Operand Destination Address	1	Irrelevant Data (Note 1)
		5	1	Operand Destination Address	0	Data from Accumulator
ASL LSR ASR NEG CLR ROL COM ROR DEC TST INC	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	1	Address of Operand	1	Current Operand Data
		5	0	Address of Operand	1	Irrelevant Data (Note 1)
		6	1/0 (Note 3)	Address of Operand	0	New Operand Data (Note 3)

TABLE 8 - OPERATION SUMMARY (Continued)

Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
EXTENDED (Continued)						
STS STX	6	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Operand (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Operand (Low Order Byte)
		4	0	Address of Operand	1	Irrelevant Data (Note 1)
		5	1	Address of Operand	0	Operand Data (High Order Byte)
		6	1	Address of Operand + 1	0	Operand Data (Low Order Byte)
JSR	9	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Address of Subroutine (High Order Byte)
		3	1	Op Code Address + 2	1	Address of Subroutine (Low Order Byte)
		4	1	Subroutine Starting Address	1	Op Code of Next Instruction
		5	1	Stack Pointer	0	Return Address (Low Order Byte)
		6	1	Stack Pointer - 1	0	Return Address (High Order Byte)
		7	0	Stack Pointer - 2	1	Irrelevant Data (Note 1)
		8	0	Op Code Address + 2	1	Irrelevant Data (Note 1)
		9	1	Op Code Address + 2	1	Address of Subroutine (Low Order Byte)
INHERENT						
ABA OAA SEC ASL DEC SEI ASR INC SEV CBA LSR TAB CLC NEG TAP CLI NOP TBA CLR ROL TPA CLV ROR TST COM SBA	2	1 2	1 1	Op Code Address Op Code Address + 1	1 1	Op Code Op Code of Next Instruction
DES DEX INS INX	4	1 2 3 4	1 1 0 0	Op Code Address Op Code Address + 1 Previous Register Contents New Register Contents	1 1 1 1	Op Code Op Code of Next Instruction Irrelevant Data (Note 1) Irrelevant Data (Note 1)
PSH	4	1 2 3 4	1 1 1 0	Op Code Address Op Code Address + 1 Stack Pointer Stack Pointer - 1	1 1 0 1	Op Code Op Code of Next Instruction Accumulator Data Accumulator Data
PUL	4	1 2 3 4	1 1 0 1	Op Code Address Op Code Address + 1 Stack Pointer Stack Pointer + 1	1 1 1 1	Op Code Op Code of Next Instruction Irrelevant Data (Note 1) Operand Data from Stack
TSX	4	1 2 3 4	1 1 0 0	Op Code Address Op Code Address + 1 Stack Pointer New Index Register	1 1 1 1	Op Code Op Code of Next Instruction Irrelevant Data (Note 1) Irrelevant Data (Note 1)
TXS	4	1 2 3 4	1 1 0 0	Op Code Address Op Code Address + 1 Index Register New Stack Pointer	1 1 1 1	Op Code Op Code of Next Instruction Irrelevant Data Irrelevant Data
RTS	5	1 2 3 4 5	1 1 0 1 1	Op Code Address Op Code Address + 1 Stack Pointer Stack Pointer + 1 Stack Pointer + 2	1 1 1 1 1	Op Code Irrelevant Data (Note 2) Irrelevant Data (Note 1) Address of Next Instruction (High Order Byte) Address of Next Instruction (Low Order Byte)

TABLE 8 - OPERATION SUMMARY (Continued)

Address Mode and Instructions	Cycles	Cycle #	VMA Line	Address Bus	R/W Line	Data Bus
INHERENT (Continued)						
WAI	9	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Op Code of Next Instruction
		3	1	Stack Pointer	0	Return Address (Low Order Byte)
		4	1	Stack Pointer - 1	0	Return Address (High Order Byte)
		5	1	Stack Pointer - 2	0	Index Register (Low Order Byte)
		6	1	Stack Pointer - 3	0	Index Register (High Order Byte)
		7	1	Stack Pointer - 4	0	Contents of Accumulator A
		8	1	Stack Pointer - 5	0	Contents of Accumulator B
		9	1	Stack Pointer - 6 (Note 4)	1	Contents of Cond. Code Register
RTI	10	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Irrelevant Data (Note 2)
		3	0	Stack Pointer	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer + 1	1	Contents of Cond. Code Register from Stack
		5	1	Stack Pointer + 2	1	Contents of Accumulator B from Stack
		6	1	Stack Pointer + 3	1	Contents of Accumulator A from Stack
		7	1	Stack Pointer + 4	1	Index Register from Stack (High Order Byte)
		8	1	Stack Pointer + 5	1	Index Register from Stack (Low Order Byte)
		9	1	Stack Pointer + 6	1	Next Instruction Address from Stack (High Order Byte)
		10	1	Stack Pointer + 7	1	Next Instruction Address from Stack (Low Order Byte)
SWI	12	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Irrelevant Data (Note 1)
		3	1	Stack Pointer	0	Return Address (Low Order Byte)
		4	1	Stack Pointer - 1	0	Return Address (High Order Byte)
		5	1	Stack Pointer - 2	0	Index Register (Low Order Byte)
		6	1	Stack Pointer - 3	0	Index Register (High Order Byte)
		7	1	Stack Pointer - 4	0	Contents of Accumulator A
		8	1	Stack Pointer - 5	0	Contents of Accumulator B
		9	1	Stack Pointer - 6	0	Contents of Cond. Code Register
		10	0	Stack Pointer - 7	1	Irrelevant Data (Note 1)
		11	1	Vector Address FFFA (Hex)	1	Address of Subroutine (High Order Byte)
		12	1	Vector Address FFFB (Hex)	1	Address of Subroutine (Low Order Byte)
RELATIVE						
BCC BHI SNE BCS BLE BPL BEQ BLS BRA BGE BLT BVC BGT BMI BVS	4	1	1	Op Code Address	1	Op Code
2		1	Op Code Address + 1	1	Branch Offset	
3		0	Op Code Address + 2	1	Irrelevant Data (Note 1)	
4		0	Branch Address	1	Irrelevant Data (Note 1)	
BSR	8	1	1	Op Code Address	1	Op Code
		2	1	Op Code Address + 1	1	Branch Offset
		3	0	Return Address of Main Program	1	Irrelevant Data (Note 1)
		4	1	Stack Pointer	0	Return Address (Low Order Byte)
		5	1	Stack Pointer - 1	0	Return Address (High Order Byte)
		6	0	Stack Pointer - 2	1	Irrelevant Data (Note 1)
		7	0	Return Address of Main Program	1	Irrelevant Data (Note 1)
		8	0	Subroutine Address	1	Irrelevant Data (Note 1)

Note 1. If device which is addressed during this cycle uses VMA, then the Data Bus will go to the high impedance three-state condition. Depending on bus capacitance, data from the previous cycle may be retained on the Data Bus.

Note 2. Data is ignored by the MPU.

Note 3. For TST, VMA = 0 and Operand data does not change.

Note 4. While the MPU is waiting for the interrupt, Bus Available will go high indicating the following states of the control lines: VMA is low; Address Bus, R/W, and Data Bus are all in the high impedance state.

**MDS
LSI**
**TMS 4044 JL, NL; TMS 4046 JL, NL
4096-WORD BY 1-BIT STATIC RAMs**

NOVEMBER 1977

- 4096 x 1 Organization
- Single +5 V Supply ($\pm 10\%$ Tolerance)
- High Density 300-mil 18- and 20-Pin Packages
- Fully Static Operation (No Clocks, No Refresh, No Timing Strobe)
- 5 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)
TMS 4044-45, TMS 4046-45	450 ns	450 ns
TMS 4044-30, TMS 4046-30	300 ns	300 ns
TMS 4044-25, TMS 4046-25	250 ns	250 ns
TMS 4044-20, TMS 4046-20	200 ns	200 ns
TMS 4044-15, TMS 4046-15	150 ns	150 ns

- 400 mV Guaranteed DC Noise Immunity with Standard TTL Loads — No Pull-Up Resistors Required
- Common I/O Capability
- 3-State Outputs and Chip Select Control for OR-Tie Capability
- Fan-Out to 1 Series 74 or 74S TTL Load
- Power Dissipation

	TYPICAL	MAX
TMS 4044/46-25, -30, -45	275 mW	495 mW
TMS 4044/46-20, -15	440 mW	645 mW

description

This series of static random-access memories is organized as 4096 words of 1 bit. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. Because this series is fully static, chip select may be tied low to further simplify system timing. Output data is always available during a read cycle.

All inputs and outputs are fully compatible with Series 74 or 74S TTL. No pull-up resistors are required. The TMS 4044/4046 series is manufactured using TI's reliable N-channel silicon-gate technology to optimize the cost/performance relationship. Both the TMS 4044 and TMS 4046 are characterized to retain data at $V_{CC} = 2.4$ V to reduce power dissipation. Furthermore, for applications such as battery back-up, the TMS 4046 has separate V_{CC} pins for the array and periphery, and data will be retained if power to the array alone is maintained.

**TMS 4044
18-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)**

**TMS 4046
20-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)**

PIN NAMES	
A ₀ -A ₁₁	Addresses
D	Data In
Q	Data Out
$\bar{E}$	Chip Select
V _{CC} (TMS 4044)	+5 V Supply
V _{CC1} (TMS 4046)	+5 V Supply (array only)
V _{CC2} (TMS 4046)	+5 V Supply (periphery only)
V _{SS}	Ground
W	Write Enable

TMS 4044 JL, NL; TMS 4046 JL, NL 4096-WORD BY 1-BIT STATIC RAMs

The TMS 4044 series and the TMS 4046 series are offered in 18-pin and 20-pin respectively dual in-line ceramic (JL suffix) and plastic (NL suffix) packages designed for insertion in mounting-hole rows on 300 mil centers. The series is guaranteed for operation from 0°C to 70°C.

operation

addresses (A0-A11)

The twelve address inputs select one of the 4096 storage locations in the RAM. The address inputs must be stable for the duration of a write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip select ($\overline{S}$)

The chip-select terminal, which can be driven directly from standard TTL circuits, affects the data-in and data-out terminals. When chip select is at a logic low level, both terminals are enabled. When chip select is high, data-in is inhibited and data-out is in the floating or high-impedance state.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable terminal. A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ must be high when changing addresses to prevent erroneously writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.

data-in (D)

Data can be written into a selected device when the write enable input is low. The data-in terminal can be driven directly from standard TTL circuits.

data-out (Q)

The three-state output buffer provides direct TTL compatibility with a fan-out of one Series 74 TTL gate or one Series 74S TTL gate. The output is in the high-impedance state when chip select ($\overline{S}$) is high or whenever a write operation is being performed, facilitating device operation in common I/O systems. Data out is the same polarity as data-in.

standby operation

There are two basic standby modes available to retain data when operating the TMS 4044/4046 series:

1. Reduce the VCC supply to 2.4 V.
2. Supply power to the array only (TMS 4046 only).

Combining modes 1 and 2 on the TMS 4046 will produce the lowest possible standby power while retaining data.

DEVICE	SUPPLY	OPERATING	STANDBY	
TMS 4044	VCC	+5 V	+2.4 V	
TMS 4046	VCC1	+5 V	+5 V	+2.4 V
	VCC2	+5 V	0 V	0 V

(nominal supply values)

During standby operation, data can not be read or written into the memory. When resuming normal operation, five cycle times must be allowed after normal supplies are returned for the memory to resume steady state operating conditions.

TMS 4044 J1, N1; TMS 4046 J1, N1 4096-WORD BY 1-BIT STATIC RAMs

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1)	-0.5 to 7 V
Input voltage (any input) (see Note 1)	-0.5 to 7 V
Continuous power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-55°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to the ground terminal.

functional block diagram

recommended operating conditions

PARAMETER		MIN	NOM	MAX	LIMIT
Supply voltage, V_{CC} (TMS 4044)	Operating	4.5	5	5.5	V
	Standby	2.4	5	5.5	
Supply voltage (array only), V_{CC1} (TMS 4046)	Operating	4.5	5	5.5	V
	Standby	2.4	5	5.5	
Supply voltage (periphery only), V_{CC2} (TMS 4046)	Operating	4.5	5	5.5	V
	Standby	0	0	5.5	
Supply voltage, V_{SS}			0		V
High-level input voltage, V_{IH}		2		5.5	V
Low-level input voltage, V_{IL}		-0.3		0.8	V
Operating free-air temperature, T_A		0		70	°C

TMS 4044 JL, NL; TMS 4046 JL, NL 4096-WORD BY 1-BIT STATIC RAMs

electrical characteristics over recommended operating free-air temperature ranges(unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	High-level voltage	$I_{OH} = -200 \mu A$	$V_{CC} = 4.5 V$		2.4			V
V_{OL}	Low-level voltage	$I_{OL} = 2 mA$	$V_{CC} = 4.5 V$			0.4		V
I_I	Input current	$V_I = 0 V$ to 5.5 V					10	μA
I_{OZ}	Off-state output current	$V_O = 2 V$ or W at 0.3 V.	$V_O = 0 V$ to 5.5 V		-10		10	μA
I_{CC}	Supply current from V_{CC}	$I_O = 0 mA$, $T_A = 0^\circ C$ (worst case)	TMS 4044/46	$V_{CC} = 5.5 V$		50	90	mA
			-25, -30, -45	$V_{CC} = 2.4 V$		95		
			TMS 4044/46	$V_{CC} = 5.5 V$		80	118	
			-15, -20	$V_{CC} = 2.4 V$		70		
I_{CC1}	Supply current from V_{CC1} (array only) (TMS 4046 only)	$I_O = 0 mA$, $T_A = 70^\circ C$ (worst case)		$V_{CC} = 5.5 V$		8	28	mA
				$V_{CC} = 2.4 V$		11		
I_{CC2}	Supply current from V_{CC2} (periphery only) (TMS 4046 only)	$I_O = 0 mA$, $V_{CC} = 5.5 V$, $T_A = 0^\circ C$ (worst case)	TMS 4044/46-25, -30, -45				83	mA
			TMS 4044/46-15, -20				111	
C_i	Input capacitance	$V_I = 0 V$, $f = 1 MHz$					8	pF
C_o	Output capacitance	$V_O = 0 V$, $f = 1 MHz$					12	pF

† All typical values are at $V_{CC} = 5 V$, $T_A = 25^\circ C$.

timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		TMS 4044-15		TMS 4044-20		TMS 4044-25		TMS 4044-30		TMS 4044-45		UNIT
		TMS 4046-15		TMS 4046-20		TMS 4046-25		TMS 4046-30		TMS 4046-45		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CRD}	Read cycle time	150		200		250		300		450		ns
t_{CW}	Write cycle time	150		200		250		300		450		ns
t_{CRW}	Read-modify-write cycle time	250		320		370		460		650		ns
t_{WV}	Write pulse width	80		100		100		150		200		ns
$t_{A(A)}$	Address set up time	0		0		0		0		0		ns
$t_{A(S)}$	Chip select set up time	60		100		100		150		200		ns
$t_{A(D)}$	Data set up time	60		100		100		150		200		ns
$t_{H(D)}$	Data hold time	0		0		0		0		0		ns
$t_{H(A)}$	Address hold time	20		20		20		20		20		ns
$t_{T(A)}$	Address transition time	5 200		5 200		5 200		5 200		5 200		ns

TMS 4044 JL, NL; TMS 4046 JL, NL
4096-WORD BY 1-BIT STATIC RAMs

switching characteristics over recommended voltage range, $T_A = 0^\circ\text{C}$ to 70°C ,
 1 series 74 TTL load, $C_L = 100\text{ pF}$

PARAMETER	TMS 4044-15 TMS 4046-15			TMS 4044-20 TMS 4046-20		TMS 4044-25 TMS 4046-25		TMS 4044-30 TMS 4046-30		TMS 4044-45 TMS 4046-45		UNIT
	MIN	NOM	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{AD} Access time from address			150		200		250		300		450	ns
t_{AS} Access time from chip select low			70		70		70		100		100	ns
t_{AW} Access time from write enable high			70		70		70		100		100	ns
t_{PVX} Output data valid after address change	10			10		10		10		10		ns
$t_{PVZ,S}$ Output disable time after chip select high			50		50		50		50		100	ns
$t_{PVZ,W}$ Output disable time after write enable low			50		50		50		50		100	ns

read cycle timing**

All timing reference points are 0.9 V and 1.0 V on inputs and 0.6 V and 2.2 V on outputs (90% points). Input rise and fall times = 10 ns.

**Write enable is high for a read cycle.

TMS 4044 JL, NL; TMS 4046 JL, NL
4096-WORD BY 1-BIT STATIC RAMs

early write cycle timing

read-modify-write cycle timing

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APPENDIX E
ROM PROGRAM LISTING

```

1 * ; *****
2 * ; *
3 * ; * DART 2 FLOPPY DISK BOOTSTRAP LOADER *
4 * ; * VERSION 5.1 5/27/79 *
5 * ; *
6 * ; *****
7 * ;
8 * ; RAM FLOPPY DISK BOOTSTRAP LOADER
9 * ; ENT BOOT
10 * ; FREE
11 * ;
12 * ; FAIL FDIS 203
13 * ;
14 * ; *****
15 * ; *
16 * ; * RAM STORAGE LOCATIONS *
17 * ; *
18 * ; *****
19 * ;
20 * ; SIAC EQU 377
21 * ; IRACK EQU 356
22 * ; SECTOR EQU 355
23 * ; SECC EQU 353
24 * ; LOOPC EQU 352
25 * ; ADDRESS EQU 350
26 * ; FIRST EQU 347
27 * ; FATAL EQU 346
28 * ;
29 * ; ***** INITIALIZATION SECTION *****
30 * ;
31 * ; ORG 176000
32 * ;
33 * ; 176000 c27 BOOT STA A 10RS ;I/O/RESET
34 * ; 176101 007
35 * ;
36 * ;
37 * ; 176002 c28 LDA A 10RS
38 * ; 176103 007
39 * ; 176003 205 RLT A 01 ;CHECK FOR BATTERY POWER FAIL
40 * ; 176005 001
41 * ; 176006 006 ;JMP TO BTA IF BATTERY POWER FAILURE
  
```

```

176007 003
40 * 176010 176 JMP FAIL ;GO TO POWER FAIL ROUTINE IF BATTERYS GOOD
176011 000
176012 203
41 * 176013 001 BTA NOP
42 * 176014 017 SEI
43 * 176015 216 LDS #STAK ;SET STACK POINTER
176016 000
176017 377
44 * 176020 001 NOP ;2 NOP FOR ROM COMPATABILITY
45 * 176021 001 NOP
46 * 176022 206 LDA A #3
176023 003
47 * 176024 227 STA A ONF1 ;TURN ON ITY AND FLOPPY DRIVE
176025 020
48 * 176026 306 LDA B #5
176027 005
49 * 176030 327 STA B =LOOPE ;SET LOAD TRY COUNTER TO 5
176031 552
50 * 176032 177 CLR FATAL ;CLEAR FATAL ERROR FLAG
176033 000
176034 346
51 * 176035 206 LDA A #1
176036 001
52 * 176037 227 STA A INPS ;SELECT DRIVE UNIT 0
176040 051
53 * 176041 275 BA JSR RSTA ;GET STATUS OF DISK
176042 376
176043 155
54 * 176044 205 BIT A #200
176045 200
55 * 176046 446 BNE RA ;LOOP UNTIL DISK READY
176047 371
56 * 176050 327 STA B LITE ;TURN ON LOAD LIGHT
176051 056
57 * :
58 * : ***** RESTORE THE HEAD TO TRACK ZERO *****
59 * :
60 * 176052 206 010 LDA A #2 ;RESTORE=10 MSEC STEP=NO HLD
176053 002
61 * 176054 275 JSR LCOM ;EXECUTE COMMAND
176055 376

```



```

62 * 176456 207
      176457 275      JSR      SKPZ      ;WAIT UNTIL COMMAND DONE
      176460 376
      176463 253
63 * 176462 205      BIF A      #4      ;CHECK FOR TRACK ZERO
      176463 004
64 *
65 *
66 *
67 *
68 * 176464 046      BNE      BC      ;NOTE THAT THE I/O RESET SHOULD HAVE
      176465 017      ;POSITIONED THE HEAD AT TRACK ZERO.
69 * 176466 175      TST      LOOPC      ;THIS BIT OF CODE IS ADDED TO VERIFY
      176467 000      ;THIS ACTION.
      176470 552      ;WE ARE AT TRACK ZERO
70 * 176471 006      BNE      BAA1
      176472 005
71 * 176473 275      JSR      FA1      ;POSSIBLE FATAL ERROR
      176474 376
      176475 243
72 * 176476 040      BRA      BC      ;CONTINUE...HOPING FOR THE BEST..
      176477 005
73 * 176500 172 BAA1  DEC      LOOPC      ;DEC. LOAD TRIES COUNTER
      176501 000
      176502 452
74 * 176503 040      BRA      B16      ;TRY IT AGAIN
      176504 345
75 *
76 *
77 *
78 *
79 *
80 *
81 *
82 * 176505 206 BC    LDA A      #10      ;SET SECTOR 8 FOR READ
      176506 010
83 * 176507 275      JSR      LSEC
      176510 376
      176511 200
84 * 176512 516      LDX      #400      ;LOAD ADDRESS IS 400
      176513 001
      176514 006

```

```

***** THIS SECTION READS THE INDEX SECTOR *****
***** IT ASSUMES THE PROGRAM TO BE LOADED *****
***** IS ON FILE 1, INDEXED BY SECTOR 8 *****
***** ON TRACK 9 *****

```

```

85 * 176515 206 LDA A #4 ;SET HLD BIT
      176516 004
86 * 176517 275 JSR READ ;GO READ SECTOR
      176520 376
      176521 215
87 * 176522 275 JSR SKPBZ
      176523 376
      176524 253
88 * 176525 205 BIT A #34 ;CHECK FOR CRC,REC NOT FOUND,DATA LATE
      176526 034
89 * 176527 047 BEQ BE ;NO ERRORS
      176530 017
90 * 176531 175 TSF LOOPE
      176532 000
      176533 352
91 * 176534 046 BNE BD1
      176535 005
92 * 176536 275 JSR FAT
      176537 376
      176540 203
93 * 176541 040 BRA BE
      176542 005
94 * 176543 172 BD1 DEC LOOPE
      176544 000
      176545 352
95 * 176546 040 BRA BE ;RETRY THIS PART
      176547 335
96 * ;
97 * ; ***** NOW THAT WE HAVE THE INDEX IN MEMORY *****
98 * ; ***** LETS COMPUTE THE BEGINNING OF EXTENT *****
99 * ;
100 * 176550 316 BE LOX #434 ;LOC. OF 1ST CHAR. OF B.O.E.
      176551 001
      176552 034
101 * 176553 246 LOA A 0,X ;FETCH THIS EBCDIC CHAR.
      176554 000
102 * 176555 275 JSR M10 ;CONVERT TO BINARY
      176556 376
      176557 166
103 * 176558 253 ADD A 1,X ;ADD IN ONES DIGIT
      176561 001
104 * 176562 227 STA A =TRACK ;STORE IN PSEUDO TRACK REGISTER

```

```

176563 356
105 *      ?
106 *      ?
107 *      ? ***** GO SEEK THIS TRACK *****
108 *      ?
109 *      176564 275 JSR      SEEK
          176565 376
          176566 230
110 *      176567 275 JSR      SKP0Z
          176570 376
          176571 253
111 *      176572 205 BIT A    #30      ;ERROR?
          176573 030
112 *      176574 047 BEQ      BG      ;NO
          176575 017
113 *      176576 175 TST      LOOPE
          176577 000
          176600 352
114 *      176601 006 BNE      BF1
          176602 005
115 *      176603 275 JSR      FAT
          176604 376
          176605 203
116 *      176606 040 BRA      BG      ;FORCE LOAD--ASKING FOR TROUBLE
          176607 005
117 *      176610 172 BE1      DEC      LOOPE
          176611 000
          176612 352
118 *      176613 040 BRA      BE      ;RETRY THIS SECTION
          176614 353
119 *      ?
120 *      ? ***** COMPUTE 1ST SECTOR TO LOAD *****
121 *      ?
122 *      176615 316 BG      LOX      #037      ;ADDRESS OF SECTOR MSU
          176616 001
          176617 037
123 *      176620 246 LDA A    0,X
          176621 000
124 *      176622 275 JSR      #10
          176623 376
          176624 166
125 *      176625 253 ADD A    1,X

```

```

126 * 176626 001          STA A  =SECTOR          ;STORE IN SECTOR PSEUDO REGISTER
      176627 227
      176630 355
127 * 176631 275          JSR      LSEC          ;LOAD SECTOR REGISTER
      176632 376
      176633 200

128 *
129 *
130 *
131 * 176634 316          LDX      #100000          ;32K +1
      176635 200
      176636 000
132 * 176637 200          LOA A  #377
      176640 377
133 * 176641 247          STA A  0,X
      176642 000
134 * 176643 143          COM      1,X          ;CLEAR DATA BUSS
      176644 001
135 * 176645 155          TST      0,X          ;WHATS REALLY THERE?
      176646 000
136 * 176647 047          BEQ      BH          ;IF ZERO, ONLY 32K MEMORY
      176650 005
137 * 176651 316          LDX      #1506          ;SECTOR COUNT FOR 64K LOAD
      176652 001
      176653 372
138 * 176654 040          BKA      BI
      176655 003
139 * 176656 316 BH       LDX      #1254          ;SECTOR COUNT FOR 32K LOAD
      176657 000
      176660 376
140 * 176661 537 BI       STX      =SECC          ;STORE IN SECTOR COUNTER
      176662 553
141 * 176663 316          LDX      #000          ;SET LOAD LOCATION
      176664 001
      176665 000
142 * 176666 537          STX      =ADDS
      176667 350
143 * 176670 177          CLR      FIRST          ;INDICATE HLD BY SETTING FIRST=0
      176671 000
      176672 307

144 *
145 *
      ***** MAIN LOAD LOOP *****

```

FLOPPY

5/22/79

14:55:12

PAGE 7

146 *					
147 *	176673 336	HLDP	LDX	=ADDRESS	;GET LOAD ADDRESS
	176674 330				
148 *	176675 117		CLK A		;ASSUME HEAD LOADED
149 *	176676 175		IST	FIRST	;DO WE WANT HEAD LOADED? (HLD)
	176677 000				
	176678 347				
150 *	176679 046		BNE	HLA	;NO--ALREADY LOADED
	176680 002				
151 *	176681 206		LOA A	#4	;YES-SET BIT FOR HLD
	176682 004				
152 *	176683 275	HLA	JSR	READ	;READ 1 SECTOR INTO MEMORY
	176684 374				
	176685 215				
153 *	176686 174		INC	FIRST	;BUMP HLD FLAG
	176687 000				
	176688 347				
154 *	176689 275		JSR	SKPRZ	;WAIT UNTIL READ DONE
	176690 376				
	176691 253				
155 *	176692 205		BIT A	#34	;ANY ERRORS?
	176693 030				
156 *	176694 047		BFD	OK	;NO
	176695 017				
157 *	176696 175		IST	LODPC	
	176697 000				
	176698 352				
158 *	176699 046		BNE	HLA	
	176700 005				
159 *	176701 275		JSR	FAT	
	176702 376				
	176703 243				
160 *	176704 040		BPA	OK	
	176705 005				
161 *	176706 172	BFI	BFC	LODPC	
	176707 000				
	176708 352				
162 *	176709 040		BPA	HLDP	;RETRY THIS SECTION
	176710 352				
163 *	176711 336	OK	LDX	=SFIC	
	176712 353				
164 *	176713 031		DEX		;DEC. SECTOR COUNTER TO SEE IF DONE

165 *	176748 357	STX	=SECL	
	176749 353			
166 *	176749 007	BEQ	DONE	;DONE IF COUNTER=0
	176751 101			
167 *	176750 174	INC	SECTOR	;INC. SECTOR PSEUDO REGISTER
	176751 000			
	176752 355			
168 *	176753 226	LDA A	=SECTOR	
	176754 355			
169 *	176755 201	CPX A	#127	;IF SECTOR=27, WE ARE DONE WITH THIS TRACK
	176755 033			
170 *	176757 147	BEQ	HI	;GO START NEW TRACK
	176759 023			
171 *	176761 226 04	LDA A	=SECTOR	
	176762 355			
172 *	176763 275	JSR	LSFC	;LOAD CONTROLLER SECTOR REGISTER
	176764 376			
	176765 200			
173 *	176766 326	LDA B	=ADDRESS+1	
	176767 351			
174 *	176770 226	LDA A	=ADDRESS	
	176771 350			
175 *	176772 313	ADD B	#128	;BUMP MEMORY POINTER BY 128 BYTES(1 SECTOR)
	176773 200			
176 *	176774 231	ADC A	#0	
	176775 006			
177 *	176775 327	STA H	=ADDRESS+1	
	176777 351			
178 *	177000 227	STA A	=ADDRESS	;RESTORE UPDATED VALUE
	177001 350			
179 *	177002 040	MOVA	MLDR	
	177003 257			
180 *	177004 205 0L	LDA A	#1	
	177005 001			
181 *	177006 227	STA F	=SECTOR	;RESET SECTOR TO 1
	177007 355			
182 *	177010 177	TRL	TRACK	;BUMP TRACK POINTER
	177011 000			
	177012 356			
183 *	177013 177	CLR	FIRST	;RESET HLD FLAG
	177014 000			
	177015 307			

FLOPPY

5/22/79

14:55:23

PAGE 9

184 *	177016 206 80	LOA A	#122	:LOAD STEP-IN COMMAND
	177017 122			
185 *	177020 275	JSR	LEOM	:EXECUTE
	177021 376			
	177022 207			
186 *	177023 275	JSR	SKPHZ	:WAIT TILL DONE
	177024 376			
	177025 253			
187 *	177026 205	BIT A	#30	:ERRORS?
	177027 030			
188 *	177030 047	BEQ	BA	:NO--GO LOAD SECTOR REG/INC. ADDRESS FOR READ
	177031 327			
189 *	177032 175	TSI	LOOPE	
	177033 000			
	177034 352			
190 *	177035 046	BNE	BN1	
	177036 005			
191 *	177037 275	JSR	FAT	
	177040 376			
	177041 203			
192 *	177042 040	BRA	BM	
	177043 315			
193 *	177044 172 BN1	DEC	LOOPE	
	177045 000			
	177046 352			
194 *	177047 040	BRA	GO	:TRY AGAIN
	177050 345			
195 *	177051 206 DONE	LOA A	#176	:SEEK TRACK 76--HEAD IS POSITIONED HERE
	177052 114			
196 *	177053 215	BSR	SEEK	:TO AVOID GLITCHES ON TRACKS WITH DATA
	177054 153			
197 *	177055 275	JSR	SKPHZ	
	177056 376			
	177057 253			
198 *	177060 205	BIT A	#30	:SEEK ERROR?
	177061 030			
199 *	177062 047	BEQ	002	:NO
	177063 016			
200 *	177064 175	TSI	LOOPE	
	177065 000			
	177066 352			
201 *	177067 046	BNE	003	

	177070 000			
202 *	177071 215	BSR	FAT	
	177072 150			
203 *	177073 040	BRA	DD2	
	177074 005			
204 *	177075 172 DD3	DEC	LOOPO	
	177076 000			
	177077 352			
205 *	177100 040	BRA	DONE	;ONE MORE TIME
	177101 307			
206 *	177102 117 DD2	CLR A		
207 *	177103 227	STA A	INT1	;CLEAR INTERRUPT MASKS
	177104 000			
208 *	177105 227	STA A	INT2	
	177106 001			
209 *	177107 175	IST	FATAL	;TEST FOR LOAD ERRORS
	177110 000			
	177111 306			
210 *	177112 047	BEO	DON4	;NONE
	177113 022			
211 *	177114 316	LOX	#MSG	;GET ERROR MESSAGE
	177115 376			
	177116 266			
212 *	177117 206 DDN2	LDA A	0,X	
	177120 000			
213 *	177121 047	BEO	DON1	;MESSAGE SENT
	177122 020			
214 *	177123 326 DDN3	LDA B	SSY1	
	177124 002			
215 *	177125 305	BIT B	#2	;TTY BUSY?
	177126 002			
216 *	177127 046	BNE	DON3	;LOOP UNTIL NOT BUSY
	177130 372			
217 *	177131 227	STA A	TTY0	;OUTPUT CHARACTER TO TTY
	177132 040			
218 *	177133 010	INX		;GET NEXT CHAR.
219 *	177134 040	BRA	DON2	
	177135 361			
220 *	177136 316 DDN4	LOX	#MSG	;SUCCESSFUL LOAD MESSAGE
	177137 376			
	177140 310			
221 *	177141 040	BRA	DON2	


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177142 354
222 * 177143 200 DONS CIA A #1
177140 001
224 * 177145 227 STA A OFF1 ;TURN OFF FLOPPY DRIVE
177146 020
224 * 177147 117 CLR A
225 * 177150 227 STA A LITE ;TURN OFF LOAD LIGHT
177151 056
226 * 177152 116 JMP 400 ;GO TO LOADED PROGRAM
177153 001
177154 000

227 * ;
228 * ; ***** READ STATUS OF CONTROLLER *****
229 * ;
230 * 177155 200 RSTA LDA A #0 ;SELECT READ-COMMAND REGISTER
177156 004
231 * 177157 227 STA A COMR
177160 050
232 * 177161 226 LDA A COMR
177162 050
233 * 177163 225 LDA A INPS
177164 053
234 * 177165 071 RTS
235 * ;
236 * ;
237 * ; ***** 2 ASCII CHARS. TO BINARY *****
238 * ;
239 * 177166 200 RLO SHL A #8F0
177167 566
240 * 177170 110 ASL A
241 * 177171 025 TFS
242 * 177172 110 ASL A
243 * 177173 110 ASL A
244 * 177174 053 AND A
245 * 177175 200 SHL A #8F0
177176 561
246 * 177177 071 RTS
247 * ;
248 * ; ***** LOAD SECTOR REGISTER *****
249 * ;
250 * 177180 500 LSHC LDA B #2
177181 012

```

```

251 * 177202 327 STA B COMR
      177203 050
252 * 177204 227 STA A LD00
      177205 052
253 * 177206 071 RTS
254 *
255 *
256 * ***** LOAD COMMAND REGISTER *****
257 * (DO NOT USE IF READ/WRITE FLAGS ARE TO BE SET)
258 *
258 * 177207 137 LCOM CLR R
259 * 177210 327 STA R COMR
      177211 050
260 * 177212 227 STA A LD00
      177213 052
261 * 177214 071 RTS
262 *
263 * ***** READ 1 SECTOR SUBROUTINE *****
264 *
265 * 177215 337 READ SIX DMA0 ;LOAD DMA TRANSFER REGISTER(S)
      177216 054
266 * 177217 306 LDA B #10 ;SET COMMAND REG--SET READ BIT
      177218 010
267 * 177221 327 STA R COMR
      177222 050
268 * 177223 212 ORA A #210 ;READ 1 SECTOR--HLD OPTIONAL
      177224 210
269 * 177225 227 STA A LD00
      177226 052
270 * 177227 071 RTS
271 *
272 * ***** SEEK SUBROUTINE *****
273 * (ASSUMES DESIRED TRACK IS IN REG. A)
274 *
275 * 177230 306 SEEK LDA B #3 ;SELECT DATA REGISTER
      177231 003
276 * 177232 327 STA R COMR
      177233 050
277 * 177234 227 STA A LD00 ;SELECT DESIRED TRACK
      177235 052
278 * 177236 206 LDA A #22 ;SET SEEK COMMAND
      177237 022
279 * 177240 215 BSR LCOM ;EXECUTE

```

```

177241 345
280 * 177242 071      RTS
281 *      ;
282 *      ;          ***** FATAL ERROR ROUTINE *****
283 *      ;
284 * 177243 306 FAT    LDA B    #5
177244 005
285 * 177245 327      STA B    =LOOPC      ;RESET LOOP COUNTER
177246 352
286 * 177247 174      INC      FATAL      ;SET FATAL ERROR FLAG
177250 000
177251 346
287 * 177252 071      RTS
288 *      ;
289 *      ;          ***** WAIT UNTIL DISK NOT BUSY *****
290 *      ;          (THIS CODE ALSO CLEARS BUSY/DONE AND RETURNS THE STATUS REG)
291 *      ;
292 * 177253 226 SKPBZ   LDA A    BSY1
177254 002
293 * 177255 205      BIT A    #200
177256 200
294 * 177257 046      BNE      SKPBZ      ;LOOP UNTIL BUSY=0
177260 372
295 * 177261 215      BSR      RSTA      ;GET STATUS REGISTER INTO REG. A
177262 272
296 * 177263 227      STA A    CLEA      ;CLEAR BUSY/DONE
177264 057
297 * 177265 071      RTS
298 *      ;
299 *      ;          ***** HD01STRAP LOADER MESSAGES *****
300 *      ;
301 * 177266 114 MSG    FCC      "LOAD ERRORS<15><12><7><7><7><7>"
177267 117
177270 104
177271 100
177272 040
177273 105
177274 122
177275 122
177276 117
177277 122
177300 123

```

FLOPPY

5/22/74

14:55:50

PAGE 14

177501 015
177502 012
177503 007
177504 007
177505 007
177506 007
177507 000
177510 114
177511 117
177512 101
177513 104
177514 000
177515 103
177516 117
177517 115
177520 120
177521 114
177522 105
177523 124
177524 105
177525 104
177526 015
177527 012
177530 000

302 * 177510 114 MSG FCC *LOAD COMPLETED<15><12>*

303 * END

LINE REFERENCES

ADDS	E	000006 *	25	142	147	175	174	177	178
BA	E	176491 *	53	55					
BAA1	F	176500 *	70	73					
BC	E	176505 *	66	72	82	95			
BU1	E	176543 *	91	94					
BF	E	176550 *	89	93	100	110			
BF1	E	176610 *	114	117					
BG	F	176615 *	112	116	122				
BH	F	176656 *	146	159					
BI	E	176661 *	139	140					
BJ1	E	176719 *	158	161					
BK	E	176741 *	156	160	163				
BL	E	177004 *	170	180					
BN	F	176761 *	171	188	192				
BW1	E	177044 *	190	193					
BO	E	177016 *	184	194					
BOOT	E	176400 *	9	33					
BT4	E	176413 *	59	41					
BTH	F	176452 *	60	74					
D02	F	177102 *	199	203	206				
D03	E	177075 *	201	204					
DON1	E	177103 *	213	222					
DON2	F	177117 *	212	219	221				
DON3	E	177123 *	214	216					
DON4	F	177136 *	210	220					
DONE	E	177051 *	166	195	205				
EMSG	F	177266 *	231	301					
FAIL	E	000000 *	12	40					
FAT	F	177203 *	71	92	115	159	191	202	284
FATAL	E	000000 *	27	50	209	286			
FIRST	E	000000 *	26	143	149	153	183		
LCON	F	177207 *	61	185	258	279			
LOOPC	F	000000 *	28	49	69	75	90	94	113
LSEC	F	177200 *	33	127	172	250			
MIO	E	177161 *	102	124	239				
MLA	F	176705 *	150	152					
NLOOP	F	176678 *	157	162	179				
MSG	E	177310 *	220	302					
READ	E	177215 *	66	152	265				
RSTA	F	177155 *	53	230	295				

14:56:29

SECC	E	000000	*	25	140	165	165				
SECTOR	E	000000	*	22	126	167	168	171	181		
SEEK	E	177230	*	109	196	275					
SKP02	E	177253	*	87	87	110	154	165	197	292	294
STAK	E	000000	*	20	45						
TRACK	E	000000	*	21	104	182					

APPENDIX F

6800 MICROPROCESSOR INSTRUCTION SET,
OCTAL LISTING

C40 196 DIR IND EXT IND REL

ARA	*	*	*	*	*	433	*	*
ABCA	*	211	* 231	* 251	* 271	*	*	*
ADCB	*	311	* 331	* 351	* 371	*	*	*
ADDA	*	213	* 233	* 253	* 273	*	*	*
ADDB	*	313	* 333	* 353	* 373	*	*	*
ANDA	*	244	* 224	* 244	* 244	*	*	*
ANDB	*	344	* 324	* 344	* 344	*	*	*
ASL	*	*	*	154	* 174	*	*	*
ASLA	*	*	*	*	*	114	*	*
ASLB	*	*	*	*	*	134	*	*
ASR	*	*	*	147	* 167	*	*	*
ASRA	*	*	*	*	*	147	*	*
ASRB	*	*	*	*	*	127	*	*
BCC	*	*	*	*	*	*	244	*
BCS	*	*	*	*	*	*	245	*
BEO	*	*	*	*	*	*	247	*
BGE	*	*	*	*	*	*	254	*
BGT	*	*	*	*	*	*	256	*
BHI	*	*	*	*	*	*	242	*
BI1A	*	225	* 225	* 245	* 265	*	*	*
BI1B	*	325	* 325	* 345	* 365	*	*	*
BLE	*	*	*	*	*	*	257	*
BLS	*	*	*	*	*	*	243	*
BCT	*	*	*	*	*	*	255	*
BHI	*	*	*	*	*	*	253	*
BNE	*	*	*	*	*	*	246	*
BPL	*	*	*	*	*	*	252	*
BRA	*	*	*	*	*	*	244	*
BSR	*	*	*	*	*	*	215	*
BVC	*	*	*	*	*	*	250	*
BVS	*	*	*	*	*	*	251	*
CHA	*	*	*	*	*	421	*	*
CLC	*	*	*	*	*	414	*	*
CLI	*	*	*	*	*	215	*	*
CLR	*	*	*	157	* 177	*	*	*
CLRA	*	*	*	*	*	117	*	*
CLRB	*	*	*	*	*	137	*	*
CLV	*	*	*	*	*	412	*	*
CMPA	*	241	* 221	* 241	* 261	*	*	*
CMPB	*	341	* 321	* 341	* 361	*	*	*

WORLDWIDE **CORPORATION**

CMQ IMM DIR IND EXT TNA REL

COM	*	*	*	143	*	163	*	*
COMA	*	*	*	*	*	103	*	*
COMB	*	*	*	*	*	123	*	*
CPK	*	214	*	234	*	254	*	274
DAA	*	*	*	*	*	231	*	*
DEC	*	*	*	152	*	172	*	*
DECA	*	*	*	*	*	112	*	*
DECB	*	*	*	*	*	132	*	*
DES	*	*	*	*	*	254	*	*
DEX	*	*	*	*	*	211	*	*
EORA	*	214	*	234	*	254	*	274
EORH	*	314	*	334	*	354	*	374
INC	*	*	*	154	*	174	*	*
INCA	*	*	*	*	*	114	*	*
INCH	*	*	*	*	*	134	*	*
INS	*	*	*	*	*	261	*	*
INX	*	*	*	*	*	210	*	*
JMP	*	*	*	156	*	176	*	*
JSR	*	*	*	255	*	275	*	*
LDAA	*	246	*	226	*	246	*	266
LDAB	*	346	*	326	*	346	*	366
LDS	*	216	*	236	*	256	*	276
LOX	*	316	*	336	*	356	*	376
LSR	*	*	*	144	*	164	*	*
LSRA	*	*	*	*	*	104	*	*
LSRB	*	*	*	*	*	124	*	*
NEG	*	*	*	144	*	164	*	*
NEGA	*	*	*	*	*	104	*	*
NEGB	*	*	*	*	*	124	*	*
NOP	*	*	*	*	*	201	*	*
ORAA	*	212	*	232	*	252	*	272
ORAB	*	312	*	332	*	352	*	372
PSHA	*	*	*	*	*	265	*	*
PSHB	*	*	*	*	*	267	*	*
PULA	*	*	*	*	*	262	*	*
PULB	*	*	*	*	*	263	*	*
ROL	*	*	*	161	*	171	*	*
ROLA	*	*	*	*	*	111	*	*
ROLB	*	*	*	*	*	131	*	*
ROF	*	*	*	146	*	166	*	*

CMD	INM	OIR	INO	EXT	INH	REL
RORA *	*	*	*	*	106 *	*
RORR *	*	*	*	*	126 *	*
RTI *	*	*	*	*	273 *	*
RTS *	*	*	*	*	271 *	*
SHA *	*	*	*	*	222 *	*
SBCA *	242 *	222 *	242 *	262 *	*	*
SBCB *	342 *	322 *	342 *	362 *	*	*
SEC *	*	*	*	*	215 *	*
SEI *	*	*	*	*	217 *	*
SEV *	*	*	*	*	213 *	*
STAA *	*	227 *	247 *	267 *	*	*
STAB *	*	327 *	347 *	367 *	*	*
STS *	*	237 *	257 *	277 *	*	*
STX *	*	337 *	357 *	377 *	*	*
SIIBA *	244 *	224 *	244 *	264 *	*	*
SIBB *	344 *	324 *	344 *	364 *	*	*
SWI *	*	*	*	*	277 *	*
TAB *	*	*	*	*	226 *	*
TAP *	*	*	*	*	226 *	*
TBA *	*	*	*	*	227 *	*
TPA *	*	*	*	*	227 *	*
TST *	*	*	155 *	175 *	*	*
TSTA *	*	*	*	*	115 *	*
TSTB *	*	*	*	*	135 *	*
TSX *	*	*	*	*	262 *	*
TXS *	*	*	*	*	265 *	*
NAI *	*	*	*	*	276 *	*

APPENDIX G

CABLE LISTS

Interior Cable Assemblies

<u>CABLE</u>	<u>TITLE</u>	<u>DRAWING</u>
	Cable Interconnect Diagram	500C3297-001
W6, W9	Async ports 1&2	500A3319-001
W7	ADC display data	500A3316-001
W8	Disk data	500A3318-001
W10	Device controller	500A3394-001
W11	Status input (or I/O controller)	500A3378-*
W12	Mag tape	500A3395-001
W13	Async port 3	500A3267-001
W18, W19	Analog inputs from J18 & J19	500A3310-*
W20, W21	Analog inputs from TB1, TB2, TB3 & TB4	500A3379-*
W23	Rainfall & Ext. interrupt	500A3314-001
W28	Mother Board power	500A3374-001
W29	M.B. battery pwr, DVC signals, 60 Hz.	500A3377-001
W30	AC power cord	500A3328-001
W31, W32, W33	Fan power	500A3313-*
W34	AC power switch	500A3315-001
W34A, W35, W37, W39	AC power switch, AC power to DC supplies	500A3312-*
W36	DC power, 5V.	5003368-001
W38	DC power, 15V.	500A3369-001
W40	DC power, 24V.	500A3370-001
W41	AC power, TTY	500A3327-001
W42	AC power, Disk	500A3324-001
W43	DC power, Disk	500A3323-001
W44	Battery, 12 V.	500A3372-001
W45	DC power, 4 volt	500A3371-001
W48	Clock set switch	500A3325-001
W50	ADC display data	5-0A3373-001

Interior Cable Assemblies (contd.)

<u>CABLE</u>	<u>TITLE</u>	<u>DRAWING</u>
W51	Gain select switch	500A3322-001
W52,W47	ADC display power; Battery Clock display power	500A3376-*
W53	Thermal limit switch	500A3326-001
W54	Channel select switch	500A3321-001
W55	Prog. load light; TTY & Disk Switches & lights	500A3311-001
W56	Status lights	500A3375-001
---	Relays RL1 & RL4	500A3381-*

External Cable Assemblies

P19, Analog Ch.00-17 to P2, Term. Panel

P18, Analog Ch.20-37 to P3, Term. Panel

P11, IOC or SIC to P5, Term. Panel

P10, DVC to P1, Device Controller Panel

P6, Async port 1 to Model 43 (Male connector)

P6, Async port 1 to Model 43 (Female connector)

P9, Async port 2 to Modem

P12, Mag.Tape Interface to P1, Mag tape unit

P24, Device Controller Panel to P24, Terminal Panel

12-Bit Successive Approximation Integrated Circuit A/D Converter

AD572

FEATURES

Performance

True 12-Bit Operation: Max Nonlinearity $< \pm 0.012\%$
Low Gain T.C.: $< \pm 15\text{ppm}/^\circ\text{C}$ (AD572B)
Low Power: 900mW
Fast Conversion Time: $< 25\mu\text{sec}$
Monotonic Feedback DAC Guarantees No Missing Codes
Hermetically-Sealed, Electrostatically-Shielded DIP

Versatility

Military/Aerospace Temperature Range:
-55 to $+125^\circ\text{C}$ (AD572S)
MIL-STD-883B Processing Available
Positive-True Serial or Parallel Logic Outputs
Short-Cycle Capability

Value

Precision $+10\text{V}$ Reference for External Application
Internal Buffer Amplifier
High Reliability Welded Metal Package
Low Cost: \$95.00 (1-24 pcs, AD572A)

GENERAL DESCRIPTION

The AD572 is a complete 12-bit successive approximation analog-to-digital converter that includes an internal clock, reference, comparator, and buffer amplifier. Its hybrid IC design utilizes MSI digital and linear monolithic chips and active laser trimming of high-stability thin-film resistors to provide modular performance, flexibility, and ease of use, combined with IC size, price, and reliability.

Important performance characteristics of the AD572 include a maximum linearity error at 25°C of $\pm 0.012\%$, gain T.C. below $15\text{ppm}/^\circ\text{C}$, typical power dissipation of 900mW, and conversion time of less than $25\mu\text{sec}$. Of considerable significance in military and aerospace applications is the guaranteed performance from -55 to $+125^\circ\text{C}$ of the AD572S, and the availability of units processed to MIL-STD-883B. Monotonic operation of the feedback D/A converter guarantees no missing output codes over temperature ranges of 0 to $+70^\circ\text{C}$, -25 to $+85^\circ\text{C}$, and -55 to $+125^\circ\text{C}$.

The design of the AD572 includes scaling resistors that provide analog input signal ranges of ± 2.5 , ± 5 , ± 10 , 0 to $+5$, or 0 to $+10$ volts. Adding flexibility and value are the $+10\text{V}$ precision reference, which also can be used for external applications, and the input buffer amplifier. All digital signals are fully DTL and TTL compatible, and the data output is positive-true and available in either serial or parallel form.

The AD572 is packaged in a hermetically-sealed, all-metal DIP. Welding rather than solder sealing eliminates any possibility of contamination from flux and solder particles. The metal construction provides excellent shielding from random electrostatic and/or electromagnetic radiation which could cause incorrect output codes. To insure a level of reliability consistent with its performance, each AD572 receives a stringent pre-cap visual inspection, high temperature storage and temperature cycling, acceleration testing, fine and gross leak testing, and operating burn-in.

The AD572 is available in three versions with differing guaranteed performance characteristics and operating temperature ranges; the "A" and "B" are specified from -25 to $+85^\circ\text{C}$, and the "S" from -55 to $+125^\circ\text{C}$.

PRODUCT DESCRIPTION

The AD572 functional diagram and pin-out are shown in Figure 1. The device consists of the following monolithic bipolar transistor and thin-film resistor circuit elements:

- 1 12-bit successive-approximation register
- 2 12-bit feedback DAC weighing network
- 3 low-drift comparator
- 4 temperature-compensated precision $+10\text{V}$ reference
- 5 high-impedance buffer follower
- 6 gated clock and digital control circuits

(continued on page 3)

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Tel: 617/329-4700 TWX: 710/394-6577
West Coast Mid-West Texas
213/595-1783 312/894-3300 214/231-5094

SPECIFICATIONS

(typical @ +25°C, ±15V and +5V unless otherwise noted)

MODEL	AD572AD	AD572BD	AD572SD
RESOLUTION	12 Bits	*	*
ANALOG INPUTS			
Voltage Ranges			
Bipolar	±2.5, ±5.0, ±10.0V	*	*
Unipolar	0 to +5, 0 to +10V	*	*
Impedance (Direct Input)			
0 to +5V, ±2.5V	2.5kΩ	*	*
0 to +10V, ±5V	1.0kΩ	*	*
±10V	10kΩ	*	*
Buffer Amplifier			
Impedance (min)	100MΩ	*	*
Bias Current	50nA	*	*
Settling Time to 0.01% of FSR for 20V step	2μsec	*	*
DIGITAL INPUTS			
Convert Command	Note 1	*	*
Logic Loading	1 TTL Load	*	*
TRANSFER CHARACTERISTICS			
Gain Error (Note 2)	±0.05% FSR (Adj to Zero)	*	*
Unipolar Offset Error	±0.05% FSR (Adj to Zero)	*	*
Bipolar Offset Error	±0.1% FSR (Adj to Zero)	*	*
Linearity Error (max)	0.012% FSR	*	*
Inherent Quantization Error	±½ LSB	*	*
Differential Linearity Error	±½ LSB	*	*
No Missing Codes	Guaranteed: 0 to +70°C	Guaranteed: -25 to +85°C	Guaranteed: -55 to +125°C
Power Supply Sensitivity			
±15V	±0.002% FSR/ΔV _S	*	*
+5V	±0.001% FSR/ΔV _S	*	*
TEMPERATURE COEFFICIENTS			
Gain (max)	±30ppm/°C (-25 to +85°C)	±15ppm/°C (-25 to +85°C)	±15ppm/°C (-25 to +85°C) ±25ppm/°C (-55 to +125°C)
Unipolar Offset	±3ppm FSR/°C	±3ppm FSR/°C (max)	**
Bipolar Offset (max)	±15ppm FSR/°C	±7ppm FSR/°C	**
Linearity	±3ppm FSR/°C	±2ppm FSR/°C	**
CONVERSION TIME (max)	25μsec	*	*
DIGITAL OUTPUTS (All Codes Positive-True)			
Parallel Data			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary/Two's Complement	*	*
Output Drive	2 TTL Loads	*	*
Serial Data (NRZ format)			
Unipolar Code	Binary	*	*
Bipolar Code	Offset Binary	*	*
Output Drive	2 TTL Loads	*	*
Status	Logic "1" during Conversion	*	*
Status	Logic "0" during Conversion	*	*
Output Drive	2 TTL Loads	*	*
Internal Clock			
Output Drive	2 TTL Loads	*	*
Frequency	500kHz	*	*
INTERNAL REFERENCE VOLTAGE			
Max External Current	±10.00V, ±5mV	*	*
Voltage Temperature Coefficient (max)	±4mA	*	*
	±20ppm/°C	±10ppm/°C	**
POWER REQUIREMENTS			
Supply Voltages/Currents			
+15V, ±5% @ +25mA		*	*
-15V, ±5% @ -20mA		*	*
+5V, ±5% @ +50mA		*	*
Total Power Dissipation	925mW	*	*
TEMPERATURE RANGE			
Specification	-25 to +85°C	*	-55 to +125°C
Operating	-55 to +125°C	*	*
Storage	-55 to +150°C	*	*

*Same specification as AD572AD

**Same specification as AD572BD

Specifications subject to
change without notice

Note 1: Positive pulse 200nsec wide (min). Leading edge
('0' to '1') resets registers. Trailing edge
('1' to '0') initiates conversion.

Note 2: With 500, 1% fixed resistor in place of Gain
Adjust pot. see Figures 4 and 5.

ASYNCHRONOUS RECEIVER/TRANSMITTER

FEATURES

- SILICON GATE TECHNOLOGY — LOW THRESHOLD circuitry
Directly TTL and CMOS Compatible
- SINGLE POWER SUPPLY — +5 VDC ONLY
- D.C. STABLE (STATIC) CIRCUITRY
- FULL DUPLEX OR HALF DUPLEX OPERATION
Transmits and Receives Serial Data Simultaneously or Alternately
- AUTOMATIC INTERNAL SYNCHRONIZATION OF DATA AND CLOCK
- AUTOMATIC START BIT GENERATION
- BUFFERED RECEIVER AND TRANSMITTER REGISTERS
- FULLY PROGRAMMABLE — EXTERNALLY SELECTABLE
Word Length
Baud Rate
Even/Odd Parity (Receiver/Verification — Transmitter/Generation)
Parity Inhibit — Verification/Generation
One, One and One-Half, or Two Stop Bit Generation
- AUTOMATIC DATA RECEIVED/TRANSMITTED STATUS GENERATION
Transmission Complete
Buffer Register Transfer Complete
Received Data Available
Parity Error
Framing Error
Overrun Error
- THREE-STATE OUTPUTS
Receiver Register Outputs
Status Flags
- AVAILABLE IN CERAMIC OR HERMETIC PLASTIC CAVITY PACKAGES

APPLICATIONS

PERIPHERALS	CARD AND TAPE READERS
TERMINALS	PRINTERS
MINI COMPUTERS	DATA SETS
FACSIMILE	CONTROLLERS
TRANSMISSION	KEYBOARD ENCODERS
MODEMS	REMOTE DATA
CONCENTRATORS	ACQUISITION SYSTEMS
ASYNCHRONOUS DATA	ASYNCHRONOUS DATA
MULTIPLEXERS	CASSETTES

GENERAL DESCRIPTION

The TR1863A and the TR1863B are ASYNCHRONOUS RECEIVER/TRANSMITTER subsystems using silicon gate process technology. The use of this low threshold process provides direct compatibility with all forms of current sinking logic. Interfacing restraints, such as external resistors, drivers and level shifting circuitry, are eliminated. All output lines have been designed to drive TTL directly.

The ASYNCHRONOUS RECEIVER/TRANSMITTER is a general purpose, programmable MOS/LSI device for interfacing an asynchronous serial data channel of a peripheral or terminal with parallel data of a computer or terminal. The transmitter section converts parallel data into a serial

PIN CONNECTIONS

*NOTE: NC means No Connection.

TR1863A CERAMIC PACKAGE

TR1863B PLASTIC PACKAGE

word which contains the data along with start, parity, and stop bits. The receiver section converts a serial word with start, data, parity, and stop bits, into parallel data, and it verifies proper code transmission by checking parity and receipt of a valid stop bit. Both the receiver and the transmitter are double buffered. The array is compatible with bipolar logic. The array may be programmed as follows: The word length can be either 5, 6, 7, or 8 bits; parity generation and checking may be inhibited, the parity may be even or odd; and the number of stop bits may be either one or two, with one and one half when transmitting a 5 bit code. NOTE: See TR1402A Data Sheet for operation with 5 level code-2 stop bits.

TRANSMITTER FLOW CHART

RECEIVER FLOW CHART

OUTPUT STRUCTURE
 DEVICES "B" & "C" COMPRISE A PUSH-PULL OUTPUT BUFFER. IN THE LOW-LEVEL STATE, OUTPUT TRANSISTOR "C" IS "ON" AND CASCODE DEVICE "B" IS OFF. IN THE HIGH-LEVEL STATE, THE OPPOSITE IS TRUE. IN THE DISCONNECTED STATE, BOTH "B" AND "C" ARE TURNED OFF CAUSING THE OUTPUT NODE TO FLOAT.

TRANSMITTER TIMING

DETAIL:

RECEIVER TIMING

DETAIL:

- (1) SEE APPLICATION REPORT NO. 1 FOR A DESCRIPTION OF START BIT DETECTION.
- (2) THE DELAY BETWEEN ORR & OR = 10 - 500 NS.
- (3) OR, ERROR FLAGS AND DATA ARE VALID AT THE NOMINAL CENTER OF THE FIRST STOP BIT.
- (4) ORR SHOULD BE HIGH A MINIMUM OF "A" NS (ONE-HALF CLOCK TIME PLUS 500 NS) PRIOR TO ORR RISING EDGE.
- (5) DATA & DE PRECEDES OR & ERROR FLAGS BY N CLOCK.
- (6) DATA FLAGS WILL REMAIN SET UNTIL A GOOD CHARACTER IS RECEIVED OR MASTER RESET IS APPLIED.

PIN DEFINITIONS

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	V _{SS} POWER SUPPLY	V _{SS}	+5 volts supply
2		NC	No Connection (Open)
3	GROUND	GND	Ground = 0V
4	RECEIVER REGISTER DISCONNECT	RRD	A high level input voltage, V _{IH} , applied to this line disconnects the RECEIVER HOLDING REGISTER outputs from the RR ₀ RR ₁ data outputs (pins 5-12)
5-12	RECEIVER HOLDING REGISTER DATA	RR ₀ -RR ₁	The parallel contents of the RECEIVER HOLDING REGISTER appear on these lines if a low-level input voltage, V _{IL} , is applied to RRD. For character formats of fewer than eight bits received characters are right-justified with RR ₁ (pin 12) as the least significant bit and the truncated bits are forced to a low level output voltage, V _{OL} .
13	PARITY ERROR	PE	A high level output voltage, V _{OH} , on this line indicates that the received parity does not compare to that programmed by the EVEN PARITY ENABLE control line (pin 39). This output is updated each time a character is transferred to the RECEIVER HOLDING REGISTER. PE lines from a number of arrays can be bussed together since an output disconnect capability is provided by Status Flag Disconnect line (pin 16).
14	FRAMING ERROR	FE	A high-level output voltage, V _{OH} , on this line indicates that the received character has no valid stop bit, i.e., the bit (if programmed) is not a high level voltage. This output is updated each time a character is transferred to the Receiver Holding Register. FE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
15	OVERRUN ERROR	OE	A high-level output voltage, V _{OH} , on this line indicates that the Data Received Flag (pin 19) was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
16	STATUS FLAGS DISCONNECT	SFD	A high-level input voltage, V _{IH} , applied to this pin disconnects the PE, FE, OE, DR and THRE allowing them to be bussed connected.
17	RECEIVER REGISTER CLOCK	RRC	The receiver clock frequency is sixteen (16) times the desired receiver shift rate.
18	DATA RECEIVED RESET	DRR	A low-level input voltage, V _{IL} , applied to this line resets the DR line.
19	DATA RECEIVED	DR	A high-level output voltage, V _{OH} , indicates that an entire character has been received and transferred to the RECEIVER HOLDING REGISTER.
20	RECEIVER INPUT	RI	Serial input data received on this line enters the RECEIVER REGISTER at a point determined by the character length, parity, and the number of stop bits. A high-level input voltage, V _{IH} , must be present when data is not being received.
21	MASTER RESET	MR	This line is strobed to a high-level input voltage, V _{IH} , to clear the logic. It resets the Transmitter and Receiver Registers, the Receiver Holding Register, FE, OE, PE, DRR and sets TRO, THRE, and TRE to a high-level output voltage, V _{OH} .
22	TRANSMITTER HOLDING REGISTER EMPTY	THRE	A high-level output voltage, V _{OH} , on this line indicates the TRANSMITTER HOLDING REGISTER has transferred its contents to the TRANSMITTER REGISTER and may be loaded with a new character.
23	TRANSMITTER HOLDING REGISTER LOAD	THRL	A low-level input voltage, V _{IL} , applied to this line enters a character into the TRANSMITTER HOLDING REGISTER. A transition from a low-level input voltage, V _{IL} , to a high-level input voltage, V _{IH} , transfers the character into the TRANSMITTER REGISTER if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is automatically transferred simultaneously with the initiation of the serial transmission of the new character.
24	TRANSMITTER REGISTER EMPTY	TRE	A high-level output voltage, V _{OH} , on this line indicates that the TRANSMITTER REGISTER has completed serial transmission of a full character including STOP bits. It remains at this level until the start of transmission of the next character.
25	TRANSMITTER REGISTER OUTPUT	TRO	The contents of the TRANSMITTER REGISTER (START bit, DATA bits, PARITY bit, and STOP bits) are serially shifted out on this line. When no data is being transmitted, this line will remain at a high level output voltage, V _{OH} . Start of transmission is defined as the transition of the START bit from a high-level output voltage V _{OH} to a low-level output voltage, V _{OL} .

PIN DEFINITIONS (CONT)

PIN NUMBER	NAME	SYMBOL	FUNCTION															
26-33	TRANSMITTER REGISTER DATA INPUTS	TR ₁ - TR ₈	The character to be transmitted is loaded into the TRANSMITTER HOLDING REGISTER on these lines with the THRL Strobe. If a character of less than 8 bits has been selected (by WLS ₁ and WLS ₂), the character is right justified to the least significant bit, RR1, and the excess bits are disregarded. A high-level input voltage, V _{IH} , will cause a high-level output voltage, V _{OH} , to be transmitted.															
34	CONTROL REGISTER LOAD	CRL	A high-level input voltage, V _{IH} , on this line loads the CONTROL REGISTER with the control bits (WLS ₁ , WLS ₂ , EPE, PI, SBS). This line may be strobed or hard wired to a high-level input voltage, V _{IH} .															
35	PARITY INHIBIT	PI	A high-level input voltage, V _{IH} , on this line inhibits the parity generation and verification circuits and will clamp the PE output (pin 13) to V _{OL} . If parity is inhibited the STOP bit(s) will immediately follow the last data bit on transmission.															
36	STOP BIT (S) SELECT	SBS	This line selects the number of STOP bits to be transmitted after the parity bit. A high-level input voltage, V _{IH} , on this line selects two STOP bits, and a low-level input voltage, V _{IL} , selects a single STOP bit. Selection of two STOP bits when programming a five (5) bit word generates 1.5 STOP bits.															
37-38	WORD LENGTH SELECT	WLS ₂ WLS ₁	These two lines select the character length (exclusive of parity) as follows: <table><tr><th>WLS₂</th><th>WLS₁</th><th>Word Length</th></tr><tr><td>V_{IL}</td><td>V_{IL}</td><td>5 bits</td></tr><tr><td>V_{IL}</td><td>V_{IH}</td><td>6 bits</td></tr><tr><td>V_{IH}</td><td>V_{IL}</td><td>7 bits</td></tr><tr><td>V_{IH}</td><td>V_{IH}</td><td>8 bits</td></tr></table>	WLS ₂	WLS ₁	Word Length	V _{IL}	V _{IL}	5 bits	V _{IL}	V _{IH}	6 bits	V _{IH}	V _{IL}	7 bits	V _{IH}	V _{IH}	8 bits
WLS ₂	WLS ₁	Word Length																
V _{IL}	V _{IL}	5 bits																
V _{IL}	V _{IH}	6 bits																
V _{IH}	V _{IL}	7 bits																
V _{IH}	V _{IH}	8 bits																
39	EVEN PARITY ENABLE	EPE	This line determines whether even or odd PARITY is to be generated by the transmitter and checked by the receiver. A high-level input voltage, V _{IH} , selects even PARITY and a low-level input voltage, V _{IL} , selects odd PARITY.															
40	TRANSMITTER REGISTER CLOCK	TRC	The transmitter clock frequency is sixteen (16) times the desired transmitter shift rate.															

MAXIMUM RATINGS

V _{CC} Supply Voltage	-0.3V to +7.0V
Clock Input Voltage*	-0.3V to +7.0V
Logic Input Voltage*	-0.3V to +7.0V
Logic Output Voltage*	-0.3V to +7.0V
Storage Temperature	-55°C to +150°C
Operating Free-Air Temperature T _A Range	0°C to +70°C**
Lead Temperature (Soldering, 10 sec.)	300°C

*GND = 0V

NOTE: These voltages are measured with respect to GND

ELECTRICAL CHARACTERISTICS

$$V_S = V_{CC} = 5V \pm 5\%, V_{DD} = 0V$$

$$T_A = 0^\circ C \text{ to } +70^\circ C \text{ unless otherwise specified}$$

SYMBOL	PARAMETER	MIN.	MAX.	CONDITIONS
I_{CC}	OPERATING CURRENT Supply Current		35 ma	$V = 5.25V$
V_{IH}	LOGIC LEVELS Logic High	2.4V		
V_{IL}	Logic Low		0.6V	$V_{SS} = 4.75V$
V_{OH}	OUTPUT LOGIC LEVELS Logic High	2.4V		$V_{SS} = 4.75V, I_{OH} = -100 \mu A$
V_{OL}	Logic Low		0.4V	$V_{SS} = 5.25V, I_{OL} = 1.6 \text{ ma}$
I_{OS}^*	Short Circuit Current		20ma	$V_{SS} = 5.25V, V_O = 0V$
I_{OC}	Output Leakage		10 μA	$V_{OUT} = 0V, SFD = RRD = V_{IH}$
I_{IL}	Input Current		+10 μA	$V_{IN} = V_{IH} \text{ or } V_{IL}$

*Only one output should be shorted at any time.

**Consult factory for extended temperature range UARTS.

SWITCHING CHARACTERISTICS — See "Switching Waveforms"

$$V_{CC} = 5V, V_{DD} = 0V$$

$$T_A = 25^\circ, C_{LOAD} = 20 \text{ pf plus one TTL load}$$

SYMBOL	PARAMETER	MIN.	MAX.	CONDITIONS
f_{clock}	Clock Frequency	D.C.	1.0 MHz*	$V_{SS} = 4.75V$ (See figures 1 & 2)
t_{pw}	Pulse Widths CRL THRL DRR MR	200 ns 200 ns 200 ns 500 ns		
t_c	Coincidence Time	200 ns		(See figures 1 & 2)
t_{hold}	Hold Time	20 ns		(See figures 1 & 2)
t_{set}	Set Time	0		(See figure 1 & 2)
	OUTPUT PROPAGATION DELAYS			
t_{pd0}	To Low State		250 ns	(See figure 3) $C_L = 20 \text{ pf, plus one TTL load}$
t_{pd1}	To High State		250 ns	(See figure 3) $C_L = 20 \text{ pf, plus one TTL load}$
	CAPACITANCE			
c_{in}	Inputs		20 pf	$f = 1 \text{ MHz}, V_{in} = 5V$
c_o	Outputs		20 pf	$f = 1 \text{ MHz}, V_{in} = 5V$

* f_{max} for TR1863A or B = 1.0 MHz

f_{clock} may be factory selected for 3.5 MHz max.

SWITCHING WAVEFORMS

Figure 1. Data Input Load Cycle

Figure 2. Control Register Load Cycle

Figure 3. Status Flag Output Delays

Figure 4. Data Output Delays

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed. Information furnished by Western Digital Corporation is believed to be accurate and reliable. However, no responsibility is assumed by Western Digital Corporation for its use, nor any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Western Digital Corporation. Western Digital Corporation reserves the right to change said circuitry at any time without notice.

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(continued from page 1)

Figure 1 AD572 Functional Diagram & Pinout

The +10V reference is derived from a low T C zener reference diode which has its zener voltage amplified and buffered by an op amp. The reference voltage is calibrated to +10V, $\pm 1\text{mV}$ by active laser trimming of the thin-film resistors which determine the closed-loop gain of this op amp.

The DAC feedback weighing network is comprised of a proprietary 12-bit analog current switch chip and silicon-chromium thin-film ladder network (separately packaged as the AD562 12-bit D/A converter). This ladder network is active laser-trimmed to calibrate all bit ratio scale factors to a precision of 0.0005% of FSR (full-scale range) to guarantee no missing codes over the appropriate temperature ranges specified for the AD572A, AD572B, and AD572S versions.

Different unipolar and bipolar analog input ranges can be selected by changing connections at the device terminal pins. The analog voltage input can be applied to either of the span (direct input) resistors. Alternatively, the unity buffer follower can be connected between the analog signal and either direct input terminal when a high impedance input is required.

THEORY OF OPERATION

On receipt of a CONVERT START command, the AD572 converts the voltage at its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows:

The 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the respective device bit output pins and to the corresponding bit inputs of the feedback DAC.

The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 2. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through.

Figure 2 Timing Diagram (Binary Code 110101011001)

13 cycles. All SAR parallel bit and STATUS flip-flops are initialized on the leading edge, and the gated clock inhibit signal removed on the trailing edge of the CONVERT START signal. At time t_0 , B_1 is reset and B_2 – B_{12} are set unconditionally. At t_1 the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2 , the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12} . After a 400nsec delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the logic "0" state.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however, serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 8).

Incorporation of this 400nsec delay period guarantees that the parallel (and serial) data are valid at the logic "1" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.

BINARY CODING

The AD572 binary output number $N_n = B_1 B_2 B_3 \dots B_{12}$ is related to the analog input voltage E_{in} for all unipolar ranges by the expression

$$\frac{B_1 2^{11} + B_2 2^{10} + B_3 2^9 + \dots + B_{12} 2^0}{2^{12}} = \frac{E_{in}}{FSR} \quad (1)$$

where B_1 = MSB, B_{12} = LSB, and FSR = full-scale range. For all bipolar ranges a fixed bipolar offset equal to $\frac{+FSR}{2}$ is internally summed with E_{in} so that the sum of E_{in} plus this offset will be positive over the rated operating range. For bipolar ranges, expression (1) becomes

$$\frac{B_1 2^{11} + B_2 2^{10} + B_3 2^9 + \dots + B_{12} 2^0}{2^{12}} = \frac{E_{in} + \frac{FSR}{2}}{FSR} \quad (2)$$

Expressions (1) and (2) can be put in an alternate form

$$\left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8} + \dots + \frac{B_{12}}{4096} \right) FSR = E_{in} \quad (3)$$

Unipolar (Binary Coding)

and

$$\left(\frac{B_1}{2} + \frac{B_2}{4} + \frac{B_3}{8} + \dots + \frac{B_{12}}{4096} \right) FSR - \frac{FSR}{2} = E_{in} \quad (4)$$

Bipolar (Offset Binary Coding)

Several examples will illustrate how this binary coding works.

UNIPOLAR RANGE

Assume $FSR = 10V$ and $B_1 B_2 B_3 \dots B_{12} = 110001000001$ then from (3) $E_{in} = +5V + 2.5V + 0.1563V + 0.0024V = +7.6587V$

-5V TO +5V INPUT RANGE

Assume $FSR = 10V$ as above, but that the bipolar offset is connected and $B_1 B_2 B_3 \dots B_{12} = 0110000000001$. Then from (4), $E_{in} = (+2.5V + 1.25V + 0.0024V) - 5V = -1.2476V$

-10V TO +10V INPUT RANGE

Assume the bipolar offset is connected as above, but that the input span is now 20V. Assuming the same digital output code as in the -5V to +5V input range example, from (4), $E_{in} = (+5V + 2.5V + 0.0049V) - 10V = -2.4951V$, or twice the value of the previous example (neglecting round-off errors).

The encoding process defined by the previous relations (1) and (2) or (3) and (4) determines that the analog input lies within one of the $2^{12} = 4096$ quantization levels between 0 and FSR (or $-FSR/2$ and $+FSR/2$). Figures 3 (A) and 3 (B) show the actual device transfer curves for unipolar and bipolar ranges (offset binary coding). They also show the ideal straight line transfer curves which pass through the center of each quantization level. As can be seen from these figures, the actual and ideal transfer curves differ by exactly $\pm 1/2$ LSB at the end of each quantization interval, giving rise to the fundamental $\pm 1/2$ LSB quantization error inherent in the digitizing process.

(A) Unipolar Range (Binary Coding)

(B) Bipolar Range (Offset Binary Coding)

Figure 3 Unipolar and Bipolar Range Transfer Curves

ANALOG INPUT AND POWER CONNECTIONS

Offset Adjust. Analog and power connections for 0 to +10V unipolar and -10V to +10V bipolar input ranges are shown in Figures 4 and 5, respectively. The Bipolar Offset pin 23 is open circuited for all unipolar input ranges, and connected to Comparator Input pin 22 for all bipolar input ranges. The zero adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 3.9M Ω resistor to Comparator Input pin 22 for all ranges. The tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a $-1200\text{ppm}/^\circ\text{C}$ tempco contributes a worst case offset tempco of $8 \times 244 \times 10^{-6} \times 1200\text{ppm}/^\circ\text{C} = 2.3\text{ppm}/^\circ\text{C}$ of FSR if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than $\pm 4\text{LSB}$, use of a carbon composition offset summing resistor typically contributes no more than $1\text{ppm}/^\circ\text{C}$ of FSR offset tempco.

Figure 4 Analog and Power Connections for Unipolar 0 to +10V Input Range with Buffer Follower

Figure 5 Analog and Power Connections for Bipolar -10V to +10V Input Range with Buffer Follower

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco < 100 ppm/°C) are used, is shown in Figure 6

Figure 6 Low Tempco Zero Adj Circuit

In either zero adjust circuit, the fixed resistor connected to pin 22 should be located close to this pin to keep the pin 22 connection runs short, since the Comparator Input pin 22 is quite sensitive to external noise pickup

Gain Adjust The gain adjust circuit consists of a 100Ω potentiometer connected between +10V Reference Output pin 18 and Gain Adjust Input pin 27 for all ranges. Both GAIN and ZERO ADJ potentiometers should be multi-turn, low tempco types 201 cermet (tempco = 100ppm/°C max)

types are recommended. If the 100Ω GAIN ADJ potentiometer is replaced by a fixed 50Ω resistor, absolute gain calibration to $\pm 0.1\%$ of FSR is guaranteed

Grounding Analog and digital signal grounds should be kept separate where possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Ground pin 26 and Digital Ground pin 15 are not connected internally; these two pins must be connected externally for the device to operate properly. Preferably, this connection is made at only one point, and as close to the device as possible. The case is connected internally to pin 15 to provide good electrostatic shielding

Power Supply Bypassing The $\pm 15V$ and $+5V$ power leads should be capacitively bypassed for optimum device performance. 1μF tantalum types are recommended; these capacitors should be located close to the device. It is not necessary to shunt these capacitors with disc capacitors to provide additional high frequency power supply decoupling (as is required with some competitive products), since each power lead is bypassed internally with a 0.039μF ceramic capacitor

CALIBRATION

External ZERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 3 and 4, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and $-4FSR$ for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range

0 to +10V Range Set analog input to $+1LSB = +0.0024V$. Adjust Zero for digital output = 000000000001, Zero is now calibrated. Set analog input to $+FSR - 2LSB = +9.9952V$. Adjust Gain for 111111111110 digital output code, full-scale (Gain) is now calibrated. Half-scale calibration check: set analog input to $+5.0000V$, digital output code should be 100000000000

-10V to +10V Range: Set analog input to $-9.9951V$, adjust Zero for 000000000001 digital output (offset binary) code. Set analog input to $+9.9902V$, adjust Gain for 111111111110 digital output (offset binary) code. Half-scale calibration check: set analog input to $0.0000V$, digital output (offset binary) code should be 100000000000

Other Ranges: Representative digital coding for 0 to +10V, -5V to +5V, and -10V to +10V ranges is shown in Table 1. Coding relationships and calibration points for 0 to +5V and -2.5V to +2.5V ranges can be found by halving the corresponding code equivalents listed for the 0 to +10V and -5V to +5V ranges, respectively

Zero and full-scale calibration can be accomplished to a precision of approximately $\pm 4LSB$ using the static adjustment procedure described above. By summing a small sine or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Handbook", D. Sheingold, Analog Devices, Inc., 1972, Part II, Chapter 3

Analog Input - Volts (Center of Quantization Interval)			Input Normalized to FSR		Digital Output Code (Binary for Unipolar Ranges, Offset Binary for Bipolar Ranges)	
0 to +10V Range	-5V to +5V Range	-10V to +10V Range	Unipolar Ranges	Bipolar Ranges	B1 (MSB)	B12 (LSB)
+9.9976	+4.9976	+9.9951	+FSR-1 LSB	+½FSR-1 LSB	1 1 1 1 1 1 1 1 1 1	1
+9.9952	+4.9952	+9.9902	+FSR-2 LSB	+½FSR-2 LSB	1 1 1 1 1 1 1 1 1 0	0
...	...	...	...	...	...	...
+5.0024	+0.0024	+0.0049	+½FSR+1 LSB	+1 LSB	1 0 0 0 0 0 0 0 0 0	1
+5.0000	+0.0000	+0.0000	+½FSR	ZERO	1 0 0 0 0 0 0 0 0 0	0
...	...	...	...	...	...	...
+0.0024	-4.9976	-9.9951	+1 LSB	-½FSR+1 LSB	0 0 0 0 0 0 0 0 0 0	1
+0.0000	-5.0000	-10.0000	ZERO	-½FSR	0 0 0 0 0 0 0 0 0 0	0

Table 1. Digital Output Codes vs Analog Input For Unipolar and Bipolar Ranges

RANGE AND BUFFER FOLLOWER PIN CONNECTIONS

Analog pin connections for each of the ranges, with and without the buffer follower being used, are shown in Table 2

Range	Buffer Follower	Connect Analog Input To Pin	Connect Span Pin	Connect Bipolar Pin 23 To
0 to +5V	Used	30 and 29 to 24	25 to 22	—
	Not Used	24	25 to 22	—
0 to +10V	Used	30 and 29 to 24	—	—
	Not Used	24	—	—
-2.5 to +2.5V	Used	30 and 29 to 24	25 to 22	22
	Not Used	24	25 to 22	22
-5 to +5V	Used	30 and 29 to 24	—	—
	Not Used	24	—	—
-10 to +10V	Used	30 and 29 to 25	—	—
	Not Used	25	—	—

Table 2. Range and Buffer Follower Pin Connections

When the analog signal source has a low impedance (as would be the case if it were the output of the sample-and-hold amplifier of Figure 9), it can be connected to either of the direct input pins 24 or 25. The buffer follower is used in the application as shown in Figure 6, in which the analog input to the converter comes directly from the output of a FET analog multiplexer. The selected channel has a typical $r_{ON} = 200\Omega$ which has a $3000\text{ppm}/^\circ\text{C}$ tempco. If the multiplexer output were connected to the 0 to +10V direct input pin 24 (5k Ω input impedance, nominal), this r_{ON} would introduce a 4% gain scale-factor loading error, which is well beyond the normal $\pm 0.25\%$ FSR external gain adjustment range, and a tempco of approximately $3000\text{ppm}/^\circ\text{C} \times 4\% = 120\text{ppm}/^\circ\text{C}$. By connecting the buffer between the multiplexer output and direct input, these errors are eliminated. The buffer amplifier input bias current (50nA typical) must flow through the analog signal source, however. This limits the upper practical source impedance to several kilohms so that the offset voltage $I_{BIAS} R_{SOURCE}$ can be kept negligible, even though the buffer amplifier dynamic input impedance $\geq 100M\Omega$. The buffer amplifier has a 2 μsec settling time to 0.01% FSR for a 20V input step. This must be added to the conversion time when the input voltage can change significantly between successive conversions (as could be the case in the circuit of Figure 7).

Figure 7. Using Buffer Follower With Multiplexed Analog Input

Short Cycle Input: A Short Cycle Input pin 24 permits the timing cycle shown in Figure 2 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 12-bit resolution is required, pin 24 is connected to +5V (pin 16). When 10-bit resolution is desired, pin 14 is connected to Bit 11 output pin 2. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision ($t_{10} + 400\text{nsec}$ in timing diagram of Figure 2). Short Cycle pin connections and associated maximum 12, 10, and 8-bit conversion times are summarized in Table 3.

Connect Short Cycle Pin 14 to Pin	Bits	Resolution (% FSR)	Maximum Conversion Time (μs)	Status Flag Reset at (Figure 2)
16	12	0.024	25	$t_{12} + 400\text{nsec}$
2	10	0.10	21	$t_{10} + 400\text{nsec}$
4	8	0.39	17	$t_8 + 400\text{nsec}$

Table 3. Short Cycle Connections

(One should note that the calibration voltages listed in Table 1 are for 12-bit resolution only, and are not those corresponding to the center of each discrete quantization interval at reduced bit resolutions.)

DIGITAL OUTPUT DATA

Both parallel and serial data are in positive-true form and outputted from TTL storage registers. Parallel data output coding is binary for unipolar ranges and either offset binary

or two's complement binary, depending on whether Bit 1 (pin 12) or its logical inverse BIT 1 (pin 13) is used as the MSB. Parallel data becomes valid approximately 200nsec before the STATUS flag returns to logic "0", permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Serial data coding is binary for unipolar input ranges and offset binary for bipolar input ranges. Serial output is by bit (MSB first, LSB last) in NRZ (non-return-to-zero) format. Serial and parallel data outputs change state on positive-going clock edges. Serial data is guaranteed valid on all negative-going clock edges, permitting serial data to be clocked directly into a receiving register on these edges as shown in Figure 8. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 2. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge. All serial data bits will have been correctly transferred and be in the receiving shift register locations shown at the completion of the conversion period.

APPLICATIONS

Sample-Hold Amplifier: A sample-hold amplifier (SHA) is normally connected between the analog signal source and AD572 analog input when the analog signal can change by more than $\frac{1}{2}$ LSB during conversion. Typical SHA-AD572 interconnections are shown in Figure 9. The STATUS output drives the SHA SAMPLE/HOLD input directly. On receipt of a CONVERT START pulse, the STATUS flag changes from "1" to "0" causing SHA mode to change from SAMPLE to HOLD. The SHA output voltage $e_{o\text{ SH}}$ is then held constant at the value existing just prior to application of the HOLD command for the complete conversion period. At the end of conversion, the STATUS flag returns to "1", restoring the SHA mode to SAMPLE, and $e_{o\text{ SH}}$ again tracks the analog signal voltage $e_{in\text{ SH}}$ (after the signal acquisition transient has subsided):

Figure 9. Sample-Hold Amplifier - AD572 Interconnections

Note that the internal (gated) clock is inhibited for the duration of the CONVERT START pulse and does not start running until the termination of this pulse (see timing). This can be used to simplify control signal timing requirements. In the circuit of Figure 9, for example, the CONVERT START signal pulse-width can be extended beyond the aperture delay time of the SHA to assure that $e_{o\text{ SH}}$ is in steady-state before conversion is initiated. This assures accurate conversion without requiring additional delay timing circuitry. The effect of varying the CONVERT START pulse-width on the conversion timing cycle is shown in Figure 10.

Figure 10. Effect of Convert Start Pulse-Width on Timing

Figure 8. Serial Data Transfer Into Shift Register With Parallel Output to Data Bus

OUTLINE DIMENSIONS PACKAGING SPECIFICATIONS

Dimensions shown in inches and (mm)

The drawing shows three views of a rectangular package:

- Top View:** A rectangle with a width of 0.215 (5.31) inches and a length of 0.74 (18.2) inches. It features a "PIN 1 IDENTIFIER" at the top-left corner and a "PIN 1 GREEN GLASS BEAD" at the bottom-left corner. The bottom edge has 12 pins with a pitch of 0.062 (1.57) inches. The total pin length is 0.105 (2.67) inches. The package is labeled "DAD572" and "12 BIT ADC".
- Side View:** Shows a height of 0.038 (0.96) inches. The pin height is 0.030 (0.76) inches. The pin pitch is 0.062 (1.57) inches.
- End View:** Shows a width of 0.200 (5.08) inches. The pin pitch is 0.062 (1.57) inches.

NOTES

- 1) PACKAGE HOUZAR WITH 100MIN. MIN. NICKEL #419E
- 2) PIN 1 HOUZAR WITH 50MIN. MIN. 24K GOLD PLATE
- 3) PACKAGE AND PIN MEET ALL REQUIREMENTS OF MIL STD 883
- 4) TOLERANCES UNLESS OTHERWISE NOTED

21 30X ± 0.1 (2.54)
4X 30X ± 0.05 ± 0.1 (2.54)

MATING SOCKET SET OF TWO 16 PIN SOCKET STAMPS WARDEN PIN
AC10201-01-91 MIL. 963.

All models ordered to the requirements of MIL-STD-883, Method 5004, Class B are identified with a /883B suffix, and receive the following processing:

PROCESS		CONDITIONS	
1 Pre-Cap Visual Inspection	In-House Criteria	1 Pre-Cap Visual Inspection	2010, Test Condition B
2 Stabilization Bake	24 hours @ +150°C	2 Stabilization Bake	1008 24 hours @ +150°C
3 Temperature Cycling	10 cycles, -65 to +150°C	3 Temperature Cycling	1010, Test Condition C, 10 cycles, -65 to +150°C
4 Constant Acceleration	5000G	4 Constant Acceleration	2001, Y ₁ plane, 5000G
5 Seal, Test, Fine and Gross	In-House Criteria	5 Seal Test, Fine and Gross	1014, Test Condition A and C
6 Operating Burn-In	48 hours @ +125°C	6 Operating Burn-In	1015, Test Condition B, 160 hours @ +125°C
		7 Final Electrical Testing	Performed at max and min operating temperatures
		8 External Visual Inspection	2009

Model	Specification Temp Range	Max Gain T C	Max Reference T C	Guaranteed Temp Range No Missing Codes	Price (1-24)
AD572AD	-25 to +85°C	±30ppm/°C	±20ppm/°C	0 to +70°C	\$ 95 00
AD572BD	-25 to +85°C	±15ppm/°C	±10ppm/°C	-25 to +85°C	\$125 00
AD572SD	-55 to +125°C	±15ppm/°C (-25 to +85°C) ±25ppm/°C (-55 to +125°C)	±10ppm/°C	-55 to +125°C	\$250 00
AD572BD/883B	} Meet all specifications after processing to the requirements of MIL STD 883, Method 5004, Class B				\$205 00
AD572SD/883B					\$320 00

-8-

Am9511

Arithmetic Processing Unit
Advanced Micro Devices
Advanced MOS/LSI

DISTINCTIVE CHARACTERISTICS

- Fixed point 16 and 32 bit operations
- Floating point 32 bit operations
- Binary data formats
- Add, Subtract, Multiply and Divide
- Trigonometric and inverse trigonometric functions
- Square roots, logarithms, exponentiation
- Float to fixed and fixed to float conversions
- Stack-oriented operand storage
- DMA or programmed I/O data transfers
- End signal simplifies concurrent processing
- General purpose 8-bit data bus interface
- Standard 24 pin package
- +12 volt and +5 volt power supplies
- Advanced N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

GENERAL DESCRIPTION

The Am9511 Arithmetic Processing Unit (APU) is a monolithic MOS/LSI device that provides high performance fixed and floating point arithmetic and a variety of floating point trigonometric and mathematical operations. It may be used to enhance the computational capability of a wide variety of processor-oriented systems.

All transfers, including operand, result, status and command information, take place over an 8-bit bidirectional data bus. Operands are pushed onto an internal stack and a command is issued to perform operations on the data in the stack. Results are then available to be retrieved from the stack, or additional commands may be entered.

Transfers to and from the APU may be handled by the associated processor using conventional programmed I/O, or may be handled by a direct memory access controller for improved performance. Upon completion of each command, the APU issues an end of execution signal that may be used as an interrupt by the CPU to help coordinate program execution.

BLOCK DIAGRAM

MOS-046

CONNECTION DIAGRAM Top View

Pin 1 is marked for orientation

MOS-047

ORDERING INFORMATION

Package Type	Ambient Temperature	Clock Frequency		
		2MHz	3MHz	4MHz
Hermetic DIP	$0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$	Am9511DC	Am9511-1DC	Am9511-4DC
	$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	Am9511DM	Am9511-1DM	

INTERFACE SIGNAL DESCRIPTION

VCC: +5 Volt power supply

VDD: +12 Volt power supply

VSS: Ground

CLK (Clock, Input)

An external timing source should be applied to the CLK pin. The Clock input may be asynchronous to the Read and Write control signals.

RESET (Reset, Input)

The active high Reset signal provides initialization for the chip. Reset terminates any operation in progress, clears the status register and places the Am9511 into the idle state. Stack contents are not affected by Reset. The Reset should be active for at least 5 clock periods following stable supply voltages and stable clock input. There is no internal power-on reset.

CS (Chip Select, Input)

$\overline{CS}$ is an active low input signal which conditions the read and write signals and thus enables communication with the data bus.

C/D (Command/Data, Input)

In conjunction with the $\overline{RD}$ and $\overline{WR}$ signals, the C/D control line establishes the type of transfers that are to be performed on the data bus.

C/D	$\overline{RD}$	$\overline{WR}$	Function
0	1	0	Enter data byte into stack
0	0	1	Read data byte from stack
1	1	0	Enter command
1	0	1	Read status

$\overline{RD}$ (Read, Input)

The active low Read signal is conditioned by $\overline{CS}$ and indicates that information is to be transferred from internal locations to the data bus. $\overline{RD}$ and $\overline{WR}$ are mutually exclusive.

$\overline{WR}$ (Write, Input)

The active low Write signal is conditioned by $\overline{CS}$ and indicates that information is to be transferred from the data bus into internal locations. $\overline{RD}$ and $\overline{WR}$ are mutually exclusive.

$\overline{EACK}$ (End Acknowledge, Input)

This active low input clears the end of execution output signal ($\overline{END}$). If $\overline{EACK}$ is tied low, the $\overline{END}$ output will be a pulse that is less than one clock period wide.

SVACK (Service Acknowledge, Input)

This active low input clears the service request output (SVREQ).

$\overline{END}$ (End Execution, Output)

This active low, open-drain output indicates that execution of the previously entered command is complete. It can be used as an interrupt request and is cleared by $\overline{EACK}$, RESET or any read or write access to the Am9511.

SVREQ (Service Request, Output)

This active high output signal indicates that command execution is complete and that post execution service was requested in the previous command byte. It is cleared by SVACK, by RESET, or by the end of a subsequent command that does not request service.

PAUSE (Pause, Output)

This active low output indicates that the Am9511 has not yet completed its information transfer with the host (or DMA) over the data bus. Whenever a data read or a status read operation is requested, PAUSE goes low. It returns high only after the data bus contains valid output data. When an existing command is still in the process of execution, and a data write, data read, or command write is requested, then PAUSE goes low for the remaining duration of the existing command plus any time needed for initiating a data read. In both cases, the host should neither change any information to the Am9511, nor (in the case of data read or status read) attempt to capture data from the Am9511 DB outputs until PAUSE has returned high. (See 'Pause Operation' section on page 5).

DB0-DB7 (Bidirectional Data Bus, I/O)

These eight bidirectional lines provide for transfer of commands, status and data between the Am9511 and the CPU. The Am9511 will drive the data bus only when $\overline{CS}$ and $\overline{RD}$ are low.

COMMAND STRUCTURE

Each command entered into the Am9511 consists of a single 8-bit byte having the format illustrated below.

Bits 0-4 select the operation to be performed as shown in the table. Bits 5-6 select the data format for the operation. If bit 5 is a 1, a fixed point data format is specified. If bit 5 is a 0, floating point format is specified. Bit 6 selects the precision of

the data to be operated on by fixed point commands (if bit 5 = 0, bit 6 must be 0). If bit 6 is a 1, single-precision (16-bit) operands are indicated. If bit 6 is a 0, double-precision (32-bit) operands are indicated. Results are undefined for all illegal combinations of bits in the command byte. Bit 7 indicates whether a service request is to be issued after the command is executed. If bit 7 is a 1, the service request output (SVREQ) will go high at the conclusion of the command and will remain high until reset by a low level on the service acknowledge pin (SVACK) or until completion of execution of a succeeding command where bit 7 is 0. Each command issued to the Am9511 requests post execution service based upon the state of bit 7 in the command byte. When bit 7 is a 0, SVREQ remains low.

COMMAND SUMMARY

Command Code								Command Mnemonic	Command Description
7	6	5	4	3	2	1	0		
FIXED POINT 16 BIT									
SF	1	1	0	1	1	0	0	SADD	Add TOS to NOS Result to NOS Pop Stack
SF	1	1	0	1	1	0	1	SSUB	Subtract TOS from NOS Result to NOS Pop Stack
SF	1	1	0	1	1	1	0	SMUL	Multiply NOS by TOS Lower half of result to NOS Pop Stack
SF	1	1	1	0	1	1	0	SMUU	Multiply NOS by TOS Upper half of result to NOS Pop Stack
SF	1	1	0	1	1	1	1	SDIV	Divide NOS by TOS Result to NOS Pop Stack
FIXED POINT 32 BIT									
SF	0	1	0	1	1	0	0	DADD	Add TOS to NOS Result to NOS Pop Stack
SF	0	1	0	1	1	0	1	DSUB	Subtract TOS from NOS Result to NOS Pop Stack
SF	0	1	0	1	1	1	0	DMUL	Multiply NOS by TOS Lower half of result to NOS Pop Stack
SF	0	1	1	0	1	1	0	DMUU	Multiply NOS by TOS Upper half of result to NOS Pop Stack
SF	0	1	0	1	1	1	1	DDIV	Divide NOS by TOS Result to NOS Pop Stack
FLOATING POINT 32 BIT									
SF	0	0	1	0	0	0	0	FADD	Add TOS to NOS Result to NOS Pop Stack
SF	0	0	1	0	0	0	1	FSUB	Subtract TOS from NOS Result to NOS Pop Stack
SF	0	0	1	0	0	1	0	FMUL	Multiply NOS by TOS Result to NOS Pop Stack
SF	0	0	1	0	0	1	1	FDIV	Divide NOS by TOS Result to NOS Pop Stack
DERIVED FLOATING POINT FUNCTIONS									
SF	0	0	0	0	0	0	1	SQRT	Square Root of TOS Result in TOS
SF	0	0	0	0	0	1	0	SIN	Sine of TOS Result in TOS
SF	0	0	0	0	0	1	1	COS	Cosine of TOS Result in TOS
SF	0	0	0	0	1	0	0	TAN	Tangent of TOS Result in TOS
SF	0	0	0	0	1	0	1	ASIN	Inverse Sine of TOS Result in TOS
SF	0	0	0	0	1	1	0	ACOS	Inverse Cosine of TOS Result in TOS
SF	0	0	0	0	1	1	1	ATAN	Inverse Tangent of TOS Result in TOS
SF	0	0	0	1	0	0	0	LOG	Common Logarithm (base 10) of TOS Result in TOS
SF	0	0	0	1	0	0	1	LN	Natural Logarithm (base e) of TOS Result in TOS
SF	0	0	0	1	0	1	0	EXP	Exponential (e ^x) of TOS Result in TOS
SF	0	0	0	1	0	1	1	PWR	NOS raised to the power in TOS Result in NOS Pop Stack
DATA MANIPULATION COMMANDS									
SF	0	0	0	0	0	0	0	NOP	No Operation
SF	0	0	1	1	1	1	1	FIXS	Convert TOS from floating point to 16-bit fixed point format
SF	0	0	1	1	1	1	0	FIXD	Convert TOS from floating point to 32-bit fixed point format
SF	0	0	1	1	1	0	1	FLTS	Convert TOS from 16-bit fixed point to floating point format
SF	0	0	1	1	1	0	0	FLTD	Convert TOS from 32-bit fixed point to floating point format
SF	1	1	1	0	1	0	0	CHSS	Change sign of 16-bit fixed point operand on TOS
SF	0	1	1	0	1	0	0	CHSD	Change sign of 32-bit fixed point operand on TOS
SF	0	0	1	0	1	0	1	CHSF	Change sign of floating point operand on TOS
SF	1	1	1	0	1	1	1	PTOS	Push 16-bit fixed point operand on TOS to NOS (Copy)
SF	0	1	1	0	1	1	1	PTOD	Push 32-bit fixed point operand on TOS to NOS (Copy)
SF	0	0	1	0	1	1	1	PTOF	Push floating point operand on TOS to NOS (Copy)
SF	1	1	1	1	0	0	0	POPS	Pop 16-bit fixed point operand from TOS NOS becomes TOS
SF	0	1	1	1	0	0	0	POPD	Pop 32-bit fixed point operand from TOS NOS becomes TOS
SF	0	0	1	1	0	0	0	POPF	Pop floating point operand from TOS NOS becomes TOS
SF	1	1	1	1	0	0	1	XCHS	Exchange 16-bit fixed point operands TOS and NOS
SF	0	1	1	1	0	0	1	XCHD	Exchange 32-bit fixed point operands TOS and NOS
SF	0	0	1	1	0	0	1	XCHF	Exchange floating point operands TOS and NOS
SF	0	0	1	1	0	1	0	PUPI	Push floating point constant 'π' onto TOS Previous TOS becomes NOS

NOTES

- 1 TOS means Top of Stack NOS means Next on Stack
- 2 AMD Application Brief "Algorithm Details for the Am9511 APU" provides detailed descriptions of each command function, including data ranges, accuracies, stack configurations, etc
- 3 Many commands destroy one stack location (bottom of stack) during development of the result The derived functions may destroy several stack locations See Application Brief for details
- 4 The trigonometric functions handle angles in radians, not degrees
- 5 No remainder is available for the fixed-point divide functions
- 6 Results will be undefined for any combination of command coding bits not specified in this table

DATA FORMATS

The Am9511 Arithmetic Processing Unit handles operands in both fixed point and floating point formats. Fixed point operands may be represented in either single (16-bit operands) or double precision (32-bit operands), and are always represented as binary, two's complement values.

16-BIT FIXED POINT FORMAT

32-BIT FIXED POINT FORMAT

The sign (positive or negative) of the operand is located in the most significant bit (MSB). Positive values are represented by a sign bit of zero ($S = 0$). Negative values are represented by the two's complement of the corresponding positive value with a sign bit equal to 1 ($S = 1$). The range of values that may be accommodated by each of these formats is $-32,768$ to $+32,767$ for single precision and $-2,147,483,648$ to $+2,147,483,647$ for double precision.

Floating point binary values are represented in a format that permits arithmetic to be performed in a fashion analogous to operations with decimal values expressed in scientific notation.

$$(5.83 \times 10^2)(8.16 \times 10^1) = (4.75728 \times 10^4)$$

In the decimal system, data may be expressed as values between 0 and 10 times 10 raised to a power that effectively shifts the implied decimal point right or left the number of places necessary to express the result in conventional form (e.g., 47,572.8). The value-portion of the data is called the mantissa. The exponent may be either negative or positive.

The concept of floating point notation has both a gain and a loss associated with it. The gain is the ability to represent the significant digits of data with values spanning a large dynamic range limited only by the capacity of the exponent field. For

example, in decimal notation if the exponent field is two digits wide, and the mantissa is five digits, a range of values (positive or negative) from 1.0000×10^{-99} to 9.9999×10^{-99} can be accommodated. The loss is that only the significant digits of the value can be represented. Thus there is no distinction in this representation between the values 123451 and 123452, for example, since each would be expressed as 1.2345×10^5 . The sixth digit has been discarded. In most applications where the dynamic range of values to be represented is large, the loss of significance, and hence accuracy of results, is a minor consideration. For greater precision a fixed point format could be chosen, although with a loss of potential dynamic range.

The Am9511 is a binary arithmetic processor and requires that floating point data be represented by a fractional mantissa value between .5 and 1 multiplied by 2 raised to an appropriate power. This is expressed as follows:

$$\text{value} = \text{mantissa} \times 2^{\text{exponent}}$$

For example, the value 100.5 expressed in this form is 0.11001001×2^7 . The decimal equivalent of this value may be computed by summing the components (powers of two) of the mantissa and then multiplying by the exponent as shown below:

$$\begin{aligned} \text{value} &= (2^{-1} + 2^{-2} + 2^{-5} + 2^{-6}) \times 2^7 \\ &= (0.5 + 0.25 + 0.03125 + 0.00290625) \times 128 \\ &= 0.78515625 \times 128 \\ &= 100.5 \end{aligned}$$

FLOATING POINT FORMAT

The format for floating point values in the Am9511 is given below. The mantissa is expressed as a 24-bit (fractional) value, the exponent is expressed as an unbiased two's complement 7-bit value having a range of -64 to $+63$. The most significant bit is the sign of the mantissa (0 = positive, 1 = negative), for a total of 32 bits. The binary point is assumed to be to the left of the most significant mantissa bit (bit 23). All floating point data values must be normalized. Bit 23 must be equal to 1, except for the value zero, which is represented by all zeros.

The range of values that can be represented in this format is $\pm(2.7 \times 10^{-20})$ to 9.2×10^{18} and zero.

FUNCTIONAL DESCRIPTION

Stack Control

The user interface to the Am9511 includes access to an 8 level 16-bit wide data stack. Since single precision fixed point operands are 16 bits in length, eight such values may be maintained in the stack. When using double precision fixed point or floating point formats four values may be stored. The stack in these two configurations can be visualized as shown below.

Data are written onto the stack, eight bits at a time, in the order shown (B1, B2, B3, ...). Data are removed from the stack in reverse byte order (B8, B7, B6, ...). Data should be transferred into or out of the stack in multiples of the number of bytes appropriate to the chosen data format.

Data Entry

Data entry is accomplished by bringing the chip select ($\overline{CS}$), the command/data line ($C/\overline{D}$), and $\overline{WR}$ low, as shown in the timing diagram. The entry of each new data word "pushes down" the previously entered data and places the new byte on the top of stack (TOS). Data on the bottom of the stack prior to a stack entry are lost.

Data Removal

Data are removed from the stack in the Am9511 by bringing chip select ($\overline{CS}$), command/data ($C/\overline{D}$), and $\overline{RD}$ low as shown in the timing diagram. The removal of each data word redefines TOS so that the next successive byte to be removed becomes TOS. Data removed from the stack rotates to the bottom of the stack.

Command Entry

After the appropriate number of bytes of data have been entered onto the stack, a command may be issued to perform an operation on that data. Commands which require two operands for execution (e.g., add) operate on the TOS and NOS values. Single operand commands operate only on the TOS.

Commands are issued to the Am9511 by bringing the chip select ($\overline{CS}$) line low, command/data ($C/\overline{D}$) line high, and $\overline{WR}$ line low as indicated by the timing diagram. After a command is issued, the CPU can continue execution of its program concurrently with the Am9511 command execution.

Command Completion

The Am9511 signals the completion of each command execution by lowering the End Execution line ($\overline{END}$). Simultaneously the busy bit in the status register is cleared and the Service Request bit of the command register is checked. If it is a "1" the service request output level ($SVREQ$) is raised. $\overline{END}$ is cleared on receipt of an active low End Acknowledge ($\overline{EACK}$) pulse. Similarly the service request line is cleared by recognition of an active low Service Acknowledge ($\overline{SVACK}$) pulse.

Pause Operation

An active low Pause ($\overline{PAUSE}$) is provided. This line is high in its quiescent state and is pulled low by the Am9511 under the following conditions:

- 1 A previously initiated operation is in progress (device busy) and Command Entry has been attempted. In this case, the $\overline{PAUSE}$ line will be pulled low and remain low until completion of the current command execution. It will then go high, permitting entry of the new command.
- 2 A previously initiated operation is in progress and stack access has been attempted. In this case, the $\overline{PAUSE}$ line will be pulled low, will remain in that state until execution is complete, and will then be raised to permit completion of the stack access.
- 3 The Am9511 is not busy, and data removal has been requested. $\overline{PAUSE}$ will be pulled low for the length of time necessary to transfer the byte from the top of stack to the interface latch, and will then go high, indicating availability of the data.
- 4 The Am9511 is not busy, and a data entry has been requested. $\overline{PAUSE}$ will be pulled low for the length of time required to ascertain if the preceding data byte, if any has been written to the stack. If so $\overline{PAUSE}$ will immediately go high. If not $\overline{PAUSE}$ will remain low until the interface latch is free and will then go high.
- 5 When a status read has been requested, $\overline{PAUSE}$ will be pulled low for the length of time necessary to transfer the status to the interface latch, and will then be raised to permit completion of the status read. Status may be read whether or not the Am9511 is busy.

When $\overline{PAUSE}$ goes low, the APU expects the bus and bus control signals present at the time to remain stable until $\overline{PAUSE}$ goes high.

Device Status

Device status is provided by means of an internal status register whose format is shown below.

BUSY Indicates that Am9511 is currently executing a command (1 = Busy).

SIGN Indicates that the value on the top of stack is negative (1 = Negative).

ZERO Indicates that the value on the top of stack is zero (1 = Value is zero).

ERROR CODE This field contains an indication of the validity of the result of the last operation. The error codes are:

- 0000 - No error
- 1000 - Divide by zero
- 0100 - Square root or log of negative number
- 1100 - Argument of inverse sine, cosine, or e^x too large
- XX10 - Underflow
- XX01 - Overflow

CARRY Previous operation resulted in carry or borrow from most significant bit (1 = Carry/Borrow, 0 = No Carry/No Borrow).

If the BUSY bit in the status register is a one, the other status bits are not defined; if zero, indicating not busy, the operation is complete and the other status bits are defined as given above.

Read Status

The Am9511 status register can be read by the CPU at any time (whether an operation is in progress or not) by bringing the chip select ($\overline{CS}$) low, the command-data line ($C/\overline{D}$) high, and lowering $\overline{RD}$. The status register is then gated onto the data bus and may be input by the CPU.

EXECUTION TIMES

Timing for execution of the Am9511 command set is shown in the table below. Speeds are given in terms of clock cycles and should be multiplied by the clock period being used to arrive at time values. Where substantial variation of execution times is possible, the minimum and maximum values are shown, otherwise, typical values are given. Variations are data dependent. Some boundary conditions that will cause shorter execution times are not taken into account. The listing is in alphabetical order by mnemonic.

Total execution times may require allowances for operand transfer into the APU, command execution, and result retrieval from the APU. Except for command execution, these times will be heavily influenced by the nature of the data, the control interface used, the speed of memory, the CPU used, the priority allotted to DMA and interrupt operations, the size and number of operands to be transferred, and the use of chained calculations, etc.

COMMAND EXECUTION TIMES

Command Mnemonic	Clock Cycles	Command Mnemonic	Clock Cycles
ACOS	6304-8284	LOG	4474-7132
ASIN	6230-7938	LN	4298-6956
ATAN	4992-6536	NOP	4
CHSD	26-28	POPD	12
CHSF	16-20	POPF	12
CHSS	22-24	POPS	10
COS	3840-4878	PTOD	20
DAOD	20-22	PTOF	20
DDIV	196-210	PTOS	16
DMUL	194-210	PUPI	16
DMUU	182-218	PWR	8290-12032
DSUB	38-40	SADD	16-18
EXP	3794-4878	SDIV	84-94
FADD	54-368	SIN	3796-4808
FDIV	154-184	SMUL	84-94
FIXD	90-336	SMUU	80-98
FIXS	90-214	SQRT	782-870
FLTD	56-342	SSUB	30-32
FLTS	62-156	TAN	4894-5886
FMUL	146-168	XCHD	26
FSUB	70-370	XCHF	26
		XCHS	18

As mentioned, the above clock cycle execution times can be converted to μsec by multiplying by the clock period used. Several examples (minimums) are shown below.

Command Description	Am9511 (2MHz)	Am9511-1 (3MHz)	Am9511-4 (4MHz)
32-Bit Floating-Point Cosine (COS)	1920 μsec	1280 μsec	960 μsec
32-Bit Floating-Point e^x (EXP)	1897 μsec	1265 μsec	949 μsec
32-Bit Floating-Point Multiply (FMUL)	73 μsec	49 μsec	37 μsec
16-Bit Fixed-Point Multiply, Lower (SMUL)	42 μsec	28 μsec	21 μsec
32-Bit Floating-Point Add (FADD)	27 μsec	18 μsec	14 μsec
16-Bit Fixed-Point Add (SADD)	8 μsec	5 μsec	4 μsec

MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	-65°C to +150°C
Ambient Temperature Under Bias	-55°C to +125°C
VDD with Respect to VSS	-0.5V to +15.0V
VCC with Respect to VSS	-0.5V to +7.0V
All Signal Voltages with Respect to VSS	-0.5V to +7.0V
Power Dissipation (Package Limitation)	2.0W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE

Part Number	Ambient Temperature	VSS	VCC	VDD
Am9511DC	0°C ≤ T _A ≤ +70°C	0V	+5.0V ±5%	+12V ±5%
Am9511DM	-55°C ≤ T _A ≤ +125°C	0V	+5.0V ±10%	+12V ±10%

ELECTRICAL CHARACTERISTICS Over Operating Range (Note 1)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
VOH	Output HIGH Voltage	I _{OH} = -200μA	3.7			Volts
VOL	Output LOW Voltage	I _{OL} = 3.2mA			0.4	Volts
VIH	Input HIGH Voltage		2.0		VCC	Volts
VIL	Input LOW Voltage		-0.5		0.8	Volts
IIX	Input Load Current	VSS ≤ V _I ≤ VCC			±10	μA
IOZ	Data Bus Leakage	VO = 0.4V			10	μA
		VO = VCC			10	
IOC	VCC Supply Current	T _A = +25°C		50	80	mA
		T _A = 0°C			85	
		T _A = -55°C			90	
IDC	VDD Supply Current	T _A = +25°C		50	80	mA
		T _A = 0°C			85	
		T _A = -55°C			90	
CO	Output Capacitance	f _c = 1.0MHz, Inputs = 0V		8	10	pF
CI	Input Capacitance			5	8	pF
CIO	I/O Capacitance			10	12	pF

SWITCHING CHARACTERISTICS over operating range (Notes 2-3)

Parameters	Description	Am9511		Am9511-1		(Preliminary) Am9511-4		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
TAPW	$\overline{\text{EACK}}$ LOW Pulse Width	100		75		50		ns
TCDR	$\text{C}/\overline{\text{D}}$ to $\overline{\text{RD}}$ LOW Set up Time	0		0		0		ns
TCDW	$\text{C}/\overline{\text{D}}$ to $\overline{\text{WR}}$ LOW Set up Time	0		0		0		ns
TCPH	Clock Pulse HIGH Width	200		140		100		ns
TCPL	Clock Pulse LOW Width	240		160		120		ns
TCSR	$\overline{\text{CS}}$ LOW to $\overline{\text{RD}}$ LOW Set up Time	50		25		25		ns
TCSW	$\overline{\text{CS}}$ LOW to $\overline{\text{WR}}$ LOW Set up Time	50		25		25		ns
TCY	Clock Period	480	5000	330	3300	250	2500	ns
TOW	Data Bus Stable to $\overline{\text{WR}}$ HIGH Set up Time		150		100		100	ns
TEAE	$\overline{\text{EACK}}$ LOW to $\overline{\text{END}}$ HIGH Delay		200		175		150	ns
TEPW	$\overline{\text{END}}$ LOW Pulse Width (Note 4)	400		300		200		ns
TOP	Data Bus Output Valid to $\overline{\text{PAUSE}}$ HIGH Delay	0		0		0		ns
TPPWR	$\overline{\text{PAUSE}}$ LOW Pulse Width Read (Note 5)	Data	3 TCY+50	5 TCY+200	3 TCY+50	5 TCY+200	3 TCY+50	5 TCY+200
		Status	1 TCY+50	3 TCY+200	1 TCY+50	3 TCY+200	1 TCY+50	3 TCY+200
TPPWW	$\overline{\text{PAUSE}}$ LOW Pulse Width Write (Note 8)		50		50		50	ns
TPR	$\overline{\text{PAUSE}}$ HIGH to $\overline{\text{RD}}$ HIGH Hold Time	0		0		0		ns
TPW	$\overline{\text{PAUSE}}$ HIGH to $\overline{\text{WR}}$ HIGH Hold Time	0		0		0		ns
TRCD	$\overline{\text{RD}}$ HIGH to $\text{C}/\overline{\text{D}}$ Hold Time	0		0		0		ns
TRCS	$\overline{\text{RD}}$ HIGH to $\overline{\text{CS}}$ HIGH Hold Time	0		0		0		ns
TRO	$\overline{\text{RD}}$ LOW to Data Bus ON Delay	50		50		25		ns
TRP	$\overline{\text{RD}}$ LOW to $\overline{\text{PAUSE}}$ LOW Delay (Note 6)		150		100		100	ns
TRZ	$\overline{\text{RD}}$ HIGH to Data Bus OFF Delay	50	200	50	150	25	100	ns
TSAPW	$\overline{\text{SVACK}}$ LOW Pulse Width	100		75		50		ns
TSAR	$\overline{\text{SVACK}}$ LOW to $\overline{\text{SVREQ}}$ LOW Delay		300		200		150	ns
TWCD	$\overline{\text{WR}}$ HIGH to $\text{C}/\overline{\text{D}}$ Hold Time	60		30		30		ns
TWCS	$\overline{\text{WR}}$ HIGH to $\overline{\text{CS}}$ HIGH Hold Time	60		30		30		ns
TWD	$\overline{\text{WR}}$ HIGH to Data Bus Hold Time	20		20		20		ns
TWI	Write Inactive Time (Note 8)	Command	3TCY		3TCY		3TCY	
		Data	4TCY		4TCY		4TCY	
TWP	$\overline{\text{WR}}$ LOW to $\overline{\text{PAUSE}}$ LOW Delay (Note 6)		150		100		100	ns

NOTES

- Typical values are for $T_A = 25^\circ\text{C}$, nominal supply voltages and nominal processing parameters
- Switching parameters are listed in alphabetical order
- Test conditions assume transition times of 20ns or less, output loading of one TTL gate plus 100pF and timing reference levels of 0.8V and 2.0V
- $\overline{\text{END}}$ low pulse width is specified for $\overline{\text{EACK}}$ tied to VSS. Otherwise TEAE applies
- Minimum values shown assume no previously entered command is being executed for the data access. If a previously entered command is being executed, $\overline{\text{PAUSE}}$ LOW Pulse Width

- is the time to complete execution plus the time shown. Status may be read at any time without exceeding the time shown
- $\overline{\text{PAUSE}}$ is pulled low for both command and data operations
- TEX is the execution time of the current command (see the Command Execution Times table)
- $\overline{\text{PAUSE}}$ low pulse width is less than 50ns when writing into the data port or the control port as long as the duty cycle requirement (TWI) is observed and no previous command is being executed. TWI may be safely violated as long as the extended TPPWW that results is observed. If a previously entered command is being executed, $\overline{\text{PAUSE}}$ LOW Pulse Width is the time to complete execution plus the time shown

READ OPERATIONS

WRITE OPERATIONS

MOS-049

APPLICATION INFORMATION

The diagram in Figure 2 shows the interface connections for the Am9511 APU with operand transfers handled by an Am9517 DMA controller, and CPU coordination handled by an Am9519 Interrupt Controller. The APU interrupts the CPU to indicate that a command has been completed. When the performance enhancements provided by the DMA and Interrupt

operations are not required, the APU interface can be simplified as shown in Figure 1. The Am9511 APU is designed with a general purpose 8-bit data bus and interface control so that it can be conveniently used with any general 8-bit processor.

Figure 1. Am9511 Minimum Configuration Example.

MOS-050

Figure 2. Am9511 High Performance Configuration Example.

MOS-051

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PHYSICAL DIMENSIONS
Dual-In-Line

24-Pin Side-Brazed

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**POWER SUPPLY APPLICATION
AND MAINTENANCE DATA
EMA "CC" CASE****SPECIFICATIONS**

INPUT: 105 to 125 VAC or 230 to 250 VAC at 47 to 63 Hz. Derate output current 10% for 50 Hz operation.

DC OUTPUT RATINGS: See Voltage/Current Rating Chart.

REGULATION: Line regulation is rated at 0.05% for a 10% input voltage change and load regulation is rated at 0.1% for a zero to full load change.

OUTPUT RIPPLE: Better than 5 mV RMS, 3 mV peak to peak typical.

OVERLOAD PROTECTION: Self restoring current limiting (loadback type) is standard.

TEMPERATURE COEFFICIENT: $\pm 0.005\%/^{\circ}\text{C}$ typical, $\pm 0.02\%/^{\circ}\text{C}$ maximum.

COOLING: Convection cooled. Moving air is recommended when mounting in a confined area.

MOUNTING: The open frame mounts on any one of three surfaces.

OUTPUT VOLTAGE ADJUSTMENT

The output of all EconoMate II power supplies may be adjusted by means of a potentiometer located on the printed circuit board. The potentiometer is labeled "EO ADJ." During the adjustment procedure, monitor the DC output voltage by connecting a meter across the output terminals.

INPUT CONNECTIONS

When operating with 115 VAC input, place a jumper between transformer terminals one (1) and two (2) and also between three (3) and four (4). Then connect the AC primary leads to terminals one (1) and four (4) as shown in Fig. 1.

When operating with 230 VAC input, place a jumper between transformer terminals two (2) and three (3) and connect the AC primary leads to terminals one (1) and four (4) as shown in Fig. 2.

SECONDARY TRANSFORMER CONNECTIONS

On certain models it will be necessary to connect the transformer secondary to the PC board before adjusting the output voltage. This is accomplished by soldering the loose wire attached to the PC board to the appropriate tap on the transformer.

LOCAL SENSING

ECONOMATE II power supplies are factory wired for local sensing. Sensing terminals are located on the PC board. A jumper connecting the DC output and sensing terminals provides local sensing as shown in Fig. 3.

REMOTE SENSING

Remote sensing is a standard feature. To sense the output voltage directly at the load, disconnect the jumpers between the DC output terminals and sensing terminals. Connect the load to the DC output terminals. Then wire the (+) and (-) sensing terminals respectively across the load as shown in Fig. 4. This permits sensing directly at the load.

VOLTAGE/CURRENT RATING CHART

MODEL	RATING
EMA-5/6CC	5V@11.0A 6V@10.0A
EMA-9/10CC	9V@8.0A 10V@7.5A
EMA-12/15CC	12V@6.0A 15V@5.0A
EMA-18/24CC	18V@4.5A 20V@4.0A 24V@3.8A

Fig. 1

Fig. 2

Fig. 3

Fig. 4

(5) (6) (10) (15)

(5) (6) (10) (15)

NOTE: 1. 100 OHM 1/4W 5%
2. 100 OHM 1/4W 5%

Sch.	Ref.	%	%	%	%	Description
R1	1	1				JUMPER 22GA BUSBAR
R1			1			100 ohms 1/2W 10%
R1				1		270 ohms 1/2W 10%
R2	1					4.02 K ohms 1/4W 1%
R2		1	1	1		1.15 K ohms 1/4W 1%
R3	1					3.16 K ohms 1/4W 1%
R4	1					68 ohms 1/4W 5%
R4		1				62 ohms 1/4W 5%
R4			1			100 ohms 1/4W 5%
R4				1		150 ohms 1/4W 5%
R5	1					68 ohms 1/4W 5%
R5		1				62 ohms 1/4W 5%
R5			1			100 ohms 1/4W 5%
R5				1		150 ohms 1/4W 5%
R6	1					0.067 ohms 3W 5%
R6		1				0.1 ohm 3W 5%
R6			1			0.15 ohm 3W 5%
R6				1		0.24 ohm 3W 5%
R7	1					0.067 ohms 3W 5%
R7		1				0.01 ohm 3W 5%
R7			1			0.15 ohm 3W 5%

Sch.	Ref.	%	%	%	%	Description
R7				1		0.24 ohm 3W 5%
R8	1					2.2 K ohms 1/4W 5%
R8		1				1.5 K ohms 1/4W 5%
R8			1			2.7 K ohms 1/4W 5%
R8				1		4.3 K ohms 1/4W 5%
R9	1	1	1	1		100 ohms 1/4W 5%
R10	1	1	1	1		3.3 K ohms 1/4W 5%
R11	1					470 ohms 1/4W 5%
R11		1				1 K ohm 1/4W 5%
R11			1			1.5 K ohms 1/4W 5%
R11				1		1.8 K ohms 1/4W 5%
R12	1	1	1	1		2 K ohms 20%
R13	1					182 ohms 1/4W 1%
R13		1				100 ohms 1/2W 1%
R13			1			1 K ohms 1/2W 1%
R14	1					1.5 K ohms 1/2W 1%
R14		1				3.48 K ohms 1/2W 1%
R14			1			2.05 K ohms 1/2W 1%
R14				1		1.15 K ohms 1/2W 1%
R15	1	1	1	1		10 ohms 1/4W 5%

Sch.	Ref.	%	%	%	%	Description
R16	1	1	1	1		10 ohms 1/4W 5%
C1	1					CAP 30,000 MFD 15V
C1		1	1			CAP 14,000 MFD 30V
C1			1			CAP 8,900 MFD 50V
C2	1					CAP 1,000 MFD 16V
C2			1			CAP 330 MFD 35V
C3	1	1	1	1		CAP 4.7 MFD 35V
C4	1	1	1	1		CAP 0.001 MFD 500V
C5	1					CAP 15 MFD 20V
C5			1			CAP 6.8 MFD 35V
C6	1					CAP 1,000 MFD 16V
C6		1				CAP 330 MFD 35V
C6			1			CAP 220 MFD 50V
CR1	1	1	1	1		BRIDGE 30 amps
CR2	1					DIODE CER 68
CR3			1			DIODE IN4752A
CR4	1	1	1	1		DIODE 100V
Q1	1	1	1	1		TRANS 64502
Q2	1	1	1	1		TRANS 64502
Q3	1	1	1	1		TRANS 64502
IC1	1	1	1	1		INT CRT Type 723

POWER/MATE CORP.

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POWER SUPPLY APPLICATION AND MAINTENANCE DATA EMA "B" CASE

SPECIFICATIONS

INPUT 105 to 125 VAC or 210 to 250 VAC at 47 to 63 Hz. Derate output current 10% for 50 Hz operation.

DC OUTPUT RATINGS See Voltage/Current Rating Chart.

REGULATION Line regulation is rated at 0.05% for a 10% input voltage change and load regulation is rated at 0.1% for a zero to full load change.

OUTPUT RIPPLE Better than 1 mV RMS, 3 mV peak to peak typical.

OVERLOAD PROTECTION Self restoring current limiting (foldback type) is standard.

TEMPERATURE COEFFICIENT $\pm 0.005\%/^{\circ}\text{C}$ typical, $\pm 0.02\%/^{\circ}\text{C}$ maximum.

COOLING Convection cooled. Moving air is recommended when mounting in a confined area.

MOUNTING The open frame mounts on any one of three surfaces.

OUTPUT VOLTAGE ADJUSTMENT

The output of all EconoMATE II power supplies may be adjusted by means of a potentiometer located on the printed circuit board. The potentiometer is labeled EO ADJ. During the adjustment procedure, monitor the DC output voltage by connecting a meter across the output terminals.

INPUT CONNECTIONS

When operating with 115 VAC input, place a jumper between transformer terminals one (1) and two (2) and also between three (3) and four (4). Then connect the AC primary leads to terminals one (1) and four (4) as shown in Fig. 1.

When operating with 230 VAC input, place a jumper between transformer terminals two (2) and three (3) and connect the AC primary leads to terminals one (1) and four (4) as shown in Fig. 2.

SECONDARY TRANSFORMER CONNECTIONS

On certain models it will be necessary to connect the transformer secondary to the PC board before adjusting the output voltage. This is accomplished by soldering the loose wire attached to the PC board to the appropriate tap on the transformer.

LOCAL SENSING

ECONOMATE II power supplies are factory wired for local sensing. Sensing terminals are located on the PC board. A jumper connecting the DC output and sensing terminals provides local sensing as shown in Fig. 3.

REMOTE SENSING

Remote sensing is a standard feature. To sense the output voltage directly at the load, disconnect the jumpers between the DC output terminals and sensing terminals. Connect the load to the DC output terminals. Then wire the (+) and (-) sensing terminals respectively across the load as shown in Fig. 4. This permits sensing directly at the load.

MODEL

Voltage/current RATING

EMA-5/6 B

5V @ 3.0A

EMA-9/10 B

6V @ 2.5A

EMA-9/10 B

9V @ 1.8A

EMA-12/15 B

10V @ 1.8A

EMA-12/15 B

12V @ 1.5A

EMA-18/24 B

15V @ 1.3A

EMA-18/24 B

18V @ 1.2A

EMA-18/24 B

20V @ 1.0A

EMA-18/24 B

24V @ 1.0A

Fig 1

Fig 2

Fig 3

Fig 4

SCHEMATIC# 27816

EMA-9/10 B

EMA-12/15 B

EMA-18/24 B

SCHEMATIC# 27817

EMA-5/6 B

NO.	PN/PART#	DESCRIPTION	QTY	REF	NO.	PN/PART#	DESCRIPTION	QTY	REF
1	747822A	Ass'y	1	1	20	AB210000	RES 10K W/W $\pm 5\%$	1	1
2	27817	SCHEMATIC	1	1	21	PF290201	POT 20K	1	1
3	27816	SCHEMATIC	1	1	22	09001500	IC	1	1
4	C6047400	CAP 4700MFD 35V	2	1	23	09001000	TRANSISTOR NPN	1	1
5	C6022604	CAP 2200MFD 40V	2	2	24	09001100	TRANSISTOR NPN	1	1
6	C6141100	CAP 4700MFD 10V	2	2	25	05051000	TRANSISTOR NPN	1	1
7	C6022700	CAP 2200MFD 35V	2	2	26	AC244000	RESISTOR 40K W/W $\pm 10\%$	1	1
8	W601000	JUMPER	4	4	27	AC244000	RESISTOR 40K W/W $\pm 10\%$	1	1
9	C6010200	CAP 401MFD 35V	1	1	28	AB215100	RES 15K W/W $\pm 10\%$	1	1
10	C7247300	CAP 4.7MFD 35V	1	1	29	W621000	JUMPER	1	1
11	C7813400	CAP 15MFD 30V	1	1	30	AC210200	RESISTOR 40K W/W $\pm 10\%$	1	1
12	C0310300	CAP 10MFD 30V	1	1	31	AC210200	RESISTOR 40K W/W $\pm 10\%$	1	1
13	C7248100	CAP 55MFD 35V	1	1	32	AC210200	RESISTOR 40K W/W $\pm 10\%$	1	1
14	C6222100	CAP 220MFD 35V	1	1	33	AC210200	RESISTOR 40K W/W $\pm 10\%$	1	1
15	09001000	DIODE 1A 200V	2	2	34	AC210200	RESISTOR 40K W/W $\pm 10\%$	1	1
16	09001000	DIODE 1A 200V	2	2	35	AC210200	RESISTOR 40K W/W $\pm 10\%$	1	1
17	09001000	DIODE 1A 200V	2	2	36	AC210200	RESISTOR 40K W/W $\pm 10\%$	1	1
18	09001000	DIODE 1A 200V	2	2	37	AC210200	RESISTOR 40K W/W $\pm 10\%$	1	1
19	09001000	DIODE 1A 200V	2	2	38	AC210200	RESISTOR 40K W/W $\pm 10\%$	1	1

NO.	PN/PART#	DESCRIPTION	QTY	REF	NO.	PN/PART#	DESCRIPTION	QTY	REF
39	AB215200	RES 15K W/W $\pm 10\%$	1	1	40	AB215200	RES 15K W/W $\pm 10\%$	1	1
41	AB215200	RES 15K W/W $\pm 10\%$	1	1	42	AB215200	RES 15K W/W $\pm 10\%$	1	1
43	AB215200	RES 15K W/W $\pm 10\%$	1	1	44	AB215200	RES 15K W/W $\pm 10\%$	1	1
45	AB215200	RES 15K W/W $\pm 10\%$	1	1	46	AB215200	RES 15K W/W $\pm 10\%$	1	1
47	AB215200	RES 15K W/W $\pm 10\%$	1	1	48	AB215200	RES 15K W/W $\pm 10\%$	1	1
49	AB215200	RES 15K W/W $\pm 10\%$	1	1	50	AB215200	RES 15K W/W $\pm 10\%$	1	1
51	AB215200	RES 15K W/W $\pm 10\%$	1	1	52	AB215200	RES 15K W/W $\pm 10\%$	1	1
53	AB215200	RES 15K W/W $\pm 10\%$	1	1	54	AB215200	RES 15K W/W $\pm 10\%$	1	1
55	AB215200	RES 15K W/W $\pm 10\%$	1	1	56	AB215200	RES 15K W/W $\pm 10\%$	1	1
57	AB215200	RES 15K W/W $\pm 10\%$	1	1	58	AB215200	RES 15K W/W $\pm 10\%$	1	1

POWER/MATE CORP.

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ETA / ETR SERIES APPLICATIONS DATA

SPECIFICATIONS

MT: 105 to 125/210 to 250 VAC at 47 to 63 Hz. Except ETA-B Models which are: 105 to 125 VAC only at 47 to 63 Hz. (Desired output current 10% for 50Hz operation.)

DC OUTPUT RATINGS:

See back page for specific models.

REGULATION: Line regulation is rated at $\pm 0.05\%$ for a 10% input voltage change. Load regulation is rated at 0.1% for a zero to full load change.

OUTPUT RIPPLE: Less than 1mV RMS. 3mV peak-to-peak is typical.

REMOTE SENSING: Standard on all but ETA-B.

OVERLOAD PROTECTION: Self-restoring current limiting, fold-back type.

TEMPERATURE COEFFICIENT: $\pm 0.005\%/^{\circ}\text{C}$ is typical.

OVERVOLTAGE PROTECTION: Optional on all but ETA-B.

COOLING: Convection cooled. Moving air is recommended when mounting in a confined area.

MOUNTING: See outline drawing.

OPERATING INSTRUCTIONS

GENERAL

ETA and ETR power supplies are carefully inspected and tested to insure conformance to the above specifications. However, to insure satisfactory performance and long life, it is important to operate and maintain the power supply properly in accordance with the following instructions.

MOUNTING

ETA power supplies are designed for convection cooling. It is important not to impede the air flow across the power supply case. Heat is the primary cause of failure in any piece of electronic equipment. Impeding the flow of convection air over your power supply may result in a shortening of its long-life design.

INPUT CONNECTIONS

On models with single AC input terminals, connect 115 VAC leads to terminals 1 and 2. On models with dual AC input terminals connect as follows:

For 115 VAC input, place a jumper between transformer terminals 1 and 2, and between 3 and 4. Then connect the AC primary leads to terminals 1 and 4, as shown in Fig. 1.

For 230 VAC input, place a jumper between transformer terminals 2 and 3 and connect the AC primary leads to terminals 1 and 4 as shown in Fig. 2.

115VAC Fig. 1

230VAC Fig. 2

OUTPUT CONNECTIONS

Positive and negative output terminals are marked and located on printed circuit boards. Some outputs have secondary leads which must be soldered to the appropriate transformer taps according to the voltage output required, as indicated in the following table:

SERIES	OUTPUT VOLTAGE	OUTPUT A TAP NO.	OUTPUT B TAP NO.
ETA-B	12V	4	7
	15V	5	8
ETA-C,D	12V	6	9
	15V	7	10
ETA-E	12V	OUTPUT B TAP NO. 9	OUTPUT C TAP NO. 12
	15V	10	13
	18V	9	12
	20V	9	12
	24V	10	13

OUTPUT VOLTAGE ADJUSTMENT

Outputs are adjustable with a potentiometer located on the printed circuit board. During the adjustment procedure, monitor the DC output voltage by connecting a meter across the output terminals.

CURRENT LIMIT ADJUSTMENT

The current limit adjustment is factory set for maximum output current as indicated in the Voltage/Current Rating Chart. However, output current can be readjusted to a lower level by means of the "I LIM ADJ" potentiometer (when provided), located on the PC board. To readjust output current, proceed as follows:

1. Turn off AC power.
2. Disconnect the load across the output terminals (if necessary).
3. Rotate I LIM ADJ potentiometer to its maximum clockwise position.
4. Connect a variable load, in series with an ammeter, across the output terminals as shown in Figure 3. This variable load should be capable of providing at least 125% of the actual full load.
5. Connect a voltmeter across the output terminals as shown in Figure 3.
6. Turn on AC power and adjust the variable load to obtain approximately 125% of the actual full load as indicated on the ammeter.
7. Adjust the I LIM ADJ potentiometer until the power supply drops between 1 and 5 mV out of regulation as indicated on the voltmeter. At this point, the power supply will produce the desired output current.
8. Turn off AC power and disconnect the variable load, ammeter and voltmeter connected across the output terminals.
9. Connect the actual load across the output terminals.

Fig. 3 Current Limit Adj Setup

LOCAL SENSING

ECONOMATE II power supplies are factory wired for local sensing. Sensing terminals are located on the PC board. A jumper connecting the DC output and sensing terminals provides local sensing as shown in Figure 4.

Fig. 4 Local Sensing

REMOTE SENSING

Remote sensing is a standard feature. To sense the output voltage directly at the load, disconnect the jumpers between the DC output terminals and sensing terminals. Connect the load to the DC output terminals. Then wire the (+) and (-) sensing terminals respectively across the load as shown in Figure 5. This permits sensing directly at the load.

Fig. 5 Remote Sensing

MODEL	OUTPUT A	SCHEMATIC NO.	OUTPUT B	SCHEMATIC NO.
ETA-12/15B	12V-7A or 15V-7A	6	12V-7A or 15V-7A	6
ETA-5B	5V-1.5A or 6V-1.3A	6	5V-1.5A or 6V-1.3A	6
ETA-515B	5V-1.5A or 6V-1.3A	6	15V-7A or 12V-7A	6
ETA-524B	5V-1.5A or 6V-1.3A	6	24V-0.5A	6

MODEL	OUTPUT A	SCHEMATIC NO.	OUTPUT B	SCHEMATIC NO.
ETA-12/15C	12V-2.0A or 15V-1.7A	3	12V-2.0A or 15V-1.7A	3
ETA-5C	5V-4.0A or 6V-3.3A	2	5V-4.0A or 6V-3.3A	2
ETA-515C	5V-4.0A or 6V-3.3A	2	15V-1.7A or 12V-2.0A	3
ETA-524C	5V-4.0A or 6V-3.3A	2	24V-1.3A	3

MODEL	OUTPUT A	SCHEMATIC NO.	OUTPUT B	SCHEMATIC NO.
ETA-12/15D	12V-4.0A or 15V-3.5A	5	12V-4.0A or 15V-3.5A	5
ETA-5D	5V-7.5A or 6V-6.5A	4	5V-7.5A or 6V-6.5A	4
ETA-515D	5V-7.5A or 6V-6.5A	4	15V-3.5A or 12V-4.0A	5
ETA-524D	5V-7.5A or 6V-6.5A	4	24V-3.0A	5

MODEL	SCHEMATIC		SCHEMATIC		SCHEMATIC	
	OUTPUT A	NO.	OUTPUT B	NO.	OUTPUT C	NO.
ETR-122E	5V, 6A or 6V, 5A	4	12V, 1.5A or 15V, 1.3A	3	12V, 1.5A or 15V, 1.3A	3
ETR-142E	5V, 6A or 6V, 5A	4	12V, 1.5A or 9V, 1.2A or 5V, .8A	1	12V, 1.5A or 15V, 1.3A	3
ETR-113E	5V, 6A or 6V, 5A	4	5V, 3A or 6V, 2.5A	2	18V, 1A or 20V, 1A or 24V, 1A	3
ETR-132E	5V, 6A or 6V, 5A	4	18V, 1A or 20V, 1A or 24V, 1A	3	12V, 1.5A or 15V, 1.3A	3

MODEL ETA-C, ETA-D, ETR

MODEL ETA-B

MODEL	A	B	C	D	E	F	G	H	J	K
ETA-C	7.87	2.50	1.25	.75	2.19	4.75	5.09	.37	3.38	4.0
ETA-D	9.38	2.75	1.25	.75	2.81	5.81	6.10	.50	4.13	4.88
ETR	11.00	2.75	1.25	.75	3.25	6.75	7.00	.50	4.12	4.88

SCHEMATIC 1

SCHEMATIC 2

SCHEMATIC 3

DESCRIPTION	SCH REF	5/8	15	24	9
SCHEMATIC		1	1	1	
CAP 4700 MFD 16V	C1 C2	2			
CAP 2200 MFD 40V	C1 C2	2	2	2	
CAP 470 MFD 16V	C3 C7	2			
CAP 220 MFD 35V	C3 C4		2		
JUMPER	C4			1	
CAP 001 MFD 100V	C5	1			
CAP 4.7 MFD 35V	C6 C8	1	1	1	
CAP 15 MFD 20V	C6	1			
CAP 001 MFD 100V	C8		1	1	1
CAP 8.8 MFD 35V	C7		1	1	
CAP 220 MFD 35V	C8		1	1	1
DIODE 1A 200V	CR1 CR2	2	2		
RECT TO 3.15A	CR3	1			
BRIDGE 5A 100V	CR3		1	1	
DIODE 2A 200V	CR5 CR4	1	1	1	
DIODE 2ENER 33V	CR4		1	1	
POT 100 ohms	R9	1	1	1	
POT 2K ohms	R11	1	1	1	1
IC	IC1	1	1	1	1
TRANSISTOR NPN	Q1	1			
TRANSISTOR NPN	Q1		1	1	1
TRANSISTOR NPN	Q2	1	1	1	1
RESISTOR 68 ohms 1/4w ± 10%	R1	1			
RES 82 ohms 1/4w ± 10%	R1				
RES 130 ohms 1/4w ± 10%	R1		1		
JUMPER	R1			1	
RESISTOR 4.02K 1/2w	R2	1			1
RES 1K ohms 1/2w ± 10%	R2				
RES 1.2K ohms 1/4w ± 10%	R2		1		
RES 100 ohms 1/4w ± 10%	R2			1	
RES 7.14K ohms 1/4w ± 5%	R3	1			1
RES 1.2K ohms 1/4w ± 5%	R3		1	1	
RES 5.6K ohms 1/4w ± 5%	R4	1			
RES 8.2K ohms 1/4w ± 5%	R4				
RES 12K ohms 1/4w ± 5%	R4		1		1
RES 15K ohms 1/4w ± 5%	R4			1	
RES 470 ohms 1/4w ± 5%	R5	1			
RES 680 ohms 1/4w ± 5%	R5		1	1	1
RES 1 ohms 3w ± 5%	R7	1			
RES 0.15 ohms 3w ± 5%	R7		1		
RES 0.27 ohms 2w ± 10%	R7			1	1
RES 3.3K ohms 1/4w ± 5%	R8	1	1	1	1
RES 880 ohms 1/4w ± 5%	R9	1			
RES 1.5K ohms 1/4w ± 5%	R9				1
RES 1.8K ohms 1/4w ± 5%	R9		1		
RES 3.9K ohms 1/4w ± 5%	R9			1	
RES 182 ohms 1/2w ± 1%	R10	1			
RES 3.48 ohms K 1/4w ± 1%	R10				
RES 2.05K ohms 1/4w ± 1%	R10		1		
RES 1.15K ohms 1/4w ± 1%	R10			1	
RES 1.4K ohms 1/4w ± 1%	R12	1		1	
RES 100 ohms 1/4w ± 1%	R12				1
RES 1K ohms 1/4w ± 1%	R12		1		
RES 10 ohms 1/4w ± 5%	R13 R14	2	2	2	
TRANSFORMER		1	1	1	
CAP 4000/30	C1				1
RES 100 ohms 1/4w ± 5%	R5				1
RES 825 1/4w ± 1%	R10				1
CAP 4.7 MFD 35V	C5				1
DIODE Z A 200V	CR1 5				5

DESCRIPTION	SCH REF	56	15	24
Cap 25000mfd 15v	C1	1		
Cap 11000mfd 25v	C1		1	
Cap 4000mfd 40v	C1			1
Cap 1000mfd 16v	C3,C7	2		
Cap 470mfd 40v	C3,C4		2	
Cap 150mfd 83v	C3,C4			2
Cap 47mfd 35v	C4	1		
Cap .001mfd 100v	C5	1		
Cap 47mfd 35v	C5		1	1
Cap 15mfd 20v	C6	1		
Cap .001mfd 100v	C6		1	1
Cap 88mfd 35v	C7		1	1
Cap 330mfd 35v	C8		1	
Cap 220mfd 50v	C8			1
Res 4.02 ohms 1/4w	R1	1		
Res 120 ohms 2w 5%	R1			
Res 100 ohms 3w 3%	R1		1	
Res 150 ohms 2w 5%	R1			1
Res 220 ohms 2w 5%	R1			1
Res 3.16k ohms 1/4w 1%	R2	1		
Res 150 ohms 1/4w 10%	R2			
Res 270 ohms 1/4w 10%	R2		1	
Res 1k ohm 2w 10%	R2			
Res 1.5k 3w 5%	R2			1
Res 2.7k ohms 1/4w 5%	R3	1		
Res 1.15 1/4w 1%	R3		1	1
Res 100 ohms 1/4w 10%	R4	1		
Res 2.7k ohms 1/4w 5%	R4		1	1
Res 3.3k ohms 1/4w 5%	R5	1		
Res 100 ohms 1/4w 10%	R5			
Res 180 ohms 1/4w 10%	R5		1	
Res 220 ohms 1/4w 10%	R5			1
Pot 100 ohms	R6	1	1	1
Res 680 ohms 1/4w 5%	R7	1		
Res 1k ohms 1/4w 5%	R7			
Res 1.5k ohms 1/4w 5%	R7		1	
Res 1.8k ohms 1/4w 5%	R7			1
Res .04 ohms 3w 1%	R8	1		
Res .007 3w 1%	R8			
Res 0.1 ohms 3w 5%	R8		1	
Res 0.2 ohms 3w 1%	R8			1
Res 182 ohms 1/4w 1%	R9	1

SCHEMATIC

4

SCHEMATIC

5

Res 3.3k ohms 1/4w 5%	R8		1	1
Pot 2k ohms 20%	R10		1	1
Res 1.5k ohms 1/4w 1%	R11		1	
Res 3.48k ohms 1/4w 1%	R12			
Res 2.06k ohms 1/4w 1%	R12		1	
Res 10 ohms 1/4w 5%	R12,R13	2		
Diode	CR1,CR2	2	2	2
Bridge 15A	CR3	1	1	1

Diode	CR4,CR6	1	1	1
Bridge 15A	CR4		1	1
Diode zener 33v	CR5		1	1
IC	IC1	1	1	1
Transistor npn	Q1		1	
Transistor npn	Q1		1	1
Transistor npn	Q2		1	1
Transistor npn	Q2			1

DESCRIPTION	SCH REF	56	15	24
Jumper	R1	1	1	
Res 180 ohms 1/4w ± 10%	R1			1
Res 620 ohms 1/4w ± 10%	R1			1
Res 4.3K 1/4w ± 5%	R2	1		
Res 1.2K 1/4w ± 5%	R2,R12		1	3
Res 3.3K 1/4w ± 5%	R3,R6	2	1	1
Res 870 ohms 1/4w ± 5%	R4,R6	2	1	1
Res 15K 1/4w ± 5%	R5	1		
Res 22K 1/4w ± 5%	R5			
Res 27K 1/4w ± 5%	R5		1	1
Res 680 ohms 1/4w ± 5%	R6,R12	1		
Res 820 ohms 1/4w ± 5%	R6		1	
Res 33 ohms 2w ± 5%	R7	1		
Res 51 ohms 2w ± 5%	R7			
Res 68 ohms 2w ± 5%	R7		1	
Res 1 ohm 2w ± 5%	R7			1
Res 150 ohms 1/4w ± 5%	R8,R12	2	1	1
Res 1K 1/4w ± 5%	R10,13	1		1
Res 1.5K 1/4w ± 5%	R10,13		1	
Res 2.2K 1/4w ± 5%	R10,13		1	
Res 100 ohms 1/4w ± 5%	R12			
Res 1.2K 1/4w ± 5%	R13	1		
Res 8.2K 1/4w ± 5%	R10			1
Cap 4700 mfd 16V	C1	1		
Cap 2200 mfd 40V	C1		1	
Cap 1000 mfd 50V	C1			1
Cap 220 mfd 35V	C2	1		
Jumper	C2		1	1
Cap 47 mfd 35V	C3	1	1	1
Cap .001 mfd 100V	C4	1	1	1
Cap 15 mfd 20V	C5	1		
Cap 58 mfd 40V	C5		1	1
Diode, Zener	CR2			1
Diode, Si	CR3	1	1	1
Transistor	Q1	1	1	1
Diode, Bridge 2.5A	CR1	1	1	1
Pot 15K	R11	1	1	1
IC	IC1	1	1	1

SCHEMATIC

6

WESTERN DIGITAL MOS/LSI

FD1771 A/B - 01 FD1771 A/B - 02

DATA SHEET

FLOPPY DISK FORMATTER/CONTROLLER

GENERAL DESCRIPTION

The FD1771 is a MOS/LSI device that performs the functions of a Floppy Disk Controller/Formatter. The device is designed to be included in the disk drive electronics, and contains a flexible interface organization that accommodates the interface signals from most drive manufacturers. The FD1771 is compatible with the IBM 3740 data entry system format.

The processor interface consists of a 8-bit bi-directional bus for data, status, and control word transfers. The FD1771 is set up to operate on a multiplexed bus with other bus-oriented devices.

The FD1771 is fabricated in N-channel Silicon Gate MOS technology and is TTL compatible on all inputs and outputs.

APPLICATIONS

- o FLOPPY DISK DRIVE INTERFACE
- o SINGLE OR MULTIPLE DRIVE
CONTROLLER/FORMATTER
- o NEW MINI-FLOPPY CONTROLLER

FEATURES

- o SOFT SECTOR FORMAT COMPATIBILITY
- o AUTOMATIC TRACK SEEK WITH VERIFICATION
- o READ MODE
Single/Multiple Record Read with Automatic Sector Search or Entire Track Read
Selectable 128 Byte or Variable Length Record
- o WRITE MODE
Single/Multiple Record Write with Automatic Sector Search
Entire Track Write for Diskette Initialization
- o PROGRAMMABLE CONTROLS
Selectable Track to Track Stepping Time
Selectable Head Settling and Head Engage Times
Selectable Three Phase or Step and Direction and Head Positioning Motor Controls
- o SYSTEM COMPATIBILITY
Double Buffering of Data 8 Bit Bi-Directional Bus for Data, Control and status
DMA or Programmed Data Transfers
All Inputs and Outputs are TTL Compatible

DEC. 76

FD1771 SYSTEM BLOCK DIAGRAM
FIG 1

A Suffix = Ceramic
B Suffix = Plastic

FD1771 PIN CONNECTIONS
FIG 2

FD177† BLOCK DIAGRAM
FIG 3

ORGANIZATION

The Floppy Disk Formatter block diagram is illustrated on Page 2. The primary sections include the parallel processor interface and the Floppy Disk interface.

Data Shift Register - This 8-bit register assembles serial data from the Read Data input (FDDATA) during Read operations and transfers serial data to the Write Data output during Write operations

Data Register - This 8-bit register is used as a holding register during Disk Read and Write operations. In Disk Read operations the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations information is transferred in parallel from the Data Register to the Data Shift Register.

When executing the Seek command the Data Register holds the address of the desired Track position. This register can be loaded from the DAL and gated onto the DAL under processor control.

Track Register - This 8-bit register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read.

Write, and Verify operations The Track Register can be loaded from or transferred to the DAL. This Register should not be loaded when this device is busy.

Sector Register (SR) - This 8-bit register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. The Sector Register contents can be loaded from or transferred to the DAL. This register should not be loaded when the device is busy.

Command Register (CR) - This 8-bit register holds the command presently being executed. This register should not be loaded when the device is busy unless the execution of the current command is to be overridden. This latter action results in an interrupt. The command register can be loaded from the DAL, but not read onto the DAL.

Status Register (STR) - This 8-bit register holds device Status information. The meaning of the Status bits are a function of the contents of the Command Register. This register can be read onto the DAL, but not loaded from the DAL.

CRC Logic This logic is used to check or to generate the 16-bit Cyclic Redundancy Check (CRC). The polynomial is $G(x) = x^{16} + x^{12} + x^5 + 1$.

The CRC includes all information starting with the address mark and up to the CRC characters. The CRC register is preset to ones prior to data being shifted through the circuit.

Arithmetic/Logic Unit (ALU) - The ALU is a serial comparator, incrementer, and decrements and is used for register modification and comparisons with the disk recorded ID field.

AM Detector - The Address Mark detector is used to detect ID, Data, and Index address marks during Read and Write operations.

Timing and Control - All computer and Floppy Disk Interface controls are generated through this logic. The internal device timing is generated from a 2.0 MHz external crystal clock.

PROCESSOR INTERFACE

The interface to the processor is accomplished through the eight Data Access Lines (DAL) and associated control signals. The DAL are used to transfer Data, Status, and Control words out of, or into the FD1771. The DAL are three state buffers that are enabled as output drivers when Chip Select (CS) and Read Enable (RE) are active (low logic state) or act as input receivers when CS and Write Enable (WE) are active.

When transfer of data with the Floppy Disk Controller is required by the host processor, the device address is decoded and CS is made low. The least-significant address bits A1 and A0, combined with the signals RE during a Read operation or WE during a Write operation are interpreted as selecting the following registers:

A1-A0	READ (RE)	WRITE (WE)
0 0	Status Register	Command Register
0 1	Track Register	Track Register
1 0	Sector Register	Sector Register
1 1	Data Register	Data Register

During Direct Memory Access (DMA) types of data transfers between the Data Register of the FD1771 and the processor, the Data Request (DRQ) output is used in Data Transfer control. This signal also appears as status bit 1 during Read and Write operations.

On Disk Read operations the Data Request is activated (set high) when an assembled serial input byte is transferred in parallel to the Data Register. This bit is cleared when the Data Register is read by the processor. If the Data Register is read after one or more characters are lost, by having new data transferred into the register prior to processor readout, the Lost Data bit is set in the Status Register. The Read operation continues until the end of sector is reached.

On Disk Write operations the Data Request is activated when the Data Register transfers its contents to the Data Shift Register, and requires a new data byte. It is reset when the Data Register is loaded with new data by the processor. If new data is not loaded at the time the next serial byte is required by the Floppy Disk, a byte of zeroes is written on the diskette and the Lost Data bit is set in the Status Register.

The Lost Data bit and certain other bits in the Status Register will activate the interrupt request (INTRQ). The interrupt line is also activated with normal completion or abnormal termination of all controller operations. The INTRQ signal remains active until reset by reading the Status Register to the processor or by the loading of the Command Register. In addition, the INTRQ is generated if a Force Interrupt command condition is met.

FLOPPY DISK INTERFACE

The Floppy Disk interface consists of head positioning controls, write gate controls, and data transfers. A 2.0 MHz $\pm 1\%$ square wave clock is required at the CLK input for internal control timing, (may be 1.0 MHz for mini floppy.)

HEAD POSITIONING

Four commands cause positioning of the Read-Write head (see Command Section). The period of each positioning step is specified by the *r* field in bits 1 and 0 of the command word. After the last directional step an additional 10 milliseconds of head settling time takes place. The four programmable stepping rates are tabulated below.

The rates (shown in Table 1) can be applied to a Three Phase Motor or a Step-Direction Motor through the device interface. When the 3PM input is connected to ground the device operates with a three-phase motor control interface, with one active low signal per phase on the three output signals PH1, PH2 and PH3. The stepping sequence, when stepping in, is Phases 1-2-3-1, and when stepping out, Phases 1-3-2-1. Phase 1 is active low after Master Reset.

The Step-Direction Motor Control interface is activated by leaving input 3PM open or connecting it to +5V. The Phase 1 pin PH1 becomes a Step pulse of 4 microseconds width. The Phase 2 pin PH2 becomes a direction control with a high voltage on this pin indicating a Step In, and a low voltage indicating a Step Out. The Direction output is valid a minimum of 24 μ s prior to the activation of the Step pulse.

When a Seek, Step or Restore command is executed an optional verification of Read-Write head position can be performed by setting bit 2 in the command word to a logic 1. The verification operation begins at the end of the 10 millisecond settling time after the head is loaded against the media. The track number from the first encountered ID Field is compared against the contents of the Track

Register If the track numbers compare and the ID Field Cyclic Redundancy Check (CRC) is correct, the verify operation is complete. If track comparison is not made but the CRC checks, an interrupt is generated, the Seek Error status (Bit 4) is set and the Busy status bit is preset. If there is no track comparison nor a valid CRC a step is made in the same direction as specified and the verify operation is repeated. The additional stepping can be repeated twice to account for two defective tracks. If no verification is received at this point, a Seek error (Bit 4) is set in the status word.

TABLE 1
STEPPING RATES

r1	r0	1771-02 CLK=2MHZ TEST=1	1771-01 CLK=2MHZ TEST=1	1771-01 CLK=1MHZ TEST=1	1771 or 01 CLK=2MHZ TEST=0	1771 or 01 CLK=1MHZ TEST=0
0	0	8ms	8ms	12ms	*APPROX 400us	*APPROX 800us
0	1	8ms	6ms	12ms		
1	0	8ms	10ms	20ms		
1	1	10ms	20ms	40ms		

*For exact times consult WDC

The Head Load (HDL) output controls the movement of the read/write head against the disk for data recording or retrieval. It is activated at the beginning of a Read, Write (E Flag On) or Verify Operation, or a Seek or Step operation with the head load bit, h, a logic one remains activated until the third index pulse following the last operation which uses the read/write head. Reading or Writing does not occur until a minimum of 10 msec delay after the HDL signal is made active. If executing the type 2 commands with the E flag off, there is no 10 msec delay and the head is assumed to be engaged. The delay is determined by sampling of the Head Load Timing (HLT) input every 10 msec. A low logic state input, generated from the Head Load output transition and delayed externally, identifies engagement of the head against the disk. In the Seek and Step commands, the head is loaded at the start of the command execution when the h bit is a logic one. In a verify command the head is loaded before stepping to the destination track on the disk whenever the h bit is a logic zero.

DISK READ OPERATION

The 2.0 MHz external clock provided to the device is internally divided by 4 to form the 500 KHz clock rate for data transfer. When reading data from a diskette this divider is synchronized to transitions of the Read Data (FDDATA) input. When a transition does not occur on the 500 KHz clock active state, the clock divider circuit injects a clock to maintain a continuous 500 KHz data clock. The 500 KHz data clock is further divided by 2 internally to separate the clock and information bits. The divider is phased to the information by the detection of the address mark.

In the internal data read and separation mode the Read Data input toggles from one state to the opposite state for each logic one bit of clock or information. This signal can be derived from the amplified, differentiated,

and sliced Read Head signal, or by the output of a flip-flop toggling on the Read Data pulses. This input is sampled by the 2 MHz clock to detect transitions.

The chip can also operate on externally separated data, as supplied by methods such as Phase Lock loop, One Shots, or variable frequency oscillators. This is accomplished by grounding the External Data Separator (XTDS) INPUT. When the Read Data input makes a high to-low transition, the information input to the FDDATA line is clocked into the Data Shift Register. The assembled 8 bit data from the Data Shift Register are then transferred to the Data Register.

The normal sector length for Read or Write operations with the IBM 3740 format is 128 bytes. This format or binary multiples of 128 bytes will be adopted by setting a logic 1 in Bit 3 of the Read Track and Write Track commands. Additionally, a variable sector length feature is provided which allows an indicator recorded in the ID Field to control the length of the sector. Variable sector lengths can be read or written in Read or Write commands respectively by setting a logic 0 in Bit of the command word. The sector length indicator specifies the number of 16 byte groups or $16 \times N$, where N is equal to 1 to 256 groups. An indicator of all zeroes is interpreted as 256 sixteen byte groups.

DISK WRITE OPERATION

After data is loaded from the processor into the Data Register, and is transferred to the Data Shift Register, data will be shifted serially through the Write Data (WD) output. Interlaced with each bit of data is a positive clock pulse of 0.5 usec duration. This signal may be used to externally toggle a flip-flop to control the direction of Write Current flow.

When writing is to take place on the diskette the Write Gate (WG) output is activated, allowing current to flow into the Read/Write head. As a precaution to erroneous writing the first data byte must be loaded into the Data Register in response to a Data Request from the FD1771 before the Write Gate signal can be activated.

Writing is inhibited when the Write Protect input is a logic low, in which case any Write command is immediately terminated, an interrupt is generated and the Write Protect status bit is set. The Write Fault input, when activated, signifies a writing fault condition detected in disk drive electronics such as failure to detect write current flow when the Write Gate is activated. On detection of this fault the FD1771 terminated the current command, and sets the Write Fault bit (bit 5) in the Status Word. The Write Fault input should be made inactive when the Write Gate output becomes inactive.

Whenever a Read or Write command is received the FD1771 samples the READY input. If this input is logic low the command is not executed and an interrupt is generated. The Seek or Step commands are performed regardless of the state of the READY input.

COMMAND DESCRIPTION

The FD1771 will accept and execute eleven commands. Command words should only be loaded in the Command Register when the Busy status bit is off (Status bit 0). The one exception is the Force Interrupt command. Whenever a command is being executed, the Busy status bit is set. When a command is completed, an interrupt is generated and the Busy status bit is reset. The Status Register indicates whether the completed command encountered an error or was fault free. For ease of discussion, commands are divided into four types. Commands and types are summarized in table 2.

COMMAND SUMMARY

TYPE	COMMAND	BITS							
		7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r1	r0
I	Seek	0	0	0	1	h	V	r1	r0
I	Step	0	0	1	u	h	V	r1	r0
I	Step In	0	1	0	u	h	V	r1	r0
I	Step Out	0	1	1	u	h	V	r1	r0
II	Read Command	1	0	0	m	b	E	0	0
II	Write Command	1	0	1	m	b	E	a1	a0
III	Read Address	1	1	0	0	0	1	0	0
III	Read Track	1	1	1	0	0	1	0	0
III	Write Track	1	1	1	1	0	1	0	0
IV	Force Interrupt	1	1	0	1	1	1	1	1

TABLE 2

FLAG SUMMARY

TYPE I	
h = Head Load Flag (Bit 3)	
h=1, Load head at beginning	
h=0, Do not load head at beginning	
V = Verify flag (Bit 2)	
V=1, Verify on last track	
V=0, No verify	
r1r0 = Stepping motor rate (Bits 1-0)	
Refer to Table 1 for rate summary	
u = Update flag (Bit 4)	
u=1, Update Track register	
u=0, No update	

TABLE 3

TYPE II

m = Multiple Record flag (Bit 4)

m = 0, Single Record

m = 1, Multiple Records

b = Block length flag (Bit 3)

b = 1, IBM format (128 to 1024 bytes)

b = 0, Non IBM format (16 to 4096 bytes)

a1a0 = Data Address Mark (Bits 1-0)

a1a0 = 00, FB (Data Mark)

a1a0 = 01, FA (User defined)

a1a0 = 10, F9 (User defined)

a1a0 = 11, F8 (Deleted Data Mark)

TABLE 4

TYPE III

s = Synchronize flag (Bit 0)

s=0, Synchronize to AM

s=1, Do Not Synchronize to AM

TYPE IV

l = Interrupt Condition flags (Bits 3-0)

l0=1, Not Ready to Ready Transition

l0=1, Ready to Not Ready Transition

l0=1, Index Pulse

l0=1, Immediate interrupt

E = Enable HLD and 10 msec Delay

E=1, Enable HLD, HLT and 10 msec Delay

E=0, Head is assumed Engaged and there is no 10 msec Delay

TABLE 5

TYPE 1 COMMANDS

The Type 1 Commands include the RESTORE, SEEK, STEP, STEP-IN, AND STEP-OUT commands. Each of the Type 1 Commands contain a rate field (r1r0), which determines the stepping motor rate as defined in Table 1, page four.

The type 1 Commands contain a head load flag (h) which determines if the head is to be loaded at the beginning of the command. If h=1, the head is loaded at the beginning of the command. HLD output is made active. If h=0, HLD is deactivated. Once the head is loaded, the head will remain engaged until the FD1771 receives a command that specifically disengages the head. If the FD1771 does not receive any commands after two revolutions of the disk, the head will be automatically disengaged (HLD made inactive). The Head Load Timing Input is sampled after a 10 ms delay, when reading or writing on the disk is to occur.

The Type 1 Commands also contain a verification (V) flag which determines if a verification operation is to take place on the destination track. If V=1, a verification is performed, if V=0, no verification is performed.

During verification, the head is loaded and after an internal 10 ms delay, the HLT input is sampled. When HLT is active (logic true), the first encountered ID field is read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, an interrupt is generated and the BUSY status bit is reset. If there is not a match but there is valid ID CRC, an interrupt is generated, the Seek Error status bit (Status bit 4) is set and the BUSY status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after two revolutions of the disk, the FD1771 terminates the operation and sends an interrupt. (INTRQ).

The STEP, STEP-IN, and STEP-OUT commands contain an UPDATE flag (U). When U = 1, the track register is updated by one for each step. When U = 0, the track register is not updated.

RESTORE (SEEK TRACK 0)

Upon receipt of this command the Track 00 ($\overline{\text{TR00}}$) input is samples. If $\overline{\text{TR00}}$ is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and an interrupt is generated. If $\overline{\text{TR00}}$ is not active low, stepping pulses (pins 15 to 17) at a rate specified by the r10r field are issued until the $\overline{\text{TR00}}$ input is activated. At this time the TR is loaded with zeroes and an interrupt is generated. If the

TROO input does not go active low after 255 stepping pulses, the FD1771 terminates operation, interrupts, and sets the Seek error status bit. Note that the **RESTORE** command is executed when **MR** goes from an active to an inactive state. A verification operation takes place if the **V** flag is set. The **h** bit allows the head to be loaded at the start of command.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read-Write head and the Data Register contains the desired track number. The FD1771 will update the Track register and issue stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the data register (the desired track location). A verification operation takes place if the V flag is on. The n bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP

Upon receipt of this command, the FD1771 issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r1r0 field, a verification takes place if the V flag is on. If the u flag is on, the TR is updated. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the command.

STEP-IN

Upon receipt of this command, the FD1771 issues one stepping pulse in the direction towards track 76. If the u flag is on, the Track Register is decremented by one. After a delay determined by the r₁ r₀ field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

STEP-OUT

Upon receipt of this command, the FD1771 issues one stepping pulse in the direction towards track 0. If the u flag is on, the TR is decremented by one. After a delay determined by the rtr0 field, a verification takes place if the V flag is on. The h bit allows the head to be loaded at the start of the command. An interrupt is generated at the completion of the command.

TYPE II COMMANDS

The Type II Commands include the Read Sector (s) and Write Sector (s) commands. Prior to loading the type II command into the COMMAND REGISTER, the computer must load the Sector Register with the desired sector number. Upon receipt of the type II command, the busy status Bit is set. If the E flag = 1 (this is the normal case) HLD is made active and HLT is sampled after a 10 msec delay. If the E flag is 0, the head is assumed to be engaged and there is no 10 msec delay. The ID field and Data Field format are shown below:

When an ID field is located on the disk, the FD1771 compares the Track Number of the ID field with the Track register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there was a match, the Sector Number of the ID field is compared with the Sector Register. If there is not a Sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and will be either written into, or read from depending upon the command. The FD1771 must find an ID field with a Track number, Sector number, and CRC within two revolutions of the disk; otherwise, the Record not found status bit is set (Status bit 3) and the command is terminated with an interrupt.

GAP	ID AM	TRACK NUMBER	ZEROS	SECTOR NUMBER	SECTOR LENGTH	CRC 1	CRC 2	GAP	DATA AM	DATA FIELD	CRC 1	CRC 2
ID FIELD									DATA FIELD			

IOAM = IO Address Mark - DATA={FE}₁₆ CLK = {C7}₁₆
Data AM = Data Address Mark - DATA={FB, F9, FA, or FB}₁₆ CLK = {C7}₁₆

Each of the Type II Commands contain a (b) flag which in conjunction with the sector length field contents of the ID determines the length (number of characters) of the Data field.

For IBM 3740 compatibility, the b flag should equal 1. The numbers of bytes in the data field (sector) is then 128×2^n where $n = 0, 1, 2, 3$.

For $b = 1$

Sector Length Field (hex)	Number of bytes in sector (decimal)
00	128
01	256
02	512
03	1024

When the b flag equals zero, the sector length field (n) multiplied by 16 determines the number of bytes in the sector or data field as shown below:

For $b = 0$

Sector Length Field (hex)	Number of bytes in sector (decimal)
01	16
02	32
03	48
04	64
*	*
*	*
*	*
FF	4080
00	4096

Each of the type II commands also contain a (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If $m = 0$ a single sector is read or written and an interrupt is generated at the completion of the command. If $m = 1$, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The FD1771 will continue to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the command register, which terminated the command and generates an interrupt.

FIG. 7
TYPE II COMMAND

- * 1. IF $\overline{1055} - 3$, THEN 15 NO 1000 $00-44$
2. IF $\overline{1055} = 1$ AND $05X = 10$ $11Z$ THEN 15 15 15 15
2. $15 = 0$ 0015 .

FIG. 8
TYPE II COMMAND

TYPE III COMMANDS

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the BUSY Status Bit is set. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the DR, and a DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	ZEROS	SECTOR ADDRESS	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the FD1771 checks for validity and the CRC error status bit is set if there is a CRC error. The Sector Address of the ID field is written into the sector register. At the end of the operation an interrupt is generated and the BUSY Status is reset.

READ TRACK

Upon receipt of the Read Track command, the head is loaded and the BUSY Status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse. As each byte is assembled it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. If bit 0 (S) of the command is a 0, the accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated.

WRITE TRACK

Upon receipt of the Write Track command, the head is loaded and the BUSY Status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the DR has not been loaded by the time the index pulse is encountered the operation is terminated making the device Not Busy, the Lost Data Status Bit is set, and the interrupt is activated. If a byte is not present in the DR When needed, a byte of zeros is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from FB to FE is about to be transferred from the DR to the DSR.

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN (HEX)	INTERPRETATION	CLOCK MARK (HEX)
F7	Write CRC Char.	FF
F8	Data Addr. Mark	C7
F9	Data Addr. Mark	C7
FA	Data Addr. Mark	C7
FB	Data Addr. Mark	C7
FC	Index Addr. Mark	D7
FD	Spare	
FE	IQ Addr. Mark	C7

The Write Track command will not execute if the DINT input is grounded; instead if the Write Protect Status bit is set and the interrupt is activated.

FIG. 11
TYPE III COMMAND
WRITE TRACK

FIG. 12
TYPE III COMMAND
WRITE TRACK

I₀ = Not-Ready-To-Ready Transition
I₁ = Ready-To-Not-Ready Transition
I₂ = Every Index Pulse
I₃ = Immediate Interrupt

NOTE: If $Igl3=0$, there is no interrupt generated but the current command is terminated and busy is reset.

STATUS DESCRIPTION

Upon receipt of any command, except the Force Interrupt command, the BUSY Status bit is set and the rest of the status bits are updated or cleared for the new command. If the Force Interrupt Command is received when there is a current command under execution, the BUSY status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the BUSY Status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

The format of the Status Register is shown below:

TYPE IV COMMAND

FORCE INTERRUPT

This command can be loaded into the command register at any time. If there is a current command under execution (Busy Status Bit set), the command will be terminated and an interrupt will be generated when the condition specified in the I₀ through I₃ field is detected. The interrupt conditions are shown below:

(BITS)							
7	6	5	4	3	2	1	0
S7	S6	S5	S4	S3	S2	S1	S0

Status varies according to the type of command executed as shown in Table 6.

STATUS REGISTER SUMMARY

BIT	ALL TYPE I COMMANDS	READ ADDRESS	READ	READ TRACK	WRITE	WRITE TRACK
S7	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY	NOT READY
S6	WRITE PROTECT	0	RECORD TYPE	0	WRITE PROTECT	WRITE PROTECT
S5	HEAD ENGAGED	0	RECORD TYPE	0	WRITE FAULT	WRITE FAULT
S4	SEEK ERROR	ID NOT FOUND	RECORD NOT FOUND	0	RECORD NOT FOUND	0
S3	CRC ERROR	CRC ERROR	CRC ERROR	0	CRC ERROR	0
S2	TRACK 0	LOST DATA	LOST DATA	LOST DATA	LOST DATA	LOST DATA
S1	INDEX	DRQ	DRQ	DRQ	DRQ	DRQ
S0	BUSY	BUSY	BUSY	BUSY	BUSY	BUSY

TABLE 6

STATUS FOR TYPE I COMMANDS

<u>BIT NAME</u>	<u>MEANING</u>
S7 Not Ready	This bit when set indicates the drive is not ready. When reset it indicates that the drive is ready. This bit is an inverted copy of the READY input and logically 'ored' with MR.
S6 PROTECTED	When set, indicates Write Protect is activated. This bit is an inverted copy of WRPT input.
S5 HEAD LOADED	When set, it indicates the head is loaded and engaged. This bit is a logical "and" of HLD and HLT signals.
S4 SEEK ERROR	When set, the desired track was not verified. This bit is reset to 0 when updated.
S3 CRC ERROR	When set, there was one or more CRC errors encountered on an unsuccessful track verification operation. This bit is reset to 0 when updated.
S2 Track 00	When set, indicates Read Write head is positioned to Track 0. This bit is an inverted copy of the TROO input.
S1 INDEX	When set, indicates index mark detected from drive. This bit is an inverted copy of the IP input.
S0 BUSY	When set command is in progress. When reset no command is in progress.

STATUS BITS FOR TYPE II AND III COMMANDS

<u>BIT NAME</u>	<u>MEANING</u>
S7 NOT READY	This bit when set indicates the drive is not ready. When reset, it indicates that the drive is ready. This bit is an inverted copy of the READY input and 'ored' with MR. The TYPE II and III Commands will not execute unless the drive is ready.
S6 RECORD TYPE/ WRITE PROTECT	On read Record: It indicates the MSB of record-type code from data field address mark. On Read Track: Not Used. On any Write Track: It indicates a Write Fault. This bit is reset when updated.
S5 RECORD TYPE/ WRITE FAULT	On Read Record: It indicates the LSB of record-type code from data field address mark. On Read Track: Not Used. On any Write Track: It indicates a Write Fault. This bit is reset when updated.
S4 RECORD NOT FOUND	When set, it indicates that the desired track and sector were not found. This bit is reset when updated.
S3 CRC ERROR	If S4 is set, an error is found in one or more ID fields; otherwise it indicates error in data field. This bit is reset when updated.
S2 LOST DATA	When set, it indicates the computer did not respond to DRQ in one byte time. This bit is reset to zero when updated.
S1 DATA REQUEST	This bit is a copy of the DRQ output. When set, it indicates the DR is full on a Read operation or the DR is empty on a Write operation. This bit is reset to zero when updated.
S0 BUSY	When set, command is under execution. When reset, no command is under execution.

FORMATTING THE DISK

(Refer to section on Type III commands for flow diagrams.)

Formatting the disk is a relatively simple task when operating programmed I/O or when operating under DMA control with a large amount of memory. When operating under DMA with limited amount of memory, formatting is a more difficult task. This is because gaps as well as data must be provided at the computer interface.

Formatting the disk is accomplished by positioning the RW HEAD OVER THE DESIRED TRACK NUMBER AND ISSUING THE Write Track command. Upon receipt of the Write Track command, the FD 1771 raises the data request signal. At this point in time, the user loads the data register with desired data to be written on the disk. For every byte of information to be written on the disk, a data request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk with a clock mark of (FF)₁₆. However, if the FD1771 detects a data pattern on F7 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation. For instance, an FE pattern will be interpreted as an ID address mark (DATA-FE, CLK-C7) and the CRC will be initialized. An F7 pattern will generate two CRC characters. As a consequence, the patterns F7 thru Fe must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by a F7 pattern.

Disks may be formatted in IBM 3740 formats with sector lengths of 128, 256, 512, or 1024 bytes, or may be formatted in non-IBM 3740 with sectors length of 16 to 4096 bytes in 16 byte increments. IBM 3740 at the present time only defines two formats. One format with 128 bytes/sector and the other with 256 bytes/sector. The next section deals with the IBM 3740 format with 128 bytes/sector and the following section details non-IBM formats.

IBM 3740 FORMATS - 128 BYTES/SECTOR

Shown in Figure 13, is the IBM format with 128 bytes/sector. In order to format this format, the user must issue the Write Track command, and load the data register with the following values. For every byte to be written, there is one data request.

<u>NUMBER OF BYTES</u>	<u>HEX VALUE OF BYTE WRITTEN</u>
40	00 or FF
6	00
1	FC (Index Mark)
26	00 or FF
6*	00
1	FE (ID Address Mark)
1	Track Number
1	00
1	Sector Number (1 thru 1A)
1	00
1	F7 (2 CRC's written)
11	00 or FF
6	00
1	FB (Data Address Mark)
128	Data (IBM uses E5)
1	F7 (2 CRC's written)
27	00 or FF
247**	00 or FF

* Write bracketed field 26 times

** Continue writing until FD1771 interrupts out. Approx. 247 bytes.

NON-IBM FORMATS

Non IBM Formats are very similar to the IBM formats except a different algorithm is used to ascertain the sector length from the sector length byte in the ID field. This permits a wide range of sector lengths from 16 to 4096 bytes. Refer to section V, Type II commands with b flag equal to zero. Note that F7 thru FE must not appear in the sector length byte of the ID field.

In formatting the FD1771, only two requirements regarding GAP sizes must be met. GAP 2 (i.e., the gap between the ID field and data field) must be 17 bytes of which the last 6 bytes must be zero and that every address mark be preceded by at least one byte of zeros. However, it is recommended that every GAP be at least 17 bytes long with 6 bytes of zeros. The FD1771 does not require the index address mark (i.e., DATA = FC, CLK = D7) and need not be present.

References:

- 1) IBM Diskette OEM Information GA21-9190-1
- 2) SA900 IBM Compatibility Reference Manual - Shugart Associates.

FIG. 13
TRACK FORMAT

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

V_{DD} With Respect to V_{BB} (Ground)	+ 20 to - 0.3V
Max Voltage to Any Input With Respect to V_{BB}	+ 20 to - 0.3V
Operating Temperature	0°C to 70°C
Storage Temperature	- 55°C to + 125°C

OPERATING CHARACTERISTICS (DC)

$T_A = 0^{\circ}\text{C}$ to 70°C , $V_{DD} = +12.0\text{V} \pm .6\text{V}$, $V_{BB} = -5.0 \pm .5\text{V}$, $V_{SS} = 0\text{V}$, $V_{CC} = +5\text{V} \pm .25\text{V}$
 $V_{DD} = 10\text{ ma}$ Nominal, $V_{CC} = 30\text{ ma}$ Nominal, $V_{BB} = 0.4\text{ ma}$ Nominal

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	μA	$V_{IN} = V_{DD}$ $V_{OUT} = V_{DD}$
I_{LO}	Output Leakage			10	μA	
V_{IH}	Input High Voltage	2.6			V	
V_{IL}	Input Low Voltage (All Inputs)			0.8	V	
V_{OH}	Output High Voltage	2.8			V	$I_O = -100\text{ }\mu\text{A}$ $I_O = 1.6\text{ mA}$
V_{OL}	Output Low Voltage			0.45	V	

NOTE: $V_{OL} \leq .4\text{V}$ when interfacing with low Power Schottky parts ($I_O < 1\text{ ma}$)

TIMING CHARACTERISTICS

$T_A = 0^\circ\text{C to } 70^\circ\text{C}$, $V_{DD} = +12\text{V} \pm 6\text{V}$, $V_{BB} = -5 \pm 25\text{V}$, $V_{SS} = 0\text{V}$, $V_{CC} = +5 \pm 25\text{V}$

NOTE: Timings are given for 2 MHz Clock. For those timings noted, values will double when chip is operated at 1 MHz.

Read Operations

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TET	Setup ADDR & CS to $\overline{\text{RE}}$	100			nsec	$C_L = 25 \text{ pf}$
THLD	Hold ADDR & CS from $\overline{\text{RE}}$	10			nsec	
TRE	$\overline{\text{RE}}$ Pulse Width	500			nsec	
TDRR	DRQ Reset from $\overline{\text{RE}}$			150	nsec	
TIRR	INTRQ Reset from $\overline{\text{RE}}$			3000	nsec	$C_L = 25 \text{ pf}$
TDACC	Data Access from $\overline{\text{RE}}$			450	nsec	
TDOH	Data Hold From $\overline{\text{RE}}$	50		150	nsec

1771B-1B

- NOTE: 1. CS MAY BE PERMANENTLY TIED LOW IF DESIRED.
 2. FOR READ TRACK COMMAND, THIS TIME MAY BE 12 TO 32 μSEC WHEN $\overline{\text{RE}} = 0$.

* TIME DOUBLES WHEN CLK=1MHz

Write Operations

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TSET	Setup ADDR & CS to $\overline{WE}$	100			nsec	See Note
THLD	Hold ADDR & CS from $\overline{WE}$	10			nsec	
TWE	$\overline{WE}$ Pulse Width	350			nsec	
TDRR	DRQ Reset from $\overline{WE}$			150	nsec	
TIRR	INTRQ Reset from $\overline{WE}$			3000	nsec	
TDS	Data Setup to $\overline{WE}$	250			nsec	
TDH	Data Hold from $\overline{WE}$	150			nsec

1771N-13

- NOTE: 1. $\overline{CS}$ MAY BE PERMANENTLY TIED LOW IF DESIRED.
 2. WHEN WRITING DATA INTO SECTOR, TRACK, OR DATA REGISTER, USER CANNOT READ THIS REGISTER UNTIL AT LEAST 600NS AFTER THE RISING EDGE OF $\overline{WE}$. WHEN WRITING INTO THE COMMAND REGISTER, STATUS IS NOT VALID UNTIL SOME 1200NS LATER. THESE TIMES ARE DOUBLED WHEN CLK=1MHz.

External Data Separation (XTDS = 0)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TPWX	Pulse Width Rd Data & Rd Clock	150		350	nsec	
TCX	Clock Cycle Ext	2500			nsec	
TDEX	Data to Clock	500			nsec	
TDDX	Data to Data Cycle	2500			nsec	

DEMO TIMING

XTDS=0 EXTERNAL DATA SEPARATION

1771M-18

- NOTE: 1. ABOVE TIMES ARE DOUBLED WHEN CLK=1MHz.
2. CONTACT VDC FOR EXTERNAL CLOCK/DATA SEPARATOR CIRCUITS.

Internal Data Separation (XTDS = 1)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TPWI	Pulse Width Data & Clock	150		1000	nsec	
TCI	Clock Cycle Interval	3500		5000	nsec	

READ TIMING
XTDS=1
INTERNAL DATA SEPARATION
PDCLOCK MUST BE FIELD HIGH

NOTE: INTERNAL DATA SEPARATION MAY WORK FOR SOME APPLICATIONS. HOWEVER, FOR APPLICATIONS REQUIRING HIGH DATA RECOVERY RELIABILITY, WDC RECOMMENDS EXTERNAL DATA SEPARATION BE USED.

Write Data Timing:

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TWGD	Write Gate to Data		1200		nsec	300 nsec $\pm$ CLK tolerance
TPWW	Pulse Width Write Data	500		600	nsec	
TCDW	Clock to Data		2000		nsec	$\pm 0.5\%$ CLK tolerance
TCW	Clock Cycle Write		4000		nsec	$\pm 0.5\%$ CLK tolerance
TWGH	Write Gate Hold to Data	0		100	nsec	

WRITE DATA TIMING

1771M-12

LAST DATA BIT
TO BE WRITTEN

Miscellaneous Timing:

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
TCD ₁	Clock Duty	175			nsec	2MHZ $\pm$ 1% See Note These times doubled when CLK = 1 MHz
TCD ₂	Clock Duty	210			nsec	
TSTP	Step Pulse Output	3800		4200	nsec	
TDIR	Dir Setup to Step	24			usec	
TMR	Master Reset Pulse Width	10			usec	
TIP	Index Pulse Width	10			usec	
TWF	Write Fault Pulse Width	10			usec	

MISCELLANEOUS TIMING

PIN OUTS

PIN NO.	PIN NAME	SYMBOL	FUNCTION
1	Power Supplies	VBB	-5V
20		VSS	Ground
21		VCC	+5V
40		VDD	+12V
19	MASTER RESET	MR	

- A logic low on this input resets the device and clears the command register. The Not Ready (Status Bit 7) is reset during $\overline{MR}$ ACTIVE. When $\overline{MR}$ is brought to a logic high a Restore Command is executed, regardless of the state of the Ready signal from the drive.

PIN NO	PIN NAME	SYMBOL	FUNCTION																				
Computer Interface:																							
7-14	DATA ACCESS LINES	DAL $\bar{0}$ DAL7	<ul style="list-style-type: none"> Eight bit inverted Bidirectional bus used for transfer of data, control, and status. This bus is a receiver enabled by $\bar{WE}$ or a transmitter enabled by $\bar{RE}$. 																				
3	CHIP SELECT	$\bar{CS}$	<ul style="list-style-type: none"> A logic low on this input selects the chip and enables computer communication with the device. 																				
5,6	REGISTER SELECT LINES	A0,A1	<ul style="list-style-type: none"> These inputs select the register to receive/transfer data on the DAL lines under $\bar{RE}$ and $\bar{WE}$ control: <table> <tr> <th>A1</th><th>A0</th><th>$\bar{RE}$</th><th>$\bar{WE}$</th></tr> <tr> <td>0</td><td>0</td><td>Status Reg</td><td>Command Reg</td></tr> <tr> <td>0</td><td>1</td><td>Track Reg</td><td>Track Reg</td></tr> <tr> <td>1</td><td>0</td><td>Sector Reg</td><td>Sector Reg</td></tr> <tr> <td>1</td><td>1</td><td>Data Reg</td><td>Data Reg</td></tr> </table>	A1	A0	$\bar{RE}$	$\bar{WE}$	0	0	Status Reg	Command Reg	0	1	Track Reg	Track Reg	1	0	Sector Reg	Sector Reg	1	1	Data Reg	Data Reg
A1	A0	$\bar{RE}$	$\bar{WE}$																				
0	0	Status Reg	Command Reg																				
0	1	Track Reg	Track Reg																				
1	0	Sector Reg	Sector Reg																				
1	1	Data Reg	Data Reg																				
4	READ ENABLE	$\bar{RE}$	<ul style="list-style-type: none"> A logic low on this input controls the placement of data from a selected register on the DAL when $\bar{CS}$ is low. 																				
2	WRITE ENABLE	$\bar{WE}$	<ul style="list-style-type: none"> A logic low on this input gates data on the DAL into the selected register when $\bar{CS}$ is low. 																				
38	DATA REQUEST	DRQ	<ul style="list-style-type: none"> This open drain output indicates that the DR contains assembled data in Read operations, or the DR is empty in Write operations. This signal is reset when serviced by the computer through reading or loading the DR in Read or Write operation, respectively. Use 10K pull-up resistor to +5. 																				
39	INTERRUPT REQUEST	INTRO	<ul style="list-style-type: none"> This open drain output is set at the completion or termination of any operation and is reset when a new command is loaded into the command register. Use 10K pull-up resistor to +5. 																				
24	CLOCK	CLK	<ul style="list-style-type: none"> This input requires a free-running 2 MHz $\pm$ 1% square wave clock for internal timing reference. 																				

Floppy Disk Interface:

25	EXTERNAL DATA SEPARATOR	XTDS	<ul style="list-style-type: none"> A logic low on this input selects external data separation. A logic high or open selects the internal data separator.
26	FLOPPY DISK CLOCK (External Separation)	FDCLOCK	<ul style="list-style-type: none"> This input receives the externally separated clock when $\overline{XTDS} = 0$. If $\overline{XTDS} = 1$, this input should be tied to a logic high.
27	FLOPPY DISK DATA	FDDATA	<ul style="list-style-type: none"> This input receives the raw read disk data if $\overline{XTDS} = 1$, or the externally separated data if $\overline{XTDS} = 0$.
31	WRITE DATA	WD	<ul style="list-style-type: none"> This output contains both clock and data bits of 500 ns duration. This output is capable of driving two TTL loads.
28	HEAD LOAD	HLD	<ul style="list-style-type: none"> The HLD output controls the loading of the Read-Write head against the media the HLT input is sampled every 10 nsec. When a logic high is sampled on the HLT input the head is assumed to be engaged.
23	HEAD LOAD TIMING	HLT	
15	Phase 1/Step	PH1/STEP	<ul style="list-style-type: none"> If the $\overline{3PM}$ input is a logic low the three phase motor control is selected and PH1, PH2, and PH3 outputs form a one active low signal out of three. PH1 is active low after MR. If the $\overline{3PM}$ input is a logic high the step and direction motor control is selected. The step output contains a 4usec high signal for each step and the direction output is active high when stepping; active low when stepping out.
16	Phase 2/Direction	PH2/DIRC	
17	Phase 3	PH3	
18	3 Phase Motor Select	$\overline{3PM}$	
29	Track Greater Than 43	TG43	<ul style="list-style-type: none"> This output informs the drive that the Read-Write head is positioned between track 44-76. This output is valid only during Read and Write Commands.
30	WRITE GATE	WG	<ul style="list-style-type: none"> This output is made valid when writing is to be performed on the diskette.
32	Ready	READY	<ul style="list-style-type: none"> This input indicates disk readiness and is sampled for a logic high before Read or Write commands are performed. If Ready is low the Read or Write operation is not performed and an interrupt is generated. A Seek operation is performed regardless of the state of Ready. The Ready input appears in inverted format as Status Register bit 7.

<u>PIN NO.</u>	<u>PIN NAME</u>	<u>SYMBOL</u>	<u>FUNCTION</u>
33	WRITE FAULT	WF	• This input detects writing faults indications from the drive. When WG = 1 and WF goes low the current Write command is terminated and the Write Fault status bit is set. The WF input should be made inactive (high) when WG becomes inactive.
34	TRACK 00	TR00	• This input informs the FD1771 that the Read-Write head is positioned over Track 00 when a logic low.
35	INDEX PULSE	IP	• Input, when low for a minimum of 10 usec, informs the FD1771 when an index mark is encountered on the diskette.
36	WRITE PROTECT	WPRT	• This input is sampled whenever a Write Command is received. A logic low terminated the command and sets the Write Protect Status bit.
37	DISK INTIALIZATION	DINT	• The input is sampled whenever a Write Track command is received. If DINT = 0, the operation is terminated and the Write Protect Status bit is set.
22	TEST	TEST	• This input is used for testing purposes only and should be tied to +5V or left open by the user.

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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