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SILICON SWITCH DEVELOPMENT FOR
OPTICAL PULSE GENERATION IN
FUSION LASERS AT
LAWRENCE LIVERMORE NATIONAL LABORATORY

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**Silicon Switch Development For Optical Pulse Generation In Fusion
Lasers At Lawrence Livermore National Laboratory**

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Abstract

We have been developing a silicon photoconductive switch for use as a Pockels cell driver in the pulse generation systems of the fusion lasers Nova and Novette. The objective has been to make 10 kV switches repeatedly and which are reliable on an operating system. We found that nonlinear phenomena in nearly intrinsic silicon caused excessive conduction at high voltage resulting in breakdown. Our experiments with doped material show that this problem can be eliminated, resulting in useful devices.

Device Requirements

In order to generate optical pulses of the required duration (1ns-10ns) for the Nova and Novette fusion lasers at LLNL,¹ a silicon switch will be used to drive a fast Pockels cell pulse gate. This device gates a pulse of the desired length out of a longer pulse from a Q-switched laser. To drive the Pockels cell with a square electrical pulse the switch discharges a charge line into a transmission line of the same impedance (50Ω). The configuration is similar to that used at the University of Rochester.² If the Pockels cell's quarter wave voltage is about 4 kV, the switch needs to hold off 8-10 kV (allowing for attenuation due to losses). To suppress optical prepulse, the dark resistance of the switch at full charge voltage must be greater than 20kΩ. The illumination to drive the switch is a 100μJ, 100 ps pulse of 1.05 μm light from a modelocked, Q-switched laser. To switch efficiently and minimize "post pulse" amplitude, the on resistance should be about 5Ω or less. To generate the required pulse widths a risetime of about 500 ps is sufficient. The actual switching time will be close to the illumination pulse width.

Physical Description

The silicon switch chip is shown in Fig. 1. The present design has a 2.5 mm interelectrode gap, but 2.0 mm gap devices have also been tested. To achieve maximum efficiency and reduce on resistance, this gap width should be as small as possible. Contacts are aluminum applied by vacuum evaporation and heated at 480°C for 30 minutes (sintered). Other types of contacts have been tried, including alloyed aluminum and gold.

A 1μm SiO₂ passivation layer is grown on the front and back surfaces, the contacts are applied and another SiO₂ layer deposited by chemical vapor deposition (CVD) process. The contacts cannot overlap the oxide layer or destruction of the contact edges occurs when high fields cause current to flow through the overlap region. The passivation prevents contamination of the high purity silicon by ions in the epoxy potting material which surrounds the switch. If only the front (electrode) side is passivated there is enough contamination that breakdown will occur on the backside.

Figure 1. Silicon switch chip.

Switches have been made from three different boules of silicon. One of the nearly intrinsic boules has 70 kΩ-cm resistivity, another has 30kΩ-cm resistivity or greater. A third, gold-doped boule is made from 10¹⁴-10¹⁵/cm³ phosphorus doped material with gold added until the resistivity reaches 3kΩ-cm.

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Figure 2 shows the switch package. The chip is bonded with silver epoxy to a 2.8 mm wide copper microstrip line on epoxy-fiberglass P.C. board. A 4 mm hole directly below the chip allows light to strike the electrode side. The chip is then cast in a special low-viscosity clear epoxy which is formulated for strong adhesion to silicon. The casting is vacuum degassed prior to hardening to remove any bubbles which might contribute to high voltage breakdown of the potting material. In the absence of this material the 2 mm interelectrode air gap would break down at about 6.5 Kv.

Figure 2. Switch package.

Figure 3. TDR trace of switch package with brass "switch" installed. Vertical scale: 10mp/div. Horizontal scale: .1ns/div.

A transition from microstrip to coaxial cable is provided by modified HN panel connectors. These connectors create the largest impedance mismatch in the system. Fig. 3 is a Time Domain Reflectometer (TDR) trace of a switch mount with the switch chip replaced by a brass plate of the same dimensions. Other types of high voltage connectors are being tested for a better match.

Importance of Low Dark Current

The 10 kV charge voltage and high dark resistance requirements for the switch pose difficult problems which are closely related. Silicon was chosen for its long carrier lifetime (hundreds of nanoseconds)³ so long pulses could be generated. Because of its lifetime and relatively small bandgap (1.12eV) silicon is prone to thermal runaway and is a poor insulator at D.C.. To avoid this, the charge line voltage is applied for about 1μs by a high voltage pulse generator which is triggered so that the peak charge voltage coincides with the arrival of the optical pulse. Even in this short interval, thermal runaway can occur if the initial conductivity and voltage are high enough. Thus the switch dark current at high voltage is an important parameter which can limit the maximum applied voltage.

Dark Current Measurements

The apparatus used to measure dark current is shown in Fig. 4. A switch chip is held and contacted by two contact fingers which form part of a microstrip transmission line connected to coaxial cables. A reed relay pulser generates a 0-1.5 kV, 600ns pulse which doubles in voltage at the switch and the resulting current is observed as the voltage across a 50Ω load.

For the devices made from nearly intrinsic material, the dark current was found to be time varying and nonlinear with voltage. Fig. 5 is a multiple exposure of several current waveforms at different voltages. When the current levels at the beginning of the pulse are plotted versus voltage, the relationship is found to be linear. For those switches in which the current attains a constant value over the pulse interval, the final current varies as the 1.7th power of voltage. The rise in current is not due to thermal runaway, since in that case the slope of the curve would increase with time whereas here it decreases. The mechanism of this current increase is presently being investigated.

Figure 4. Dark current measurement apparatus.

Figure 5. Dark current waveforms for "intrinsic" chips at 1.0, 1.5, 2.0, 2.5, 3.0 kV pulse voltage. 1V/div., 100ns/div.

At lower voltage the current waveform shows different features (Fig. 6), which are predicted by the theory of transient one-carrier charge injection in an insulator.⁴ At the beginning of the voltage pulse a wave of injected charge moves across the electrode gap. The peak in the curve corresponds to the arrival of this wave at the opposite electrode after which the current decreases as the space charge relaxes to a nonuniform distribution. Inserting values for gap width (L) and the time interval before the current peak (t_1) in the following expression:

$$\mu = \frac{0.786L^2}{t_1 V} \frac{\text{cm}^2}{\text{secV}}$$

one can compute the mobility (μ). The values computed from these curves agree well with published values of mobility for pure silicon in low electric field.³

Figure 6. Typical low voltage (<300V) current waveform.

Figure 7. Dark current waveforms for doped chips at 1.0, 1.5, 2.0, 2.5, 3.0 kV pulse voltage. 1V/div., 100ns/div.

The high voltage conductivity varies in magnitude from switch to switch. One wafer produced chips whose apparent resistance at 3 kV varied by more than a factor of four. One important material parameter which can strongly affect the high voltage conductivity and which can vary widely in a sample of high purity silicon is the impurity concentration. This may determine trap distribution or shift the Fermi level up or down. If impurities "freeze out" non-uniformly, large concentration gradients may exist across a single wafer.

Breakdown

When these switches are potted and higher voltages applied, those devices which exhibit the highest conductivity will "break down" at the lowest voltage. Before breakdown, dark current increases rapidly over the charging interval and is unstable in amplitude. Once breakdown has occurred, a high conductivity channel is etched between the electrodes. This breakdown may be thermal runaway developing rapidly due to initially large power dissipation in the chip. Similar breakdown can be caused in a high resistivity chip if it is illuminated enough to reduce the resistance to a few kilohms.

Doped Switches

Fig. 7 is a series of current waveforms similar to Fig. 5 but for a device made of gold-doped material (with a 2 mm electrode gap as before). The I-V relationship is linear, and the resistance is higher and more uniform for all gold-doped chips than for similar intrinsic devices. The large uniform dopant concentration may be more significant than other randomly distributed impurities. When mounted and potted, these switches easily hold off 10 kV, 1 μ s pulse bias. With 100 μ J 100ps illumination, the on resistance is about 5 Ω . The electrical risetime is measured using a Tektronix 7104 oscilloscope with a 7S12 TDR/sampler plug-in and a 7M11 delay line. Unfolding the measurement apparatus risetime, the switch risetime is around 170 ps.

Conclusion

Photoconductive switches made from nearly intrinsic material exhibit nonlinear dark current characteristics and nonuniformity which limit their usefulness. Charge injection is occurring in the devices but not all features of the current-voltage characteristic are explained at present. These problems can be solved by doping the silicon material. We are presently investigating these phenomena in more detail. It is hoped that further experiments will yield optimum doping concentrations for silicon.

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