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ABSTRACT

The preparation of CuInSe_2 thin films by simultaneous elemental evaporation is reported to be more reproducible with the application of Electron Impact Emission Spectroscopy (EIES) for deposition rate control.

Rapid diffusion processes occurring at the high substrate temperatures are described as precluding the use of thick selenide layers highly deficient in In as part of the cell structure.

Growth of cell degrading copper nodules in low resistivity, P-type CuInSe_2 films exposed to CdS is discussed.

A point defect model for the vacuum deposited CuInSe_2 films based upon In and Se vacancies is suggested and reported to be consistent with the film properties.

Fabrication of thin-film CdS/ CuInSe_2 cells is discussed and demonstrate the repeatable achievement of 2-5% efficient cells. These cells are described as possessing high photocurrents ($25\text{-}34\text{mA/cm}^2$) and low open circuit voltages (150-310mV) when tested under simulated AM-1 conditions.

Detailed analysis of cells as a function of temperature and lighting conditions is described. The cell measurements are reported to be in good agreement with a cell model and indicate that the low voltage is caused by a high resistivity selenide layer at the junction.

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The preparation of CuInSe₂ thin films using EIES (Electron Impact Emission Spectroscopy) to control the simultaneous elemental evaporation process has continued to demonstrate favorable results as more experience is acquired with the system. Process reproducibility in terms of film resistivity and composition (as determined by EDAX measurements) have been considerably improved in comparison to the earlier approaches.

Use of an initial, thick CuInSe₂ layer deficient in In as a means for minimizing the amount of In contained in the CdS/CuInSe₂ cell has been found to be neither feasible nor practical. At the high substrate deposition temperatures, diffusion from this layer into the final selenide layer was sufficient to make the final layer unacceptable.

One of the major limitations of the deposited selenide films with respect to cell performance has been determined to be the formation of copper nodules. These nodules of several microns in size form only in low resistivity, P-type CuInSe₂ films exposed to CdS. High resistivity, P-type films, N-type films, and selenide films by themselves have not exhibited the nodular growth. All cells containing nodules have shown low efficiencies and have degraded with heat treatment.

Development of a model for the point defect chemistry of the vacuum deposited CuInSe₂ thin films has been initiated. The model attributes the film electrical properties to the existence of In vacancy acceptors, Se vacancy donors, and Cd donors on Cu lattice sites. The model was found consistent with experimental film results and appears to explain the dependence of film properties on the deposition parameters.

Cell fabrication technology has progressed to a point where cells of 2-5% efficiency can be repeatably achieved. Under simulated AM-1 conditions, these cells have possessed high short circuit currents (25-34mA/cm²) and low open circuit voltages (150-310mV). A detailed analysis of cell performance as a function of temperature and lighting conditions has been made and compared to a photovoltaic cell model. The model has been found in agreement with all of the experimental measurements and indicates that the low open circuit voltage characteristic was due to high resistivity selenide at the junction.

Finally, until a probe caused defect occurred, the photovoltaic response of a high efficiency (5.7%) thin-film CdS/CuInSe₂ cell has been found to remain unchanged after ten months of laboratory storage.

This is the second quarterly report of work on "Cadmium Sulfide/Copper Ternary Heterojunction Cell Research", SERI Contract XJ-9-8021-1. The copper ternary is the semiconductor compound copper indium diselenide (CuInSe_2) and was the subject of two prior research programs (1,2). For the current program, the objective is to continue the development of a large area, low cost, stable, polycrystalline thin-film photovoltaic solar cell based upon the CdS/CuInSe_2 material system. The program is directed towards achieving, at the earliest possible time, a 10% efficient thin-film cell on low cost substrates by low cost fabrication methods. Accordingly, the technical approach is to improve the performance and fabrication economics of earlier developed cells produced by vacuum evaporation techniques (simultaneous elemental evaporation for CuInSe_2) onto inexpensive substrates. The specific research tasks include: 1) Investigating cell designs and film preparation procedures which would minimize the amount of the rather rare and expensive In contained in the cell structure; 2) Developing a low cost cell metallization system; 3) Investigating the use and effect of graded selenide films on the cell characteristics; 4) Conducting a detailed analysis of the CdS/CuInSe_2 cell properties; and 5) Continuing development of a cell conceptual model.

The first reported experimental example of a CdS/CuInSe_2 heterojunction solar cell was fabricated using a single crystal of CuInSe_2 and a vacuum deposited CdS film (3-5). This single crystal device exhibited a uniform photovoltaic quantum efficiency of 70% between wavelengths of 0.55 to 1.25 microns. For an incident solar intensity of 92mW/cm^2 , the device produced a photocurrent of 38mA/cm^2 , on open circuit voltage of 0.55V, and a conversion efficiency of 12%. Other than the Si, GaAs, and InP/ CdS semiconductor systems, this is the only case of a photovoltaic device with a demonstrated efficiency greater than 10%.

Following the development of a single crystal cell, polycrystalline thin-film cells were prepared using vacuum evaporation techniques for both the CdS and CuInSe_2 layers (6-8). The CuInSe_2 films used in the cells were formed by codeposition of the CuInSe_2 and Se in order to form controlled resistivity, P-type layers. These cells have shown photocurrents of 28mA/cm^2 , open circuit voltages of 0.49V, and efficiencies of 6.6% when tested with a light intensity of 100mW/cm^2 . The cells have been approximately 1 cm^2 in area and have not been coated with any anti-reflection layers.

As established in a previous study, the elemental evaporation process for the selenide film formation is believed to possess a number of favorable features, including semiconductor film quality and suitability for scale up to high volume production (2). It is the approach Boeing has taken to further the development of this attractive thin-film solar cell. By utilizing these films to fabricate solar cell devices, a cell efficiency of 5.7% has been achieved. Cell performance of this magnitude is viewed as being very encouraging and is also felt to provide an indication regarding the future potential of the planned technical approach.

3.0 TECHNICAL DISCUSSION

3.1 Preparation and Properties of CuInSe_2 Films

Thin films of CuInSe_2 have continued to be prepared by the simultaneous elemental evaporation process with EIES rate control for In and Cu described in the First Quarterly Report. No major revisions or modifications to the deposition fixturing have been found necessary. However, one change has been made with respect to the EIES controller in utilizing the emission lines at 3247Å and 3274Å for copper instead of the 2182Å line. A fall off in sensitivity of the 2182Å line signal which may have been due to a degradation in the photomultiplier tube for this UV wavelength was noted during the course of deposition runs. Since the copper signal at this wavelength was already low, it was decided to monitor the much higher intensity, longer wavelength lines and make corrections for the overlapping In emission at 3265Å. This approach has been shown to be more reproducible and predictable than the earlier technique. It is believed that we are now at the limits of the control capability of the instrumentation for the present system configuration. While it would be desirable to have tighter control for such a composition sensitive material as CuInSe_2 , we feel the system should be adequate to proceed with the cell development studies.

An indication as to the present degree of process control achievable with the EIES deposition system is given by the results of EDAX measurements on a series of CuInSe_2 film samples. The EDAX data on 11 thin-film deposits and the stoichiometric bulk standard provided by Prof. Loferski of Brown University is summarized in Table 3.1-1. The data suggests that the analysis method itself is reasonably accurate by comparing different points on the same sample and it also demonstrates only small variations from sample to sample. The latter observation is particularly apparent in the sample series including Nos. 176, 177, 179, and 180 where the deposition parameters had been maintained essentially constant.

One final point with respect to the EDAX results is that they implied a trend relating In content and resistivity. For example, the lowest resistivity samples analyzed (Nos. 159 and 174) were also the lowest in percentage of In. Since the resistivities for the samples listed in Table 3.1-1 varied over such a large range ($<1\text{K}\Omega/\square$ to approximately $10^8\Omega/\square$) with only minor variations in composition by EDAX, developing an exact composition-resistivity relationship does not appear to be justified at the present time.

The selenide films of 2.5 to 3.5 μm in thickness have been deposited onto heated polycrystalline alumina substrates at a deposition rate of approximately 0.1 $\mu\text{m}/\text{min}$. A sliding mask structure has been used to define on the substrate film regions of varying composition for post deposition analysis. The substrate spatial configuration is shown in Figure 3.1-0. Depositing a test strip of film layers onto the unmetallized substrate has been found extremely valuable not only in characterizing the individual layer but also the sandwiched layers.

During the just completed quarter, all of the selenide films have been deposited at substrate temperatures of 450°C or 500°C. SEM photographs of films deposited at these two temperatures are presented in Figure 3.1-1 and 3.1-2. The higher temperature does produce a larger grain size deposit ($\approx 1\mu\text{m}$) but the increase is seen to be quite small. Much larger grain size films have been achieved with a two-layer deposition technique where the first layer is In deficient in composition and this is followed by deposition of the stoichiometric material. An example of the film structure resulting from the two-layer process is shown in the SEM photomicrographs presented in Figure 3.1-3 and 3.1-4. Grain sizes in excess of 10 μm are indicated in the figures.

The use of an initial In-deficient layer has been explored because of several factors other than developing large crystallite size deposits. For example, such films are very low resistivity, P-type material which is favorable for achieving an ohmic back contact and developing a back surface field for enhanced collection efficiency. Moreover, if a composite of a thick In-deficient layer and a relatively thin stoichiometric film could be formed as the P-type semiconductor, the total amount of In contained in the cell would be minimized. In view of these possible advantages, a considerable amount of research effort was expended in attempting to develop the composite concept.

The general conclusion of the studies has been that it is not a practical approach due to process control and excessive diffusion difficulties. With the high selenide deposition temperatures, the low resistivity In-deficient layer was found to operate as a diffusion source for P-type defects into the stoichiometric film and rapidly converted the final layer into low resistivity material. Only by overcompensating the diffusion process with the final layer, e.g., making the final layer very thick, making the initial layer thin, using an initial layer with very slight In-deficiency, or using excess In in the final layer, could the composite be produced with desired resistivity and P-type.

In the course of the In-deficient layer studies, another selenide film process highly significant to the device operation became apparent. This was the formation of growth nodules in the selenide layer. All cells containing nodules were found to have low efficiency and, in contrast to the high efficiency cells where post deposition heat treatments improve the photoresponse, these devices rapidly degraded under any baking conditions.

Figures 3.1-5 and 3.1-6 are SEM photomicrographs of a selenide film containing a large number of the nodules. Analysis of the nodules with an electron beam microprobe has shown them to be pure copper. It has been observed that the conditions necessary for nodule formation are: 1) the selenide film must be of low resistivity (less than approximately $50\text{K}\Omega/\square$) and P-type and 2) the selenide film must be exposed to CdS. Nodules have not been detected in high resistivity P-type CuInSe_2 , N-type CuInSe_2 , nor in any selenide deposit by itself, i.e., where CdS was not deposited. The CdS surface grown on a selenide film with nodules exhibits the unusual growth features shown in Figures 3.1-7, 8, and 9. Free copper in contact with the CdS and the large voids which have developed would explain why cells formed with such deposits would be of poor quality and further degrade with heat treatment. A large increase in the CdS sheet resistivity has been measured on all cells which contain the nodules and again implies the interdiffusion of copper.

Mechanisms for the growth of these nodules have yet to be defined. While copper nodules have also been observed in Cu_2S films, they appear to possess a different structure, they can be formed in the Cu_2S film by itself, and they can be formed electrochemically. Additional studies of the nodules developed in our CuInSe_2 thin films are anticipated because of their high importance to device performance and the type of device that can be constructed. For instance, in order to avoid nodule formation, the tendency has been to deposit selenide film layers such that the surface is high resistivity. With these structures, very high photocurrents have been achieved but also quite low voltages. Attempts to increase the voltage by depositing low resistivity films have, however, met with little success due to the nodule formation.

TABLE 3.1-1 SUMMARY OF CuInSe₂ COMPOSITION BY EDAX

Sample		Analysis Position			Average (wt. %)
		1	2	3	
Theoretical	Std.				
	Cu				18.90
	In				34.14
	Se				46.96
Brown Univ.	Std.				
	Cu	18.54	18.23	18.70	18.49
	In	34.87	34.46	35.31	34.88
	Se	46.59	47.31	45.99	46.63
Film #154					
	Cu	17.58	17.20	17.61	17.46
	In	36.67	36.81	36.45	36.64
	Se	45.75	45.99	45.93	45.89
Film #155					
	Cu	16.87	17.17	17.27	17.10
	In	36.34	36.19	36.86	36.46
	Se	46.79	46.74	45.87	46.46
Film #156					
	Cu	17.11	16.51	16.87	16.83
	In	36.25	36.53	36.48	36.42
	Se	46.64	46.96	46.65	46.75
Film #159					
	Cu	18.21	17.89	17.71	17.94
	In	34.57	35.67	33.59	34.61
	Se	47.22	46.44	48.70	47.45
Film #174					
	Cu	18.57	18.71	18.55	18.61
	In	34.30	34.83	35.20	34.78
	Se	47.13	46.46	46.25	46.61
Film #176					
	Cu	17.60	18.08	17.89	17.86
	In	35.44	36.07	35.44	35.65
	Se	46.96	45.85	46.67	46.49
Film #177					
	Cu	17.38	17.61	17.51	17.50
	In	36.04	35.69	35.91	35.88
	Se	46.58	46.70	46.58	46.62
Film #179					
	Cu	17.38	17.67	17.57	17.54
	In	36.23	35.94	35.14	35.77
	Se	46.39	46.39	47.29	46.69
Film #180					
	Cu	17.40	17.84	17.83	17.69
	In	36.41	35.68	35.45	35.85
	Se	46.19	46.48	46.72	46.46
Film #190					
	Cu	17.48	17.72	17.74	17.65
	In	36.27	36.62	35.95	36.28
	Se	46.25	45.66	46.31	46.07
Film #192					
	Cu	17.48	17.72	17.74	17.65
	In	36.27	36.62	35.95	36.28
	Se	46.25	45.66	46.31	46.07

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FIGURE 3.1-0 SAMPLE CONFIGURATION ON 2"x2"x0.025" ALUMINA SUBSTRATE

FIGURE 3.1-1 CUINSE₂ FILM DEPOSITED AT 450°C. 5000X, 60°

FIGURE 3.1-2 CUINSE₂ FILM DEPOSITED AT 500°C. 5000X, 40°

FIGURE 3.1-3 TWO-LAYER CUINSE₂ FILM DEPOSITED AT 500°C. 2000X, 40°

FIGURE 3.1-4 TWO-LAYER CUINSE₂ FILM DEPOSITED AT 500°C. 5000X, 40°

FIGURE 3.1-5 LOW RESISTIVITY CuInSe_2 FILM WITH COPPER NODULES. 2000X, 40°

FIGURE 3.1-6 LOW RESISTIVITY CuInSe_2 FILM WITH COPPER NODULES. 5000X, 40°

FIGURE 3.1-7 CDS FILM SURFACE OVER SELENIDE DEPOSIT WITH COPPER NODULES, 1000X, 45°

FIGURE 3.1-8 CDS FILM SURFACE OVER SELENIDE DEPOSIT WITH COPPER NODULES. 2000X, 40°

FIGURE 3.1-9 CDS FILM GROWTH STRUCTURES OVER COPPER NODULE. 7000X, 40°

Another interesting aspect associated with selenide films exhibiting the copper nodules has been a large increase in resistivity. An explanation of this result and other properties of the vacuum deposited selenide films based upon point defect chemistry is being developed. Although the specific defect model has not been finalized, it is suggested that the selenide films contain In and Se vacancies. The In vacancies act as acceptors while a Se vacancy would be a donor. Depending upon the relative concentration of these two defects, either P-type or N-type films can be deposited as has been observed. Increasing the Cu deposition rate (reducing the In:Cu ratio) would result in increasing P-type behavior which again is what has been observed experimentally. It has, however, been suggested in the literature on single crystal CuInSe_2 that the acceptor responsible for P-type behavior is Cu vacancies (9). This model is in opposition to our deposited polycrystalline film results where the conductivity of P-type films increased with Cu deposition rate. It is further believed that Se vacancies are a consequence of high substrate temperatures and should increase with increasing temperature. We have noted that higher Cu rates are necessary with increasing substrate temperature. Higher Cu rates would generate more In vacancies which could compensate the higher Se vacancy concentration.

Another facet of the defect centers model concerns the effect of Cd from the CdS on the selenide film properties. If Cd occupies the Cu sites in the CuInSe_2 lattice, it would act as a donor whereas it would be an acceptor on the In sites. It has been reported that Cd acts primarily as a donor in single crystal CuInSe_2 (9). This behavior of Cd has also been seen in our deposited thin film of CuInSe_2 , i.e., a large increase in resistivity for P-type films and a resistivity decrease for N-type deposits in substrate areas where the selenide has been exposed to CdS. The effect of CdS on the selenide resistivity has been most evident as a result of probing the film areas defined as shown in Figure 3.1-0. In the case of the low resistivity, highly P-type deposits, a strong (several orders of magnitude) resistivity gradient with the resistivity increasing in the direction away from the substrate edge and towards the edge of the CdS layer has always been detected. Where the film deposition conditions have produced N-type films in either the overlap region and/or the high resistivity film area, the gradient direction has been reversed. The magnitude of the gradient in the N-type films has, however, been considerably smaller--usually less than one order of magnitude. These gradients are seen to be consistent with the incorporation of Cd donors in the selenide film material. It is of further interest to note that the number of Cu nodules formed in the low resistivity, P-type material also increase as the edge of the CdS film is approached. While the resistivity and nodule density variations follow the expected amount of CdS 'spray' under the deposition mask, the mechanisms involved are less clear and will require, especially with reference to nodule growth, additional analysis. There has been some indication that at lower substrate temperature, which according to our model would favor lower Se vacancies and, thus, lower In vacancies and a lower Cu:In ratio, the density of nodules has also been lowered. If this preliminary result can be confirmed and if acceptable quality films can be produced at lower temperatures, then a solution may be construed for the nodule growth problem.

3.2 CdS/ CuInSe_2 Cell Development

During this quarter, cells were produced according to the redesigned structure described in the First Quarterly Report. A low resistivity In-deficient CuInSe_2 layer of various thickness was first deposited on heated (450-500°C) Mo-metallized alumina substrates. After completing this deposit, the In content in the vapor stream was stepwise increased to a value which would form CuInSe_2 of the proper resistivity to make a good heterojunction with CdS.

The stepwise changing of the In content in the CuInSe₂ has the following advantages: 1) Minimize the cell In content, 2) Introduce a built-in field to enhance carrier collection, and 3) Prevent formation of Cu nodules in the junction are as discussed in the last section.

The in-situ deposited CdS had either one thin (<1μm) undoped layer plus a thick layer (>2μm) of In-doped low resistivity material or just one layer of In-doped material. Substrate temperature for the CdS depositions has been in the 150-175°C range and the deposition rate about 0.6μm/min.

When the deposition conditions were such that Cu nodules were not formed on the selenide surface, the cells had similar characteristics of high short circuit current (25-34mA/cm²) and low open circuit voltages (150-310mV). Efficiencies of these cells ranged from 2 to 5 percent.

The J-V characteristics of one of the best cells under simulated AM-1 (100mW/cm²) illumination is shown in Figure 3.2-1. The cell had a short circuit current of 33mA/cm², open circuit voltage of 0.305V, fill factor of 0.52, and efficiency of 5.25%.

The selenide near the junction of this type cells was always high resistivity. The detailed analysis of the cell characteristics presented in the next section reveals that the open circuit voltage is limited by this low doping, high resistivity selenide layer.

3.3 Cell Analysis and Modeling

In this section, the performance of our CdS/CuInSe₂ solar cell is analyzed in detail. The main objective of the analysis is to determine why our cells give such high short circuit current (>30mA/cm²) and low open circuit voltage (<0.35V) and, subsequently, to suggest ways to improve the cell performance.

Under simulated AM-1 solar illumination, the experimental device being investigated had:

Area - 1cm²
V_{oc} - 0.305V
J_{sc} - 33mA/cm²
η - 5.25%
F.F. - 0.52

The dark I-V characteristic is shown in Figure 3.3-1. The diode factor, A, and the reverse saturated current, J₀, were found to be 1.15 and 3 x 10⁻⁶A/cm², respectively. These values agreed with the measurements of the V_{oc}-J_{sc} characteristics as a function of light intensity and were independent of a bias light of different wavelengths from 450nm to 650nm. The J₀ as a function of temperature were determined by measuring the V_{oc}-J_{sc} characteristic at various temperatures. The results are shown in Figure 3.3-2 which gives the temperature dependence of J₀ as:

$$J_0 = J_{00} \exp - \frac{\Delta E}{AkT}$$

where ΔE = 0.77eV and J₀₀ = 1.93 x 10⁵A/cm².

FIGURE 3.2-1 J-V CHARACTERISTICS UNDER SIMULATED AM1 ILLUMINATION

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FIGURE 3.3-2 J_0 AS A FUNCTION OF INVERSE TEMPERATURE

The variation of open circuit voltage with temperature and AM-1 illumination was also measured as shown in Figure 3.3-3. The V_{oc} varies linearly with temperature for high temperature ($T > 260^\circ K$). The decrease of slope below $260^\circ K$ may be due to the Mo/CuInSe₂ or Al/CdS contacts becoming non-ohmic and high resistivity at low temperatures. The intercept of the linear portion at $T = 0$ gives:

$$V_{oc}(T=0) = 0.73V$$

The dark capacitance of the cell has been measured as a function of reverse bias. The $1/C^2$ vs. reverse bias is shown in Figure 3.3-4. The capacitance at zero bias is 7.6 nf/cm^2 . Since our CdS doped with In is of low resistivity, the $1.16 \mu\text{m}$ depleted region ($V = 0$) should all be in the CuInSe₂ side of the junction.

Finally, the cell efficiency and fill factor were measured for different light intensities (ELH lamp) at room temperature. Results as a function of J_{sc}/J_0 are shown in Figure 3.3-5. Both fill factor and efficiency increase as the light intensity decreases. At the lowest input light intensity (4.46 mW/cm^2), an efficiency and fill factor as high as 8.6% and 0.6, respectively, were observed. The decrease of efficiency and fill factor with light intensity may be due to the combination of high J_0 and series/shunt resistance as explained by Mitchell (10).

The cell performance, high J_{sc} and low V_{oc} , can be explained by the model developed by Rothwarf (11) in connection with our measured results. In his model, the characteristics of the cell can be represented by:

$$J_{sc} = J_0 \left(\exp \frac{-qV_{oc}}{AkT} - 1 \right)$$

where J_{sc} is the short circuit current or the light generated current and A is the diode factor. If the cell transport property is dominated by interface recombination, J_0 should be:

$$J_0 = qN_c S_I \exp \frac{-\Delta E}{AkT}$$

where N_c is the density of states for the CdS conduction band, S_I is the effective interface recombination velocity and

$$\Delta E = E_{g1} - \Delta\chi - \delta_1$$

where E_{g1} is the CuInSe₂ band gap energy, $\Delta\chi$ the difference in electron affinity between CdS and CuInSe₂, and δ_1 the position of the Fermi level in CuInSe₂ relative to the valence band. For this model, the diode factor A is one and the open circuit voltage is then given by:

$$V_{oc} = E_{g1} - \Delta\chi - \delta_1 + \frac{AkT}{q} \ln \frac{J_{sc}}{qN_c S_I}$$

According to the dark I-V (Figure 3.3-1) and $J_{sc} - V_{oc}$ measurements, the diode factor of our experimental cell is 1.15 which indicates the transport mechanism may be dominated by the interface recombination as the model predicts.

The slope of the J_0 vs. $(kT)^{-1}$ curve (Figure 3.3-2) gives:

$$\Delta E = E_{g1} - \Delta\chi - \delta_1 = 0.77 \text{ eV}$$

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FIGURE 3.3-3 OPEN CIRCUIT VOLTAGE AS A FUNCTION OF TEMPERATURE

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FIGURE 3.3-4 DEPENDENCE OF DARK CAPACITANCE PER UNIT AREA UPON REVERSE BIAS

FIGURE 3.3-5

EFFICIENCY AND FILL FACTOR AS A FUNCTION OF ILLUMINATION

and agrees very well with the V_{oc} vs. kT measurement (0.73eV). Since $E_{g1} = 1.04\text{eV}$ and $\Delta\chi = 0.08\text{eV}$ (12), it follows that:

$$\delta_1 = 0.19 - 0.23\text{eV}$$

The measured $J_{00} = 1.93 \times 10^5 \text{A/cm}^2$ yields the product of $N_C S_I$, i.e.,

$$N_C S_I = 1.21 \times 10^{24} \text{cm}^{-2}\text{sec}^{-1}$$

For an estimated, typical value of $N_C = 2 \times 10^{18} \text{cm}^{-3}$,

$$S_I = 6.05 \times 10^5 \text{cm/sec}$$

This is consistent with the calculated value of $6.9 \times 10^4 - 6.9 \times 10^5 \text{cm/sec}$ (2) for S_I based upon the lattice mismatch between CdS and CuInSe₂ at the interface.

The hole concentration of the CuInSe₂ layer close to the junction may be calculated from the δ_1 value. With an estimated value of $4.18 \times 10^{18} \text{cm}^{-3}$ for N_v (the CuInSe₂ valence band effective density of states) the hole concentration of the CuInSe₂ layer close to the junction should be:

$$p = 2.36 \times 10^{15} - 4.88 \times 10^{14} \text{cm}^{-3}$$

Since the In-doped CdS is very low resistivity, the depletion region width calculated from the above hole concentration and the measured V_D (0.73---0.77V) is:

$$W = 6.0 \times 10^{-5} - 1.29 \times 10^{-4} \text{cm}$$

which agrees with the value obtained from the capacitance measurement at zero bias or $1.16 \times 10^{-4} \text{cm}$.

From the above analysis, the model is seen to be consistent with all cell measurements. The low open circuit voltage is mainly due to the high δ_1 value, i.e., too high resistivity of the CuInSe₂ layer. The high short circuit current of the cell, 33mA/cm^2 , which approaches the single crystal cell can be explained by the $1.16\mu\text{m}$ wholly depleted CuInSe₂ region. Since the CuInSe₂ absorption coefficient for photon energies greater than E_g is over 10^4cm^{-1} , nearly all of the absorption of the solar spectrum will be in the $1.16\mu\text{m}$ depleted region. The electric field in this depleted region can be estimated to be:

$$\Sigma = \frac{2V_D}{W} = 1.33 \times 10^4 \text{V/cm}$$

The light generated electron-hole pairs will be separated by such high fields and collected. The maximum transit time of the holes (assuming $\mu = 10\text{cm}^2/\text{V-sec}$) under this high field is:

$$t = 8.9 \times 10^{-10} \text{sec}$$

Hence, all the light generated carriers are collected before they can recombine in the grain boundaries.

In conclusion, in order to improve the open circuit voltage, the δ_1 (or the resistivity of the CuInSe₂) should be reduced. Short circuit current may be reduced from the present high values but the overall cell efficiency could be improved.

3.4 Stability of CdS/CuInSe₂ Cell

The periodic I-V measurements described in the First Quarterly Report on Boeing's highest efficiency (5.7%) thin-film CdS/CuInSe₂ cell to detect possible degradation under laboratory environment conditions have been discontinued. Unfortunately, the repeated probing of the grid contact resulted in a 'chipping-out' of a small section of the main grid bus bar and some of the cell layers beneath the bar. Two collector grid lines are no longer connected to the bus bar which has produced the expected decrease in fill factor and efficiency. Up until the time this probe caused degradation had occurred, no change in the performance of the cell had been detected in the ten months subsequent to the cell fabrication. Considering that the cell was unpassivated and no attempt had been made for storage in an inert atmosphere, we remain quite encouraged as to the prospects for long term stability for the CdS/CuInSe₂ thin-film cell.

4.0 PLAN FOR NEXT QUARTER

During the next quarter (September 1, 1979 - November 30, 1979), the program plan includes the following:

- 1) Preparation and characterization of lower resistivity CuInSe_2 thin films with emphasis on understanding and avoiding the Cu nodule growth process.
- 2) Continuing the development of the point defect model for vacuum deposited CuInSe_2 thin films.
- 3) Fabrication and analysis of CdS/CuInSe_2 heterojunction test structures incorporating improved cell design concepts.
- 4) Application of experimental cell data to the development of the cell conceptual model.

5.0

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