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**AUTOMATED ARRAY ASSEMBLY TASK. DEVELOPMENT OF LOW-COST
POLYSILICON SOLAR CELLS**

Quarterly Technical Report No. 1

By
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Gregory T. Jones

June 1979

Work Performed Under Contract No. NAS-7-100-955265

Sensor Technology, Incorporated
Chatsworth, California

MASTER

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PREFACE

The information presented in this report on the Production Process and Equipment Development Area (formerly Automated Array Assembly Task) represents work performed from January 1979 through June 1979, by Sensor Technology, Inc., in Chatsworth, California. This program is directed by Sang S. Rhee. Principal contributors include Kimberly L. Allison, Gregory T. Jones and Sanjeev Chitre.

The JPL Technical Program Manager is Dale Burger.

ABSTRACT

Work on the "Development of Low-Cost Polysilicon Solar Cells" was conducted during this reporting period. This project covers the period from January, 1979, through June, 1979.

Wacker material was the only polysilicon material considered during this reporting period, due to late delivery of other material types. A batch of 10.1% efficient Wacker polysilicon solar cells were produced using the baseline fabrication sequence with standard POCl_3 gettering, spray-on-dopant junction formation and SiO_2 AR coating. The highest efficiency obtained from this batch was 10.5%.

The average crystal grain size for a sample lot of Wacker polysilicon wafers was found to be 0.16 inches. This result was employed to show that insufficient grid-line coverage of polysilicon crystal grains can lead to a significant power loss.

A theoretical and experimental comparison between single crystal and polysilicon solar cell efficiencies was used to investigate the impact of the structural properties of polysilicon material on solar cell efficiency. The experimental data obtained in this study are in agreement with the theoretical predictions of the diffusion length model of polysilicon material.

On the basis of this correlation, it was concluded that the lower efficiencies of polysilicon solar cells made from Wacker polysilicon material, relative to single crystal silicon solar cells, are not due to processing inadequacies, but rather to grain boundary effects.

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INTRODUCTION

The production of low-cost, large area, high efficiency polysilicon solar cells is the overall goal of this program. The major tasks which comprise this project include: (1) development of a low-cost polysilicon solar cell process sequence which achieves ten percent (10%) efficient large area polysilicon solar cells in batch quantities, (2) development of a front surface grid pattern optimized with respect to crystal grain size, (3) investigation of a polysilicon wafer surface macrostructure or texturizing process suitable for large scale production, (4) study of junction formation techniques, (5) investigation of antireflective coatings suitable for polysilicon solar cells, and (6) exploration of other processes, as necessary, to obtain high efficiency or low-cost polysilicon solar cells.

The silicon wafer material used in making polysilicon solar cells consists of polycrystalline structures which are characterized by a high degree of planar crystallographic defects in the form of grain boundaries. The primary factor influencing

polysilicon solar cell efficiency is minority carrier recombination which occurs primarily at the grain boundaries (minority carrier sinks). The two types of polycrystalline structures which may be used in polysilicon solar cells are randomly oriented and fibrously oriented crystal grain structures. Figure 1 shows randomly oriented crystal grains. In this case, only the top most crystal grains are able to contribute to the solar cell power output. Figure 2 shows the superior fibrously oriented crystal grains. In this structure minority carriers within each crystal grain can cross the junction and the entire thickness of the cell. Hence, this polycrystalline solar cell can be thought of as a parallel combination of filamentary solar cells, each of which can act as a normal cell except for some recombination which takes place at the sides of each crystal grain, as well as, at the front surface and back contact. Polysilicon solar cells with fibrously oriented grains can be processed for high efficiency solar cells.

The polysilicon wafer material studied this quarter was supplied by Wacker Chemical Corporation. Other polysilicon materials were not investigated due to late delivery by their respective suppliers.

Figure 1. Polysilicon solar cell with randomly oriented crystal grains.

FIGURE 2. Polysilicon solar cell with fibrously oriented crystal grains.

The Wacker material is characterized by fibrously oriented crystal grains.

Work was performed this quarter, in the following five areas: (1) study of polysilicon solar cell process methods for Wacker material, (2) investigation of junction formation techniques which include POCl_3 diffusion and spray-on dopants (3) exploration of other process techniques which include gettering and spray-on dopants, (4) determination of the suitability of a particular grid pattern design for 4" x 4" square Wacker Polysilicon material, and (5) theoretical and experimental comparison between polysilicon and single crystal silicon solar cell efficiencies.

TECHNICAL DISCUSSION

A. STUDIES OF POLYSILICON SOLAR CELL PROCESS METHODS FOR WACKER MATERIAL

Several polysilicon solar cell process methods for Wacker polysilicon wafers were investigated for the purpose of identifying one or more fabrication sequences which yield 10% efficient polysilicon solar cells in batch quantities. Preliminary experiments proceeded by utilizing Wacker polysilicon wafers in experimental test runs through Sensor Technology's standard single crystal solar cell fabrication sequence. This solar cell fabrication sequence is tailored specifically for 3.5" round, single crystal silicon solar cells. Since the scope of the preliminary investigations was to identify trends which indicate directions for a more intensive study; the standard single crystal silicon solar cell fabrication sequence was not adjusted for processing 4" x 4" Wacker polysilicon wafers.

1. Baseline Processing Sequence

Our preliminary work began by utilizing Wacker polysilicon wafers in experimental test runs through Sensor Technology's standard single crystal silicon solar cell fabrication sequence, which is shown in Figure 3. The grid pattern design utilized for

FIGURE 3: Block diagram of the baseline processing sequence for polysilicon solar cells.

the Wacker polysilicon solar cells is shown in Figure 4. The primary motivation for performing the preliminary tests was to investigate the applicability of current standard single crystal silicon solar cell process methods to Wacker polysilicon material. During the course of this activity, an unacceptable number of wafers were broken. Since polysilicon wafers have poor mechanical strength, special care in wafer handling during solar cell fabrication was found to be essential. Representative electrical performance data from this first polysilicon solar cell Batch P-100 are as follows:

SAMPLE SIZE : 10 (20% yield)

I_{SC} (A): 1.48

V_{OC} (V): .535

I_{PP} (A): 1.11

V_{PP} (V): .385

η (%) : 7.61

FF : .540

The relatively poor, overall electrical performance data presented above indicates a need to explore alternative process methods for achieving an improvement in the electrical performance of Wacker polysilicon solar cells.

FIGURE 4: Gridline Pattern For Wacker Polysilicon Solar Cells.

In this capacity, our initial efforts were directed toward the following areas: (1) POCl_3 gettering; our standard gettering procedure includes thermal treatment of silicon wafers in the presence of POCl_3 to grow a phosphosilicate glass layer on the silicon surface, followed by etching, or removal of the glass layer and (2) spray-on-dopant junction formation. Each of the above topics are discussed in this task.

2. Gettering Study

Phosphosilicate glass gettering has been used for some time to remove unwanted electrically active impurities from silicon wafers. (1) The grain boundaries in polysilicon wafers are planar crystallographic defects which may contain a large amount of residual impurities. For this reason, it appeared worthwhile to investigate the usefulness of including a gettering treatment in polysilicon solar cell fabrication. A discussion of the major activities performed in this area is presented below.

a) POCl_3 Gettering and POCl_3 Diffusion

Two batch tests were performed with 3.94 x 3.94 inch square, 15.7 mil thick Wacker polysilicon wafers. Batch P-101 was processed using the baseline solar cell fabrication sequence shown in Figure 3 with standard POCl_3 gettering, POCl_3 diffusion, edge grinding and no A.R.coating. Batch P102 was processed identically as Batch P-101, except for the addition of an A.R.coating step. The I-V curves for Batch P-101 and Batch P-102 are shown in Figures 5 and 6 respectively, and the electrical performance results are shown in Table 1.

Upon comparison of the average efficiency of the gettered Batch P-101 (8.7%) with the average efficiency of the baseline Batch P-100 (7.69%), it appears that the inclusion of a POCl_3 gettering step in the baseline processing sequence will improve the Wacker

FIGURE 5: Electrical performance Of Gettered Wacker Polysilicon Solar Cells Without AR Coating, Batch P-101.

FIGURE 6: Electrical Performance Of Gettered Wacker Polysilicon Solar Cells With SiO AR Coating, Batch P-102.

TABLE 1: Summary Of Electrical Performance Of
3.85 x 3.85 in. Square Wacker Poly-
silicon Solar Cells.

BATCH	I _{sc} (a)	V _{oc} (v)	I _{pp} (a)	V _{pp} (v)	η (%)	FF	$\frac{\Delta\eta}{\eta}$ (%)	$\frac{\Delta FF}{FF}$ (%)
P-101 POCl ₃ gettering, NaOH etch, POCl ₃ diffusion, w/o AR coating (with SiO ₂).								
1	2.4	0.525	2.10	0.400	8.78	0.67	+1.30%	+1.52%
2	2.4	0.525	2.10	0.390	8.56	0.65	-1.30%	-1.52%
Ave.	2.4	0.525	2.10	0.395	8.67	0.66		
P-102 POCl ₃ gettering, NaOH etch, POCl ₃ diffusion, with SiO AR coating.								
High	2.60	0.525	2.20	.410	9.43	0.661	+ 3.58%	+ .60%
Low	2.50	0.515	2.10	.400	8.78	0.652	- 3.56%	- .76%
Wt.Ave.	2.55	0.520	2.15	0.405	9.10	0.657		

polysilicon solar cell efficiency.

b) Intermediate Gettering Study

A POCl_3 gettering treatment in combination with a two-stage texturizing process sequence was shown to be a highly effective method for producing high efficiency single crystal silicon solar cells. (2) In particular, it was found that the placement of a POCl_3 gettering step between the two sequential texturizing steps (intermediate gettering) provides a higher efficiency improvement than gettering prior to the texturization process, for single crystal silicon solar cells. Since the attainment of high efficiency polysilicon solar cells is a vital component of this project, an intermediate gettering study was performed with Wacker polysilicon wafers. This study proceeded by comparing intermediate gettering as described above, with the standard gettering treatment performed earlier.

Three batch tests were performed in this task. Batches P-230 and P-231 were processed using the baseline solar cell fabrication sequence shown in Figure 3 with POCl_3 gettering. Batch P-220 was processed using the baseline fabrication sequence with intermediate gettering. The electrical performance

results for each batch test is shown in Table 2. The average efficiency of batch P-230, 8.4%, is slightly higher than the average efficiency of the intermediate gettered polysilicon solar cells, 8.1%. It appears from the data that the use of the standard gettering treatment results in a marginally higher efficiency improvement for Wacker polysilicon solar cells, than intermediate gettering.

3. Spray-on-Dopant Junction Formation

Spray-on dopant junction formation is an innovative low-cost solar cell processing technique which has been investigated for single crystal silicon solar cells. ⁽³⁾ This process method was found to yield solar cell efficiencies comparable to the efficiencies of POCl_3 diffused solar cells. Since the fabrication of low-cost polysilicon solar cells is an important goal of this project, the spray-on dopant junction formation process was evaluated for Wacker polysilicon material.

The solar cells processed in this task followed the baseline fabrication sequence given in Figure 3 with spray-on n^+ dopant replacing the POCl_3 diffusion and with the utilization of the POCl_3

TABLE 2: Summary Of Electrical Performance Results for The
Intermediate Gettered And Standard Gettered
3.85 x 3.85 Inch Square Wacker Polysilicon
Solar Cells.

BATCH	I _{sc} (a)	V _{oc} (v)	I _{pp} (a)	V _{pp} (v)	η (%)	FF	$\frac{\Delta\eta}{\eta}$ (%)	$\frac{\Delta FF}{FF}$ (%)
P-220 Texturize (20% NaOH, 10 min.), Getter (900°C, 45 min.), Texturize (1% NaOH, 10 min.), POCl ₃ Diffusion (900°C, 35 min.)								
1	2.250	.525	1.900	.385	7.654	.619	- 5.74	- 2.52
2	2.400	.525	2.050	.400	8.580	.651	+ 5.67	+ 2.52
Ave.	2.325	.525	1.975	.393	8.120	.635		
P-230 Pregetter (900°C, 45 min.), NaOH etch (20% NaOH, 20 min.), POCl ₃ Diffusion (900°C, 35 min.)								
1	2.55	.520	2.00	.385	8.057	.580	- 4.54	- 4.29
2	2.55	.520	2.05	.385	8.258	.595	- 2.16	- 1.82
3	2.55	.525	2.10	.410	9.00	.643	+ 6.63	+ 6.11
Ave.	2.55	.522	2.05	.393	8.44	.606		
P-231 Pregetter (900 C, 35 min.), NaOH etch (20% NaOH, 15 min.), POCl ₃ Diffusion (900 C, 25 min.)								
1	2.45	.530	2.15	.410	9.22	.679		

gettering and SiO A.R. coating options. The I-V curves for the spray-on doped 3.85 x 3.85 inch square Wacker polysilicon solar cells, Batch P-103, are presented in Figure 7 and the electrical performance results are given in Table 3.

The highest efficiency achieved from the n^+ spray-on-doped polysilicon solar cell batch was 10.5%. The weighted average efficiency in this batch was 10.1%. For comparison, the weighted average efficiencies of all previous batch tests ranged from 7.61% for the baseline fabrication sequence, to 9.1% for the gettered batch P-102, with SiO AR coating. It is clear that the use of spray-on-dopant junction formation in place of our conventional $POCl_3$ diffusion process, has led to a significant efficiency improvement for Wacker polysilicon solar cells.

The outcome of the spray-on-dopant junction formation study with Wacker polysilicon material provided several encouraging results. It was demonstrated that 10% efficient polysilicon solar cells in batch quantity can be achieved by utilizing the baseline fabrication sequence in Figure 3 with

FIGURE 7: Electrical Performance Of Spray-On Doped Wacker Polysilicon Solar Cells With SiO AR Coating, Batch P-103.

TABLE 3: Summary Of Electrical Performance Results
For Spray-On Doped 3.85 x 3.85 Inch Square
Wacker Polysilicon Solar Cells.

BATCH	I _{sc} (a)	V _{oc} (v)	I _{pp} (a)	V _{pp} (v)	η (%)	FF	$\frac{\Delta\eta}{\eta}$ (%)	$\frac{\Delta FF}{FF}$ (%)
P-103	POCl ₃ getter, NaOH etch, spray-on N ⁺ dopant, with SiO AR coating.							
High	2.875	.525	2.55	.395	10.53	.667	+ 4.36%	+1.52%
Low	2.80	.510	2.45	.375	9.61	.643	- 4.75%	-2.13%
Ave.	2.825	.520	2.475	.390	10.09	.657		

gettering, spray-on-dopant junction formation, and SiO₂ AR coating. This result fulfills a crucial goal of this project, that is, the production in batch quantity of 10% efficient polysilicon solar cells. In addition, the low cost of the spray-on-dopant junction formation process⁽³⁾ provides yet another advantageous reason for its use with Wacker polysilicon material.

B. GRID PATTERN DESIGN ANALYSIS

The grid pattern design shown in Figure 4 was not rigorously analyzed prior to its use in the studies of polysilicon solar cell process methods. An initial analysis was performed on this grid pattern design to determine its suitability for use on 4" x 4" Wacker polysilicon wafers. The complete study encompassed the following three areas: (1) crystal grain size measurements, (2) gridline spacing sensitivity analysis, and (3) trunkline width sensitivity analysis. Each area is discussed below.

1. Crystal Grain Size Measurements

The average crystal grain size, d_g , in a sample lot of 4" x 4" Wacker polysilicon wafers was computed on the basis of a statistical analysis.

of crystal grain size measurements. The photograph of a typical polysilicon wafer utilized for computing d_g , is shown in Figure 8. A total of two hundred individual grains were measured from a random sampling of grains in four polysilicon wafers. A complete measurement consisted of visually measuring both the longest and shortest grain dimensions. After the completion of two hundred such measurements, the average crystal grain size, d_g , was computed from the statistically averaged values of the longest and shortest grain dimensions (d_l , and d_s , respectively) in the following manner:

$$d_l = 0.212"$$

$$d_s = 0.105"$$

$$d_g = \frac{1}{2}(d_l + d_s) = 0.16"$$

The average crystal grain size for the Wacker polysilicon material examined in this study was found to be 0.16 inches.

2. Gridline Spacing Sensitivity Analysis

The main objective of this study was to lay the groundwork for an ongoing investigation to identify

FIGURE 8: Picture Of A Typical Wacker
Polysilicon Wafer Used In Computing
The Average Crystal Grain Size, d_g .

the necessary criteria which must be satisfied to optimize the gridline spacing for the polysilicon solar cell grid pattern design shown in Figure 4. An important criterion, which was emphasized during this reporting period, is that the spacing between successive gridlines must be less than the average crystal grain size. This constraint can be explained qualitatively by noting that each crystal grain will have a high probability of being contacted by a gridline if the gridline spacing is less than the average grain size. If this condition is not met, a large number of crystal grains may not be contacted by gridlines, which implies that a significant portion of the current generated at these grains will be lost at the grain boundaries (minority carrier sinks) due to recombination.

The average crystal grain size for a sample lot of Wacker polysilicon wafers was measured and found to be 0.16 inches. Since the gridline spacing for the grid pattern design shown in Figure 4 is 0.125 inches, this spacing appears to be compatible with the average crystal grain size on the basis of the foregoing discussion.

The suitability of using the grid pattern design of Figure 4 on polysilicon material with an average crystal grain size of 0.16 inches, was investigated. On the basis of the above discussion, this particular gridline spacing will be unsuitable if it can be demonstrated that a significant power loss occurs due to insufficient gridline coverage of the crystal grains. In order to rigorously establish the existence of this situation, several tasks must be performed. First, the area of each crystal grain which was not contacted by a gridline, would have to be measured for a statistically valid number of polysilicon solar cells. Once this is accomplished, the ratio of the total crystal grain area per polysilicon solar cell which is not contacted by gridlines with the total polysilicon solar cell area, must be computed and then statistically averaged. This statistically averaged value represents the total power loss due to insufficient gridline coverage of the crystal grains.

Instead of performing the time-consuming tasks outlined above, a probability analysis was performed for the two hundred random crystal grains measured earlier. The following equation was utilized to compute the probable power loss, Q , associated with the random sampling of 200 crystal grain size measurements:

$$Q = \frac{\sum_{i=1}^n \left[\left(1 - \frac{g_i + t_o}{s} \right)^{u_i} (g_i + t_o)^2 N_i \right]}{A} \quad (1)$$

$$u_i = 1 \quad \text{for } g_i < (s - t_o)$$

$$u_i = 0 \quad \text{for } g_i \geq (s - t_o)$$

where g_i = the size of i^{th} crystal grain

s = the gridline spacing (.125 inches)

t_o = the gridline width

N_i is the number of crystal grains with size " g_i " in the 200 random grain size measurement.

A is the total area of the 200 random grain size measurements.

Each element of Q for the grid pattern design in Figure (4) is tabulated in Table 4. The numerical value of Q was computed and found to be 0.94%. For this case, the power loss associated with insufficient gridline coverage of polysilicon crystal grains is minimal. This result shows that the present gridline spacing is close to the optimum value. On the other hand, for a gridline spacing of 0.16", the value of Q is 4.24%. It can thus be seen that insufficient gridline coverage of polysilicon crystal grains could be a significant factor to contend with for gridpattern design optimization.

TABLE 4: Tabulation Of The Numerical Values
Used In Computing The Probable Power
Loss, Q, For The Gridpattern Design
Of Figure 4.

$g_i + t_o$	N_i	$\frac{g_i + t_o}{S}$	$1 - \frac{(g_i + t_o)}{S}$	$(g_i + t_o)^2 N_i (1 - \frac{(g_i + t_o)}{S})$
.12 in	11	.96	.04	.0063 in ²
.11 in	10	.88	.12	.0145 in ²
.10 in	6	.80	.20	.012 in ²
.09 in	8	.72	.28	.018 in ²
.08 in	1	.64	.36	.0023 in ²
TOTAL				.0.0531 in ²

$$Q \equiv \frac{\text{Probable crystal grain area which isn't hit by gridlines}}{\text{Total area of 200 random crystal grain size measurements}} = \left(\frac{.0531}{5.63} \right) = .943\%$$

$$S = 0.125 \text{ in}$$

$$t_o = 0.010 \text{ in}$$

$$(g_i)_{\text{max}} = 0.11 \text{ in}$$

$$(g_i)_{\text{min}} = 0.07 \text{ in}$$

3. Trunkline Width Sensitivity Analysis

A trunkline width sensitivity analysis was performed for the Wacker polysilicon solar cell grid pattern design shown in Figure 4. Single crystal solar cell analysis methods were utilized. The trunkline width sensitivity analysis proceeded by calculating, and then summing together all resistive power loss components, including shadowing losses, in terms of relevant parameters. The numerical values of all parameters were specified in this sum, with the one exception of the trunkline width, which was denoted by "t". The sum of the power loss components was then differentiated with respect to "t". This result was set equal to zero, to solve for the value of "t" which yields a minimum value for the total sum of power loss components. The result of this calculation indicates that the optimum value of "t" should be 0.0657 inches. By substituting this value of "t" back into the equation for the total sum of power loss components, the total power loss amounts to 16.26%. By substituting the value of "t" used in Figure 4 (0.075 inches) into this same equation, the total power loss is 16.32% which is only 0.06% higher than the value obtained with the optimized trunkline width. The results of this analysis indicate that the efficiencies of Wacker polysilicon solar cells

utilizing the grid pattern design shown in Figure 4, will not undergo significant improvement by merely adopting the calculated version of the optimized value of the trunkline width.

C. THE INFLUENCE OF GRAIN SIZE ON POLYSILICON
SOLAR CELL EFFICIENCY

The impact of the structural properties of polysilicon material on solar cell efficiency can be approximated with the use of the diffusion length model of polysilicon.⁽⁴⁾ The diffusion length model for polysilicon was utilized to obtain a theoretical comparison between single crystal and polysilicon solar cell efficiencies. The major reason for performing this comparison was to determine whether the lower efficiencies obtained for polysilicon solar cells relative to single crystal solar cells are due primarily to grain boundary effects or to processing inadequacies. A discussion of the results achieved from the theoretical and experimental comparison between single crystal and polysilicon solar cell efficiencies is discussed below.

1. Theoretical Comparison Between Single
Crystal and Polysilicon Solar Cell Efficiency

(4)

The diffusion length model of polysilicon material contends that the influence of a grain boundary extends one diffusion length, L_p . Assuming fibrous oriented crystal grains with square cross-section, the effective size of each grain (d_g) is reduced by $2L_p$. Consequently, an approximate expression for the ratio of the efficiencies of polysilicon solar cells with the efficiencies of single crystal solar cells of the same geometrical area is as follows:

$$\frac{\eta_p}{\eta_s} = \left(1 - \frac{2L_p}{d_g} \right)^2 \quad (2)$$

where d_g is the geometrical grain size.

In order to apply this formula to Wacker polysilicon wafers, the geometrical grain size, d_g , and the diffusion length, must be known. The average diffusion length was given by the polysilicon wafer supplier as 200 microns. The average grain size was obtained on the basis of random visual grain size measurements from a sample lot of Wacker polysilicon wafers. The statistical analysis performed on the measured grain sizes indicated that the average

geometrical grain size is 0.16 inches or 4064 microns. Substituting $d_g = 4064$ microns, and $L_b = 200$ microns, into equation (2) yields a relative efficiency ratio of 0.813 between polysilicon solar cells and single crystal silicon solar cells. If the actual experimental efficiency ratio between polysilicon and single crystal silicon solar cells approaches the predicted theoretical value of 0.813, the diffusion length model is a valid approximation. An additional implication is that polysilicon solar cell efficiencies will not equal the efficiency of single crystal silicon solar cells without some means of grain boundary passivation.

2. Experimental Comparison Between Single Crystal and Polysilicon Solar Cell Efficiency

An experimental comparison between single crystal and polysilicon solar cell efficiency was made to check the validity of the theoretical efficiency ratio obtained from the diffusion length of polysilicon material. Three inch diameter single crystal solar cells which are identified by Batches S-311, S-312 and S-313; and 4" x 4"

Wacker polysilicon solar cells which are identified by Batches P-311, P-312 and P-313; were processed and tested. The baseline fabrication sequence given in Figure 3 was used to process the surfaced etched Batches P-311 and S-311, intermediate gettered Batches P-312 and S-312 and standard gettered Batches P-313 and S-313. Following the nickel plating step, the single crystal wafers were cut by laserscribe into 1.90" x 1.90 squares and the 4" x 4" square Wacker polysilicon wafers were cut into four 1.90" x 1.90" squares to facilitate comparison of their electrical performances and comparison of their efficiency ratios.

The electrical performances of the single crystal solar cells and polysilicon solar cells were compared and are shown in Figures 9 and 10 for surface etched Batches P-311 and S-311, and intermediate gettered Batches P-312 and S-312 respectively. The electrical performance results for the surface etched batches, intermediate gettered batches and standard gettered batches are shown in Table 5.

The ratio of the weighted average efficiencies of the surface etched batches (P-311 and S-311), and the intermediate gettered batches (P-312 and S-312) were computed on the basis of the results shown in Table 5. The experimental efficiency ratios for each case are presented below:

FIGURE 9: Electrical Performance Comparing Surface Etched Single Crystal And Wacker Polysilicon 1.90" X 1.90" Solar Cells, Batches S-311, And P-311.

FIGURE 10: Electrical Performance Comparing Intermediate Gettered Single Crystal And Wacker Polysilicon 1.90" X 1.90" Solar Cells, Batches S-312 And P-312.

TABLE 5: Summary of Electrical Performance Results
For Single Crystal And Wacker Polysilicon
1.90" x 1.90" Solar Cells From Batches P-311
And S-311, P-312 And S-312, and P-313 And
S-313, For Comparison.

BATCH	I _{sc} (a)	V _{oc} (v)	I _{pp} (a)	V _{pp} (v)	η (%)	FF	$\frac{\Delta\eta}{\eta}$ (%)	$\frac{\Delta FF}{FF}$ (%)
P-311 Surface etched polysilicon.								
High	.630	.525	.570	.405	9.41	.698	+34.1%	+45.9%
Low	.490	.510	.350	.375	5.35	.525	-23.7%	-12.8%
Wt. Ave	.555	.515	.425	.405	7.016	.602		
S-311 Surface etched single crystal.								
High	.665	.560	.590	.440	10.58	.700	+11.30%	+ 0.0%
Low	.595	.550	.500	.420	8.56	.642	-10.00%	- 8.29%
Wt. Ave.	.600	.555	.530	.440	9.51	.700		
P-312 Intermediate gettered polysilicon.								
High	.595	.520	.530	.395	8.53	.677	+ 9.55%	+ 2.11%
Low	.535	.505	.465	.380	7.20	.654	- 7.57	- 1.36
Wt. Ave.	.560	.515	.490	.390	7.79	.663		
S-312 Intermediate Gettered Single Crystal.								
High	.650	.550	.580	.440	10.40	.714	+ 7.00%	- 3.48%
Low	.635	.545	.550	.430	9.64	.683	- 0.82%	- 1.01%
Wt. Ave.	.635	.545	.555	.430	9.72	.690		

TABLE 5: CONTINUED

BATCH	I_{sc} (a)	V_{oc} (v)	I_{pp} (a)	V_{pp} (v)	η (%)	FF	$\frac{\Delta\eta}{\eta}$ (%)	$\frac{\Delta FF}{FF}$ (%)
P-313 Standard gettered polysilicon.								
High	.585	.520	.525	.405	8.67	.699	+ 9.47	+1.895
Low	.520	.505	.450	.375	6.87	.643	-13.26	-6.268
Wt. Ave.	.550	.515	.505	.385	7.92	.686		
S-313 Standard gettered single crystal.								
1	.580	.545	.535	.40	8.72	.677		

$$(1) \quad \frac{\eta_{(P-311)}}{\eta_{(S-311)}} = 0.7377 \quad (\text{surface etching})$$

$$(2) \quad \frac{\eta_{(P-312)}}{\eta_{(S-312)}} = 0.801 \quad (\text{intermediate gettering})$$

Within the limits of experimental error, these experimental efficiency ratios are in agreement with the theoretical efficiency ratio of 0.813 obtained earlier.

The implications of the polysilicon and single crystal silicon solar cell efficiency comparison are stated below:

- a. It provides experimental evidence which points to the validity of the diffusion length model of polysilicon solar cells, i.e., confirmation that L_B is a crucial parameter in polysilicon solar cell efficiency.
- b. The good correlation between the theoretical and experimental efficiency ratios indicates that the lower efficiency of polysilicon solar cells relative to single crystal

silicon solar cells is primarily due to grain boundary effects rather than processing inadequacies.

- c. The efficiency improvement of intermediate gettered polysilicon solar cells relative to surface etched polysilicon solar cells, is larger than for the analogous single crystal case. A possible explanation for this observation is the presence of a high concentration of impurities in the grain boundary regions.

CONCLUSIONS AND RECOMMENDATIONS

The work performed in the development of low cost polysilicon solar cells has led to a number of conclusions and recommendations. Experimental results indicate that the inclusion of standard POCl_3 gettering in the baseline polysilicon solar cell fabrication sequence, will greatly improve the efficiency of polysilicon solar cells made from 4" x 4" square Wacker polysilicon material. The highest efficiency achieved from all Wacker polysilicon solar cells fabricated to date, was 10.5%. The processing sequence utilized in this case was the baseline fabrication sequence with standard POCl_3 gettering, spray-on dopant junction formation and SiO_2 AR coating. The average efficiency of this polysilicon solar cell batch was 10.1%, which fulfills a crucial goal of this project.

The initial studies performed on the solar cell grid pattern design for Wacker material have shown that the power loss associated with insufficient gridline coverage of polysilicon crystal grains could be a significant factor to contend with in optimizing the gridline spacing of polysilicon solar cells. The experimental data obtained in the comparison between single crystal silicon and polysilicon solar cell efficiencies are in agreement with the theoretical predictions of the diffusion length model of polysilicon material. On the basis of this correlation,

the lower efficiencies of polysilicon solar cells made from Wacker polysilicon material, relative to single crystal silicon solar cells, are not due to processing inadequacies, but rather to grain boundary effects.

To extend and verify the work performed during this reporting period, it is recommended that the following areas should be investigated: (1) alternative gettering methods, (2) polysilicon wafer surface preparation methods, (3) diffusion time and temperature optimization, and (4) in-depth study of spray-on-dopant junction formation for Wacker material.

PROGRESS SUMMARY AND PROGRAM PLAN

The progress summary and program plan for the Development of Low-Cost Polysilicon Solar Cells is given in the milestone chart in Table 6.

Table 6: Milestone Chart for Development of Low-Cost Polysilicon Solar Cells

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1. R. L. Meek and C. F. Gibbon, J. Electrochem, Soc. 121, 444; 1974.
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