MASTER

RECEIVED BY TIC MAR 21 1980

December, 1979

ERC41020.26TPR

DEVELOPMENT OF POLYCRYSTAL GaAs SOLAR CELLS

Quarterly Technical Progress Report No. 3
for period 08/01/79 through 10/30/79

By

D. L. Miller, Marshall J. Cohen and J. S. Harris, Jr.
Rockwell International Electronics Research Center
Thousand Oaks, California 91360

Joseph Ballantyne
Cornell University
Ithaca, New York 14853

Elias Stefanakos
North Carolina A & T State University
Greensboro, North Carolina 27411

For

Solar Energy Research Institute
1536 Cole Boulevard
Golden, Colorado 80401

Prepared under Contract No. XS-9-8032-1

Approved by:

J. S. Harris, Jr.
Program Manager

DISCLAIMER

This book was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States nor any agency thereof, nor any of their employees, makes any warranty expressed or implied, or assumes the legal liability of responsibility for any third party's use or the results of such use of any information, apparatus, product or process disclosed in this report or represents that its use by such third part would not infringe privately owned rights.

Rockwell International
Electronics Research Center

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency Thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

TABLE OF CONTENTS

	<u>Page</u>
1.0 INTRODUCTION.....	1
2.0 ROCKWELL INTERNATIONAL.....	2
2.1 Materials Growth and Characterization.....	4
2.2 Grain Boundary Passivation.....	8
3.0 CORNELL UNIVERSITY	
3.1 SIMS.....	12
3.2 Scanning Light Microscopy.....	13
3.3 DLTS.....	15
4.0 NORTH CAROLINA A & T STATE UNIVERSITY.....	25
4.1 Current Controlled LPE.....	25
4.2 Model of Grain Boundaries.....	27
4.3 Passivation of Grain Boundaries by Impurity Diffusion..	27
4.3.1 Passivation Experiments on a Single Grain Boundary.....	29
4.3.2 I-V and C-V Measurements on Polycrystal GaAs Grain Boundaries.....	34

LIST OF FIGURES

	<u>Page</u>
Fig. 2.1 Conductivity of polycrystal GaAs films on Vistol substrates before (-----) and after (——) Ru treatment.....	10
Fig. 2.2 Dark I-V characteristics of Au Schottky barriers to polycrystal GaAs on Mo substrates before (——) and after (-----) Ru treatment.....	11
Fig. 3.1 Band structure at metal-semiconductor interface.....	14
Fig. 3.2 Photocurrent vs. reverse bias demonstrating effects of diffusion length.....	16
Fig. 3.3 Variation of the diffusion length in the vicinity of a grain boundary.....	17
Fig. 3.4 Band diagram in the vicinity of a grain boundary during DLTS measurement.....	19
Fig. 3.5 DLTS scan at grain boundary diode.....	22
Fig. 3.6 DLTS signal vs. temperature at grain boundary diode.....	23
Fig. 3.7 DLTS signal vs. voltage for grain boundary diode.....	24
Fig. 4.1 Surface photomicrograph of GaAs epigrowth on Mo substrate from Sn melt.....	26
Fig. 4.2 Model of partial passivation.....	28
Fig. 4.3 Evacuated ampoule for potassium diffusion. (1) Pyrex tube, (2) GaAs bicrystal, (3) control sample, (4) potassium contained in small Pyrex tube.....	30
Fig. 4.4 Sample dimensions and configuration for single grain boundary measurements.....	31
Fig. 4.5 I-V characteristics of a single grain boundary.....	32
Fig. 4.6 I-V characteristics of a single grain boundary.....	33
Fig. 4.7 Resistance versus inverse temperature for a single grain boundary.....	35

LIST OF FIGURES

	<u>Page</u>
Fig. 4.8 Energy band diagram of bicrystal in region of grain boundary.....	37
Fig. 4.9 Capacitance-voltage data for bicrystal grain boundary. (Sample A12).....	39
Fig. 4.10 Current-voltage characteristic of bicrystal grain boundary (Sample A12).....	40
Fig. 4.11 Current-voltage data for bicrystal grain boundary. (Sample A12).....	42

DISTRIBUTION LIST

Solar Energy Research Institute
Photovoltaics Program Office
PVPO - Documentation
1536 Cole Blvd.
Golden, CO 80401

Department of Energy
Technical Information Center
P.O. Box 62
Oak Ridge, TN 37830

Solar Energy Research Institute
Contracts Branch
Ref: XS-9-8032-1
1536 Cole Blvd.
Golden, CO 80401

Department of Energy
Chicago Operations Office
Attn: Office of Public Affairs
9800 S. Cass Ave.
Argonne, IL 60439

Dr. M. B. Prince
Section Leader
Photovoltaics R&D
Mail Station 404
600 E.St., NW
Washington, D.C. 20545

Electronics Research Center Distribution

F. H. Eisen
J. S. Harris, Jr.
D. L. Miller
M. J. Cohen
H. T. Yang
P. D. Dapkus
Group Secretary
Contracts & Pricing
Library

Subcontractors

Howard University
2300 6th St., NW
Washington, D.C. 20059
Attn: Alfred Hoyte
Dept. of Electrical Engineering

North Carolina A&T State University
312 N. Dudley St.
Greensboro, NC 27422
Attn: Prof. Lee Stefanakos
Dept. of Electrical Engineering

Cornell University
Dept. of Electrical Engineering
Ithaca, NY 14850
Attn: Prof. Joseph Ballantyne

DISTRIBUTION LIST (Cont.)

Outside Distribution

S. M. Bedair
Research Triangle Institute
P.O. Box 12194
Research Triangle Park, NC 27709

Ronald Bell
Varian Associates
611 Hansen Way
Palo Alto, CA 94304

S. S. Chu
Southern Methodist University
Dept. of Electrical Engineering
Dallas, TX 75275

Ralph L. Dawson
Sandia Laboratories
Division 5154
Albuquerque, NM 87165

John C. C. Fan
MIT-Lincoln Lab
Wood Street
Lexington, MA 02173

S. K. Ghandi
Rensselaer Polytechnic Institute
Department of Engineering
Troy, NY 12181

Harold J. Hovel
IBM Research Lab
Yorktown Heights, NY 10598

W. D. Johnson
Bell Telephone Laboratories
Room HO-4D-411
Holmdel, NJ 07733

G. L. Pearson
Stanford University
Stanford Electronics Laboratories
Stanford, CA 94305

Donald Smith
Perkin Elmer
Electro-Optical Division
Norwalk, CN 06856

R. J. Stirn
Jet Propulsion Laboratory
4800 Oak Grove Dr.
Pasadena, CA 91103

ABSTRACT

During this quarter, the progress to date of the program was evaluated with a goal of designing programs for the coming year. The experimental efforts of the quarter reflected this evaluation and were focused on the subsequent redirection of the program. Highlights of the quarter include the growth of Ge on Fe substrates and the investigation of various grain boundary passivation schemes.

1.0 INTRODUCTION

Progress in the development of high efficiency single crystal GaAs solar cells has been phenomenal over the past three years. Over this period, GaAs cell efficiencies have gone from 16% to nearly 25%, the highest value for any solar cell, and approaching the theoretical limit for a single cell structure. Numerous systems studies of various solar cell options suggest that the lowest, long term solar electric generating costs will be achieved by very low cost, polycrystal or amorphous thin film devices. The successful reduction of the adverse effects of grain boundaries could lead to polycrystal solar cells with efficiencies of more than 15%. The realization of 10% conversion efficiency in a thin film polycrystal structure is the goal of this program.

During this past quarter, three of the institutions participating in this program (Rockwell International, Cornell University and North Carolina A&T State University) prepared proposals in response to SERI RFP No. RS-9-8350. During the quarter, the progress to date of the program was evaluated with a goal of designing programs for the coming year. The experimental efforts of the quarter reflected this evaluation and were focussed on the subsequent redirection of the research.

The proposals submitted this quarter outline three separate programs. This report, therefore, is organized by institution rather than by task as in the previous reports. The progress this quarter at Rockwell International, Cornell University and North Carolina A&T State University are summarized in sections 2-4.respectively. No contribution was received from Howard University this quarter.

2.0 ROCKWELL INTERNATIONAL

One of the major goals of the program at Rockwell, as well as elsewhere, has been to develop a materials technology to produce thin films of GaAs on potentially low cost conducting substrates which would yield high efficiency polycrystal solar cells. The majority of the effort thus far has gone into the non-epitaxial growth of GaAs on fine-grained polycrystal conducting substrates such as graphite or Mo. The main approaches to improving the grain size have been principally alterations in the substrate and GaAs growth conditions. Investigations of substrates and their surface preparation include: growth directly on graphite, ordered graphite, glasses, ceramics, large grained Al and Fe, and growth on graphite glasses and metallic substrates coated with pyrolytic graphite, W and Mo. Variations in growth conditions include: substrate temperature, Ga/As ratio, total beam or gas fluxes, partial layer coverage with a high temperature anneal to achieve nuclei coalescence and larger grains before the main growth occurs and the simultaneous use of an etching species such as HCl during CVD growth.

The motivation for this avenue of research has been the assumption that the main source of the degradation of solar cell performance arising from the presence of grain boundaries in polycrystal material is the loss of photocurrent due to excess recombination. Since the diffusion lengths in GaAs are inherently short, it has been asserted that solar cells made from polycrystal GaAs with grain sizes of order 4-5 microns should exhibit sufficient current collection so that 10% AM1 conversion efficiencies could be attained. This statement implicitly neglects the role of grain boundaries in reducing both the fill factor and open circuit voltage through increased series resistance and decreased shunt resistance.

The successful result of this general approach is a 6.5% efficient MOS polycrystal GaAs solar cell fabricated with 10-20 micron thick active layers which exhibited average grain sizes of order 10 microns. (S.M.U.)

As expected from the high absorption coefficient of GaAs, the short circuit current of these cells approached that of single crystal cells with the same structure. The severely degraded open circuit voltage and fill factor, however, reduced the 14-16% single crystal efficiency to 6.5%. Thus, while this grain size was sufficient to achieve reasonable short circuit currents, the grain boundaries caused enough problems in high series resistance and shunting to degrade performance well below the program goals. This result is an important intermediate step in the development of high efficiency polycrystal GaAs cells because it points out that large grain size is important, but not the complete solution to reaching high efficiency.

An early result of our efforts to grow large grain thin film GaAs on potentially low cost conducting substrates by MBE was the achievement of texture in films grown on graphite. The films were polycrystal with a grain size of order the film thickness (1-2 μm) and were columnar in nature. All the crystallites had the $\langle 111 \rangle$ direction normal to the plane of the film but were randomly oriented within the planes of the film. Numerous attempts were made to increase the grain size by surface treatment and annealing to achieve coalescence at the nucleation stage. The resulting films were very flat-topped, unlike the irregular films observed with both halide transport and MOCVD; however, the increased grain size was never realized.

Two of the problems associated with direct growth of GaAs on many low cost substrates are the tendency for GaAs decomposition and loss of As at temperatures above 750°C and the reactive nature of both the Ga and As and their tendency to form compounds or alloys with many metallic substrates. The temperature limit makes it difficult to experiment on crystallization techniques using high temperatures to achieve nuclei coalescence and larger grains because Ga droplets form which short out the junctions in solar cells. Experiments with GaAs growth directly on large grained Al and Fe alloys resulted in low temperature eutectics forming with Ga which prevented any subsequent GaAs growth.

We have also carried out a number of experiments with the MOCVD system. While some success has been achieved in getting grain sizes larger than the film thickness by using HCl in the growth, the same limits of temperature and reactivity have prevented full exploration of techniques to achieve large grain size. Results of the groups at SMU and Lincoln Labs by halide transport are similar for growth of GaAs directly on a disordered or fine grain substrate.

We are thus led to the conclusion that *"it appears unlikely that a technique can be developed which can produce polycrystal films of GaAs directly on disordered substrates with a grain size that is significantly (10X; or more) larger than the film thickness."*

In this quarter, we have begun exploring a family of techniques we refer to collectively as induced epitaxy. Their common goal is to achieve large grain, almost single crystal, films of GaAs on foreign substrates which will provide the foundation to realize the high efficiency program goals.

2.1 Materials Growth and Characterization

Measurements were continued on structures deposited on Mo. GaAs layers grown by MBE on Al which was deposited on Mo substrates showed rectification at the back contact, between the Al and the GaAs. Crystallite size and growth morphology were similar, for Al layers reacted with either Ga or As before deposition of the GaAs.

A GaAs layer 2 μm thick was grown by MBE on Vistol (polycrystal sapphire). Some areas showed a smooth, nearly single crystal appearing structure, but areas at the substrate grain boundaries grew with small grains very similar to those observed on Mo or graphite. The lateral resistivity of the layer was extremely high ($>10^8 \Omega$ between 0.010" metal dots deposited on 0.040" centers), even for relatively smooth areas which were contained entirely on a single substrate grain. GaAs grown simultaneously on a GaAs

substrate was n-type with $n \cong 4 \times 10^{16}/\text{cm}^3$, so that the high resistivity on Vistol was probably due to grain boundaries.

An attempt was made to increase the grain size of GaAs grown on graphite, by increasing the substrate temperature. We have found that it is possible to grow GaAs at substrate temperatures as high as 640°C (compared to usual temperature of $500\text{--}580^\circ\text{C}$) if a very large As/Ga flux ratio is used. GaAs was grown on Carbone Lorraine graphite at 640°C , $2\text{ }\mu\text{m}$ thick, undoped and then the substrate temperature was lowered to 580°C and an additional $2\text{ }\mu\text{m}$ of p-type GaAs was deposited. The crystallite size, as seen in the SEM, was still small ($\leq 2\text{ }\mu\text{m}$) and comparable to growth at $560\text{--}580^\circ\text{C}$. This is not understood, since our earlier work with graphite substrates showed a definite increase in grain size as substrate temperature increased. Preliminary measurements with tungsten probes indicated very high breakdown voltages in the undoped region, with low breakdown voltages in the p-type layers. Further measurements are in progress.

Approaches involving the growth of GaAs by MBE directly on low cost materials have continued to give layers with maximum grain size approximately equal to the GaAs layer thickness, which has also been observed by others with VPE and CVD growth techniques. Since we feel that considerably larger grain size is necessary in order to obtain 10% conversion efficiency, we have begun an investigation of the growth of GaAs on Ge. As has been demonstrated by Stirn at JPL and others, Ge layers on low cost materials can be recrystallized to yield large grains (several mm across). Cells produced on these layers by MOCVD, however, had relatively poor characteristics. Since the lattice match between GaAs and Ge is good, and very good GaAs cells have been produced on single crystal Ge by Bozler et al. at Lincoln Labs, we have done some preliminary investigations of the growth of GaAs on Ge by MBE. We have been able to achieve good epitaxy, and have grown GaAs cell structures on Ge substrates which exhibit V_{oc} of over .96 volt at 1 SUN, and over 1 volt at ~ 3 SUNs. The interfacial properties at the Ge-GaAs heterojunction appear to be dominated by diffusion of Ga and As into the Ge,

and Ge incorporation into the GaAs. These processes are in turn strongly dependent on the growth conditions and substrate temperature. We feel that MBE growth may have advantages here in limiting the Ge incorporation because of the relatively low growth temperature. Because of these initially encouraging results, we intend to re-investigate the GaAs-Ge structure, and are preparing to grow GaAs layers on large grain polycrystal Ge substrates to determine the effect of crystallographic orientation and of grain boundaries on the GaAs electrical properties.

Studies related to the epitaxy of Ge on Fe, and of GaAs on Ge, were begun this quarter. Large grain polycrystal Fe/Si sheet was obtained which has crystallite sizes of 1-10 mm. Substrates have been cut from this material for use in the MBE apparatus. Experiments are in progress to determine the best chemical methods to prepare a clean surface on this material.

GaAs has been grown by MBE on polycrystal Ge substrates, as well as $\langle 100 \rangle$ single crystal Ge substrates, as part of a continuing investigation of the conditions which lead to good layer morphology and electrical properties. Good GaAs layer properties, as indicated by Schottky barrier I-V and C-V measurements, have been obtained on Ge $\langle 100 \rangle$ by MBE under two very different sets of growth conditions. We earlier had demonstrated good epitaxy of GaAs on $\langle 100 \rangle$ Ge using a substrate temperature of 630°C and a growth rate of $1\text{ }\mu\text{m/hr.}$; most recently we have also obtained good epitaxy at a substrate temperature of 460°C and a growth rate of $0.25\text{ }\mu\text{m/hr.}$ In both cases, the quality of the layers, as indicated by Schottky barrier reverse leakage current and surface roughness, is very sensitive to the growth parameters and substrate preparation techniques.

It appears that, although it is probably possible to find conditions which lead to good epitaxy by MBE on most of the low-index Ge planes, the conditions for good epitaxy vary considerably from plane to plane. This was illustrated by GaAs growth on Ge $\langle 110 \rangle$ and Ge $\langle 111 \rangle$ planes, and by results obtained on polycrystal Ge. GaAs was grown on these three substrates mounted on the same holder with Ge $\langle 100 \rangle$ substrates. Good epitaxy was achieved on

the Ge $\langle 100 \rangle$ substrate, using the growth parameters described above. Growth on the $\langle 110 \rangle$ and $\langle 111 \rangle$ substrates produced a dense carpet of very small GaAs needles, which gives the substrate a black, sooty appearance. Growth on the polycrystal Ge showed variations from grain to grain, with most of the areas having a morphology intermediate between the smooth epitaxy on Ge $\langle 100 \rangle$ and the needle growth on $\langle 110 \rangle$ or $\langle 111 \rangle$.

These results suggest that it will be very important to obtain a recrystallized Ge substrate with a high degree of texturing, i.e., consisting primarily of crystallites with the same surface plane. Growth on large grain, textured Fe sheets may provide this texturing. Experiments are now beginning which should determine the feasibility of this approach.

Experiments were also conducted to determine whether recrystallized Fe might be used as a substrate for Ge epitaxy. The combination would then be used as a substrate for GaAs solar cell growth. The potentially attractive feature of recrystallized Fe is that it can easily be produced with large grains, several mm across, with a strong preferred orientation. The process used for this is to mechanically work the sample to provide an appropriate stress field in the Fe sheet. Annealing the sheet promotes grain growth; the preferred orientation apparently arises from interactions between the stress field and the growing grain boundaries. This process is used commercially to produce transformer iron. The Ge $\langle 100 \rangle$ and Fe $\langle 100 \rangle$ planes are very closely lattice matched, and Fe has been grown epitaxially on GaAs at room temperature at ERC. The initial experiments reported here were done to determine whether Ge could be grown epitaxially on clean, oriented Fe. If this could be achieved, large-grain Ge substrates could be produced which might be suitable for GaAs solar cell growth. The use of a low temperature process such as MBE could reduce Fe diffusion into the Ge and GaAs.

Fe layers were grown on single crystal Ge substrates at room temperature by vacuum evaporation. The Ge had been cleaned by ion bombardment and annealing until a good LEED pattern was visible. After evaporation of several hundred angstroms of Fe onto the Ge, an excellent LEED pattern was

observed, which indicated that epitaxial Fe had been grown on the Ge. This LEED pattern faded fairly rapidly, however, presumably due to the relatively poor vacuum obtained in the unbaked chamber. 200Å of Ge was evaporated over the Fe film before the LEED pattern completely vanished, however. This Ge layer showed no LEED pattern until it was heated to near 450°C, when a faint pattern appeared. Subsequent deposition of more Ge at a substrate temperature of 450°C failed to produce any pattern at all.

Although this experiment was not conclusive, it is somewhat encouraging. First, the observation of epitaxy of Fe on Ge at room temperature is indicative of the good lattice match, and also demonstrates that the interfacial bonding is conducive to epitaxy, at least at room temperature, without the tendency for the formation of interfacial compounds. The lack of a LEED pattern for Ge deposited on the Fe at room temperature was expected, since Ge deposited on single crystal Ge at room temperature is also amorphous. Development of only a partial LEED pattern upon heating to 450°C is inconclusive. Further experiments will be done to determine whether Ge can be grown epitaxially on clean crystallized Fe. The availability of ESCA in the same chamber will allow measurements to be made of any Fe diffusion through the Ge layer, also.

2.2 Grain Boundary Passivation

In previous reports, we described a series of experiments aimed at achieving an understanding of the electronic properties of grain boundaries in polycrystal GaAs. The conclusion of these experiments is that a majority of grain boundaries are not harmful to solar cell performance. The behavior of the remaining few, however, is sufficient to reduce conversion efficiencies to below useful values. At the grain boundary, the density of dangling bonds is sufficiently high to allow a two dimensional metallic delocalization of the trapped carriers. When an electrically active grain boundary traverses the junction, the result is a conducting shunt which is somewhat protected by the depletion region surrounding the grain boundary.

In the initial stages of this program, it was assumed that the different problems associated with grain boundaries would be subject to different cures and the trade-offs between these cures would place fundamental limits on polycrystal solar cell performance. It is clear from the results of the first two years of this program that this is not the case and that should it be possible to remove the grain boundary dangling bonds from the bandgap, all aspects of solar cell performance would be improved simultaneously. We have begun, this quarter, to explore chemical passivation of grain boundaries.

Workers at Bell Laboratories have reported an improvement in the performance (in particular, the open circuit voltage) of GaAs electrochemical and polycrystal Schottky barrier solar cells after a "ruthenium treatment". The treatment consisted of dipping the GaAs into a dilute solution of RuCl_3 and apparently adsorbing Ru^{3+} ions on the surface of the GaAs. In order to investigate the effects of this treatment on the band structure of polycrystal GaAs in the vicinity of grain boundaries, we carried out a series of measurements on polycrystal GaAs grown by MBE on Vistal and on Mo substrates. By using both insulating and conducting substrates, we were able to measure both majority carrier and junction properties.

The current-voltage characteristics before and after Ru treatment of the GaAs on Vistal (using alloyed Au-Ge contacts) are shown in Fig. 2.1 and of Au-GaAs-Mo Schottky barriers in Fig. 2.2. The treatment resulted in a large decrease in the bulk resistivity of the polycrystal GaAs on Vistal but no change in the I-V characteristics of the Schottky barriers. Efforts are continuing to isolate the mechanisms by which adsorption of Ru^{3+} increases the open circuit voltage of polycrystal GaAs Schottky barrier solar cells. The work will be expanded to include other possible passivants.

Fig. 2.1. Conductivity of polycrystal GaAs films on Vistol substrates before (-----) and after (——) Ru treatment.

ERC41020.26TPR

Fig. 2.2. Dark I-V characteristics of Au Schottky barriers to polycrystalline GaAs on Mo substrates before (—) and after (-----) Ru treatment.

3.0 CORNELL UNIVERSITY

3.1 SIMS

Work on the SIMS characterization of solar cell materials during the quarter were directed in two areas: (1) improvement of the detectability of important poor sensitivity elements through molecular detection, and (2) set up of an increased sensitivity imaging system.

Group IVA elements generally have poor sensitivity which is explained qualitatively by their ambiguous valence. In many cases, we have found the sensitivity for these elements can be improved by monitoring a molecular species which contains the elemental species in question. Halide implants of Ge and Si were profiled and the GeX^+ or SiX^+ and X^+ signals were monitored ($\text{X} = \text{F}, \text{Cl}$). The SiF^+ signal was approximately four times that of F^+ and the GeCl^+ signal was comparable to the Cl^+ signal. We feel that it may now be possible to detect both Si and Ge in GaAs at lower levels by using the appropriate halide primary beam, i.e., Si detection should be improved with a F^+ beam while a Cl^+ beam for Ge detection may produce GeCl^+ signals in a "cleaner" mass range. (Ge isotopes are close to both the Ga and As masses. It is suspected that GaCl^+ and AsCl^+ will be much smaller than Ga^+ and As^+ signals implying better GeCl^+ detectability than Ge^+ detectability.)

An intensifying T.V. camera has been added to the imaging section of the IMS-300. A computer digitizing and manipulation interface allows for image integration. Initial results show a total image signal of 20 Hz can be imaged. While this is an improvement over the imaging possible with electron film methods, the most important contribution is the experimental ease now possible for obtaining low intensity images. This system is expected to have a large impact on the imaging of segregation of impurities to grain boundaries in polycrystalline GaAs epilayers, as previously it was difficult

to image all species which might segregate to the boundary. The new system has been found to reduce the time of this type of study by a factor of 100.

3.2 Scanning Light Microscopy

We have made considerable progress toward measuring minority carrier diffusion lengths in polycrystalline GaAs and have determined diffusion lengths in a polycrystalline specimen designated CF-6.

The technique that we use consists of illuminating a Schottky barrier on the sample with a 1 μm diameter spot of monochromatic light in the SLM and measuring the resulting photocurrent as a function of reverse bias of the barrier. The metal-semiconductor interface band structure is diagrammed in Fig. 3.1. The $1/\alpha$ absorption depth remains constant for the wavelength of illuminating radiation used (approximately 0.8 μm at 799 nm and 0.2 μm at 633 nm). The depletion width of the barrier, w (approximately 0.3 μm), increases with increasing reverse bias. Any electron-hole pairs generated by the light within w or within a diffusion length of w will contribute to the measured photocurrent, assuming negligible recombination takes place. The change in photocurrent with w is given by

$$J_p = K[1 - \exp(-\alpha w)/(1 + \alpha L_p)] \quad (1)$$

where K is a constant involving the incident photon flux and the transmittance of the Schottky metal film, α is the absorption coefficient of GaAs for the wavelength used, and L_p is the minority carrier diffusion length. By normalizing J_p to the zero-bias photocurrent, K can be eliminated, such that

$$I_{\text{norm}} = [1 + \alpha L_p - \exp(-\alpha w)]/[1 + \alpha L_p - \exp(-\alpha w_0)] \quad (2)$$

Fig. 3.1. Band structure at metal-semiconductor interface.

where w_0 is the zero-bias depletion width. Knowing α and measuring w using C-V techniques, one can calculate and plot I_{norm} for various values of L_p . By fitting measured values of I_{norm} to these curves, L_p can be determined. Our results of this are shown in Fig. 3.2.

The sample that we have studied so far, CF-6, is a small piece of a polycrystalline MBE specimen supplied by Rockwell (MBA-164). Originally this sample had an array of Al Schottky dots evaporated onto the surface. We removed these dots and deposited our own semitransparent Au dot matrix. From C-V measurements we found the doping density to be 3.4×10^{16} donors cm^{-3} and the barrier height to be 0.95 volts.

According to our measurements, the diffusion length is not constant throughout the sample. The data of Fig. 3.2 is for three separate arbitrary points on the sample. At one point L_p is $0.16 \mu\text{m}$ and at the other two L_p is $0.44 \mu\text{m}$. These measurements were made using the 799 nm line from a Kr ion laser. At this wavelength, α is $1.2 \times 10^4 \text{ cm}^{-1}$.

Further study to determine how the diffusion length changes at a grain boundary has resulted in the data plotted in Fig. 3.3. The reflectance data shows the position of the grain boundary near the center of the scan. The slightly smaller peak to the right is caused by a defect in the specimen and Schottky layer. The point by point diffusion length plot shows the diffusion length falling from a value of about $0.4 \mu\text{m}$ in one crystallite to a value near zero at the grain boundary and remaining near zero in the other crystallite. This behavior is consistent for the length of the grain boundary under the Schottky layer. The data shown in Fig. 3.3 was taken using the 633 nm HeNe laser line for which α is $4.4 \times 10^4 \text{ cm}^{-1}$. The same scan using 799 nm light shows similar results but with some significant differences which we are presently investigating.

3.3 DLTS

The technique of deep level transient spectroscopy has been applied to grain boundaries by using the rectifying grain boundary itself as a DLTS

Fig. 3.2 Photocurrent vs. reverse bias demonstrating effects of diffusion length.

Fig. 3.3. Variation of the diffusion length in the vicinity of a grain boundary.

capacitor. In applying these techniques to various samples, we noticed the changes in the capacitance of the grain boundary after electrical or optical excitation were not a significant fraction of the zero-bias capacitance of the sample. One would expect that since the capacitance of the grain boundary is due to the occupied grain boundary states, that if the occupation of these states is changed by some excitation, the capacitance should change by some value comparable to the zero-bias value. By using a different pulsing technique which fills the grain boundary states more efficiently, we have been able to observe the expected changes in the capacitance.

The charge on a grain boundary is not constant under applied bias. With applied bias, states which are empty at equilibrium can fill. (A consequence of this is the breakdown voltage is greater than $4\phi_B$ where ϕ_B is the barrier height.) When the applied bias is removed, the grain boundary and surrounding depletion regions are not in thermal equilibrium, as shown in Fig. 3.4. We can monitor the decay of the trapped carriers as a function of temperature and produce a DLTS spectrum.

When this is done, the capacitance levels change by as much as forty percent. At temperatures low enough to freeze the electrons in the boundary the capacitance will stay at the non-equilibrium value. The difference between the equilibrium and the non-equilibrium value will give the amount of charge added to the boundary.

$$Q_{\text{Added}} = q \epsilon A N_d (1/C_{\text{equilib.}} - 1/C_{\text{nonequilib.}}) \quad (3)$$

Assuming one can saturate the states in the boundary, the total boundary states will be given by

$$N_T = \epsilon A N_d / C_{\text{nonequilib.}} \quad (4)$$

Band diagram of grain boundary during pulsing

where N_T is in units of cm^{-2} , and C is the capacitance per unit area.

We now calculate the manner in which the non-equilibrium capacitance decays back to equilibrium. The capacitance of a grain boundary barrier can be expressed as

$$C = \frac{1}{2} \sqrt{\frac{q\epsilon(N_D - N_A)}{2V_b}} \quad (5)$$

where

V_b = barrier height in volts,

$N_T = 2N_D w = 2\sqrt{(N_D - N_A)2\epsilon V_b/q}$, and

$$V_b = \frac{N_T^2}{4[2\epsilon(N_D - N_A)]} .$$

N_T decays back to equilibrium as

$$N_T(t) = N_T(o)(1 + A(V)e^{-e_n t}) , \quad (6)$$

where $N_T(o)$ is the number of traps occupied at equilibrium and $A(V)$ is the filling constant for addition of traps. This filling constant is a function of the voltage pulse applied to the grain boundary, and e_n is the emission rate for electrons from the trap. (We assume an n-type semiconductor and a single majority carrier trap.) Consequently,

$$C = \frac{1}{2} \sqrt{\frac{q\epsilon(N_D - N_A)}{2V_b(1 + A(V)e^{-e_n t})^2}} . \quad (7)$$

In particular, if we excite the grain boundary such that $A(V) \ll 1$, then

$$C \cong C_0 [1 - A(V) e^{-ent}]. \quad (8)$$

This means that the DLTS analysis is the same as for normal DLTS for small perturbations.

A particularly simple scan for one of these GaAs grain boundary diodes is shown in Fig. 3.5. The material is bulk GaAs obtained from Crystal Specialties. The emission constant is plotted as temperature in Fig. 3.6. Other samples show similar peaks but in all cases the peaks are distinct and sharp. The DLTS signal level versus voltage for this sample is plotted in Fig. 3.7. This graph shows a saturation for pulse voltages greater than 1 volt.

In conclusion, by using this voltage filling technique levels are seen which appear to correspond to the grain boundary core. These levels are distinct and sharp.

ERC41020.26T PR

Fig. 3.5 DLTS scan at grain boundary diode.

Fig. 3.6. DLTS signal vs. temperature at grain boundary diode.

Fig. 3.7. DLTS signal vs. voltage for grain boundary diode.

4.0 NORTH CAROLINA A&T STATE UNIVERSITY

4.1 Current Controlled LPE

The growth of GaAs by the CCLPE technique on graphite has not been successful. Only small randomly occurring GaAs crystallites have been observed on mechanically polished graphite substrates. Polycrystalline layers have been deposited from Ga melts onto chemically etched Mo substrates. However, these layers appear to be recrystallized Mo or a Mo-Ga compound, and very little As is observed by X-ray microprobe analysis.

Tin melts saturated with GaAs at 650°C were used for attempts at transient LPE growth on Mo substrates which had been electropolished (5% H₂SO₄ - 95% methanol). Growths from the saturated tin melt on single crystal GaAs substrates resulted in excellent epilayers. Hall measurements indicated carrier concentrations of approximately $7 \times 10^{18} \text{ cm}^{-3}$ in these single crystal epilayers.

The LPE growth attempts on Mo substrates from the tin melts resulted in only a few scattered dendrites with apparently incomplete wetting of the substrate. A large globule of Sn generally remained on the substrate after sliding the melt away. A photomicrograph of a dendritic growth region after etching in hot HCl is shown in Fig. 4.1. Tungsten probes applied to a dendritic growth region indicated a breakdown voltage of about one volt on a transistor curve tracer.

It is concluded that liquid phase epitaxial growth of polycrystalline GaAs upon the metallic substrates investigated (graphite and Mo) does not yield satisfactory semiconductor layers for material characterization or device fabrication. There are difficulties with (a) uniform coverage, (b) melt-substrate reaction, and (c) poor melt removal caused by the rough polycrystalline surface.

Fig. 4.1 Surface photomicrograph of GaAs epitaxial growth on Mo substrate from Sn melt.

4.2 Model of Grain Boundaries

We have developed a model to explain the changes in grain boundary characteristics after diffusion. The K atom which is introduced into the grain boundary during diffusion tends to serve as a simple donor at the interface due to its single weakly-held S^1 electron. The K^+ ion locally compensates those defect states at the interface thereby reducing the space charge depletion width W and the associated band bending $e\Phi_b$. However, due to the relatively short diffusion time, we expect a high concentration near the surface and decreasing inward from the surface along the grain boundary. The model used to explain the results is shown in Fig. 4.2.

From Fig. 4.2, it is evident that a majority carrier (b) approaching the grain boundary will experience the full depletion width W and band bending $e\Phi_b$; but, carriers (a) and (c) see a reduced depletion width and band bending due to the partial passivation. This model predicts: (1) a reduction in the rectifying properties of the grain boundary after diffusion due to a reduction in the blocking potential of the space charge region; (2) a reduction in the grain boundary resistance after diffusion; (3) a non-straight line fit to the activation energy versus inverse temperature due to the fact that not all carriers experience the same band bending at the grain boundary; and (4) a return to the nearly unpassivated grain boundary I-V characteristics after 20 μm is etched away.

4.3 Passivation of Grain Boundaries by Impurity Diffusion

This quarter we report the first encouraging results in our grain boundary passivation efforts. Our study of the basic physics of grain boundary interfaces suggests that the passivating impurity must satisfy certain basic requirements:

- (1) the impurity must serve as a donor at the interface,
- (2) the impurity must diffuse rapidly into the grain boundaries,
- (3) intragrain diffusion must remain small during the diffusion cycle,

Fig. 4.2 Model of partial passivation.

- (4) the passivating impurity must remain localized at the interface for long time stability requirements.

The alkaline metals seem to be excellent candidates for grain boundary diffusion.

For our passivation experiments, we selected potassium (K) as the diffusing impurity. Potassium has a substantially larger radius than Li. The larger atomic radius should eliminate intragrain diffusion of the element during the diffusion cycle. However, the impurity should still diffuse freely into and along the grain boundary due to the much higher diffusion constant associated with the grain boundary. In addition, the large atomic radius of the impurity should prohibit the out diffusion of the impurity atom from the grain boundary into the bulk thus making the anticipated passivation stable.

4.3.1 Passivation Experiments on a Single Grain Boundary

In the passivation process, a small amount of potassium is transferred in a nitrogen purged glove bag into a pyrex ampoule containing the GaAs sample (see Fig. 4.3). The ampoule is then evacuated with a molecular sieve trapped mechanical pump and a sputter ion-sublimation vacuum pump. After sealing, the ampoule is heated in a small oven for the diffusion cycle. The diffusion cycle is carried out at 140°C for 75 minutes. The sample is then removed and tin contacts alloyed in the configuration shown in Fig. 4.4. We used four contacts so that the outer two could be used to check the ohmic nature of the contacts.

The I-V characteristics of a single grain boundary (a) before diffusion, (b) after diffusion, and (c) after diffusion and after etching 20 μm is shown in Fig. 4.5. So that comparisons can be made more easily, we have replotted these three curves using the same set of axes as is shown in Fig. 4.6. Before diffusion, the bad grain boundary shows strong rectifying property due to a large band-bending ($\Phi_b = .87$ volts as determined later). After diffusion, the strong rectifying property of the grain boundary is

Fig. 4.3. Evacuated ampoule for potassium diffusion.
(1) Pyrex tube, (2) GaAs bicrystal, (3) control
sample, (4) potassium contained in small Pyrex tube.

Typical Sample Dimensions

Fig. 4.4 Sample dimensions and configuration for single grain boundary measurements.

ERC41020.26TPR

(a) before diffusion of K

(b) after diffusion of K

(c) after diffusion and after etching 20 μ m from the surface.

Fig. 4.5 I-V Characteristics of a single grain boundary

Fig. 4.6 I-V characteristics of a single grain boundary.

diminished. Even after etching away some 20 μm of the surface, we still find evidence of partial passivation. The fact that the passivation extends at least 20 μm is very important for thin film passivation.

A plot of the activation energy $k_B \ln(R_B T)$ versus $(1/T)$ before and after diffusion reveals some important grain boundary characteristics. First, before diffusion the experimental points are fitted quite well with a straight line of slope $e\Phi_b = .87 \text{ eV}$, (Fig. 4.7). Secondly, after diffusion there is a reduction in the grain boundary resistance, R_B . Lastly, we note that after diffusion the experimental points can no longer be fitted with a straight line.

4.3.2 I-V and C-V Measurements on Polycrystal GaAs Grain Boundaries

The filamentary polycrystal GaAs samples are being characterized by current-voltage and capacitance-voltage measurements. The latter measurements are being investigated as a more convenient method of determining the barrier height or band bending associated with a grain boundary before and after the diffusion of a passivation impurity. The technique previously used was a measurement of the low voltage ($< kT/q$) resistance of a grain boundary as a function of temperature.

Several factors enter into the measurement of the capacitance-voltage characteristic of the grain boundary in a GaAs bicrystal. If the series bulk and contact resistance is significant compared to the capacitance reactance of the depletion region, then the capacitance determined from the capacitance meter will be in error. The capacitance meter indicates a capacitance C' which is related to the actual series capacitance C_s by

$$C' = \frac{C_s}{1 + \omega^2 C_s^2 R_s^2} \quad (9)$$

Fig. 4.7 Resistance versus inverse temperature for a single grain boundary.

where ω is the measurement frequency and R_s is the series resistance. Thus, R_s tends to cause the indicated capacitance to be less than the true capacitance.

In associating the observed capacitance with the depletion region of the grain boundary, the biased characteristic of this boundary must be examined. A biased grain boundary is shown in Fig. 4.8(b). The capacitance per unit area of the grain boundary can be written as

$$\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} = \frac{\ell_1}{\epsilon} + \frac{\ell_2}{\epsilon}$$

where $\ell_1 = \sqrt{\frac{2\epsilon(\Phi_{b1} + V_a)}{qN_1}}$, $\ell_2 = \sqrt{\frac{2\epsilon\Phi_{b2}}{qN_2}}$, and V_a is the bias assumed to be applied across the reverse-biased depletion region.

Therefore,

$$\frac{1}{C} = \left(\frac{2}{q\epsilon N_1} \right)^{\frac{1}{2}} \left[(\Phi_{b1} + V_a)^{\frac{1}{2}} + \left(\Phi_{b2} \frac{N_1}{N_2} \right)^{\frac{1}{2}} \right]. \quad (10)$$

If the grain boundary is symmetrical, e.g., $N_1 = N_2 = N_d$, and $\Phi_{b1} = \Phi_{b2} = \Phi_b$, then we can write

$$\left(\frac{1}{C} - \frac{1}{2C_0} \right)^2 = \frac{2}{q\epsilon N_d} (\Phi_b + V_a) \quad (11)$$

where C_0 is the measured capacitance at zero bias.

A plot of the left hand side of the above equation versus V_a should yield a straight line. The slope of the line can be used to obtain the donor density N_d , and the intercept yields the band bending Φ_b .

(a) Unbiased condition

(b) Biased condition

Fig. 4.8 Energy band diagram of bicrystal in region of grain boundary.

In order to select polycrystal GaAs material for subsequent grain boundary passivation studies, it is desirable to perform simple measurements upon the samples before proceeding with the processing. Many of the polycrystal wafers obtained from Morgan Semiconductor do not meet our specification of carrier concentration in the 10^{16} cm^{-3} range (n-type). Quite frequently the material sent to us is discovered to be semi-insulating, or more heavily doped than desired. Also, the grain boundary concentrations are subsequently found to be much higher than that observed in the sawed or lapped wafer surface.

The wafers and sawed silamentary GaAs samples are now being characterized by the breakdown voltage of tungsten probes, current-voltage and capacitance-voltage measurements. The breakdown voltage of the biased probes on a single grain gives an approximate value for the carrier concentration.

We have acquired some "scrap" GaAs wafers from Bell Laboratories. One of these wafers is polycrystalline, n-type, with "breakdown" voltages of probe contacts in the 40-50 volt range within single crystal grains. A portion of this wafer was cut into approximately $10 \times 1.2 \times 0.8$ mm filaments. One surface of the wafer was chemically-mechanically polished (Clorox-water) before cutting. Several tin dots were alloyed into each filamentary sample. Caro etching of the contacted samples revealed grain boundaries which were not observed in the lapped or polished surfaces.

Capacitance-voltage measurements were made on single grain boundaries in the above material. The cross-sectional areas were approximately 10^{-2} cm^2 . In most cases, the C-V data are fairly symmetric with respect to bias polarity. One result observed in most of the samples was that the capacitance does not decrease monotonically with increasing bias voltage, but achieves a minimum, then increases. This is illustrated in Fig. 4.9. The I-V characteristic of this sample obtained from a transistor curve tracer is shown in Fig. 4.10. The capacitance behavior is not understood, but may be caused by a diffusion capacitance associated with increased current across the grain boundary. These measurements were performed in the dark,

Fig. 4.9 Capacitance-voltage data for bicrystal grain boundary.
(Sample A12)

Fig. 4.10 Current-voltage characteristic of bicrystal grain boundary.
(Sample A12)

since both the C-V and I-V measurements indicated a sensitivity to room lighting.

A log I vs. log V plot of the current voltage data for grain boundary sample A12 is shown in Fig. 4.11. An $I = AV^n$ exponential relationship fitted to these data yields $n \cong 3.7$.

While the above types of measurements may not apply directly to the thin film GaAs solar cell goals, they are necessary for characterizing the results of grain boundary passivation experiments, and possibly may improve the understanding of the grain boundary interactions in solar cell device structures.

Fig. 4.11 Current-voltage data for bicrystal grain boundary.
(Sample A12)