425.
5-14-80

DR-1195

DOE/JPL/954847-79/6

PHASE 2 OF THE AUTOMATED ARRAY ASSEMBLY TASK OF THE
LOW-COST SILICON SOLAR ARRAY PROJECT

Technical Quarterly Report No. 5 for July 1–September 30, 1979

By
M. G. Coleman
R. A. Pryor
T. G. Sparks

Work Performed Under Contract No. NAS-7-100-954847

Motorola Inc.
Semiconductor Group
Phoenix, Arizona

MASTER

U.S. Department of Energy

Solar Energy

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency Thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

DISCLAIMER

"This book was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof."

This report has been reproduced directly from the best available copy.

Available from the National Technical Information Service, U. S. Department of Commerce, Springfield, Virginia 22161.

Price: Paper Copy \$6.00
Microfiche \$3.50

PHASE 2 OF THE AUTOMATED ARRAY ASSEMBLY TASK
OF THE LOW-COST SILICON SOLAR ARRAY PROJECT

TECHNICAL QUARTERLY REPORT NO. 5

1 JULY 1979 - 30 SEPTEMBER 1979

MOTOROLA REPORT NO. 2345/6

JPL CONTRACT NO. 954847

PREPARED BY

MOTOROLA INC. SEMICONDUCTOR GROUP
5005 EAST MCDOWELL ROAD
PHOENIX, ARIZONA 85005

M.G. COLEMAN, R.A. PRYOR, T.G. SPARKS

THE JPL LOW-COST SOLAR ARRAY PROJECT IS SPONSORED BY THE U. S. DEPARTMENT OF ENERGY AND FORMS PART OF THE SOLAR PHOTOVOLTAIC CONVERSION PROGRAM TO INITIATE A MAJOR EFFORT TOWARD THE DEVELOPMENT OF LOW-COST SOLAR ARRAYS. THIS WORK WAS PERFORMED FOR THE JET PROPULSION LABORATORY, CALIFORNIA INSTITUTE OF TECHNOLOGY BY AGREEMENT BETWEEN NASA AND DOE.

PROJECT NO. 2345

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

THIS PAGE
WAS INTENTIONALLY
LEFT BLANK

TABLE OF CONTENTS

<u>SECTION</u>	<u>TITLE</u>	<u>PAGE</u>
1.0	Summary	1
2.0	Introduction	2
3.0	Technical Discussion	4
3.1	Ion Implantation	4
3.2	Plasma ETching Processes	9
3.3	Plated Metallization	19
4.0	Conclusions	26
5.0	Recommendations	27
6.0	Current Problems	27
7.0	Work Plan Status	27
8.0	List of Action Items	27
9.0	Milestones	27

LIST OF FIGURES

<u>FIGURE NUMBER</u>	<u>TITLE</u>	<u>PAGE</u>
1	Major Peaks of PH_3 Source Ion Spectrum	6
2	Major Peaks of AsH_3 Source Ion Spectrum	7
3	Major Peaks of BF_3 Source Ion Spectrum	8
4	Plasma Etch Equipment Configurations (a) Baseline Process, (b) Parallel Plate Modification	13
5	Etch Mask Configuration	14
6	Line Definition from Random Gas Collisions and Accelerated Ions	15
7	Plasma Etching Equipment Configuration for the Simultaneous Etching of Both Sides of a Substrate	17

1.0 SUMMARY

In this report, ion implantation, metallization, and plasma pattern etching of silicon nitride tasks are highlighted. Experiments were performed to evaluate solar cells formed by simulated unanalyzed beam ion implantation, comparing these cells with analyzed beam implanted cells. Plasma patterning of silicon nitride with mechanical masks has been improved, primarily through equipment modifications. Finally, nickel and copper plating have been performed on solar cells, demonstrating feasibility of this base-metal system. The contract has been modified to delay the plasma silicon and texturing etching efforts to the next quarter.

2.0 INTRODUCTION

There is a high probability that flat plate solar photovoltaic modules will become a major source of electricity generation throughout most of the world, and that the silicon solar cell will be the preferred generating element. In order to provide a realistic framework on which to build an effective program of R&D and demonstration for silicon solar cell modules, a series of objectives has been established to lead to a 1986 goal of 50¢/peak watt. At this price, solar-generated electricity will be able to compete with electric power generated by any other means, provided the solar cell modules are sufficiently reliable (e.g., have a mean life of 20 years).

To reach the 1986 JPL goal will require several advancements: 1) a cheaper source of pure silicon, 2) a much more economical way of transforming the source silicon into large, thin, (essentially) single crystal substrates having a controlled geometry, 3) an economical, large module package that will protect the interconnected solar cells it contains for at least 20 years from degradation caused by exposure to the weather, 4) an automated process sequence that produces high efficiency, reliable, cheap solar cells, tests them, interconnects them, and encapsulates them, and 5) a large market, of the order of 500 Mw/year.

When the JPL/ERDA LSSA Project started, the Motorola Solar Energy R&D Department participated in the Phase I of the Automated Array Assembly Task. The Phase I study identified a few potentially powerful process sequences for silicon solar cell production, and experimentally verified the overall consistency of the process sequence. It concluded that no basic technological innovations were necessary for solar cell fabrication or encapsulation in order to meet the long range LSSA Project goals. Detailed economic analyses

were performed, based on today's technologies, and showed that it should be possible to meet the JPL cost projections for solar panels.

The overall conclusion of the Array Automated Assembly Task, Phase 1, was one of cautious optimism. The present program, for Phase 2, has as its objective the further development of specific process steps (in a particular, powerful process sequence) leading to a completely specified solar cell (and module) production process sequence. This sequence must be capable of a high degree of automation and control. A detailed economic analysis is a major part of the program to ensure that the most cost-effective approach is taken.

During the first part of the Phase II program, feasibility of the process sequence and its individual process steps were confirmed. This, the second part of the Phase II program, is concerned with specification of process control parameters and limits which will allow progress toward automation of the process sequence. The main objective of this contract is sufficient process control limit definition to permit advanced equipment prototypes to be designed for incorporation into an advanced pilot line facility.

3.0 TECHNICAL DISCUSSION

3.1 ION IMPLANTATION

Ion implantation equipment which is commercially available today is not capable of being incorporated into a process sequence which can meet the 1986 DOE goal of \$0.70/peak watt (1980 dollars). There are several factors which limit today's implanters. First, the throughput of cells in today's machines is too low, being limited both by low ion beam currents and by mechanical transport mechanisms. Second, today's machines are very complex, resulting in three specific problems: (1) high cost, (2) large size, and (3) extensive maintenance. Restated, the cost per machine is far too high for the throughput rate of the equipment, while the large size and low throughput require significant additional capital investment for building floorspace.

Two major areas of cost reduction are available for ion implantation. First, major increases in ion beam current levels are necessary to make ion implantation a viable long range solar cell manufacturing technology. (Increases of more than an order of magnitude, to at least 100 mA, are required.) In addition, reduction of equipment cost is required to ensure that ion implantation is a preferred technology for future solar cell high volume manufacturing. If successful, these innovations would ensure that ion implantation will be the favored long range process for both p-n junction and BSF formation. A new machine design philosophy, however, is required to achieve these objectives.

One of the major factors now limiting ion beam current (and throughput) is the requirement of mass analysis of the ion beam. In general, any ion beam will contain all of the possible molecular and atomic species which can be formed from the source material. In addition, the ion beam may have foreign species from the source chamber, vacuum walls, or pump oil. In order to implant only one atomic or molecular specie, the beam is mass analyzed to eliminate all the undesired species.

Mass analysis is commonly performed by accelerating the ion beam, and then changing the direction of the beam by passing it through a magnetic field. Ions which are too heavy are not bent enough, while ions which are too light are bent beyond the desired direction. Only ions with the specifically desired mass can pass through the analyzer. By changing the field strength of the analyzing magnet, the desired specie can be chosen. Mass analyzed spectra for three source gases, phosphine (PH_3), arsine (AsH_3), and boron trifluoride (BF_3), are presented in Figures 1 through 3, respectively.

The mass analysis process creates a non-focused diverging ion beam. Following analysis, thus, the beam is normally focused by magnetic fields to the desired beam geometry. While this is suitable for small beam currents, at high beam currents the beam becomes self-shielding from the magnetic fields, requiring greater complexity of equipment.

The equipment components for mass analysis and beam focusing are both large and expensive, major factors in the total cost and floorspace requirements of present equipment. If mass analysis is not, in fact, required for ion implanted solar cells, the equipment can be greatly simplified. Such a simplification would be highly desirable from a cost stand-point.

A series of experiments to investigate the feasibility of utilizing an unanalyzed beam has been initiated. For these experiments, all of the major components of the ion beam, as identified in the spectra of Figures 1 through 3, are implanted into the cell in proportion to their relative intensities in the spectra. This, in effect, simulates an unanalyzed beam implantation from the gaseous sources. It is not a full simulation, however, since trace components of the beam are ignored. However, if high quality solar cells can be fabricated from the present experiments, the potential feasibility of an unanalyzed beam machine utilizing gaseous sources can be established. The experiments, thus, while not sufficient, provide necessary information for the utilization of unanalyzed ion beams for solar cell fabrication.

FIGURE 1
MAJOR PEAKS OF PH₃ SOURCE ION SPECTRUM

FIGURE 2
MAJOR PEAKS OF AsH_3 SOURCE ION SPECTRUM

FIGURE 3
MAJOR PEAKS OF BF_3 SOURCE ION SPECTRUM

In these simulations, the major ionic species present in the ion source are implanted in proportion to their relative concentrations in the source mass spectrum. Different isotopes of the same species are not implanted. The species implanted are identified in Table 1 for each source. Groups of wafers for fabricating solar cells are divided such that one half of each lot received only the analyzed species component of the ion beam while the other half received the simulated unanalyzed implant.

Cells have now been completed for both the arsine and phosphine sources. Data for specific cells made from the analyzed and simulated unanalyzed implants are shown in Table 2. For these two types of implants, no statistical difference can be observed for the arsine and phosphine sources. For arsenic and phosphorus doping, thus, no deleterious effects can be seen from the implantation of hydrogenated ions.

Experiments are continuing with implants of boron from a boron trifluoride (BF_3) source. The results of these experiments will be presented in a future report.

3.2 PLASMA ETCHING PROCESSES

In the process sequence under development for this contract, a silicon nitride layer deposited on the surface of the solar cell must be etched away in the configuration of the desired metal contact pattern. This patterning of the silicon nitride has been achieved by use of a plasma etching technique.

A baseline process was established and previously reported for the plasma patterning process. Further, it has been applied to textured surface solar cells. This technology is aimed at selectively and simultaneously etching ohmic contact patterns into the silicon nitride on both sides of a silicon substrate without significantly etching the silicon surface beneath these ohmic contacts. It is, of course, desirable to pattern both sides simultaneously in

TABLE 1

SIMULATED UNANALYZED ION BEAM IMPLANTS

GAS SOURCE	PH_3	AsH_3	BF_3
Primary Species (Control)	$\text{P}^{31} (+1)$	$\text{As}^{75} (+1)$	$\text{B}^{11} (+1)$
"Unanalyzed" Species	$\text{P}^{31} (+1)$ $\text{P}^{31} (+2)$ $\text{P}_2^{31} (+1)$ $\text{H}_2 (+1)$	$\text{As}^{75} (+1)$ $\text{As}^{75} (+2)$ $\text{As}_2^{75} (+1)$ $\text{H}_2 (+1)$	$\text{B}^{11} (+1)$ $\text{F}^{19} (+1)$ $\text{BF}^{30} (+1)$ $\text{BF}_2^{49} (+1)$

TABLE 2

CHARACTERISTICS OF SELECTED ION IMPLANTED SOLAR
CELLS FABRICATED UTILIZING ANALYZED AND SIMULATED
UNANALYZED ION BEAMS. (NON-OPTIMIZED PROCESS)

	I_{SC} (A)	V_{OC} (V)	F.F. (%)
Arsine (AsH_3) Source			
As^{75} (+1)	1.335	0.575	71.2
Unanalyzed	1.375	0.585	73.7
Phosphine (PH_3) Source			
P^{31} (+1)	1.325	0.582	74.7
Unanalyzed	1.350	0.580	73.6

order to minimize the number of process steps and to maximize equipment throughput. In this way, front and back symmetry of the patterns can be readily achieved without the necessity of realignment to an existing pattern on one side.

Advancements in ion-enhanced plasma etching of the silicon nitride layer have been demonstrated. These advancements are the result of modifications in equipment configuration.

The baseline equipment configuration, figure 4A, has the cell on the RF powered electrode with the vacuum chamber walls as the ground electrode. This equipment has been modified to have a grounded electrode parallel to the power electrode, figure 4B. This is similar to the arrangement used for RF sputter etching, and in general increases the plasma potential and ion density (1). As expected, an increase in etch rate was observed; unexpectedly (but fortunately) a significant improvement in etch anisotropy also occurred. This etch anisotropy is evidenced by better dimensional replication of the mask in the nitride pattern.

To evaluate the improved etch anisotropy, a metal mask was placed over the cell separated from the surface by a spacer ring as in figure 5. The nitride was then etched with plasma conditions similar to these utilities for the baseline process. Various thicknesses of spacers were used with resulting separations of 0.005 to 0.020 inches. The maximum line definition lost (width increase) was 10% for the 0.020 inch separation. To obtain such results, an ion-enhanced etching mechanism (reactive ion etching) must predominate the process. As illustrated in Figure 6, random gas motion of unaccelerated ions and neutral species would cause etched lines several times larger than the mask opening, even without surface migration of absorbed neutral and ionic species. The accelerated ions, as assumed, would have paths essentially normal to the power electrode and possibly have a focusing effect at the narrow line opening in the mask.

(1) J. L. Vossen, Journal of the Electrochemical Society, Vol. 126, pg. 319 (February 1979).

FIGURE 4

PLASMA ETCH EQUIPMENT CONFIGURATIONS (A) BASELINE PROCESS, (B) PARALLEL PLATE MODIFICATION.

FIGURE 5
ETCH MASK CONFIGURATION

FIGURE 6
LINE DEFINITION FROM RANDOM GAS COLLISIONS
AND ACCELERATED IONS.

This effect has been observed in various ion sources (2), and could explain the etched lines being narrower than the mask openings when the mask is in direct contact with the surface.

Of major significance is the fact that the required pattern can be etched without intimate contact between the mask and cell surface. This implies that a double sided process is feasible and may be easily implemented. Also, the process can now be applied successfully to sheet substrates which may be less flat (and more fragile) than as-sawed, single crystal material.

The plasma reactor was further modified by adding another grounded electrode, and changing the power electrode to allow the substrate to be held between two metal masks, as illustrated in Figure 7. Using this new configuration, the silicon nitride layer is etched in CF_4 with 8.5% O_2 , at 100 watts of RF power, and at a pressure of 0.1 Torr. The front side of the cell is placed face down on the bottom mask to obtain better resolution for the front pattern, while the back side has an approximately 0.010 inch spacing between the substrate and mask. The results were excellent, generating simultaneous patterns with sharp geometries equal to those previously generated one side at a time. Good solar cells were fabricated using these simultaneously formed front and back ohmic patterns.

The process of simultaneously forming front and back surface contact patterns in silicon nitride layers has now been fully demonstrated. The remaining efforts in this task will be to define the control parameters necessary to design production equipment. The most important of these is the mask geometry.

The masks used during these most recent experiments are thicker than those used in the reported single side baseline process, i.e. 12 mils versus about 5

(2) H. R. Kaufman, J. M. E. Harper, and J. J. Cuomo, Journal of Vacuum Science and Technology, Vol. 16, pg. 899 (May/June 1979).

FIGURE 7: PLASMA ETCHING EQUIPMENT CONFIGURATION FOR THE SIMULTANEOUS ETCHING OF BOTH SIDES OF A SUBSTRATE.

mils. Thicker masks are required to support the substrate, but have a limitation in the line width which can be formed using common etching techniques. Linewidths on the 12 mil masks are 7-8 mils. Several methods are being investigated to permit producing masks with 2 mil openings in a 20-30 mil thick plate. At present this represents a major requirement in developing of a production-ready process.

A constrain of the current equipment design is the low gas flow rate, when operating in the ion-enhanced pressure region near 0.1 Torr. This flow rate is difficult to control, causing some process control variations. Accordingly, the equipment required additional changes to increase vacuum pumping speed. After some modification, an improvement was noted in maintaining stable gas flows in the $3 \text{ cm}^3/\text{minute}$ range. However, this is still not totally adequate for a reproducible, efficient process.

Another limitation of the current process is what can be generically called "wall effects". These include both vacuum variations and ion recombination effects due to the chamber's size and electrical interactions, since the chamber is itself an electrode at ground potential. "Wall effects" of the current equipment physically limit the size of substrates that can be uniformly etched, the usable pressure range, and the etch rate. These effects should be reduced by utilizing a more suitable equipment configuration; to this end, a unit designed as a parallel-plate development system has been obtained as a replacement for the unit used for experiments to date.

The new unit uses a Pyrex bell jar for the vacuum chamber; this eliminates the conductive ground surface near the electrodes. It also has a triple electrode configuration - an RF power electrode between two ground electrode plates, with gas inlets in all three. This is easily adaptable to simultaneous front and back

pattern etching. The system's design allows higher pumping speeds of reactive gases and a lower residual gas level of 10^{-4} Torr. Also, larger rectangular electrodes, 4" x 10", offer the capability of handling ribbon substrates. Experimentation in this new unit are continuing.

3.3 PLATED METALLIZATION

Several developments in plated metallization are being studied simultaneously for this contract. Using the palladium-nickel-solder metal system developed under JPL Contract Number 954689 as a baseline process, new procedures are being generated to substitute copper for solder as the conductive layer and to eliminate the use of electroless palladium for the silicon contact layer.

Copper plating may provide the most cost effective solar cell conductor available. However, as discussed in previous reports, the use of a copper layer requires an effective barrier metal to prevent copper diffusion into the silicon. From both theoretical and practical standpoints, nickel is the ideal, cost-effective barrier. Therefore, the nickel layer in the baseline palladium-nickel-solder (PNS) process must be retained in some form.

In the past, experiments attempting to plate electroless nickel directly to silicon using the usual ammonia-based nickel chloride bath have yielded inconsistent, and therefore unsuccessful, results. In some instances, excellent bond strength and contact resistance would be obtained, while in some others, contact strength would be totally inadequate. The primary reason for inconsistent contact performance was a tendency for the plating bath to produce an oxide interface layer on the silicon surface faster than it produced a plated nickel layer. This oxide interfacial layer prevented the effective (and controllable) nickel silicide formation needed for adherence.

The interfacial oxide problem was solved in the baseline (PNS) process by using immersion and electroless plated palladium layers, but the electroless palladium layer contributes a significant cost to the process. Experiments have been initiated to eliminate the electroless palladium plating step in the PNS process, using only an immersion palladium silicon surface preparation followed by an electroless nickel deposition. While this has been readily performed it has not yet resulted in consistently satisfactory nickel layer adhesion. It seems that the same oxidizing effects may be present whether the specified nickel solution is used on bare silicon or on silicon sparsely coated with palladium from an immersion palladium solution. Studies are underway to determine the reasons for unsatisfactory adhesion, and to eliminate the problem and obtain consistently strong nickel contacts.

The direct use of nickel and nickel-silicide ohmic contact layers is being re-evaluated. In fact, it has been discovered that consistently strong nickel contacts can be obtained after heat treatment of nickel layers formed directly on the silicon surface by electroplating. Apparently this is possible because of the differences between the behavior of the alkaline electroless nickel bath specified in the PNS process and the acid electrolytic nickel bath used in the present experiments. The nickel layer produced by the alkaline electroless bath is a nickel-phosphorus mixture, containing a few percent phosphorus, while the layer produced by the acid electrolytic bath is essentially pure nickel with no component of phosphorus. Moreover, in directly plating the nickel layer onto silicon with the electrolytic nickel process, there appears to be no tendency to form an interfacial oxide. Thus, the nickel is in intimate contact with the silicon surface. The result is to allow the controllable formation of a very adherent nickel-silicide layer (Ni_2Si) at very low temperatures ($250 - 300^\circ\text{C}$) and in time intervals of 15 - 60 minutes.

Experiments were conducted using a commercial electrolytic nickel bath. A formulation based on nickel sulfamate was chosen because this chemistry is widely recognized as providing nickel deposits with very low internal stress. Low stress is important for building reasonable deposit thickness without generating adhesion problems before nickel silicide formation and for not imparting stress to the silicon crystal lattice near the junction (which could degrade current-voltage characteristics of a solar cell).

The electrolytic nickel plating solutions were prepared from nickel sulfamate solutions manufactured by Allied-Kelite of Des Plaines, Illinois. Instructions for preparing and using the plating solutions were obtained from technical data sheets for the "Barrett Sulfamate Nickel Plating Process, Type SN". The basic formula for the Barrett SN solution is 76.5 g/l of nickel metal in the form of nickel sulfamate plus 30 g/l of boric acid. The nickel metal content is supplied by Barrett Sulfamate Nickel Replenisher Solution, Type SNR-24, which contains 180 g/l of nickel metal. Other solution additives such as an anode corrosion chemical (Barrett Additive "A", 3 g/l) and an anti-pit agent (Barrett SNAP, 0.4 g/l) may be used (but were not used for most of the experimental studies). Optimum operating parameters given for the Barrett SN process include a bath temperature of 49°C, solution pH of 4.0, tank voltage between 6 and 12 volts, and cathode current density between 10 and 20 mA/cm². Typical 3 inch diameter solar cells with patterned front metal and solid back metal have an exposed area of about 50 cm². Therefore, cathode currents of about 0.5 to 1.0A were actually used.

Experiments with electrolytic nickel were performed with the plating solution contained in quartz beakers on top of magnetic stirring hotplates. A sulfur depolarized nickel anode was used. Plating voltage and current were supplied with a standard regulated power supply, and typical plating times ranged between 1 and 10 minutes.

It was determined that for at least some solar cell structures, nickel plating could be initiated directly on the exposed silicon front and back surfaces with no pretreatment other than a dilute hydrofluoric acid (e.g., 10:1 H₂O:HF or 50:1 H₂O:HF) rinse to ensure oxide-free silicon surfaces. In performing the electrolytic nickel plating process, no tendency to form oxide interfaces between the silicon and nickel was observed. This is probably the major reason for the excellent adhesion obtained with nickel layers which have been deposited with this bath (and subsequently heat-treated). Such layers, after treatments of as little as 15 minutes at 300°C, have passed the requirement that vertical pull-test failure occur by silicon substrate fracture. Moreover, the process of applying the nickel layer and forming the nickel silicide contact does not degrade solar cell electrical performance.

There are, however, some precautions to be noted before the successful production-ready development of electrolytically plated nickel contacts is completed. First, the plating process is dependent on solar cell structure since electrolytic plating performance depends very much on silicon surface conductivity. Therefore, cells with both a front surface diffusion and a back surface enhancement will adapt more readily to the electrolytic process than cells with no back surface layer. Secondly, electrolytic processing requires electrical contact to the solar cell so that it may be made cathodic. The proper fixturing required to make effective electrical contact to the bare silicon of the solar cell, and yet not shadow the cell or rob current from the cell, is not a trivial design problem and may require a fair amount of engineering development.

Consideration of the electrolytic plating process will continue in future months, along with additional work in re-evaluating the use of electroless nickel formulations on bare silicon and silicon prepared by using the immersion palladium plating step of the baseline PNS process.

In addition to being necessary as a barrier to copper, nickel serves an additional function for copper plating of solar cell metallizations. The nickel layer increases surface conductivity of the cell contact areas, so that, once a nickel layer is present, even though it has only moderate conductivity itself, it expedites the subsequent uniform electroplating of additional layers of metal. Major requirements for obtaining a satisfactory copper layer are design of the fixturing for making electrical contact to the cell while plating, and the choice of the electrolytic copper plating solution chemistry.

In experiments to date, electrical connections to the external power supply (providing electrolytic bias) for copper plating were made in the same fashion as those described for electrolytic nickel plating. That is, fixturing was employed which was as simple as an alligator clip, or as elaborate as specially constructed holders consisting of copper rings and contacts mounted in teflon handles. Of course, making electrical contact to the nickel for copper plating is much easier than making contact to the silicon plate the nickel layer. The nickel layer guarantees more uniform current distribution across the surface of the cell and hence more uniform plating. In addition, the plating bath contact itself is more consistent because it is metal (fixture) to metal (solar cell nickel layer) rather than metal to silicon. Optimization of a plating contact fixture has not yet been attempted but should be a straightforward exercise in engineering design.

Choice of an electrolytic copper plating solution is less obvious. Initial copper plating experiments utilized a cyanide solution, such as for the Lea-Ronal* Q-Level Copper Plating Process. Such processes are known to provide highly efficient copper depositions with good throwing power. By providing good throwing power and uniformity of deposit, effects of the actual electrical contact fixturing, and position of the cell in the plating tank with respect to the anode, are subordinated.

*Lea-Ronal Inc., Freeport, New York 11520

There are, however, several difficulties with cyanide copper processes. One immediate problem is the safety requirement of a cyanide plating hood and drain which are separate from all other acid facilities. This means that the plating tanks and rinse baths must be separate from any pre-plating, acid cleaning facilities or any pre-copper plating solutions such as acid electrolytic nickel plating baths. Another problem with cyanide copper plated layers is the inherently high internal stress in the metal layer. Of the four widely used types of electrolytic copper solutions (sulfate, fluoborate, pyrophosphate, and cyanide), the cyanide solutions deposit layers with significantly more internal stress. Such stress can promote future delamination of plated copper layers as well as impart strain to the silicon lattice in the vicinity of the metallurgical p-n junction, and thus introduce fill factor degradations.

To circumvent cyanide problems, subsequent experiments were initiated with acid copper sulfate solutions. The first tests were made using the Lea-Ronal Copper Gleam PC bath which is advertised to provide a bright ductile copper deposit particularly suited to the needs of the printed circuit industry. This bath consists of copper sulfate (8-12 oz/gal), sulfuric acid (22-28 oz/gal), chloride ion (30-60 ppm), and a proprietary brightener (Lea-Ronal Copper Gleam PC, 0.4 - 0.6% vol.). The operating temperature range for this bath is 70-90°F. It was used at room temperature (within this range), proving successful in that it was capable of plating to the nickel layer on the solar cell, and of being operated in the same hood along side the electrolytic nickel plating solution.

Cells were prepared with nickel plated contacts using the electrolytic procedure previously described. Some of these cells were heat treated while others were not. Both types were then plated with electrolytic copper using the sulfate bath described above. After copper was plated, the cells were given

heat treatments for 30 minutes at 300°C and survived with no degradation in cell electrical characteristics. As discussed in previous reports, this temperature cycle should be sufficient to severely impact cell performance if no barrier is present to prevent copper diffusion into the silicon. As a control, cells were prepared by plating copper directly on the surface of the silicon with no intermediate nickel layer. When given the same thermal cycle, these cells degraded severely, resembling shunt resistances rather than solar cells. It is apparent that the electroplated nickel barrier layer is pin-hole free and performing its expressed function.

Anticipating that it may be desirable to reduce internal stress to a minimum in thickly plated copper layers, experiments are being initiated to study low stress copper plating solutions. An excellent reference (3) has been found which gives detailed measurements of the properties, such as stress, of deposits from numerous copper solutions. Those solutions providing the lowest measured stress deposits will be considered for further study under the present contract. The first studies are starting with low stress formulations of copper sulfate and sulfuric acid solutions. Results developed from these experiments will be discussed in future reports.

(3) V. A. Lamb, C. E. Johnson, and D. R. Valentine, Journal of the Electrochemical Society, 117, 291C, 1970.

4.0 CONCLUSIONS

Several conclusions can be reached from results obtained during this period.

1. An unanalyzed ion beam shows promise of being utilized to fabricate high quality solar cells; this would ensure implantation cost-effectiveness.
2. Simulation of unanalyzed ion implants from arsine and phosphine sources has resulted in solar cells statistically identical to those made with analyzed arsenic and phosphorus implants. Arsine and phosphine, thus, are potentially suitable sources for unanalyzed high beam current ion implantation for solar cells.
3. Plasma patterning of silicon nitride has been accomplished in the reactive ion etching mode with cell-mask separation as great as 20 mils (500 micrometers).
4. Modification of electrode geometries can be made to allow simultaneous plasma patterning of the Si_3N_4 layer on cell front and back surfaces. The process is now ready for precise specification of control and equipment parameters.
5. Electroplated nickel has been demonstrated to provide a silicon contact with high adherence after heat treatment to form nickel silicide. Electroplated nickel does not appear to experience the competing silicon oxidation mechanism previously seen in electroless plating of nickel. Electroplated nickel has the possibility, thus, of eliminating the need for the palladium interfacial layers utilized in Motorola's plated metal system.
6. Thermal stress tests have shown nickel to be a suitable barrier to copper penetration into silicon.

5.0 RECOMMENDATIONS

No specific recommendations can be made at this time.

6.0 CURRENT PROBLEMS

No current problems have been identified.

7.0 WORK PLAN STATUS

Work is progressing according to plan, as modified.

8.0 LIST OF ACTION ITEMS

No items requiring unusual action have come to light during this report period.

9.0 MILESTONES

Status of program is shown in the Milestone Chart.

[illegible]

Milestone Chart (Cont)

	1	2	3	4	5	6	7	8	9	10	11	12	13
	A	M	J	J	A	S	O	N	D	J	F	M	A
DOCUMENTATION													
1. Revised Program Plan		▲											
2. Program Integration Meetings	▲				▲				△				△
3. Program Review Meetings		▲		▲		▲		△		△		△	
4. JPL Workshops									△				
5. SAMICS Cost Analysis				▲				△					△
6. Monthly Technical Progress Report		▲	▲		▲	▲		△	△		△	△	
7. Quarterly Technical Progress Report				▲			▲			△			
8. Final Report (Draft)												△	
9. Final Report (Distribution)													△
10. Financial Management Report		▲	▲	▲	▲	▲	▲	△	△	△	△	△	△