05
3/1/82
(28)

(2)

MASTER

lb. 302

SERI/TR-9010-2-T1
(DE82006856)

POLKA DOT SOLAR CELL

Final Report for April 1, 1980—May 29, 1981

Work Performed Under Contract No. AC02-77CH00178

General Electric Company
Corporate Research and Development
Schenectady, New York

U.S. Department of Energy

Solar Energy

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency Thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

DISCLAIMER

"This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof."

This report has been reproduced directly from the best available copy.

Available from the National Technical Information Service, U. S. Department of Commerce, Springfield, Virginia 22161.

Price: Printed Copy A03
Microfiche A01

Codes are used for pricing all publications. The code is determined by the number of pages in the publication. Information pertaining to the pricing codes can be found in the current issues of the following publications, which are generally available in most libraries: *Energy Research Abstracts, (ERA)*; *Government Reports Announcements and Index (GRA and I)*; *Scientific and Technical Abstract Reports (STAR)*; and publication, NTIS-PR-360 available from (NTIS) at the above address.

POLKA DOT SOLAR CELL

Final Report

Subcontract No. XS-0-9010-2
under
Prime Contract No. EG-77-C-01-4042
Period Covered: 80 April 01 - 81 May 29

General Electric Company
Corporate Research and Development
Schenectady, New York

Prepared for the
U.S. Department of Energy
Solar Energy Research Institute
Golden, Colorado

TABLE OF CONTENTS

	Page
I Introduction	1
II Epitaxial Emitter Cell	
A. Introduction	2
B. Optimization Model	2
C. Dependence of Surface Recombination Velocity on Doping	12
D. Solution Growth of Si from Sn	12
E. Optimization of Epitaxial Growth	13
III As Implanted Front Junctions	
A. Front Junction Processing Experiments	25
B. PDC with As Implanted Front Junctions	27
IV Arsenic Diffusion from Sn – As Source	27
V Polka Dot Cell Process Development	29
References	32

LIST OF ILLUSTRATIONS

Figure		Page
1	Definition of symbols used for the modeling of the epitaxial cell	3
2a	Cell efficiency versus layer emitter thickness for $L_o = 116 \mu\text{m}$ and $R_s = 30 \text{ ohms/sq}$	4
2b	Open circuit voltage versus emitter thickness	5
2c	Short circuit current versus emitter thickness	5
3	Majority carrier density versus emitter thickness for constant sheet resistance	6
4a	Cell efficiency versus emitter thickness for $L_o = 116 \mu\text{m}$ and $R_s = 10 \text{ ohms}$	8
4b	Open circuit voltage versus emitter thickness	8
5a	Cell efficiency versus emitter thickness for $L_o = 35 \mu\text{m}$ and $R_s = 10 \text{ ohms/sq}$	9
5b	Open circuit voltage versus emitter thickness	9
6a	Cell efficiency versus emitter thickness for $L_o = 35 \mu\text{m}$ and $R_s = 30 \text{ ohms/sq}$	10
6b	Open circuit voltage versus emitter thickness	10
7a	Cell efficiency versus emitter thickness for $L_o = 35 \mu\text{m}$ and $R_s = 100 \text{ ohms/sq}$	11
7b	Open circuit voltage versus emitter thickness	11
8	Definition of normalized surface potential ν_s and trap location ν	12
9	Schematic diagram of epitaxial growth system	13
10	Log (EBIC signal) versus distance on a cleaved junction from sample LP35B.	14
11	QEBIC collection efficiency versus beam energy for sample LP35B	15
12	Sample LP14 showing early stages of nucleation and growth.	18
13	Schematic of growth morphology which could result in holes in the epitaxial film	18

14	EBIC and secondary images of LP35B	19
15	Optical micrograph and EBIC image of LP36A	20
16	EBIC line scan across LP35B	21
17	Electron beam collection efficiency versus beam energy for sample LP36B	22
18	Electron beam collection efficiency versus beam energy for sample LP26	23
19	Minority carrier lifetime determined by EBIC and/or QEBIC versus majority carrier density	24
20	SEM secondary electron image of epitaxial growth on a (100) surface	24
21	Electron beam collection efficiency versus beam energy for As implanted diodes annealed at 900 or 1000°C for 30 and 5 min. respectively.	26
22	Original cell design with interdigitated metal fingers making contact with the substrate and deep N ⁺ areas	29
23	First design modification to reduce the area covered by metallization	30
24	Second design modification which will further reduce the metal contact area and the length of junction edge	31

LIST OF TABLES

I	Summary of Epitaxial Samples	16
II	As Implanted Front Junctions	26
III	Arsenic Diffusion Experiments	28

I. INTRODUCTION

The Polka Dot Solar cell is a new cell geometry concept which is expected to achieve efficiencies approaching the theoretical limit of 22% for silicon under one sun terrestrial illumination, and higher values in concentrated sunlight. Fabrication can be accomplished by a simple, low-cost sequence, devoid of high-resolution alignment steps. The front surface can be planar, resulting in simplified encapsulation and increased reliability. The basic design and construction sequence for a Polka Dot cell is described in the contract proposal and will not be repeated here. The principal goals of this research program were to develop improved models for Polka Dot cell operation, undertake studies directed towards improved front junctions and to develop novel gettering methods for cell improvement. Most of the contract effort was directed towards improved and novel front junctions.

A model was developed for thick epitaxial layer front junctions with moderate doping levels. This structure has the potential advantage of higher open circuit voltages and/or smaller sheet resistance than a conventional heavily doped front junction. The modeling studies indicate that the optimum thickness would be $\sim 10 \mu\text{m}$ with a doping level $\sim 3 \times 10^{17} \text{ cm}^{-3}$ and passivated with an oxide to a surface recombination velocity less than 1000 cm/sec. Ignoring the substrate limitations, open circuit voltages of 740 mV at 1 sun are predicted. With state-of-the-art substrates, open circuit voltages of 680 mV are predicted. The principal reason such junctions have potential advantages are that the moderate doping avoids heavy doping effects. In order to achieve sheet resistances comparable to a thin junction, the junction must be thick. However, because the majority carrier mobility increases as the doping is decreased, the required increase in thickness is not as great as would be expected, based on the ratio of the doping levels of a conventional and $3 \times 10^{17} \text{ cm}^{-3}$ junction.

The thick epitaxial cell requires long diffusion lengths in the top junction (emitter). Liquid phase epitaxy of silicon, from liquid tin was selected to demonstrate the concept. High minority carrier lifetimes have been observed in such films, probably because of the gettering effect of the liquid tin bath. In addition, the moderate growth temperatures $\leq 900^\circ\text{C}$ are desirable to preserve the high lifetime of the substrate. Films of the required thickness with diffusion lengths $\sim 30 \mu\text{m}$ were obtained. Electron Beam Induced Conductivity (EBIC) measurements indicated that there is still some problem with lifetime uniformity in the films. Model calculations predict that the best films would produce cells with efficiencies $\sim 23\%$.

Arsenic implantation for front junction fabrication was investigated. Emphasis was on a newly proposed short high temperature annealing sequence which minimizes dopant clustering. The reported decrease in sheet resistance, for the short quench anneal was observed. As compared to a conventional anneal a slight decrease in short circuit current, as inferred from EBIC data, was observed. The increase in sheet conductance would probably more than compensate for the slight decrease in short circuit current, especially in concentrator cells. Because of lack of funds no attempt was made to fabricate cells with As implantation by this method.

Gettering of N⁺P cells by an Arsenic diffusion from a Tin-Arsenic source was investigated. Conditions suitable for achieving shallow diffused junctions by this technique were determined. Due to lack of reproducibility in the diagnostic measurements, no conclusive results were obtained.

A modified Polka Dot Cell process sequence for the contact structures was designed. These modifications consisted of reducing the metallization contact area to reduce the dark current contribution from the ohmic contacts. Cells were processed using this new process and mask design but no test results have been obtained.

II. EPITAXIAL EMITTER CELL

A. Introduction

A thick epitaxial emitter offers some interesting potential advantages compared to standard cell structures. The classic optimization for the front junction of a photovoltaic cell results in a very thin, heavily doped emitter. The heavy doping reduces the emitter lifetime, thereby degrading both the open circuit voltage and the short circuit current. With a thin emitter, the loss in short circuit current is minimal. It is expected that the very heavy doping will minimize the injection of minority carriers into the low lifetime region and hence losses in open circuit voltage will also be small. However, because of band gap narrowing, the injected minority carrier current is not reduced as much as expected, resulting in a loss of about 10% in open circuit voltage and efficiency when compared to the predictions ignoring band gap narrowing. An alternative approach is to maintain the emitter doping level below the region of significant band gap narrowing ($< 3 \times 10^{17}$) and increase the thickness to achieve similar useful sheet resistances of 10 to 100 ohms/sq. Because of the increase in mobility at lower dopings, reducing the doping from 10^{20} to 10^{17} cm $^{-3}$ requires only a factor of 100 increase in emitter thickness to maintain the same sheet resistance. If the diffusion length in the emitter is sufficiently long, and the surface is well passivated, such a front junction should permit open circuit voltages 0.75 volts. Actual cells would be limited by recombination in the substrate to 0.70 volts. For concentrator applications, a fully optimized cell might trade off front junction quality against emitter sheet resistance. Sheet resistance of 10 ohms/sq with open circuit voltages near 0.7 volts are projected.

Progress on the design and fabrication of such front junctions are described in the following three sections.

B. Optimization Model

The cell structure and definitions are shown in Figure 1. The forward current J_o of the diode is given by:

$$J_o = e \frac{n_i^2}{N_E} (\exp(\beta V) - 1) \frac{\exp(-W/L)[D_p/L - S_v] - \exp(W/L)[D_p/L + S_v]}{2[(S_v L/D_p) \sinh(W/L) + \cosh(W/L)]} + e \frac{n_i^2}{N_B} [\exp(\beta V) - 1] \frac{D_n}{L_s} \quad (1)$$

In this equation N_E and N_B are the emitter and substrate dopings, L and L_s are the emitter and substrate diffusion lengths, W is the emitter (top junction) depth, V is the forward junction voltage, D_p is the diffusion constant of the top layer, S_v is the surface recombination velocity of the top surface, n_i^2 is the pn product of the emitter in the first term and the substrate in the second term, and $\beta = e/kT$.

The second term is the diffusion length (L_s) limited recombination in the substrate. We assume the cell thickness is several diffusion lengths and ignore back field

Figure 1. Definition of symbols used for the modeling of the epitaxial cell.

effects. The first term is due to recombination at defects in the uniform top n-layer or at the surface. The minority carrier recombination current density into the top surface is by definition $S_v p$ where p is the minority carrier density. The sheet resistance of the top layer is

$$R_s = (e\mu_e NW)^{-1} \quad (2)$$

The pn product n_i^2 in equation (1) is assumed to include band gap narrowing effects. For the numerical examples we have used the experimental fit to Slotbooms⁽¹⁾ data for p type material. The form used is:

$$\frac{n_i^2}{n_{i0}} = \exp(\beta \Delta E_g^e)$$

$$\Delta E_g^e = 9mV[\ln(N/10^{17}) + \sqrt{[\ln(N/10^{17})]^2 + 0.5}] \quad (3)$$

This probably overestimates band gap narrowing for n-type material. However, since the optimum cell will have dopings less than 3×10^{17} , band gap narrowing is a small correction in the model in the region of interest. The diffusion length, L , in the top layer is assumed to be given by:

$$L^{-2} = \tau_o^{-1} + N C_N / D_p \quad (4)$$

where C_N is the Auger recombination coefficient and $L_o^2 = \tau_o D_p(o)$ an asymptotic value for lightly doped material. We regard the Auger coefficient as an empirical number characteristic of the present state of the silicon processing art rather than a fundamental value, as discussed in the project status report.

$C_N = 0.4 \times 10^{-31} \text{ cm}^{-6} \text{ sec}^{-1}$ is characteristic of most processed silicon although much smaller values have been reported and larger values have been observed on wafers as received from vendors before processing (see for example ref. 2). The short circuit current is calculated from the minority carrier collection probability given by

$$P(z) = \frac{\sinh(z/L) + (D_p/L S_v) \cosh(Z/L)}{\sinh(W/L) + (D_p/L_E S_v) \cosh(W/L)} \quad z < W \quad (5)$$

$$= \exp\left(\frac{W-z}{L}\right) \quad z > W$$

$P(z)$ is the probability that a minority carrier generated at a depth z is collected by the junction at depth W . This again assumes a uniform emitter diffusion length. The solar spectrum is based on a Table given by Thekaekara for AM1 conditions.⁽³⁾ The maximum short circuit current from this spectrum, assuming one electron-hole pair per photon is 39.2 mA/cm^2 . The absorption coefficients used are based on a tabulation given by Sah.⁽⁴⁾

For the optimization modeling all effects due to the substrate are ignored. For good quality substrates with diffusion lengths $> 100 \mu\text{m}$ the effect of recombination on the short circuit current is small. However, the effect on the open circuit voltage can be large. This will be considered later. A computer program was written to calculate the efficiency, short circuit current, open circuit voltage and fill factor of the epitaxial cells described by the above equations. In the normal mode the program calculates these parameters as a function of the top layer thickness, W , for a specified n-layer sheet resistance, R_s . Figures 2a-c show the result of this calculation for a sheet resistance of 30 ohms/square . Figure 3 shows directly the n-layer doping versus thickness for several sheet resistances. For large layer thicknesses the efficiency falls off rapidly because of the assumed $100 \mu\text{m}$ limit on the diffusion length. The efficiency at small thicknesses asymptotically approaches a nearly constant value of 22% for small values of surface recombination velocity. This limit is controlled by the assumed dependence of band gap narrowing on doping. For surface recombination velocities larger than 300 cm/sec the efficiency begins to fall rapidly. Surface recombination is even more important for deeper junctions. The n-layer thicknesses of interest for the epitaxial cell are in the range of 1 to $50 \mu\text{m}$. Here the efficiencies can significantly exceed those of conventional cells.

Figure 2a. Cell efficiency versus layer emitter thickness for $L_0 = 116 \mu\text{m}$ and $R_s = 30 \text{ ohms/sq}$.

Figure 2b. Open circuit voltage versus emitter thickness.

Figure 2c. Short circuit current versus emitter thickness.

Figure 3. Majority carrier density versus emitter thickness for constant sheet resistance.

Figures 2b and 2c show the open circuit voltage (V_{oc}) and the short circuit current J_{sc} separately. It can be seen that the peak efficiency is determined by a competition between the increasing open circuit voltage with emitter thickness and the decreasing short circuit current. Since the sheet resistance is fixed, increasing the emitter thickness decreases the importance of band gap narrowing, but increases the loss of photo-generated carriers by bulk recombination.

Cells of this type will be limited by the substrate contribution to the diode leakage prefactor J_o . Assuming present state of the art substrates with a diffusion length of $100\text{ }\mu\text{m}$ and doping of $2 \times 10^{17}\text{ cm}^{-3}$ the substrate contribution to J_o would be $2.4 \times 10^{-13}\text{ A/cm}^2$. This corresponds to a substrate limited open circuit voltage of 0.67 volts and a limiting AM1 efficiency of 22.5%. Hence there is a wide range of thicknesses, dopings and surface recombination velocities which will optimize the cell design for present state of the art substrates. However, if improved processing technology or materials technology is developed this technique provides a superior method to exploit such advantages. For a 30 ohm/square cell the optimum cell has emitter thicknesses in the range 2 to $20\text{ }\mu\text{m}$ and dopings of 10^{17} to $3 \times 10^{18}\text{ cm}^{-3}$. For the lighter doping, a surface recombination velocity $< 100\text{ cm/sec}$ is required while for the higher doping $S_v < 1000\text{ cm/sec}$ is sufficient. For limiting efficiencies of 23% heavily doped emitters $> 10^{19}$ and $\sim 1\text{ }\mu\text{m}$ thick are also possible. However, these would require a $S_v < 1000\text{ cm/sec}$. This would be much more difficult to achieve on such a heavily doped surface. As discussed in a following section, the minimum achievable surface recombination velocity is proportional to the doping density so that if the minimum S_v achievable at 10^{17} were 100 cm/sec then at 10^{19} the minimum S_v would be 10^4 .

Figures 4a and 4b show similar calculations for a 10 ohm/square top layer. There is an optimum design region for dopings of 2×10^{17} to $6 \times 10^{17}\text{ cm}^{-3}$ and thicknesses of 10 to $40\text{ }\mu\text{m}$. The maximum efficiency is 21% which is nearly the same as the substrate limited efficiency. In order to achieve this optimum efficiency, good control of doping, thickness, surface recombination velocity and lifetime will be required. Figures 5 through 7 show similar calculations for $L_o = 35\text{ }\mu\text{m}$.

Figure 4a. Cell efficiency versus emitter thickness for $L_o = 116\mu\text{m}$ and $R_s = 10$ ohms.

Figure 4b. Open circuit voltage versus emitter thickness.

Figure 5a. Cell efficiency versus emitter thickness for $L_0 = 35 \mu\text{m}$ and $R_s = 10$ ohms/sq.

Figure 5b. Open circuit voltage versus emitter thickness.

Figure 6a. Cell efficiency versus emitter thickness for $L_o = 35 \mu\text{m}$ and $R_s = 30 \text{ ohms/sq.}$

Figure 6b. Open circuit voltage versus emitter thickness.

Figure 7a. Cell efficiency versus emitter thickness for $L_0 = 35 \mu\text{m}$ and $R_s = 100 \text{ ohms/sq.}$

Figure 7b. Open circuit voltage versus emitter thickness.

C. Dependence of Surface Recombination Velocity on Doping.

The Hall-Shockley-Reed model of surface recombination can be expressed as:

$$S_v = \left(\frac{n_b + p_b}{2n_i} \right) \int_{-E_g/2}^{E_g/2} \frac{\sqrt{K_n K_p} N_T(v) dv}{[\cosh(v - U_o) + \cosh(u_s - U_o)]} \quad (6)$$

where n_b and p_b are the bulk electron and hole densities, $N_T(v)$ is the trap density at v in energy units, u_s is a surface potential parameter and $U_o = \ln(K_p/K_n)$. The definitions of u_s and v are indicated in Figure 8. v and u_s are potentials in units of kT/e . K_n and K_p are the capture rates for the surface states for electrons and holes respectively. Low level injection conditions are assumed.

Figure 8. Definition of normalized surface potential v_s and trap location v .

As has been made explicitly clear, $(n_b + p_b)$ factors completely out of the expression. For n-type silicon, $n_b + p_b = N$. If we assume that the trap parameters, K_n , K_p and $N_T(v)$ are independent of doping density then S_v is a function only of the doping level N and u_s . For large positive applied voltages to an MOS gate or large values of fixed positive charge in the top oxide layer, the surface Fermi level will be near the band edge and $u_s = \frac{1}{2}$ (band gap) $\frac{e}{kT}$. The Fermi level tends to limit near the band edge because of the high density of interface states in this region. Even for well processed interfaces with a low interface state density near mid gap the density near the band edges is much larger. Hence, if the density and characteristics of the interface states are independent of doping and if there are sufficient interface states near the band edges to limit the maximum surface potential, then the minimum achievable surface recombination velocity will be proportional to the doping. This argues for the selection of more lightly doped n-layers.

D. Solution Growth of Si from Sn

The epitaxial emitter cell described in the previous sections requires a thick ($\sim 10 \mu\text{m}$), moderately doped epitaxial emitter ($\sim 10^{17} \text{ cm}^{-3}$), with high minority carrier lifetime ($\sim 10 \mu\text{sec}$). Solution growth of Silicon from Tin was selected as a promising candidate for two principle reasons: 1) it is a low temperature process ($\sim 900^\circ\text{C}$ or lower) which would be compatible with preserving the substrate lifetime, 2) it has been demonstrated to produce high lifetime epitaxial layers.

Solution growth from liquid tin can produce high lifetime layers because tin is a getter for most heavy metals which could act as lifetime killers. During growth these

metals segregate into the tin bath. Previous work at General Electric⁽⁵⁻⁷⁾ demonstrated lifetimes of 2 to 10 μsec in moderately doped ($\sim 10^{15} - 10^{16}$) n-type silicon. This corresponds to diffusion lengths as large as 100 μm , which are what are required for the epitaxial cell.

A dip type of epitaxial deposition system was set up (Figure 9). All high temperature parts of the system were constructed of quartz. High purity (5N) tin was vacuum purified at 800°C. Some black condensate was observed to boil off the tin. This was analyzed by x-ray fluorescence and found to contain mercury. The 90g tin charge was etched in HCl and then vacuum baked a second time before use in the epitaxial system. The melt was always maintained in a stream of high purity H_2 purified using a palladium diffuser. The temperature was maintained to better than $\pm 1^\circ\text{C}$ long term stability and somewhat better short term stability using a standard furnace controller and Type K thermocouple. The temperature was monitored using a Type S thermocouple. Temperature uniformity in the Sn bath was checked using a thermocouple inside a quartz tube inserted in the Sn melt. The temperature variation from top to bottom of the bath was 0.5°C.

A typical growth procedure consisted of saturating the melt with high resistivity boron doped float zone silicon wafers, and stirring the melt during saturation. After saturation a substrate wafer was mounted on a quartz paddle using a quartz clip and carbon screw and inserted into the melt. The carbon screw never contacted the Sn melt. A high flow of H_2 (300 cc/min) was used to minimize contamination and oxidation of the wafer surface during insertion. The wafer was held above the melt for 3 minutes to reach thermal equilibrium. At this point the melt temperature was about 3°C above its saturation temperature. The wafer was then inserted into the melt and the temperature slowly raised to about 10°C above the saturation temperature, over a

Figure 9. Schematic diagram of epitaxial growth system.

30 minute period, while stirring the wafer in the melt at about 1 rpm. The direction of rotation was reversed to every 10 sec. to completely agitate the melt. At this point the temperature was ramped down at various rates. In some cases stirring was continued for 10 minutes to improve nucleation of the epitaxial film. After the desired growth period the wafer was removed and etched in aqua regia or hot HCl to remove small amounts of residual tin.

Just prior to epitaxial growth the wafers were cleaned in hot $\text{H}_2\text{O}_2\text{-H}_2\text{SO}_4$, rinsed in DI water, boiled in HNO_3 , rinsed in DI water etched in 50% HF, rinsed in DI water and spun dry.

The segregation coefficient for boron is high, and for As and other n-type dopants it is low, so the initial growth is p-type until all of the boron is depleted. Hence the boron dopant introduced by the saturation wafer results in only a very thin p-type epitaxial layer on the substrate. Even for melt back with more heavily boron doped wafers, the thickness of the initial p-type layer will be less than the melt back thickness.⁽⁷⁾ Because the surface is cleaner, melt back should give the best quality junctions.

E. Optimization of Epitaxial Growth

Two Electron Beam methods were used to determine the minority carrier diffusion lengths in the epitaxial layers. The first method required cleaving the junctions and mounting the chip edge normal the electron beam. Figure 10 shows a typical EBIC (Electron Beam Induced Conductivity) trace across the cleaved junction edge. As has

LP35B 1981-4-28

20 keV

Figure 10. Log (EBIC signal) versus distance on a cleaved junction from sample LP35B. Insert shows the location of the cleaved junction relative to the horizontal distance scale.

been shown by Van Roosbroeck⁽⁸⁾ the slope of the log of the signal versus distance from the junction depletion region edge is nearly linear and related to the diffusion length. Berz and Kuiken⁽⁹⁾ explicitly proved that this conclusion is independent of the generation volume. The slope is nearly independent of the surface recombination velocity and is approximately 0.5 decades per diffusion length. This assumes the surface recombination velocity is uniform across the edge. Our experience has been n-type free silicon surfaces rapidly reach a rather high and stable value of surface recombination velocity under electron bombardment, so this requirement is well satisfied. P-type surfaces tend to be unstable and often invert under bombardment, so this technique is much less useful for p-type material. The chips are typically mounted slightly off 90° as shown in Figure 10. This explains the rise in signal as the beam passes the top edge of the chip. The thickness of the epitaxial layer was also determined from these same line scans or EBIC images of the cleaved junction.

The second method used chips mounted with the top surface normal to the beam. In this method the absolute electron beam induced diode current was measured as a function of beam energy. This is the QEBIC (Quantative Electron Beam Induced Conductivity) method.^(10,11) Figure 11 shows a typical set of data for the same sample as Figure 10. The curves are based on a model assuming a uniformly doped epitaxial

Figure 11. QEBIC collection efficiency versus beam energy for sample LP35B.

layer of thickness W , a minority carrier diffusion length L_p , and a normalized surface recombination velocity $s = S_v/D_p$. The layer thickness W is determined independently from the cleaved junction images. The surface recombination velocity S_v is observed to be within a factor of 10 of the kinetic limit (7×10^6 cm/sec) as can be determined from the behavior at low beam energies. Higher beam energies are relatively insensitive to S_v , as can be seen in Figure 11. The surfaces were radiation damaged using the electron beam prior to measurement, to assure a large and stable surface recombination velocity. In samples where the diffusion length is larger than one half the layer thickness, the cleaved junction method is not useful. This is because the asymptotic region where $\log$ (EBIC signal) is almost linear in distance starts at about one diffusion length. Once the beam is more than halfway across the epitaxial layer width, recombination at the top surface begins to compete for carriers. This is the reason for the dip in signal near the top surface seen in Figure 10. Hence for samples with a diffusion length more than 0.5 of the layer thickness, the QBIC method was used. For samples such as the one of Figure 10, where the EBIC diffusion length was less than 0.4 of the layer thickness the EBIC and QBIC methods agreed. Comparing Figure 10 and 11 it can be seen that the two methods gave 15 and 17 μm respectively which is good agreement. The effect of the competing recombination at the top surface in the EBIC method tends to reduce the apparent diffusion length. This agrees with the difference between the two measurements in this case. Table I summarizes the growth conditions and results obtained. ΔT is the total temperature drop relative to the maximum temperature after melt back, ΔT_M is the melt back temperature difference, i.e. the difference between the saturation temperature and the temperature after melt back, W is the epitaxial layer thickness of the n-type epitaxial layer and Δt is the growth time. The temperature ramp is approximately linear, although for the

Table I
Summary of Epitaxial Samples

Run	ΔT °C	ΔT_M °C	$\Delta T/\Delta t$ °C/min	W μm	$W/\Delta t$ $\mu\text{m}/\text{min}$	L_p μm	Growth Area cm^2	ρ $\Omega\text{-cm}$	N_D cm^{-3}	τ μsec	
9	25	1.5	.24	30	.30	20	2.5	0.4	1.3×10^{16}	0.4	
10	34	0	.31	60	.55		2.5	0.4			
11	27	3.5	.26	50	.50		2.5				
12	27	4.5	.24	50	.45		2.5				
21	19	3	.14	40	.29	~15	2.5				incomplete nucleation
22	25	14	.27	47	.54	19	2.5	0.3	1.8×10^{16}	0.37	
23	33	10	.23	36	.25	18	2.5	0.18	3×10^{16}	0.37	holes in film
24	19	8	.17	25	.2	23	2.5				holes
25	38	3.5	.09	20	.05		2.5	0.1	10^{17}		holes in film
26	40	11.0	.66	43	.75	≥ 30	5	0.23	2.2×10^{16}	1.0	
27	55	8.5	.52	23	.22		5	0.16	4×10^{16}		holes
29	80	3.5	.31	52		17	5	0.22	2.2×10^{16}	0.3	
30	37	13	.05	50	.07	19	5	0.7	7×10^{15}	0.33	
31	32	9	.23	26	.19		5	0.026	10^{18}		0.37g Sb added
32	29	10	.26	29	.26	8	5	0.020	1.5×10^{16}	0.3	0.30g Sb added
33	49	10	.18	32	.11	18	5	0.6	8×10^{15}	0.3	New Sn
34	23	10	.13				5				holes
35	39	10	.11	35	.10	17	5				
36	93	11	.73	70	.55	30	5	0.6	8×10^{15}	0.8	

larger temperature drops the ramp rate dT/dt is as much as a factor of 2 smaller at the end of the growth period. L_p is the minority carrier diffusion length measured by EBIC and/or QEBIC, and ρ is the average film resistivity based on four point probe and the thickness W . The doping level N_D and the minority carrier lifetime τ are based on ρ and L_p assuming standard mobilities. Runs #13 through #20 are not included, because they were experiments directed towards improving the surface morphology by variations in melt back conditions, wafer cleaning, and furnace controller adjustments.

Generally the diffusion lengths determined by EBIC and QEBIC were 15 to 20 μm . In two cases diffusion lengths $\sim 30 \mu\text{m}$ were obtained. These two cases achieved the highest growth rates of 0.55 and 0.75 $\mu\text{m}/\text{min}$. Similar high growth rates were obtained on two other occasions however the junctions were very poor and reliable EBIC data could not be obtained.

In most cases the wafer was melted back about 10°C while stirring. This corresponds to a melt back distance of 5 to 10 μm . Observed deposition rates varied between 0.1 and 0.5 $\mu\text{m}/\text{min}$. As discussed by Baliga⁽⁶⁾ cooling rate should be proportional to growth rate since the Silicon surface is in quasi-equilibrium with the melt. However for the higher cooling rate there is a greater tendency to nucleate growth on the quartz paddle and to establish dendritic type of growth structures at the wafer edges. This consumes silicon, thereby reducing the growth rate. In some cases the growth surface was doubled by introducing two wafers into the melt. This reduced the growth rate by a factor of two as expected.

Typically small pieces of the wafers were scribed from the back and broken into chips of area $\sim 15\text{mm}^2$. Most of these chips had reverse leakages of 100 to 1000 μA at 1 volt and soft breakdowns at a few volts. In some cases the junctions were shorted. Forward characteristics could not be investigated because ohmic contacts to the moderately doped n and p surfaces were not provided. Examination of these junctions in the SEM, in the EBIC and secondary mode, indicated holes in the films and the possibility of Sn inclusion at the junction region. In general a slow growth rate produced smoother surfaces but tended to produce holes and inclusions. We believe this is due to poor nucleation and/or constitutional supercooling. Figure 12 shows the typical growth morphology observed after melt back and short growth times on (111) surfaces. As the growth proceeds there is the possibility of producing a trapped solvent region which cannot be replenished rapidly enough from the melt to maintain Si growth. (See Figure 13) This results in a Sn inclusion or a hole in the film. This type of growth instability is essentially constitution supercooling. At higher cooling rates the supersaturation of the melt is higher and nucleation at a larger number of sites is possible. Baliga has observed that the growth rate saturates at 1 $\mu\text{m}/\text{min}$. At this high growth rate the growth is kinetically controlled. In the kinetic region he did not observe Sn inclusions due to constitutional supercooling which can occur at slower growth rates.

At slow growth rates the growth process is controlled by diffusion of dissolved Si. Hence the rate of replenishment of dissolved Si into a cavity such as shown in Figure 13 will be very small and the cavity will be stable. At high growth rates the growth rate is controlled by migration and adsorption on the surface. In this case the excess Si concentration will tend to be maintained at a higher level in the cavity and

Figure 12. Sample LP14 showing early stages of nucleation and growth. Horizontal picture width = 2.2 mm.

Figure 13. Schematic of growth morphology which could result in holes in the epitaxial film.

the formation of inclusions and holes will be reduced. Figure 14 shows an SEM secondary and EBIC image of a sample grown at $0.1 \mu\text{m}/\text{min}$. The total layer thickness is $35 \mu\text{m}$. The EBIC image shows the holes as areas of higher gain because the beam penetration is much closer to the junction depletion region. At 20 keV the maximum electron range is about $4 \mu\text{m}$. Except for the holes, the film is quite uniform and the EBIC signal is uniform, indicating no other serious recombination defects in the film. Some low gain defects can be seen. The dark circle in the center is due to radiation damage from the electron beam and indicates some surface sensitivity of the EBIC signal to electron beam damage. This is the electron beam damage effect mentioned earlier. The slow growth rate films typically have surface ripples with a period of 1 mm and height $0.5 \mu\text{m}$.

Figure 14. Top: EBIC image of LP35B.
Bottom: Secondary image.
Both taken at 20 keV. Horizontal width of micrograph = 1.4 mm.

Figure 15 shows an EBIC image at 30 keV of LP36 grown at a higher growth rate of $0.55 \mu\text{m}/\text{min}$. Also shown is an optical micrograph of the same film (not the same area) showing the more pronounced surface ripples of height $\sim 2 \mu\text{m}$ and closer spacing $\sim 0.2 \text{ mm}$. The EBIC image shows a high density of dark spots which are due to regions of high recombination. The size of dots is consistent with the electron scattering of the 30 keV beam. Qualitative examination of the dependence of the EBIC signal on beam energy indicates that the defects are in the bulk of the film and not on the surface. Note the fine black lines which are due to the surface ripples on the film.

↑ line scan

Figure 15. Top: Optical micrograph of LP36A. Horizontal width = 1.2 mm. Bottom: EBIC image of LP36B. Horizontal width = 2.5 mm.

Their higher resolution and dependence on beam energy indicates they are near surface defects. Figure 16 shows a EBIC line scan across this sample. The central area was heavily radiation damaged (0.3 Coul/cm^2) and has a lower average signal. Note that the signal variation due to the recombination defects is $\sim 50\%$. The recombination lengths quoted in Table I are the best observed which means in the case of the QBIC method that data is taken outside these recombination regions. It should be pointed out that the low density of recombination defects in Figure 14 is not typical of most of the low growth rate samples. In general the density of recombination defects is similar to Figure 15. Some of the wafers were slow cooled from 950°C to below 600°C at 3°C/min . This produced no detectable reduction in the severity of the recombination defects. Possibly a gettering step would be beneficial. The high density of these recombination defects must be reduced for this junction growth method to be applied to photovoltaic cells.

LP35B 1981-4-28

Figure 16. EBIC line scan across LP35B.

Figures 17 and 18 show QBIC data for the two samples with the longest diffusion lengths. LP36B was grown at $0.55 \mu\text{m/min}$, soon after replacement of the Sn bath. It had a diffusion length of $30 \pm 10 \mu\text{m}$. The diffusion length measured by EBIC on a cleaved junction varied between 20 and $40 \mu\text{m}$ depending upon the location. LP26 has a diffusion length of $30 \mu\text{m}$ based on the QBIC data. The EBIC data on cleaved junctions gave a lower limit of $20 \mu\text{m}$. It was limited because of the layer thick thickness of $45 \mu\text{m}$. The EBIC method fails when the diffusion length is comparable to the layer thickness. In all cases the QBIC data is taken in areas heavily radiation damaged by the electron beam. Before radiation damage the signals are as much as

Figure 17. Electron Beam Collection Efficiency versus beam energy for sample LP36B.

10 times larger. A low energy electron beam can damage only the silicon surface and not the bulk. The observation of this large surface sensitivity confirms that the diffusion lengths are comparable to the junction depth. For some samples with diffusion lengths, much smaller than the layer thickness, this surface sensitivity was not observed, as expected.

For samples LP32 a total of 0.67g high purity Sb was added to the bath (0.75 wt %). This resulted in a resistivity of .02 ohm-cm or a donor concentration of $1.5 \times 10^{18} \text{ cm}^{-3}$. This corresponds to a concentration segregation coefficient of 6×10^{-3} . At this Sb concentration the diffusion length was reduced to $8 \mu\text{m}$. Figure 10 shows a plot of the observed lifetime versus donor concentration based of the measured sheet resistances, layer thickness and assuming standard values for the minority carrier diffusion coefficient. The minority carrier lifetime is essentially independent of doping between 2×10^{15} and $2 \times 10^{18} \text{ cm}^{-3}$. The solid curve shows the assumed dependence of lifetime used for the original simulation of the epitaxial solar cell. As can be seen the diffusion length in these layers falls about a factor of 10 to 30 below the original assumption. Using the lower curve in Figure 19 the optimization model yields the curves in Figures 5, 6, and 7 for 100 and 30 and 10 ohm/sq. epitaxial layers. For 10 ohms/sq. the efficiency is limited by the short circuit current because of the shorter

Figure 18. Electron Beam Collection Efficiency versus beam energy for sample LP26.

diffusion lengths. However for 30 ohms/sq., efficiencies of 22 to 23% should be achievable for an emitter thickness of $8 \mu\text{m}$ a surface recombination velocity $< 300 \text{ cm/sec.}$ and a doping level of 10^{18} cm^{-3} . For 100 ohms/sq. the design margin is wider bearing in mind that substrate recombination will limit the open circuit voltage to about 670 to 700 mv and the efficiency to about 22 to 23%.

The efficiencies quoted in the analysis assume no reflection losses from the front surface, and no grid shadowing losses. For the Polka Dot Cell the deletion of grid shadowing losses is justified. Anti-reflection coatings would be used but textured surfaces could be a problem. This growth method does not work on (100) surfaces. This was attempted and the results are shown in the SEM micrograph in Figure 20. The more rapid growth of the (111) planes results in the random pyramid structure. An attractive possibility is to use the oriented etched PDC cell surface as the substrate for the epi epitaxial growth. All of the faces are (111) planes. One very quick attempt using a slow growth rate resulted in growth in only a few of the holes. This is probably due to gas entrapment in the holes. Probably some changes in the substrate position an increase in the growth rate, agitation of the sample during the initial growth or introduction of the sample into the tin bath under vacuum would eliminate this problem.

Figure 19. Minority carrier lifetime determined by EBIC and/or QBIC versus majority carrier density. The solid curves are based on equation (4) for the indicated limiting diffusion lengths L_0 and an Auger coefficient $C_N = 0.4 \times 10^{-31} \text{ cm}^6 \text{ sec}^{-1}$.

Figure 20. SEM secondary electron image of epitaxial growth on a (100) surface. Magnification bar = $50 \mu\text{m}$.

III. As IMPLANTED FRONT JUNCTIONS

A. Front Junction Processing Experiments

High dose As implantation was explored as an alternative method for front junction fabrication. The investigation was motivated by the work of Tsai et al.⁽¹²⁾ who observed that very short high temperature annealing cycles could significantly increase the sheet conductivity of high fluence As implanted junctions while still preserving the shallow junction depth. They observed as much as a 50% decrease in sheet resistance using a 5 min. 1000°C annealing cycle as compared to a 75 min. 900°C anneal. The measured junction depths were the same for each case. Rutherford Backscattering confirmed that the distribution of As is unchanged. The differences are therefore due to a change in the concentration of active As. This has been explained by an As clustering model based on a three As and one electron cluster. The focus of the Tsai et al. work has been shallow junctions for MOS-FET's and emitters in bipolar transistors. No work has been reported on the suitability of these junctions for solar cells.

Six <100> wafers were given a PH₃ diffusion at 850°C for 1 hour, then driven in and slow cooled. Square diode areas 0.15" across were defined and silicon etched to remove the PH₃ diffused region. Two wafers were dry oxidized at 1000°C for 1 hour. The measured oxide thickness by ellipsometry was 612Å. The wafers were implanted with different As fluences and energies. After implantation the wafers were scribed in half and subjected to two different annealing schedules. The A halves were annealed for 30 minutes at 900°C and the B halves at 1000°C for 5 minutes with about 2 minutes insertion and pulling time. The sheet resistance and electron beam collection efficiency of the diodes were measured. Table II summarizes the results. For the high fluence implants the sheet resistance of the short high temperature annealed halves (B) is smaller as expected. For lower fluence implants (2 and 4) the low temperature anneal gives the same or smaller sheet resistance. This is because As clustering is negligible for small As concentrations. The electron beam collection efficiency data show quite the opposite trend. In general the collection efficiency is smaller for the halves annealed at the higher temperature. This indicates that either the mobility or the lifetime in the heavily doped layer is less for the high temperature anneal. This suggests that an anneal for a long time at a lower temperature ~900°C for 30 minutes to 1 hour followed by the short high temperature step could be more effective. The As clustering model predicts that the last high temperature anneal would reduce the clustering of the As and increase the sheet conductance. If the lower collection efficiency is due to radiation damage which can be annealed by the long low temperature anneal then this two-step annealing would be useful. It is also possible that the short temperature anneal results in a reduced lifetime in the implanted layer because of impurities are more effectively gettered into the implanted layer by the short, high temperature anneal. Sample 7 is from a second lot which did not use the PH₃ diffusion step. The diodes were defined by an oxide mask.

Figure 21 shows the measured collection efficiency versus beam energy for wafer #1 implanted at 120 keV and 10¹⁶ cm⁻² through 600Å of SiO₂ and annealed for 5 min at 1000°C or 30 min. at 900°C. This is compared to the collection efficiency of a PH₃ diffused layer with a sheet resistance of 30 ohms/square. As can be seen, the PH₃ diffused layer is superior both in collection efficiency and sheet resistance. However, it is possible that the junction quality of the As junction could be superior because of the gettering effect discussed above. It is planned to try these high dose As implants in the PDC process.

Table II
As Implanted Front Junctions

Wafer	As Energy KeV	Fluence cm ⁻²	Oxide	R _s Ω	E-beam Collection Eff. at				
					11 keV	2	3	5	20
1A	120	2×10 ¹⁶	Yes	50	0.05	.16	.17	.56	.90
1B				30		.09	.17	.43	.89
2A	120	5×10 ¹⁵	Yes	27					
2B				50					
3A	120	2×10 ¹⁶	No	68	.14	.1	.33	.59	.85
3B				18		.015	.05	.3	.64
4A	30	10 ¹⁵	No	59					
4B	120	6×10 ¹⁴		59	.17	.25	.37	.6	.89
5A	80	10 ¹⁶	No	41	.046	.09	.20	.54	.82
5B				27					
6A	30	10 ¹⁶	No	50	.06	.18	.35	.66	.9
6B				32	.037	.10	.24	.57	.89
7A	80	2×10 ¹⁶	No	47.7		.01	.065	.37	.92
7B				32.8		.008	.05	.35	.88

A) 900°C 30 min

B) 1000°C 5 min

Figure 21. Electron Beam Collection Efficiency versus beam energy for As implanted diodes annealed at 900 or 1000°C for 30 and 5 min. respectively. Dotted curve is the typical behavior of a shallow PH₃ diffusion with similar sheet resistivity.

B. PDC with As Implanted Front Junctions

It was initially planned that two groups of Polka Dot cells would be prepared with all the process steps the same except that one group would have the front junction produced by arsenic implantation and the other would use the normal phosphorus diffusion. Implementation of this plan had to be delayed while a workable process sequence was developed. This has now been accomplished but at a time beyond the duration of this contract so the proposed comparison has not yet been carried out. PDC development is continuing and it is expected that As implanted cells will be fabricated, with results to be reported elsewhere.

IV. ARSENIC DIFFUSION FROM Sn-As SOURCE

Efficient carrier collection in N^+P cells requires a shallow N^+ region formed on a p-type substrate having a long minority carrier diffusion length. Most cells are presently made using phosphorus as the n-type dopant. As discussed in the previous contract report, arsenic may offer advantages over phosphorus so several methods of forming suitable junctions are being investigated. Implanted regions are under study as described above in Section III. Sealed-tube arsenic diffusion is also being explored as a means of achieving cells with long minority carrier lifetimes, using liquid-phase metal gettering to eliminate deep-level impurities during diffusion.

The long minority carrier lifetimes required in thyristor manufacture are obtained by sealed-tube gallium diffusion in which sufficient gallium is used to insure the presence of a liquid phase of metallic gallium during diffusion. Liquid metal gettering is also the principle that is used in forming indium alloyed junctions on germanium. In the present study liquid tin was used as the gettering agent, with arsenic added to produce a vapor pressure corresponding to the desired surface concentration.

P-type silicon wafers were sealed in evacuated quartz ampoules with a small tray containing the desired Sn and As additions. Previous work such as that of Murota et al., Japan J. Appl. Phys. 17, 457 (1978), indicated that temperatures in the range 950 to 1050°C for 30 minutes should produce suitable junction profiles. Figure 6 of Sandhu and Reuter, IBM J. Res. Develop. 15, 464 (1971) indicates that several hundred mm of arsenic pressure would give a surface concentration in the range 1 to $2 \times 10^{20} \text{ cm}^{-3}$ at these temperatures. To avoid explosions, the amount of As used was less than the amount (3.5 grams) that would produce 1 atmosphere of As_4 pressure at 1050°C in the ampoule, which had a volume of 1 liter. The amount of Sn used was varied since very little information could be found about the partial pressure of As over Sn-As mixtures. Three diffusion experiments were carried out using diffusion times longer than suggested above to make it easier to measure the impurity profiles. P-type CZ and FZ wafers with boron concentrations of $2 \times 10^{17} \text{ cm}^{-3}$ were used, and the results are summarized in Table III.

Sn/As-1 contained 26.7 g Sn and 1.7 g As in a graphite tray. Ten wafers were diffused at 1050°C for 12.7 hours, after which the ampoule was removed from the furnace to cool the wafers rapidly and minimize As cluster formation. The wafers were found to be coated with a gray deposit which was presumed to have been caused by the graphite tray. A quartz tray was used in subsequent experiments, resulting in much cleaner wafers. The arsenic concentration achieved in this diffusion experiment was lower than desired so the source concentration was increased for the next experiment.

Table III
Arsenic Diffusion Experiments

Experiment	Temp (°C)	Time (hr.)	ρ_{sheet} (ohms)	x_j (μm)	C_{max} (cm^{-3})
SnAs-1, CZ	1050	12.7	39	0.7	4E19
SnAs-1, FZ	1050	12.7	28	0.95	2.8E19
SnAs-3, CZ	1040	14	10	1.6	2E20
SnAs-3, FZ	1050	14	10	2.1	1E20
AST-2, FZ	1050	8.3	35-50	1.4	4E19
AST-3, CZ	975	2.5	100	0.3	2E19
AST-4, CZ	975	2	51	0.35	5E19

Sn/As-2 contained 4.5 g Sn and 2.3 g As in a quartz tray. The wafers came out with a transparent film several fringes thick and a sheet resistance of several hundred ohms. The results did not appear significant and the problem was attributed to the use of old, partially oxidized As, or to a leaky ampoule.

Sn/As-3 was a repeat of the previous run, but using a new supply of 6-9's As. The wafers were diffused at 1050°C for 14 hours and then furnace cooled to 950°C before the ampoule was pulled from the furnace. Measurements indicated a sheet resistance of ~ 10 ohms and a junction depth of ~ 2 microns. The impurity profiles indicated by spreading resistance probing were very broad with C_{max} occurring near the middle of the N^+ region rather than at the surface. This result indicates that arsenic precipitation had taken place near the surface, lowering the concentration of active arsenic in that part of the diffused layer. This could have been avoided by cooling rapidly from the diffusion temperature, and this will be done in future experiments.

Three open-tube diffusion experiments were also performed, using Emulsitone 3739N as the arsenic source. AST-2 was diffused at 1050°C for 40 minutes in O_2 followed by 8 hours in a N_2 ambient, then rapidly pulled from the furnace. The next two were shorter diffusions carried out at 975°C, intended to produce shallow junctions suitable for front surface solar cells. AST-3, which was performed in a N_2 atmosphere, yielded a rather low value for C_{max} . The furnace atmosphere was changed to $\text{N}_2 + 10\% \text{O}_2$ for AST-4 and this resulted in a satisfactory arsenic profile.

Junctions were mesa etched so the diffusion length could be measured in these diffused wafers by the surface photovoltage method. However, the results obtained lacked reproducibility due to some defect in the experimental procedure and the cause has not yet been determined, so nothing conclusive can be reported at this time.

V. POLKA DOT CELL PROCESS DEVELOPMENT

The original plan for fabricating Polka Dot cells was to selectively etch the interconnect holes first and then form the junctions and substrate contacts. It was found that the holes interfered seriously with subsequent patterning steps so the process sequence was modified so patterning could be done before the holes were etched. This revision has been accomplished and cells are now being carried through the entire process successfully. However, this did not take place before the present contract ended, so much of the work that had been planned could not be carried out in time to be reported here.

One of the investigations that was to have been performed was to modify the patterning of the back of the cell to reduce the length of junction edge and the reaction of the area that is covered by metallization. These changes are illustrated by Figures 22 through 24. In the original design (Figure 22) the backs of the cells had interdigitated metallization fingers which were soldered to a matching set of fingers on the heat sink (not shown). The junction came to the surface along a convoluted path that followed the fingers. This path was quite long and contributed significantly to the dark current and limited the open-circuit voltage of the cell. The dark current was further augmented by the large fraction of metal coverage on the back of the cell.

Figure 22. Original cell design with interdigitated metal fingers making contact with the substrate and deep N⁺ areas. The back of the cell is covered with glass except in the shaded electrode areas.

The first modification was to open windows through the back oxide in the form of a 61×61 array of 6-mil squares, as shown in Figure 23. Interdigitated metal fingers were then evaporated over the back of the cell so 31 of the fingers made contact to the substrate while the other 30 fingers contacted the deep N^+ area through these window openings. This change has been made and has significantly reduced the fraction of the back area that is contacted by the metallization.

Figure 23. First design modification to reduce the area covered by metallization. Contact to the silicon is made through an array of 6-mil squares (double cross-hatched areas) cut through the back oxide.

The second modification has yet to be carried through. It will make contact to the substrate only between every 4th row of interconnect openings, as illustrated in Figure 24. It will reduce the metallized area by another factor of 4 and the length of junction edge by a factor of 2. Some increase in series resistance is expected and will be evaluated in order to derive an optimum design compromise. The masks for this modification have been obtained and used to produce an initial lot of cells. These cells are nearing completion but test results have not yet been obtained.

Figure 24. Second design modification which will further reduce the metal contact area and the length of junction edge. The deep N⁺ diffusion covers the entire back of the cell except for 10-mil squares along every 4th row through which the substrate contacts are made.

REFERENCES

- [1] J.W. Slotboom and H.C. DeGraaff, Solid-State Electron., Vol. 19, pp. 857-862, 1976.
- [2] G.E. Possin, M.S. Adler, B.J. Baliga, IEEE Transactions on Elect. Dev. *ED-27*, pp. 983-88, 1980.
- [3] M.P. Thekaekara, "Data on Incident Solar Energy," J. of Environmental Science, *17*, pp. 21-49, 1974.
- [4] C.T. Sah, Contract # DOE/JPL-9546 E5-7E11 (April 1978).
- [5] B. Jayant Baliga, J. Electrochemical Soc., *127*, pp. 1168-72, 1980.
- [6] B. Jayant Baliga, J. Electrochemical Soc., *124*, pp. 1628-31, 1977.
- [7] B. Jayant Baliga, J. Electrochemical Soc., *126*, pp. 138-143, 1979.
- [8] W. Van Roosbroeck, J. Appl. Phys. *26*, pp. 380-391, 1955.
- [9] F. Berz and H.K. Kuiken, S.S. Elect. *19*, pp. 437-445, 1970.
- [10] G.E. Possin and C.G. Kirkpatrick, SEM-1979-I Washington, D.C., SEM Inc., pp. 245-256, April 1979.
- [11] G.E. Possin and C.G. Kirkpatrick, J. of Microscopy *118*, pp. 291-296, 1980.
- [12] M.Y. Tsai, F.F. Morehead, J.E. Baglin, and A.E. Michel, J. Appl. Phys., *51*, pp. 3230-35, 1980.