DEVELOPMENT OF ADVANCED ELECTROMAGNETIC EXPLORATION SYSTEM

PREPARED FOR

UNITED STATES DEPARTMENT OF ENERGY
WASHINGTON, D.C.

BY

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951 0392

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FINAL REPORT

CONTRACT NO. DE-AC07-78ET28404

AUGUST 1979

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1.0 INTRODUCTION

Electromagnetic (EM) Exploration methods have been used successfully to locate and delineate geothermal energy areas. The electrical properties of rock in geothermal energy systems are significantly different, usually of lower resistivity, than the host media. Thus the presence of geothermal activity can often be detected by measuring earth resistivity at different depths. There are a number of ways in which the earth resistivity can be measured in the field. These consist of:

- Galvanic Measurements (Dipole-Dipole)
(Dipole-Bipole)
- Magneto Telluric (E/H)
- Controlled Source EM
- Induced Polarization (IP)

Different sets of electronic equipment are normally required to perform surveys of these types. Consequently, a need existed for a universal EM exploration system which could be used to accomplish any one or all of these surveys.

In January, 1978, the Department of Energy contracted with Westinghouse to design, develop, and test a universal high-power electromagnetic exploration system. The system to be developed under this contract was ultimately going to be used to enhance exploration and boundary delineation efforts for geothermal energy.

The system initially proposed by Westinghouse consisted of a 5 kW controlled source ultra stable EM transmitter and a 5-channel amplitude and phase detection receiving system with induction coils, cryogenic magnetometers and electric dipole antennas as receiving sensors. The analog receiving system proposed under this procurement was considered to be state of the art at the time the proposal was prepared; however, by the time the contract was awarded, it was evident that a change of design to an all-digital microprocessor based receiving system was in order. This was proposed informally to the Department of Energy Technical Project Officer early in the program and approval was granted to proceed in this direction on the basis that no schedule or cost impact would result therefrom. It was Westinghouse's belief at that time that the microcomputer based system could be implemented with the existing funds and within the schedule allocation. Furthermore, it was felt that taking the digital approach would lead to a much more flexible and powerful exploration tool and one which would not be obsolete shortly after it was built.

There was significant progress made on this program in the development of the microprocessor based receiving system. Unfortunately, the estimate that the new design approach would not incur additional costs proved to be erroneous, and consequently, Westinghouse was not able to carry the project through to its final completion. However, the progress made on this system has been thoroughly documented and could be resumed at any time if funding were to become available.

This report details the electronics system design for both the transmitting system and the receiving system, the laboratory test results obtained on the system completed thus far, and the effort needed to complete the system. It is strongly recommended, based on the results thus far obtained, that funding be acquired to complete the development of the system.

2.0 RECEIVER DESCRIPTION

The electromagnetic (EM) receiver described in this report is a design expected to advance the state of the art and demonstrate the feasibility of a cost effective, highly flexible and very portable EM exploration receiver. This has been done by utilizing a low power microprocessor (IM6100) to implement random sampling of the signal and performing a least squares analysis to the resulting samples.

The main features of the EM receiver are:

- Capability to determine amplitude and phase of a selected frequency component in each of five (5) analog channels to within 0.1%.
- Frequency range of 1 mHz to 1 kHz with $3\frac{1}{2}$ digits of resolution.
- Selectable bandwidth: 0.1 mHz to 1 Hz.
- Mini-cassette tape storage of processed data.
- Portable and light weight. Instrument case weighing no more than thirty pounds.
- Flexibility provided by microprocessor (IM6100) controlled instrument.
- Signal processing includes modeling of signal plus noise rather than simply producing the single frequency Fourier Transform.
- Power provided by rechargeable batteries intended for ten (10) hours of operation.
- CMOS microprocessor and other components provide low power drain. 200 ma @ 10 VDC.
- Temperature compensated crystal 4.096 MHz reference with $\pm 3 \times 10^{-7}$ stability and low power consumption 5 ma @ 12 VDC.
- Capability for phase locking 4.096 MHz reference to a more precise standard such as WWV.

A block diagram of the receiver is shown in Figure 1. Measurements are made in two orthogonal horizontal axes of the electric and magnetic fields (designated E_x, E_y & H_x, H_y) and along the vertical axis of the magnetic field (H_z). The five analog signals are sampled and input into

FIGURE 1 EM EXPLORATION RECEIVER BLOCK DIAGRAM

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respective sample and hold circuits for microprocessor selection and processing. The three magnetic field sample and hold circuits also have provisions to accept the magnetometer outputs when the S.H.E. magnetometer is used instead of the ferrite loop antenna. Each sampled signal is analog to digital (A/D) converted for use by the microprocessor. The clock and sample control circuit controls the sample and hold circuits for each of the five channels on instructions from the microprocessor. Samples are taken in an irregular or random time interval determined by a software routine.

The frequency of the measured signal is selected by thumbwheel switches on the front panel. Frequency range is from 10^{-3} Hz to 10^{+3} Hz. The frequency synthesizer circuit employs a phase lock loop to lock the selected frequency to the 4.096 MHz reference clock of the receiver. An external frequency source such as WWV can also be used as a reference. The frequency select interface provides the frequency and scale information to the microprocessor.

At the time a sample of the five electromagnetic field components is taken, the output of the frequency synthesizer is brought into the phase reference circuit in order to retain phase angle information of the source waveform. Absolute phase information between transmitter and receiver is possible only if the external synch to WWV is employed. Otherwise, relative phase shift between analog channels is obtained, without any absolute reference.

After the data is sampled and digitized, the microprocessor performs a least-squares fit of the data to a mathematical model. To do this, five sets of matrix equations must be generated and solved. The microprocessor uses a hardware multiplier, and 4 K of RAM memory to accomplish this through a software program which is loaded into the memory from a mini-dek cassette. Results to be used for interpretation or even further processing can be retained on a cassette recording.

2.1 Receiver Theory

This section provides some background theory on which the receiver operation is based. The receiver uses synchronous detection based upon a least squares fit of a mathematical model, consisting of the source field and leading noise terms, to the received data. This technique effectively reduces biasing errors. In doing this, the microprocessor must set up and solve five sets of matrix equations to produce the desired amplitudes of the in-phase and quadrature components of the five fields.

2.1.1 Synchronous Detection

A received signal can be modelled as the sum of three terms - an in phase component, a quadrature component, and noise.

$$S(t) = A \sin(\omega t) + B \cos(\omega t) + N(t).$$

Synchronous detection schemes generally assume the amplitudes may be obtained by Fourier transforms

$$A = \frac{2}{T} \int_0^T S(t) \sin(\omega t) dt$$

$$B = \frac{2}{T} \int_0^T S(t) \cos(\omega t) dt$$

where T is the period of measurement. This assumption is correct provided:

1. T is selected to assure the received signal components are orthogonal, or

$$\int_0^T \sin(\omega t) \cos(\omega t) dt = 0.$$

This is done by selecting $T = \frac{n\pi}{\omega}$, where n is an integer.

2. The noise $N(t)$ is orthogonal to $\sin(\omega t)$ and $\cos(\omega t)$.

$$\int_0^T N(t) \sin(\omega t) dt = \int_0^T N(t) \cos(\omega t) dt = 0.$$

This second assumption is rarely achieved.

2.1.2 Biasing Errors

$N(t)$ may be written as

$$N(t) = \sum_{m=1}^{\infty} \left\{ P_m \sin (120 \pi m t) + q_m \sin (120 \pi m t) \right\} \\ + c + at + bt^2 + N'(t).$$

P_m and q_m are amplitudes of 60 Hz fundamental and harmonics, and

$$N'(t) = \sum_{i=3}^{\infty} d_i t^i.$$

The P_m and q_m terms may either be notched out by analog filtering, or forced to zero by requiring the source frequency to be submultiples or odd multiples of 30 Hz. However, no choice of T or ω will force the t terms to transform to zero.

$$\frac{2}{T} \int_0^T (c + at + bt^2) \sin (\omega t) dt = -\frac{2a}{\omega}$$

$$\frac{2}{T} \int_0^T (c + at + bt^2) \cos (\omega t) dt = \frac{4b}{\omega^2}$$

(For high frequencies, the noise effects are less pronounced, as the transforms become small. Also, high pass filters may be used. However, at low frequencies where $T \approx 1/\omega$ filter design is nontrivial.) The result is biasing of amplitudes A and B due to the noise.

$$A' = A - \frac{2a}{\omega} + \frac{2}{T} \int_0^T N'(t) \sin (\omega t) dt \\ B' = B + \frac{4b}{\omega^2} + \frac{2}{T} \int_0^T N'(t) \cos (\omega t) dt$$

in the presence of linear or quadratic noise.

2.1.3 Least Squares Solution

Given the computational capabilities of a Harris/Intersil 6100 microprocessor, it is possible to perform a least-squares fit to the data of the in-phase and quadrature components of the source field plus some of the leading terms of the noise. This technique substantially reduces the bias errors due to these terms.

The fitting of a mathematical model to a set of known functions by the method of least squares is a well known classical technique. However, the details are reviewed here as a reference for the discussion to follow.

Given a data set $\{S(t_j)\}_{j=1}^J$ and a set of L linearly independent functions $f_\ell(t)$, a least-squares fit of the function set to the data set implies the error

$$S = \sum_{j=1}^J \left\{ S(t_j) - \left[\sum_{\ell=1}^L \lambda_\ell f_\ell(t_j) \right] \right\}^2$$

is minimized over all possible values of coefficients λ_ℓ . This minimization is accomplished by equating partial derivatives to zero, equivalent to solving L equations of the form

$$\sum_{\ell=1}^L \lambda_\ell \left\{ \frac{2}{J} \sum_{j=1}^J f_k(t_j) f_\ell(t_j) \right\} = \frac{2}{J} \sum_{j=1}^J f_k(t_j) S(t_j) \quad k = 1, L$$

Clearly, the extent to which b and c bias the calculation of A and B is dependent on ω and the relative amplitudes of a to A and b to B . But, for example, if $\omega = .002\pi$, $T = 1$ hour, and $b = 1 \gamma/\text{hr}$, the bias induced in A is $-.09\gamma$. For signals on the order of $.25\gamma$ this represents a 35% error. And, $1 \gamma/\text{hr}$ is a relatively small linear drift to be expected in the earth's field for measurements made over time periods of six hours or less. Similar bias errors can be expected from quadratic drifts. (It may be well to point out here that the linear and quadratic drifts are actually the leading terms in the sine and cosine of other frequencies in the noise.)

One possible solution to the biasing problem is to make measurements before and after measurements of the source field are made to obtain estimates of "a" and "b". However, such estimates are likely to be in error by as much as the estimates themselves.

Another solution is to record data for periods which are long compared to the periods of the noise spectra. In this case, the linear and quadratic terms become very small. (Monotonic drifts do not exist for long periods.) However, a more time efficient method is available.

2.1.4 Matrix Solution

For the EM exploration receiver, the function set f_ℓ consists of the linearly independent functions

$$\sin (\omega t_j)$$

$$\cos (\omega t_j)$$

$$\phi_j$$

$$\phi_j^2$$

$$1$$

The data set $S(t_j)$ includes the five sampled EM field components

$$H_x(t_j)$$

$$H_y(t_j)$$

$$H_z(t_j)$$

$$E_x(t_j)$$

$$E_y(t_j)$$

Five sets of matrix equations of the form $\Gamma \Lambda = R$ must be solved, one set for each element of the data set $S(t_j)$. The matrix elements are given below in terms of the actual received signals and computed values.

Γ matrix

$$\gamma_{k\ell} = \sum_{j=1}^J f_k(t_j) \cdot f_\ell(t_j)$$

$$\begin{bmatrix}
 \sum_{j=1}^J \sin^2(\omega t_j) & \sum_{j=1}^J \cos(\omega t_j) \cdot \sin(\omega t_j) & \sum_{j=1}^J \phi_j \cdot \sin(\omega t_j) & \sum_{j=1}^J \phi_j^2 \cdot \sin(\omega t_j) & \sum_{j=1}^J 1 \cdot \sin(\omega t_j) \\
 \sum_{j=1}^J \sin(\omega t_j) \cdot \cos(\omega t_j) & \sum_{j=1}^J \cos^2(\omega t_j) & \sum_{j=1}^J \phi_j \cdot \cos(\omega t_j) & \sum_{j=1}^J \phi_j^2 \cdot \cos(\omega t_j) & \sum_{j=1}^J 1 \cdot \cos(\omega t_j) \\
 \sum_{j=1}^J \sin(\omega t_j) \cdot \phi_j & \sum_{j=1}^J \cos(\omega t_j) \cdot \phi_j & \sum_{j=1}^J \phi_j^2 & \sum_{j=1}^J \phi_j^3 & \sum_{j=1}^J 1 \cdot \phi_j \\
 \sum_{j=1}^J \sin(\omega t_j) \cdot \phi_j^2 & \sum_{j=1}^J \cos(\omega t_j) \cdot \phi_j^2 & \sum_{j=1}^J \phi_j^3 & \sum_{j=1}^J \phi_j^4 & \sum_{j=1}^J 1 \cdot \phi_j^2 \\
 \sum_{j=1}^J \sin(\omega t_j) \cdot 1 & \sum_{j=1}^J \cos(\omega t_j) \cdot 1 & \sum_{j=1}^J \phi_j \cdot 1 & \sum_{j=1}^J \phi_j^2 \cdot 1 & \sum_{j=1}^J 1^2
 \end{bmatrix}$$

This matrix must be formed only once during each 16 ms sampling period, since the elements depend only upon the time and total number of samples.

Λ vector

Λ is a column vector whose elements are the coefficients of the function set f_ℓ . It is this vector that is to be solved for, by

$\Gamma^{-1} R = \Lambda$. Five vectors must be found, one solution for each of the five channels.

$$\Lambda = \begin{bmatrix} \lambda_1 \\ \lambda_2 \\ \lambda_3 \\ \lambda_4 \\ \lambda_5 \end{bmatrix}$$

λ_1 and λ_2 correspond to the in-phase and quadrature coefficients A and B. The magnitude of the corresponding EM field component is then given by

$$|S_i(t)| = \sqrt{\lambda_1^2 + \lambda_2^2}, \quad \angle S_i(t) = \tan^{-1} \frac{\lambda_2}{\lambda_1}$$

The noise term coefficients $\lambda_3, \lambda_4, \lambda_5$ (c, a, and b respectively) can be solved for if a study of the noise statistics is desired.

R vector

Five separate R column vectors must be formed, one for each EM field component. The vectors are detailed below.

$$\rho_k = \sum_{j=1}^J f_k(t_j) \cdot S(t_j)$$

H_x

$$\begin{bmatrix} H_x(t_j) \cdot \sin(\omega t_j) \\ H_x(t_j) \cdot \cos(\omega t_j) \\ H_x(t_j) \cdot \phi_j \\ H_x(t_j) \cdot \phi_j^2 \\ H_x(t_j) \end{bmatrix}$$

 H_y

$$\begin{bmatrix} H_y(t_j) \cdot \sin(\omega t_j) \\ H_y(t_j) \cdot \cos(\omega t_j) \\ H_y(t_j) \cdot \phi_j \\ H_y(t_j) \cdot \phi_j^2 \\ H_y(t_j) \end{bmatrix}$$

 H_z

$$\begin{bmatrix} H_z(t_j) \cdot \sin(\omega t_j) \\ H_z(t_j) \cdot \cos(\omega t_j) \\ H_z(t_j) \cdot \phi_j \\ H_z(t_j) \cdot \phi_j^2 \\ H_z(t_j) \end{bmatrix}$$

 E_x

$$\begin{bmatrix} E_x(t_j) \cdot \sin(\omega t_j) \\ E_x(t_j) \cdot \cos(\omega t_j) \\ E_x(t_j) \cdot \phi_j \\ E_x(t_j) \cdot \phi_j^2 \\ E_x(t_j) \end{bmatrix}$$

 E_y

$$\begin{bmatrix} E_y(t_j) \cdot \sin(\omega t_j) \\ E_y(t_j) \cdot \cos(\omega t_j) \\ E_y(t_j) \cdot \phi_j \\ E_y(t_j) \cdot \phi_j^2 \\ E_y(t_j) \end{bmatrix}$$

2.2 Receiver Circuit

2.2.1 Frequency Synthesizer

The frequency synthesizer circuit is shown in Figure 2 and the board in Figures 2a & b. The frequency synthesizer takes the internal 4.096 MHz clock and reference signal, divides it down to 409.6 kHz, and uses that as the reference for the MC14569 phase detector. A three decade divider chain (MC14568 and MC14569) results in the output of the oscillator being $(100 M_2 + 10 M_1 + M_0) \times 4096 \text{ Hz}$ where M_2 , M_1 and M_0 are BCD thumbwheel switch positions on the front panel. A scale select switch, also on the front panel, allows this output to be further divided by a factor 10^N where $N = 0, 1, 2, 3, 4$. The resulting output is selected to be 4096 times the frequency to be received. The receiver frequency range is from .001 Hz to 1000 Hz. An external reference signal, such as provided by WWV or another stable source, can be used for transmitter/receiver synchronization.

2.2.2 Frequency Select Interface

The frequency and scale select switch information is made available to the microprocessor data bus through the frequency select interface circuit shown on Figure 3. The selected BCD code is held in three MC14503 3-state buffers until requested by the microprocessor through the (MC14515) decoder. RA1 is a pull down resistor network for ease of individual board checkout or troubleshooting.

Figure 2a Frequency Synthesizer Circuit Card Assembly

Figure 2b Frequency Synthesizer

FREQUENCY SELECT INTERFACE

FIGURE 3

Figure 3a Frequency Select Interface Circuit Card Assembly

Figure 3b Frequency Select Interface

2.2.3 Clock and Sample Control Circuits

If the incoming signals were sampled at a fixed rate, then this rate would need to be greater than twice the highest frequency present to prevent aliasing. This is the classical Nyquist criterion. If, however, the samples are irregularly spaced, then for some distributions the average sampling rate need only be a fraction of the highest frequency present. Appendix A discusses in detail the algorithm implemented by the receiver which produces a distribution of sample times which minimizes the aliasing of all frequencies in the passband of the input amplifiers.

The clock and sample control circuits are shown in Figure 4 and the board layout in Figure 4a and 4b. A temperature compensated CMOS crystal oscillator of frequency 4.096 MHz with $\pm 3 \times 10^{-7}$ stability is used as the clock and reference signal in the receiver. This clock may be phase locked to an external 100 kHz CMOS compatible reference.

Referring to the schematic, two sample controls are provided (sample control #1 and sample control #2), which in turn control one of two sample and hold circuits located on each of the five input channels (E_x , E_y , H_x , H_y , H_z).

The Q_5 output of U11, a 12-bit divider, inhibits or enables each of two groups (U1, U2, U3 and U4, U5, U6) of programmable 12-bit down counters alternately at a 31.25 Hz rate. Each group of counters is loaded with a random 12-bit number (Appendix A) during its inhibit time. The random number is determined by software routine and is latched alternately into the two sets of down counters. Upon being enabled, they count down at a 256 kHz rate. When C_{out} goes low, counting is inhibited. Also a high level, sample control #1 or sample control #2, signal is sent to the respective sample and hold circuits on each of the five input channels, and a data sample is taken and held.

The purpose of having two sample and holds in each channel is because it is possible to have two samples taken which are only 3.9 μ sec apart. Neither the microprocessor nor the A/D converter have the speed to process a sample from a single sample and hold and reset in time for the next sample in such a short time interval.

A write strobe is AND' d with the 31.25 Hz counter enable signal to load the random number into the down counters alternately during the inhibit time or when C_{out} is low. This write strobe is developed from a pseudo device select circuitry referred to as sample control interface shown in Figures 5 and 5a.

CLOCK AND SAMPLE CONTROL

FIGURE 4

Figure 4a Clock and Sample Control Circuit Card Assembly

Figure 4b Clock and Sample Control

CLOCK AND SAMPLE SELECT

FIGURE 6

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Figure 5a Clock and Sample Select

2.2.4 Phase Reference Circuit

The phase reference circuit is shown in Figure 6 with board layout shown in Figure 6a and 6b. The output (A) of the frequency synthesizer is brought into the clock input of the three counters U1, U2, U3 formed by three MC4516's. In general, the outputs of these counters represent the phase angle of the source waveform. When the analog channels are sampled, the outputs of the three counters are simultaneously latched into the upper or lower twelve bits of the three 4508 dual four bit latches (U4, U5, U6). The outputs of these latches are then read by the microprocessor using circuitry formed by a MC14514 decoder to provide the desired latch selection. The microprocessor uses this data to compute $\sin(\omega t_j)$, $\cos(\omega t_j)$, ϕ_j^2 , and ϕ_j .

It is also possible to provide phase and/or frequency synchronization with the transmitter. The REFS signal can be used to preset the three (U1, U2, U3) counters simultaneously with the transmitter from a stable external source to obtain phase synchronization, or by using it to reset the (U1, U2, U3, U4) dividers in the frequency synthesizer, frequency synchronization can be achieved. The phase reference circuit uses the same basic board type with the electric and magnetic field circuits. J1 is used to strap the board for phase reference configuration (See Figure 7), J2 is used to assign the selected code lines from U7 to enable the proper latches (U4, U5 or U6) on instructions from the microprocessor.

2.2.5 Electric Field Circuit

Figure 8 shows one of two identical field circuits, one for each of two channels. Figures 8a and 8b show the layout of the board. Each channel or board contains two sample and hold amplifiers, AD583, (reason for which is discussed in Section 2.2.3 Clock and Sample Control Circuit), which receive the same signal from one of the external E field preamplifiers. When one of the sample control lines goes high, the corresponding sample and hold amplifier (U10, or U11) retains the E field signal voltage which is being input at that instant of time. The microprocessor, through the device select decoder U7 (MC14515) and a write strobe, closes the corresponding analog switch of U9 (AD7513) which passes the sampled voltage value to the A/D converter. After the A/D converter has performed the conversion and the digital output is read by the microprocessor, the switch is again opened. After each of the two electric and three magnetic field channels have been separately connected to the same A/D converter through each respective analog switch (AD7513) and digitized, the sample control line is reset (goes low) and the sample and hold amplifiers are placed back in the track mode.

For the microprocessor to select the proper analog switch U9 (AD7513 is a dual switch), a decoder circuit U7 (MC14515) is used to control the selected switch when the proper device select code is sent out by the microprocessor. The magnetic field, electric field, and

FIGURE 6A PHASE REFERENCE (1 EACH). CIRCUIT CARD ASSEMBLY.

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Figure 6b Phase Reference

Strapping

J1

J2

				Device Select Code			
				DX8	DX9	DX10	DX11
0	REF	Sample CTRL #1	S0	0	0	0	0
0	REF	Sample CTRL #2	S1	0	0	0	1

Figure 7 Phase Reference Circuit Strapping

FIGURE 8A ELECTRIC FIELD (2 EACH). CIRCUIT CARD ASSEMBLY.

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Figure 8b Electric Field Sample and Hold (2 each)

phase reference boards are essentially the same with only selected portions being used for each respective circuit. J1 is used to strap the board for one of three configurations. J2 is used to strap a different device select code for each signal and hold circuit (U10, U11), on each board. The strapping and codes for the electric field boards is shown in Figure 9.

2.2.6 Magnetic Field Circuit

The magnetic field circuit is shown in Figure 10 with component layout in Figures 10a and 10b. Three identical circuits are needed, one for each of three channels, H_x , H_y , and H_z . The magnetic field circuitry is similar to the electric field circuitry except for the addition of counters (U1, U2, U3) and latches (U4, U5, U6) to accommodate the S.H.E. magnetometer outputs. If the analog output of the magnetometer should exceed 10V, it is auto-reset to zero and a TTL pulse and sign signal are produced which are input into the clock and UP/DOWN pins of the counter (U1, U2, U3) respectively. By counting these pulses (twelve bits of count) with regard to sign, plus taking into account the twelve bits of programmable gain of the A/D converter, a dynamic range of 144 dB is possible for slowly varying signals. Appendix C describes the magnetometer system. Ferrite loop antennas may also be used instead of the magnetometer. In this case, the counter outputs are ignored by the microprocessor. The ferrite loop antenna is discussed in Section 2.2.10.

There are three identical circuits, one for each magnetic field component H_x , H_y , and H_z with the exception of different device select strapping on J2^y for each sample and hold circuit. The reason for two sample and hold amplifiers U10 and U11 is discussed in the Clock and Sample Control Circuit Section 2.2.3.

When one of the two sample control lines goes high, determined by the random sample routine and the clock and sample circuitry, the corresponding sample and hold amplifier, U10 or U11 retains the H field signal voltage which is being input at that instant of time. The microprocessor, through the device select decoder U7, closes the corresponding analog switch of U9, which passes the sampled voltage value to the A/D converter. In addition, magnetometer pulse and polarity information at the instant the sample is taken, is latched into U4, U5, U6. The microprocessor reads this data during the time the analog switch U9 is closed by activating the read strobe. Counters U1, U2, U3 are reset by sending the proper code (S10) to U7 and activating the write strobe. After each of the five channels (E_x , E_y , H_x , H_y , H_z) has been connected to the A/D converter and digitized, the sample control line is reset (goes low) and the sample and hold amplifiers are placed back in the track mode. The microprocessor then proceeds with processing the digitized data, generating a new random sample time, and then proceeding with the digitizing operation of the other set of sample and hold amplifiers.

E_x and E_y

J1

E_x

J2

Sample CTRL #2
Sample CTRL #1

E_y

J2

Sample CTRL #2
Sample CTRL #1

				Device Select Code			
				DX8	DX9	DX10	DX11
E_x	Sample CTRL #1	S2		0	0	1	0
E_x	Sample CTRL #2	S3		0	0	1	1
E_y	Sample CTRL #2	S12		1	1	0	0
E_y	Sample CTRL #1	S13		1	1	0	1

Figure 9 Electric Field Circuit Strapping

FIGURE 10A MAGNETIC FIELD (3 EACH). CIRCUIT CARD ASSEMBLY.

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Figure 10b Magnetic Field Sample and Hold (3 each)

J1 is used to strap all three boards to magnetic field configurations. J2 is used to strap a different device select code for each sample and hold (U10 and U11) on each board. The strapping and codes for the magnetic field boards is shown in Figure 11.

2.2.7 Analog to Digital Converter Circuit

A single A/D converter is used to convert the five input channels. A schematic of the A/D converter is shown in Figure 12 with the board layout in Figures 12a and 12b. The A/D circuit U4 is a twelve bit, low power device (AD1210) which does a conversion in nominally 200 μ seconds. The purpose of U8 is to provide programmable gain control as each analog signal from the sample and holds is sent to the A/D U4. Gain is selected by software and decoded by U9. As the selected gain is input to U8, the OR gates consisting of U7 and U10 are used to pass a pulse to U3 which in turn provide a minimum of 7.8 μ seconds settling time for A1 before starting conversion. The cc signal notifies the processor when a conversion is complete and the digitized signal is available to be read by the microprocessor in latches U1 and U2.

2.2.8 Multiplier

A hardware multiplier is used to provide fast multiplication. Figures 13, 14, and 15 show the schematic of the multiplier located on three boards; multiplier-1, multiplier-2, and multiplier-3 respectively. Multiplier-2 contains a IM 6101A PIE (U1) which is used to provide the necessary interface for inputting a twelve-bit multiplier and twelve-bit multiplicand and outputting two twelve-bit halves of the twenty-four bit product to the bus.

The multiplicand Y is loaded into registers U1, U2, and U3 on board 1 when the WRITE 1 pulse occurs. At this time, if FLAG 3 = 1 (Y - positive integer), then the SY flip-flop, U3 on board 2, receives the sign bit. If FLAG 3 = 0, (Y = two's complement integer), then the SY flip-flop remains in the clear state.

The multiplier X is loaded into U7, U8, and U9 on board 1 when the WRITE 2 pulse occurs. At this time, if FLAG 1 = 1 (X = positive integer), then the SX flip-flop, U3 on board 2, receives the sign bit. If FLAG 1 = 0, (X = two's complement integer), then the SX flip-flop remains in the clear state.

The trailing edge of the WRITE 2 pulse sets the SYN CH1 flip-flop (U9 on board 3) after SYN CH1 is set, SYN CH2 is set on the next rising edge of CK pulse. SYN CH2 remains set for exactly one period of CK. The SYN CH2 signal loads the counter U7 (board 3) with a binary eleven or 1011_2 . The counter counts down to zero. During each period for which

H_x , H_y and H_z
J1

H_x
J2

S4
S5

H_y
J2

S6
S7

H_z
J2

S9
S14

Device Select Code

		DX8	DX9	DX10	DX11
H_x Sample CTRL #1	S4	0	1	0	0
H_x Sample CTRL #2	S5	0	1	0	1
H_y Sample CTRL #1	S6	0	1	1	0
H_y Sample CTRL #2	S7	0	1	1	1
H_z Sample CTRL #2	S9	1	0	0	1
H_z Sample CTRL #1	S14	1	1	1	0
U1, U2, U3, Reset	S10	1	0	1	0

Figure 11 Magnetic Field Circuit Strapping

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A/D CONVERTER
FIGURE 12

FIGURE 12A A/D CONVERTER. CIRCUIT CARD ASSEMBLY.

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Figure 12b A/D Converter

MULTIPLIER-1

FIGURE 13

J1
1 10

MR1	• •	SO
MC	• •	MC
MW2	• •	MW1
SI	• •	KI
KO	• •	MP

FIGURE 13A MULTIPLIER - BOARD 1. CIRCUIT CARD ASSEMBLY.

Figure 13b Multiplier - 1

MULTIPLIER-2
FIGURE 14

J2
 1 10
 MW2 • • D
 MR2 • •
 XM • •
 MW2 • • MW2
 MC • • 50

J1
 1 10 50
 MR1 • • 50
 MC • • MC
 MW2 • • MW1
 SI • • KI
 KO • • MP

FIGURE 14A MULTIPLIER - BOARD 2. CIRCUIT CARD ASSEMBLY.

Figure 14b Multiplier - 2

MULTIPLIER-3

FIGURE 16

J2

	1	10	
MW2	.	.	D
MR2	.	.	
XM	.	.	
MW2	.	.	MW2
MC	.	.	50

FIGURE 16A MULTIPLIER - BOARD 3. CIRCUIT CARD ASSEMBLY.

Figure 15b Multiplier - 3

the counter is not zero, MC has one negative going pulse for each positive going pulse of CK. Twelve such pulses are produced. One is produced during SYN CH2 and eleven as the counter counts down.

Multiplication is performed by twelve sequential shift and add cycles. These cycles occur on the rising edge of the MC clock produced by U7 on board 3. The 4.096 MHz CLK signal is divided by 4 with U10 and the resulting 1.024 MHz signal is used to generate the MC signal. Figure 16 is the timing diagram for generation of MC. Each rising edge of MC causes the shift and add network (U7, U8, U9, U10, U11 on board 1 and U1, U4, U5, U8 on board 3) to change state.

The multiplication done, signal D is produced by U7, board 3, when the twelve clock cycles of the MC clock are complete. This signal is read by the microprocessor via SENSE 1 on the PIE U1 on board 2. The lower twelve bits of the product are available at U2 and U3 on board 3 and the higher twelve bits at U12 and U13 on board 1.

J3 on board 2 is used to strap the desired PIE address code on SEL 3 thru SEL 7. The multiplier PIE address is SEL 3 = 0, SEL 4 = 0, SEL 5 = 0, SEL 6 = 1 and SEL 7 = 1.

2.2.9 Magnetic Tape Mine Cassette Transport and Interface

A Braemar CM-600 Mini-dek digital mini cassette tape transport is used for program and data storage. The unit is small, weighing only 8 ounces. It is powered by 5 VDC requiring 1 Watt in the Read/Write mode. The unit can handle a 2400 baud rate and record tapes of up to 100 feet long at 800 BPI.

The recording technique used is saturation recording. It does not use a tape-drive speed control system, resulting in the need for a speed independent recording system. The cassette interface circuit shown in Figures 17 and 18 is used to accomplish this.

The recording method uses a variable-width data pulse in conjunction with a fixed width bit cell. For a ONE, the pulse lasts for 3/4 of the cell; for a ZERO, 1/4. Referring to Figure 17, the upper portion consisting of U11, U12, U13, U16, and U18 is used for detection and control of the cassette tape speed, direction, read/write mode and several other functions. The microprocessor does this by utilizing FLAGS 2, 3, and 4 and SENSE lines 3 and 4 of the in/out interface PIE.

The digital data is input to the cassette tape interface through pin seven (7), port #2 of the LP-12FMR microprocessor in/out interface. The UART clock signal is divided by eight (Q_3) and sixteen (Q_4) by U15

TIMING DIAGRAM FOR GENERATION OF MC

FIGURE 16

Figure 17a Cassette Interface Circuit Card Assembly

Figure 17b Cassette Tape Interface

to provide different length pulses to represent ZERO and ONE. For a ONE, the pulse lasts for $3/4$ of the cell; for a ZERO, $1/4$. The incoming data, TRO, latches the D flip-flop (U17) high or low which in turn is AND'd with the respective ONE (Q3) or ZERO (Q4) pulse from U15. The resulting pulses on pin four (4) of the CM-600 MINI-DEK connector are represented as follows:

To read data from the tape, the variable width cells are read by the pulse width demodulator circuit shown in Figure 18 and in block diagram form in Figure 17. The data from the tape enters the cassette interface board on pin (13) of the CM-600 MINI-DEK connector. The data is inverted and is used by U7 to reset the three up/down counters, U1, U2 and U3, at the start of each bit cell. The counters count up at the start of each bit cell and continue until the data line goes low at which point the counters count down. If the input data is a ZERO, the up count lasts for $1/4$ of a cell and the down count has time ($3/4$ of a cell) enough to count back to zero causing the output of U5 to go low. For a ONE input, the counters U1, U2, U3 count up for $3/4$ of the cell time and never count back down in the given time, consequently the output of U5 remains high.

The output of U5 is delayed sufficiently long that when the next data cell clocks the U7 (pin 1) flip flop, the input to U7, pin 9 is used to set the output of U7 (pin 13). Consequently, when the output of U5 goes low, the next bit cell output of the demodulator is low or "0". If the output of U5 never goes low, then the next bit cell output is high or "1". The output of the demodulator is then one bit "delayed" from the input. U9 and U10 form a phase-locked loop to synchronize the UART on the microprocessor in/out board to the incoming data. This method of data encoding provides a self-clocking feature allowing tape-speed variations of up to 50% with virtually no effect on the ratio of the variable width to fixed width of individual bit cells.

2.2.10 Preamplifiers and Ferrite Loop Antenna

Figure 19 shows the schematic of the magnetic field induction coil preamplifier. Three of these are needed, one for each component of the H field. This preamplifier is for use in the frequency range of 1 Hz to 1000 Hz. Below 1 Hz the magnetic field spectrum is covered by the S.H.E. magnetometer with an optional 60 dB preamplifier available on each magnetic field circuit board.

The induction coil preamplifier utilizes two dual instrumentation amplifiers (PMI OP-10Y) which has an extremely low equivalent input voltage noise level. ($10 \text{ nV}/\sqrt{\text{Hz}}$). The preamplifier has a selectable gain of 0, 20, and 40 dB, as well as a fixed gain of 80 at the input transformer and 1.5 at the output transformer. Power is provided by two 12.6 VDC dry cell batteries. Two voltage regulators are used to decouple the output from input amplifier stage.

Figure 20 shows the schematic of one of two electric field horizontal wire antenna preamplifiers. It uses the same instrumentation amplifier (PMI OP-10Y) as the H field circuit except a simpler design. This preamplifier is single-ended and direct coupled to provide a fairly flat response over the whole frequency range from 1 mHz to 1 kHz. This preamplifier provides selectable gain positions of 40, 60 and 80 dB. Power is provided by two 12.6 V dry cell batteries with voltage regulators used for decoupling as in the H field preamplifier. Both types of preamplifiers also contain a passive 60 Hz notch filter with attenuation of 40 dB.

To sense the orthogonal magnetic fields, an induction coil antenna, developed by USGS, is used. Figure 21 shows the dual axis configuration. The advantage of this configuration is that self noise is minimized due to the closed magnetic reluctance path of the ferrite core, when the two coils, located parallel to each other, are connected in series. Each coil is wound with three hundred turns of #14 wire and glued to a square ferrite core configuration less than twenty inches square.

The sensitivity of the antenna is shown in Figure 22.

2.2.11 Computer System

The computer portion of the Westinghouse EM receiver is a 12-bit CMOS microprocessor development system manufactured by Cybertek, Inc. The system consists of:

- 1 ea LP-12 Low Power 12-bit Computer Board, utilizing
 IM6100A microprocessor.
- 1 ea LP-12F-MR Terminal Interface Board
- 4 ea LP-12D 1K RAM module
- 1 ea LP-12J(CP) Control Panel Module.

FIGURE 10 H FIELD INDUCTION COIL PREAMP.

FIGURE 20 E FIELD HORIZONTAL ANTENNA PREAMP.

Ferrite Loop Antenna

Figure 21

Figure 22 Square Frame Antenna Calibration

The IM6100 uses a PDP-8 instruction set, and utilizes a 12-bit multiplexed address and data bus. The 4 K of directly addressable RAM provides storage for the system program, data storage, and sine/cosine lookup table. The Control Panel Module contains the monitor program in three 1K X 4 EPROMS. The Terminal Interface Board uses a UART to communicate with a ASR-33 teletype and mini-dek cassette.

Documentation and specifications for the Cybertek system is given in Appendix B. Also included is documentation on the IM6100 microprocessor and IM6101 Peripheral Interface Element.

2.3 System Integration and Software

The data acquisition process performed by the hardware circuitry is controlled by the microprocessor. Several possible schemes for dealing with the asynchronous nature of the sampling were considered. The most obvious approach considered use of system interrupts as the means of controlling and sequencing the various tasks. Disadvantages of the interrupt processing far outweighed any advantages. While more efficient use of available computational time is possible, the increased complexity of the software would result in longer system development time.

By designing software which masks the asynchronous chain of events involved in the sampling, conversion and storage of the data, complexity is reduced. A description of the software approached is detailed in Section 2.3.1.

Figure 23 depicts a very general overview of a system run, from initialization to data output. The majority of time is spent collecting data and setting up matrices. The solution to the matrix problem is done externally, at a later time.

2.3.1 Sequence of Events

The 4.096 MHz system clock is divided by 2^{16} to yield a 62.5 Hz signal (16 ms period). Each 16 ms period is designated a time frame. Only one sample command can occur in a given time frame, although the command instant is random within the corresponding frame. The shortest possible time interval between successive samples is 3.9 μ secs. The amount of time available to begin processing data until the data is sampled again is unknown. It is conceivable that situations may arise when data acquisition and matrix formation will overlap. Designing software to handle this overlap is not straightforward, and is further complicated by the primitive architecture and instruction set of the IM6100.

A basic approach around these timing difficulties is to always use the next time frame to manipulate data acquired during the present frame.

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FIGURE 23 SYSTEM FLOWCHART

A run shall be defined as the sample acquisition and processing (matrix construction) for the five data channels. Each run requires some time in 3 consecutive frames. Referencing Figure 24, the sequence for Run 1 goes as follows:

- (1) A random number is generated at the beginning of Frame A. This random number is read into the sample control counter circuitry.
- (2) At the beginning of Frame B, the corresponding sample control counter is enabled. The counter counts down, reaching zero at random time t_{12} . The S/H amplifiers go into hold at this time.
- (3) Time during Frame C (period t_{13}) is used to A/D convert the five channels and construct the matrices.

The nature of the system requires data to be sampled once per frame. Therefore, Run 2 is staggered 16 ms later than Run 1. Run 3 uses Frames C, D, and E.

By overlaying three runs in Figure 24, it becomes apparent three separate tasks must be carried out during each frame. To summarize these tasks, refer to Frame C.

- (1) At the beginning of each frame, a random number is generated and sent out at t_{31} (Run 3).
- (2) S/H amplifiers are switched into hold mode at random time t_{22} (Run 2).
- (3) Matrix construction using the data from the previous frame is done during time period t_{13} (Run 1).

The complete data acquisition process involves a continuous number of these individual runs.

2.3.2 Software Procedures

I. Control Signals

Four control signals are connected to the MPU. The sense signal marks the beginning of each 16 ms time frame. On each rising edge of the sense line, a random number must be generated and latched into the sample control counter circuitry.

A set of signals, called Sample Control #1 and Sample Control #2, are used to switch the S/H amplifiers between sample and hold modes. The fourth control signal is Conversion Complete ($\overline{cc}$), verifying the end of an analog to digital conversion.

FIGURE 24 SEQUENCE OF EVENTS FOR MATRIX CONSTRUCTION

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II. Channel Selection

A maximum of nine analog and digital data channels must be serviced during a run. Five analog channels must be routed separately to the ADC. The four digital channels are the phase reference and 3 magnetometer outputs. Necessary multiplexing is accomplished by using three state latches, each hardwired to a different address. Inputting data involves placing an address on the data bus, issuing a write command, and then issuing a read command.

The multiplex address uses the four lowest order bits of the system bus. An encoding table is shown in Figure 25.

III. ADC

The ADC hardware has a software program-made gain feature used to keep the converted value in an intermediate digital range. The gain word uses bits DX2 - DX5. To initiate an A/D conversion, a word consisting of both gain and address is sent out on the bus. The conversion begins automatically, and $\overline{cc}$ signals end of conversion.

Figure 26 lists the gain words.

IV. Random Number Generator

A software algorithm implementing a 24 bit shift register is used to generate a pseudorandom string of numbers. An assembler listing is shown in Appendix A. Total time to generate a new number is 145 μ sec.

2.3.3 Control Panel Memory

The Harris/Intersil 6100 microprocessor allows parallel use of the 4K memory space thru two memory select lines. Control panel memory, entered thru the control panel request interrupt, is typically used to store a ROM system control program.

During system development, a 1K monitor program stored in EPROM was located in the highest memory space in control panel memory. The program allowed simple memory modification functions, memory listing capability, and program execution, in the main memory space.

The final system will have no need of a general monitor program. Instead, a bootstrap and diagnostic test routine will be located in CPM, allowing automatic system initialization and circuit checkout.

Figure 25 MULTIPLEXER ADDRESSING CODES

Device Selected	DX8	DX9	DX10	DX11
Phase Ref. S.C. #1	0	0	0	0
Phase Ref. S.C. #2	0	0	0	1
E _x S.C. #1	0	0	1	0
E _x S.C. #2	0	0	1	1
H _x S.C. #1	0	1	0	0
H _x S.C. #2	0	1	0	1
H _y S.C. #1	0	1	1	0
H _y S.C. #2	0	1	1	1
Freq. Select	1	0	0	0
H _z S.C. #1	1	0	0	1
Mag. Reset	1	0	1	0
Scale Select	1	0	1	1
E _y S.C. #1	1	1	0	0
E _y S.C. #2	1	1	0	1
H _z S.C. #2	1	1	1	0
Not Used	1	1	1	1

Figure 26 A/D GAIN SETTINGS

Gain	DX2	DX3	DX4	DX5
2	0	0	0	0
2	0	0	0	1
4	0	0	1	0
8	0	0	1	1
16	0	1	0	0
32	0	1	0	1
64	0	1	1	0
128	0	1	1	1
256	1	0	0	0
572	1	0	0	1
1024	1	0	1	0
2048	1	0	1	1
4096	1	1	0	0
2	1	1	0	1
2	1	1	1	0
Not used	1	1	1	1

The last setting (1111) must not be used as a gain word. This word is used to read the ADC.

3.0 TRANSMITTER DESCRIPTION

The EM transmitter is designed to be as portable as possible while still being capable of providing 5 kW of signal over the frequency range of 1 mHz to 1 kHz using a single portable AC generator. Figure 27 shows a block diagram of the transmitter. The transmitter utilizes a transistor bridge to produce typically a sinusoidal waveform. However, the waveform generator can be programmed to generate any reasonable symmetric waveform. During each half cycle, the lower bridge transistor is switched on and off at high frequency (nominally 40 kHz) to produce an output current which, after filtering, has the frequency, phase, and amplitude determined by the waveform generator. A description of each of the circuits follows:

3.1 Transmitter Circuits

3.1.1 Frequency Synthesizer Circuit

The transmitter frequency synthesizer circuit is identical to the receiver synthesizer described in Section 2.2.1. The operating frequency, 1 mHz to 1 kHz, is selected using front panel thumbwheel switches and the scale select switch. The output A from U5 is a square wave providing clock pulses to the waveform generator.

3.1.2 Waveform Generator Circuit

The waveform generator shown in Figure 28 provides two outputs for the current controller. The first (C) is a sign bit for the waveform to be transmitted, and the second (B) is the desired output waveform reference to which the actual output is compared.

A square wave clock signal of the selected frequency is input into the counter chain consisting of U1, U2, and U3. These counters count from 0 to 511 every half cycle of the transmitter frequency, addressing the 512 X 8 EPROM (U4). This EPROM is programmed according to the relation $256 \sin(\text{address}/512) \pi$. The D/A converter U5 converts the digital output of the EPROM to a full wave rectified sine wave whose amplitude is determined by the signal REF (+). This, in turn, is determined by U11, a D/A converter, which is programmed by BCD current select thumbwheel switches with a range of 0 to 10 amps in .1A steps. U7, U8, U9, and U10 are counters and gates used to synchronize the transmitter frequency to an external source.

3.1.3 Current Controller Circuit

The circuit shown in Figure 29 is used to switch on and off the appropriate legs of the output transistor bridge and to control current through the lower right and lower left legs.

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FIGURE 27 EM TRANSMITTER BLOCK DIAGRAM

FIGURE 20. WAVEFORM GENERATOR

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Figure 28a Waveform Generator Circuit Card Assembly

FIGURE 29 CURRENT CONTROLLER

Figure 29a Current Controller Circuit Card Assembly

The waveform generator provides two signals to the current controller. The first (C) is a square wave of the desired frequency which alternately enables and disables the upper right and lower left or upper left and lower right bridge driver circuits through gates U1, U2 and U3.

The second signal (B) is the desired output waveform reference which is applied to comparators A1 and A3. This signal is compared to the output of the current monitor amplifier on the lower right and lower left legs of the output bridge. If the output from the current monitor is less than the waveform generator output (B) the second comparator A2, or A4 goes high, which turns on the appropriate bridge leg. When the current monitor output exceeds the waveform generator output, the lower bridge leg is turned off. This current regulation occurs at a 40 kHz rate, but only the sinusoidal waveform frequency is seen by the output. A low pass filter and diode network on the input of A2 and A4 insure that the output transistors are not switched so frequently that switching losses become significant.

3.1.4 Bridge Driver Circuit

A Bridge Driver circuit, shown in Figure 30, is used to drive each of the four output transistors. Additionally the lower right and lower left legs use the current isolation amplifier to monitor current flow through that leg and provide a signal to the current controller for comparison to the current reference signal from the waveform generator.

The appropriate output from the current controller is input into an optical coupler U2. The input is optically coupled because, during switching, the driver circuitry changes up to several hundred volts relative to control electronics. The driver circuit provides approximately one ampere during "on" periods and a reverse bias of minus five volts during "off" periods. An additional output is provided to sink the turn-off current from the base of the output transistor. This enhances the turn-off speed.

3.1.5 Output Bridge

The output bridge utilizes a discrete Darlington approach to minimize drive requirements while allowing access to the second base for increased turn off speed. The Darlington transistor also acts like an active Baker's clamp to prevent saturation and its resulting slower turn-off time. The output bridge shown in Figure 31 uses a Darlington 2N6676 to drive a Westinghouse D60T405010 NPN output transistor on each leg. The D60T is capable of 40 amperes of collector current with a sustained $V_{CEO} = 400 \text{ V}$.

FIGURE 30 BRIDGE DRIVER

FIGURE 30A BRIDGE DRIVER ASSEMBLY

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FIGURE 3-1 TRANSMITTER OUTPUT BRIDGE

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During any given half cycle, one of the upper bridge legs is on continuously while the alternate lower bridge acts as a switching regulator to control the current through the load. This current is monitored by a $0.1\ \Omega$ current monitor resistor and the voltage across it is coupled to the current controller by an optically coupled isolation amplifier located on the bridge driver board. The lower leg output transistors are then switched on and off at a 40 kHz nominal rate, to provide current regulation during any given half cycle when that half of the bridge is conducting.

The damper diodes and inductor serve the same purpose as in switching regulators. The inductor smooths out the current pulses from the bridge while the diodes provide a temporary current path during transistor "off" periods.

3.1.6 Power Supplies

The low voltage ($\pm 5\text{VDC}$) power supplies for the four bridge drivers are DC/DC converters, one of which is shown in Figure 32. Physically, these are located on the respective bridge driver boards. This power supply provides effective isolation of the bridge driver from the control electronics. All four supplies have a 12 VDC input, thus allowing a situation where the entire transmitter can be supplied from a single 12 V lead acid battery if the output load is less than $0.2\ \Omega$.

A three phase rectifier high voltage power supply connected to virtually any standard power source provides power for the output bridge. Figure 33 shows a schematic of the power supply. Single phase and DC sources may use any two of the three inputs. The standard power source is an Onan Model 5.5 TT series electric generator providing 5.5 kW at 120 or 240 VAC.

The Low Voltage Power Supply shown in Figure 34 provides the necessary voltages for the control electronics. This supply is a commercial $\pm 15\text{ VDC}$ (Acopian D15-20) followed by regulators to provide the other DC voltages required. Physically, this supply is located on the current controller board.

FIGURE 32 BRIDGE DRIVER POWER SUPPLY

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FIGURE 33 HIGH VOLTAGE POWER SUPPLY

FIGURE 34 LOW VOLTAGE POWER SUPPLY

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4.0 CONCLUSIONS

Success in implementing a microprocessor into an EM exploration receiver is demonstrated by this project despite the fact that final hardware construction and final processing software has not been completed. The digital based design of the receiver has been implemented into hardware, and debugged on a circuit by circuit basis. Having successfully achieved this, it is a straightforward and relatively easy task to achieve a comprehensive processing instrument. This can be done by implementing the final processing software. The software developed so far is aimed at demonstrating the performance of the various receiver circuits. This software is also the basis from which the final field processing software can be written.

The transmitter portion of this project is fully designed and circuits layed out. Some hardware is built but not yet tested. No difficulties are foreseen here since the basic design has proven itself in past instruments and the new features such as programmable waveform generator and new higher power output transistors are an improvement intended to provide flexibility and greater reliability.

The objective of this project is to develop a highly flexible and portable EM exploration system. The efforts expended thus far have demonstrated the feasibility of achieving this goal. The additional time requirements needed to develop a digital instead of an analog based receiver were not sufficiently realized at the onset.

5.0 RECOMMENDATIONS

This Universal EM Exploration System, under development by Westinghouse for the Department of Energy, Division of Geothermal Energy, is seen as a potentially useful tool which can be used to enhance exploration and boundary delineation efforts for geothermal energy. The flexibility and portability of this system underscores the desire to complete the remaining tasks.

The objectives of this project can be achieved with additional funding, preferably through DOE, Division of Geothermal Energy. However, if DOE funding is not available, Westinghouse would like to retain the hardware and complete the project with its own funding or that of some other interested agency which would benefit from the system.

APPENDIX A

SAMPLING SPECTRUM

APPENDIX A

Sampling Spectrum

The true spectrum of the incoming signal $S(t)$ is given by

$$F_S(\omega) = \int_{-\infty}^{\infty} S(t) e^{j\omega t} dt \quad \text{where } j = \sqrt{-1}. \quad (\text{A-1})$$

The process of sampling the signal $S(t)$ yields a sequence $X(K) = S(t_K)$.

The spectrum of this sequence is given by

$$F_X(\omega) = \sum_{K=1}^J S(t_K) e^{j\omega t_K}.$$

The apparent spectrum, $F_X(\omega)$, is not generally the same as the true spectrum, $F_S(\omega)$. The apparent spectrum differs from $F_S(\omega)$ because $S(t)$ was sampled at discrete points in time over a finite length of time. If samples are taken over some finite length of time T , then there is not enough information to distinguish between frequencies which differ by some amount on the order of $\frac{1}{T}$.

The effect of sampling at discrete points in time can be modelled with a sampling function $d(t)$, where

$$d(t) = \sum_{K=1}^J \delta(t - t_K) \quad (\text{A-2})$$

where $\delta(\cdot)$ is the Dirac delta function.

Then

$$F_X(\omega) = \int_{-\infty}^{\infty} S(t) d(t) e^{j\omega t} dt. \quad (\text{A-3})$$

The spectrum of $d(t)$ is given by

$$F_d(\omega) = \sum_{K=1}^J e^{j\omega t_K}. \quad (\text{A-4})$$

Since $F_X(\omega)$ is the spectrum of the product of two functions, it is also the frequency convolution of the spectrum of the two functions.

$$F_X(\omega) = \frac{1}{2\pi} \int_{-\infty}^{\infty} F_S(\omega - \alpha) F_d(\alpha) d\alpha. \quad (A-5)$$

The ideal spectrum for $d(t)$ would be

$$F_d(\omega) = 2\pi\delta(\omega)$$

in which case $F_X(\omega) = F_S(\omega)$. This corresponds to $d(t) = 1$ which implies continuous measurement of $S(t)$ over infinite time.

To obtain an acceptable approximation to continuous measurement, the sampling spectrum $F_d(\omega)$ should contain a narrow peak at $F_d(0)$ and be minimized elsewhere. If $S(t)$ contains a coherent noise source of a particular radian frequency ω_n and magnitude C , then this frequency will appear as interference of frequency ω_0 with a magnitude of $C F_d(\omega_n - \omega_0)/F_d(0)$. The spectrum of $F_d(\omega)$ provides a measure of how well the receiver rejects unwanted (out of band) frequencies. Since the sampling function, $d(t)$, is determined by the receiver, this function can be chosen, in advance, to provide an acceptable sampling spectrum.

The receiver is assumed to be able to process samples at a rate $\beta = \frac{1}{\tau}$. If samples are chosen uniformly, that is $t_K = (K - 1)\tau$, then the following sampling spectrum is obtained.

$$|F_d(\omega)|^2 = \frac{\sin\left(\frac{\omega\tau J}{2}\right)^2}{\sin\left(\frac{\omega\tau}{2}\right)}. \quad (A-6)$$

This spectrum contains narrow peaks at the points $\omega = 2\pi K\beta$. As a result, aliasing occurs for frequencies which differ by integer multiples of β .

This type of aliasing can be eliminated by choosing the t_K in a random fashion. (For example, see references 1-3). The particular method chosen for this design was to divide time into intervals of duration τ . One sample is taken at a randomly chosen moment within each interval.

$$t_K = \tau(K - 1 + f_K) \text{ where } 0 \leq f_K < 1 \quad (\text{A-7})$$

The f_K are generated using a pseudo-random number generator. The spectrum $F_d(\omega)$ is given by

$$F_d(\omega) = \sum_{K=1}^J e^{j\omega\tau(K - 1 + f_K)} \quad (\text{A-8})$$

In this case $|F_d(0)|^2 = J^2$.

For values of $\omega > \frac{1}{J\tau}$, $F_d(\omega)$ is the sum of independent random vectors. In this case, the expected value (mean) of $|F_d(\omega)|^2$ is J .

$$\begin{aligned} E[|F_d(\omega)|^2] &= \sum_{K=1}^J E[e^{j(K - 1 + f_K)\omega\tau}]^2 \\ &= \sum_{K=1}^J 1 = J \end{aligned} \quad (\text{A-9})$$

The average value of $|F_d(\omega)/F_d(0)|$ is then $J^{-1/2}$. This becomes arbitrarily small for increasing values of J .

The pseudo-random number generator, which determines the f_K , is a 24 bit shift register sequence. This sequence is easily generated in software. Figure S1, S2, and S3 show the resulting spectrum for $J = 64, 128$, and 256 , respectively. The frequency axis is normalized for $\beta = 1$. The spectrum is normalized such that $F_d(0) = 0$ dB. The average value of the spectrum of these figures have the theoretically predicted value of $20 \log_{10}(J^{-1/2})$ decibels. If $\beta = 62.5$ Hz, then Figure A1 corresponds to about one second of data. The average value is about -18 dB.

One minute of data would yield an average value of -36 dB. Ten minutes would result in an average value of -46 dB, while one hundred minutes would result in an average value of -56 dB.

Figure S4 shows the approximate sampling spectrum which results when $d(t)$ consists of 256 equally spaced samples.

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Figure S-2

Figure S-3

Figure S-4

APPENDIX A

Bibliography

- Masry, Elias, "Poisson Sampling and Spectral estimation of Continuous-Time Processes," IEEE Transactions on Information Theory, Vol. IT-24, pp. 173-183, March 1978.
- Masry, E. and M. C. Lui, "Discrete-Time Spectral Estimation of Continuous-Parameter Processes - A New Consistent Estimate," IEEE Transactions on Information Theory, Vol. IT-22, pp. 298-312, May 1976.
- Beutler, F. J., "Alias Free Randomly Timed Sampling of Stochastic Processes," IEEE Transactions on Information Theory, Vol. IT-16, pp. 147-152, March 1970.

RANDOM NUMBER GENERATOR SUBROUTINE.
 WHEN CALLED, THE SUBROUTINE RETURNS THE RANDOM NUMBER IN THE
 ACCUMULATOR.
 ROUTINE IS LOCATED BEGINNING AT LOCATION 2000.

2000/7777	RETURN ADDRESS
2001/7777 7200	CLA
2002/7777 1233	TAD RNL
2003/7777 7004	RAL
2004/7777 7002	BSW
2005/7777 1233	TAD RNL
2006/7777 7010	RAR
2007/7777 7200	CLA
2010/7777 1234	TAD RNH
2011/7777 7010	RAR
2012/7777 7421	MQL
2013/7777 1233	TAD RNL
2014/7777 7010	RAR
2015/7777 3233	DCA RNL
2016/7777 1233	TAD RNL
2017/7777 7004	RAL
2020/7777 7002	BSW
2021/7777 1233	TAD RNL
2022/7777 7010	RAR
2023/7777 7701	CLA MQL
2024/7773 7010	RAR
2025/7777 3234	DCA RNH
2026/7777 1233	TAD RNL
2027/7577 7010	RAR
2030/7777 3233	DCA RNL
2031/7777 1233	LOAD RN FOR RETURN
2032/7777 5600	RETURN
2033/7777 3155	RNL
2034/7777 7741	RNH

APPENDIX B

COMPUTER SYSTEM

1.0 INTRODUCTION

The LP-12DS provides a complete 12 bit computer system which is ready to operate with the addition of a 5 volt power supply and a teletype. CY-BUG, a monitor which can be quickly and effectively used to prepare and operate programs for the LP-12DS, resides in "background control panel" memory on the LP-12CP module leaving all of "real" memory available to the user. This unique feature of the 6100 microprocessor permits two blocks of memory (up to 4K each) to exist in the same memory address space with one or the other being selected by the MEMS/ or CPSEL/ signals from the microprocessor.

The LP-12L module supplied with the development system contains 1K of NMOS RAM; three additional 1K x 12 RAM blocks (9 IC's) may be installed in sockets provided on this module. CMOS 6514 RAM chips can be obtained from CYBERTEK which may be used for applications that demand very low power.

Expansion of the LP-12DS can easily be accomplished by adding fully tested and assembled LP-12 family modules or special custom circuitry assembled by the user on LP-12U universal prototyping cards.

RAM memory can be added using LP-12D, LP-12L, LP-12J and LP-12A modules depending on the amount of RAM desired and additional functions which might be added at the same time. PARALLEL I/O may be added by using an LP-12C or LP-12B module. PROM memory can be added using an LP-12E or an LP-12J module. See the LP-12 Computer Reference Manual for the specifications of each of the modules. The LP-12DS mother board bus allows new modules to be connected to the LP-12 system with no additional interconnect wiring.

2.0 CONFIGURATION

The addition of a power supply and terminal (such as the ASR-33 teletype) is all that is required to make the LP-12DS operational. The following sections describe the standard arrangement of modules in the development chassis, power supply and signal wiring, teletype modifications and standard strapping options. All LP-12DS systems are configured and tested under these conditions prior to shipment. Figure 2-1 depicts the Functional Block Diagram for the standard configuration of the LP-12DS development system.

2.1 MODULE ARRANGEMENT

The modules of the LP-12DS are placed in the LP-12N-12 Development Chassis as follows:

- Slot 1 - LP-12 Computer
- Slot 2 - LP-12F Terminal Interface
- Slot 3 - LP-12CP Background CY-BUG
- Slot 4 - LP-12L RAM
- Slot 5 - 12 Available for user assignment

This arrangement establishes the LP-12 Computer as the module with highest priority for response to any hardware initiated interrupt. Modules placed in each subsequent slot have the next highest priority (i.e. - slot 12 module has lowest priority). If it becomes necessary to change this order of priority wiring changes are required on the LP-12M-1-12 mother board and on each affected module. The object of these changes is to arrange mother board and module wiring to connect V_{DD} to the PRIN terminal of the 6101 PIE on the module having highest priority first, thence from the POUT terminal of that 6101 PIE to the PRIN terminal of the 6101 PIE having the second highest priority, and so on. Each module has pads to permit the options wiring of V_{DD} to PRIN. The motherboard bus lines PIN and PO chain the priority signal from module to module.

2.2 POWER AND SIGNAL WIRING

A 5 volt (V_{DD}) power supply or appropriate battery must be connected to the red (+) and black (-) banana jack terminals of the LP-12N-12 chassis. The LP-12DS standard configuration operates correctly through a V_{DD} range of +4 to +7 volts. Type "A" components are available for application necessary to extend V_{DD} as high as +10 volts. V_{DD} (+) is connected to pins 2, 4, 57, and 59 of connector P1 on all LP-12 modules. V_{SS} (-) is connected to pins 1, 3, 58, and 60 on connector P1 on all LP-12 modules. Odd numbered pins are on the component side of all modules, with pin 1 to the left when facing the component side of the board, with the connector edge down.

The LP-12 60 wire bus transmits all signals required to interface all LP-12 modules with each other, as well as power and interrupt priority signals. Pin assignments for the LP-12 bus are listed in Table 2-1, and bus signal definitions are provided in Table 2. Note that spare user lines are available in the bus.

A cable for connecting J7 on the LP-12F Terminal Interface module to 20mA teletype transmit and receive loops is furnished with the LP-12DS. Refer to Section 2.4 for modifications which may be required to make your system operate with a specific teletype.

LP-12DS CONFIGURATION DIAGRAM

PIN ASSIGNMENTS FOR LP-12DS MOTHERBOARD BUS

COMPONENT SIDE		REVERSE SIDE	
PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	VSS (GND)	2	VDD
3	VSS (GND)	4	VDD
5	VCM (J2-9)	6	(SPARE)
7	(SPARE)	8	(SPARE)
9	(SPARE)	10	MEMS
11	DATA F	12	(SPARE)
13	SWSEL/	14	IFETCH
15	DMAGNT	16	DMAREQ/
17	CPREQ/	18	CPSEL/
19	RUN	20	RUNHLT/
21	PO	22	PIN
23	RESET/	24	INTGNT
25	SKPINT/	26	C2/
27	XTA	28	C1/
29	CO/	30	WAIT/
31	MEMS/	32	XTB
33	LXADR	34	DEVS/
35	LINK	36	WE/
37	DX11	38	DX10
39	DX0	40	DX9
41	DX1	42	DX8
43	DX2	44	DX7
45	DX3	46	DX6
47	DX4	48	DX5
49	4.096 Mhz Clock	50	SENSE
51	READ STROBE	52	CC
53	WRITE STROBE	54	SAMPLE CONTROL #2
55	NOT USED	56	SAMPLE CONTROL #1
57	VDD	58	VSS (GND)
59	VDD	60	VSS (GND)

TABLE 2-2
BUS SIGNAL DEFINITIONS

SIGNAL NAME	DEFINITION
DATAF	Data field indicates the execute phase of indirectly addressed AND, TAD, ISZ, and DCA instructions, so that data transfers are controlled by the Data field, DF, and not the Instruction Field, IF, if Extended Memory Control hardware is used to extend the addressing space from 4K to 32K words.
SWSEL/	Switch Register Select for the OR THE SWITCH REGISTER INSTRUCTION (OSR). OSR is a Group 2 Operate Instruction which reads a 12 bit external switch register and OR's it with the contents of the AC.
IFETCH	Instruction Fetch Cycle - Active high when CPU is fetching an instruction from memory.
DMAREQ/	Direct Memory Access Request---DMA is granted at the end of the current instruction. Upon DMA grant, the CPU suspends program execution until the DMAREQ line is released.
DMAGNT	Direct Memory Access Grant---DX lines are tri-state while LXMAR, R/W, and MEMSEL/ are not. They can be tri-stated by the BDIS/ signal on J2.
C/PREQ/	Control Panel Request---a dedicated interrupt which bypasses the normal device interrupt request structure.
CPSEL/	The Control Panel Memory Select becomes active, instead of the MEMSEL, for control panel routines. Signal may be used to distinguish between control panel and main memories.
RUN	This signal indicates the runstate of the CPU and may be used to power down the external circuitry.
RUN-HLT	Pulsing the Run-Halt line causes the CPU to alternately run and halt by changing the state of the internal RUN-HLT flip-flop on the positive transition of the signal.
PIN,P0	These pins are used to establish the priority of the PIE interrupt. The highest priority PIE if the chain will have its PIN line tied to V _{DD} and, if it is not the interrupting PIE, it will put out a high on P0. The P0 would be connected to the PIN of the next I/O module in the chain.
SKP-INT/	Time-multiplexed output from PIE to the 6100---if active during IOT SKIP instructions the next sequential instruction will be skipped. The interrupt operates at all other times.
INTGNT	Peripheral device Interrupt Grant.
XTA	External coded minor cycle timing--signifies input transfers to the 6100.
C0/,C1/,C2/	Control line inputs from peripheral devices during an I/O transfer. (All are active low.) All are pulled high on the LP-12 module and C1/ and C2/ are controlled by PIE's on modules as required.
XTB	External coded minor cycle timing--signifies output transfers from the 6100.
WAIT/	Indicates that peripherals or external memory is not ready to transfer data. The CPU state gets extended as long as WAIT/ is active. The CPU is in the lowest power state with clocks running.
MEMS/	Memory Select for memory transfers. (Same as 6100 MEMSEL/ with time delay of 40ns.)
LXADR	The Load External address Register pulse is used to store memory and peripheral address externally. (Same as 6100 LXMAR with time delay of 40ns.)
DEVS/	Device Select for I/O transfers. (Same as 6100 DEVSEL/ with time delay of 40ns.)
WE/	External coded minor cycle timing--used in conjunction with the Select Lines to specify read or write operations. (Same as 6100 R/W with time delay of 40ns.)
LINK	Link flip-flop.
DX0-11	DataX---multiplexed data in, data out, and address lines.

3.0 FUNCTIONAL DESCRIPTION

The following sections describe the operating functions of the LP-12DS modules; reference to appropriate schematic diagrams and specification sheets is necessary to obtain a thorough understanding of system functions.

The 6100 microprocessor used in the LP-12DS has the same instruction set as the Digital Equipment Corporation (DEC) 12-bit PDP-8/E minicomputer. Programs written and assembled for the PDP-8/E will run on the LP-12 with no or little modification. DEC PDP-8 programming manuals, PDP-8 software and PDP-8 user documentation available from DEC or the DEC user society (DECUS) are the best sources for programming information for the 6100 microprocessor. Manuals, software, and documentation may be purchased from DEC at Maynard, Massachusetts.

3.1 LP-12 FUNCTIONAL DESCRIPTION

The LP-12 provides a crystal controlled (2.4576MHz) 6100 microprocessor, a 6101 peripheral interface element (PIE), 256 x 12 words of RAM, a socket for a 6312 1K x 12 word ROM, a programmable interval timer, a 12 bit latched input port, and a 12 bit latched output port.

3.1.1 INSTRUCTIONS

The LP-12's microprocessor obtains its instruction from memory modules via the LP-12DS bus lines. No special distinction is made to the memory between instructions and data. Address, data-in and data-out bits flowing to or from the microprocessor memory and I/O devices are time multiplexed on the DX0 through DX11 bus lines. Data may be obtained from memory, manipulated, placed back in memory and later obtained by the processor and executed as instructions.

Refer to the 6100 specification sheet in the LP-12 Manual specification section for a complete list and description of the 6100 microprocessor instructions.

There are three general classes of 6100 instructions. They are Memory Reference Instruction (MRI), Operate Instruction (OPR) and Input/Output Transfer Instruction (IOT). Memory Reference instructions (MRI's) operate on the contents of a memory location or use the contents of a memory location to operate on the accumulator or program counter. This class of instructions includes JUMPS, LOGICAL ANDS, BINARY ADDS, INCREMENT and SKIP, DEPOSIT and CLEAR AC. The opcodes (3 most significant bits of word) for MRI's are 0 through 5. Bit assignments, operation codes, execution times and other data are defined in the manufacturer's specification on the 6100 microprocessor provided in the LP-12 Reference Manual.

The Operate Instructions (OPR's) have an opcode of 7. The OPR instructions affect the registers and processor status without affecting memory or I/O conditions. The nine least significant bits of the 12 bit instruction designate the exact execution of the instruction and are referenced as microinstructions. There are three groups of microinstructions in the OPR instructions. Group 1 is used to perform logical operations on the contents of the accumulator and link. Group 2 are used primarily to test the contents of the accumulator and then conditionally skip the next sequential instruction. Group 3 are used to perform logical operations on the contents of the AC and MQ. Similar data for OPR instructions (NOP, INCREMENT AC, ROTATE AC, BYTE SWAP, CLEAR AC, COMPLEMENT AC, COMPLEMENT LINK, SKIP, etc.) are also provided in the LP-12 Reference Manual.

The Input/Output Transfer (IOT) instructions have an opcode of 6 and are used to initiate the operation of I/O devices and to transfer data between I/O devices and the LP-12's 6100 microprocessor. The LP-12DS permits Programmed Data Transfer, Interrupt Transfers and Direct Memory Access (DMA) Transfer between the processor and I/O devices. The 6101 parallel Interface Element (PIE) is utilized for correct signaling required by the IOT instruction. Refer to the 6100 specification and the 6101 specification in the LP-12 Reference Manual for complete data on the IOT instruction for Programmed Data Transfers and Interrupt Transfers.

3.1.2 I/O (INPUT/OUTPUT) OPERATION

The LP-12 provides one 12-bit input, one 12-bit output, four single bit inputs and 4 single bit outputs. Control of data to and from the LP-12 I/O ports is accomplished by the 6101 PIE. Multiple READ, WRITE, SENSE and FLAG functions of the PIE serve to condition, initiate, and verify I/O transfers. Signal triggering on levels or edges, write and sense polarities, flag values and interrupt enables are programmed via the A and B registers of the PIE. Bit assignments, PIE initialization commands, interrupt control requirements, and other specifics of I/O operations are included in the LP-12 Reference Manual and in the manufacturer's specifications. Input and output port device code assignments are listed in the STRAPPING OPTIONS section of the LP-12 Reference Manual. Also see Figure 3-1 for J3 straps provided.

3.1.3 INTERVAL TIMER

The LP-12 is supplied with the interval timer connected for operation with a 30 KHZ clock. The timer will generate single processor interrupts at a programmed interval which starts when a reset pulse is output from a timer control register (U4-4 on schematic CY-001B) and ends when the timer has counted through the programmed interval. Control instructions and information necessary to alter the timer clock frequency are contained in the LP-12 Reference Manual, Section 3.2.

3.1.4 MEMORY

The 256 x 12 RAM and 1K x 12 ROM capability of the LP-12 provides memory for data read/write and system control in many microprocessor applications. If additional memory is needed, other LP-12 modules (LP-12L 4K RAM, LP-12J 256 RAM - 2K UV EPROM, for example) can be connected to the 60 line computer bus.

Memory address assignments are dependent on established ROM programs, where these are used. In a typical single board application the ROM is plugged into J7 of the LP-12 module. The ROM would be masked so that locations 6000g through 7777g contain the control program while locations 0000g through 0377g designate the 256 x 12 RAM which is selected by the RSEL signal line of the ROM connected to the RAM. In the LP-12DS there is no ROM on the LP-12 so the LP-12CP module provides the RSEL signal for the RAM on the LP-12 module via bus line 9 in the motherboard.

FIGURE 3-1
LP-12 J2, J3, J4 STRAPPING OPTIONS
(Standard Connection for LP-12DS)

VDD
PIH
MEMS/
ROMS/
RSO/
RAMS/
BDIS/
VCM

- (1) Connection 15 to 16 makes LP-12 highest priority
- (2) Connection 14 to 11 allows RAM on LP-12 to be selected by MEMS/
- (3) Connection 6 to 12 gets RSO/ from LP-12L via pin 9 of edge connector P1.

NOTE: Since RAMS/ (11) is connected, memory on LP-12L must not conflict with address locations.

PLUG DESIGNATION: 12-J2-3

- Used when no ROM on LP-12 and 3K or less RAM used on LP-12L or LP-12DS -

J5-18
J6-6
WR1
TSR
E9-GND
SI2
SI1
RD1

- (1) Connection 1 to 13 connects timer output pulse to LP-12 PIE sense input 4.
- (2) Connection 2 to 12 to 11 to 10 grounds unused sense inputs

PLUG DESIGNATION: 12-J3-1

VDD
GND
VDD
GND
P1-56

- (1) Connection 1, 2, 3, 4, 5 to 16 assigns all "1"s to device address code so board responds to I/O addresses 7608 to 7778
- (2) Connection 6 to 8 wires on-board crystal to the 6100 oscillator pins.

PLUG DESIGNATION: 12-J4-1

FIGURE 3-2
LP-12J2 STRAPPING OPTION
(STRAPPING SOCKET WIRING FOR LP-12 WITH LP-12 RAM ENABLED)

J2
[Conf. No. 12-J2-1]

- (1) Wiring 15 to 16 makes the LP-12 the highest interrupt priority
- (2) Wiring 14 to 13, 11 allows the ODT ROM and the RAM on the LP-12 to be selected by MEMS/.
 ROM is 6000g - 7777g
 RAM is 0000g - 0377g
- (3) Wiring 14 to 5 sends MEMS/ off the board via Pin 10 of edge connector P1 for use by LP-12D memory boards in the system.

USED WHEN ODT IS ON LP-12 and 2K or LESS OF RAM ON LP-12L or LP-12D MODULES

FIGURE 3-3
LP-12 J2 STRAPPING OPTION
(USED WHEN ODT ROM IS ON LP-12 and 3K of RAM IS USED ON LP-12L or LP-12D)

J2

PLUG DESIGNATION: 12-J2-2

- (1) Connection 16 to 15 makes highest priority
 - (2) Connection 14 to 13 connects MEMS/ to ROMS/ to enable ODT ROM to be used on LP-12 at locations 6000g - 7777g
 - (3) Connection 13 to 5 sends MEMS/ off board via pin 10 of P1 for enabling LP-12D RAM modules.
- NOTE: Since RAMS/ is not connected the RAM on the LP-12 does not get enabled in order to prevent it to conflict with memory on LP-12D or LP-12L modules assigned to locations 0000g - 0377g.

FIGURE 3-4
LP-12 J2 STRAPPING OPTION
(USED WHEN NO ROM on LP-12 and 4K of RAM USED on LP-12L or LP-12D MODULES)

J2

PLUG DESIGNATION: 12-J2-4

The LP-12 RAM and ROM memories have tri-state outputs and internal edge triggered address latches which permit address and data information to be time multiplexed on the same bus lines. Memory control is accomplished by the following signals:

MEMS/	Allows read and write operations for main memory when low.
LXADR	Provides an address strobe to initiate storage of memory addresses.
CPSEL/	Allows read and write operation for control panel memory when low.
WE/	Selects read (high) or write (low) function.
WAIT/	Halts transfer of data to or from peripherals or external memory when low.
DMAREQ/	Halts CPU program execution, permits direct memory access when low (Generated by external device)
DMAGNT	Microprocessor output (low) at the end of current instruction indication suspension of instruction fetches until DMAREQ line is released.
XTA	Microprocessor output (high) to indicate data being transferred into the microprocessor.
XTB	Microprocessor output (high) to indicate data being transferred out of the microprocessor.
ROMS/	Same function as MEMS/. Strapping option allows read to LP-12 ROM by either MEMS/ or an external signal.
RAMS/	Same function as MEMS/. Strapping option allows read and write to LP-12 RAM by either MEMS/ or an external signal.
RSO/	Generated by LP-12D, LP-12L, LP-12J, and LP-12CP modules to replace LP-12 6312 ROM RSEL output when using external RAM to simulate the 6312 ROM or when no 6312 ROM is used on the LP-12.

3.2 LP-12F FUNCTIONAL DESCRIPTION

The LP-12F module interfaces asynchronous serial devices such as teletypes or CRT terminals to LP-12 computer systems. This module is normally supplied with 20mA TRANSMIT and RECEIVE terminal interfaces for operation with a teletype such as the ASR-33. CYBERTEK dwg. CY004T is a schematic diagram of these interfaces as well as RS232 TRANSMIT, RS232 RECEIVE, and READER RUN interfaces. Users may construct these or other special interfaces on 16 pin carriers which plug into the LP-12F module.

3.2.1 MULTIPLE BAUD RATE (OPTIONAL)

The following baud rates can be selected by operating dip switches on the LP-12FMR module: 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, and 9600. A strapping option permits generation of 19,200 baud. Different baud rates can be assigned to I/O port #1 and #2 by program commands; both ports cannot operate simultaneously at different rates, however.

3.2.2 SECOND I/O PORT

A second I/O port provides CMOS SERIAL INPUT and OUTPUT lines, READ and WRITE signals, two FLAG outputs, a READER RUN output, two SKIP or INTERRUPT inputs, with program control of edge or level sensitivity of the SKIP/INTERRUPT inputs and the active state (high or low) of the WRITE signal. When the multiple baud rate option (LP-12FMR) module is used, the baud rate of I/O port #2 may be different from that of port #1, with the #1 port disabled by program control.

3.2.3 OPERATOR DEVICES

Operator devices which provide the following functions are included on the LP-12F:

- a. RESET pushbutton (S2) - Initializes processor FLAGS, clears AC and LINK. Halts the processor, leaving DX lines three stated, PC set to 7777g. The READER RUN and BAUD RATE SELECTION (LP-12FMR only) flip-flops and the UART on the LP-12F module are reset.
- b. RUN-HALT pushbutton (S1) - Pulsing this line causes the processor to alternately run and halt at each positive transition of this signal.
- c. RUN LED - When the LED is illuminated the RUN line is high and the processor is operational. The RUN line can be used to power down external devices.
- d. PIE ADDRESS - Dip switch SC establishes the address to which the LP-12F will respond. Should be set to 00111 for LP-12DS configuration.
- e. PARITY - Dip switch SA position 1 permits parity generation and checking when closed. SA position 5 selects odd parity when closed, even parity when open.
- f. STOP BIT SELECT - Dip switch SA position 2 selects 1.5 stop bits for 5 character format and 2 stop bits for other formats, when open.
- g. CHARACTER LENGTH SELECT - Dip switch SA positions 3 and 4 program character length as follows:

Position				
3	closed	closed	open	open
4	closed	open	closed	open
Length	5	6	7	8
- h. BAUD RATE SELECTION - Settings of dip switch SB (LP-12FMR only)
 Octal DIP switch B (SB) allows selection of baud rate for LP-12F-MR.

SB:	8	7	6	5	Baud
	0	0	0	0	0
	0	0	0	1	0
	0	0	1	0	50
	0	0	1	1	75
	0	1	0	0	134.5
	0	1	0	1	200
	0	1	1	0	600
	0	1	1	1	2400

SB:	8	7	6	5	Baud
	1	0	0	0	9600
	1	0	0	1	4800
	1	0	1	0	1800
	1	0	1	1	1200
	1	1	0	0	2400
	1	1	0	1	300
	1	1	1	0	150
	1	1	1	1	110

See LP-12F assembly drawing for switch positions "0" and "1".

FIGURE 3-5
LP-12F J3 STRAPPING OPTIONS
(STANDARD CONNECTION FOR LP-12DS)

PLUG DESIGNATION: 12F (110)-J3-1

FIGURE 3-6
LP-12F-MR J3 STRAPPING OPTIONS
(CONNECTION FOR LP-12DS with LP-12F-MR)

PLUG DESIGNATION: 12F-MR-J3-3

LP-12 LOW POWER COMPUTER MODULE SPECIFICATION

- . INTERSIL/HARRIS 6100 MICROPROCESSOR
- . EXECUTES PDP-8/E * INSTRUCTION SET
- . 256 WORDS OF RAM MEMORY
- . SOCKET FOR 1K WORDS OF ROM
- . PROGRAMMABLE INTERVAL TIMER
- . 12-BIT LATCHED OUTPUT PORT
- . 12-BIT LATCHED INPUT PORT
- . 2 SINGLE-BIT LATCHED OUTPUTS
- . 4 SINGLE-BIT LEVEL/EDGE TRIGGERABLE SKIP/INTERRUPT INPUTS
- . DECODED INPUT AND OUTPUT STROBE FOR OFF-BOARD I/O DEVICE
- . COMMON BUS ARRANGEMENT, PLUS MULTIPLEXED DATA AND ADDRESS SIGNALS
- . BUS DISABLE CONTROL FOR DIRECT MEMORY ACCESS
- . SINGLE VOLTAGE POWER SUPPLY WITH TTL COMPATABILITY AT 5V
- . MASKABLE VECTORED INTERRUPTS
- . ALL LOW POWER CMOS DESIGN
- . CRYSTAL OR EXTERNAL CLOCK CONTROLLED
- . OPTIONS FOR VOLTAGE, SPEED AND TEMPERATURE RANGE INCLUDE
 - 4 to 10 V OPERATION
 - 0 to 8 MHZ OPERATION AT 10 V 25°C
 - COMMERCIAL, INDUSTRIAL AND MILITARY OPERATING TEMPERATURE RANGES
- . COMPACT 4" x 5" SIZE

The LP-12 Low Power Computer Module is the heart of a family of small, low power CMOS logic modules. These modules are designed to be easily interconnected to provide sophisticated computer power for numerous control applications at a low cost relative to comparable minicomputers. In many applications only the LP-12 Module and interface logic peculiar to the application are required. When additional memory and I/O are required a simple bus scheme enables other modules of the family to fill the requirement.

Functionally, the LP-12 provides a crystal controlled 6100 microprocessor, bus signal control logic, I/O control logic, RAM memory with an 18 pin socket for ROM, a programmable interval timer, a 12 bit latched input port and a 12 bit latched output port. A 60 pin edge connector provides common bus interconnect signals between LP-12 family modules. Selected strapping options are provided using 16 pin DIP sockets.

The power consumption of the LP-12 is typically less than 40 mw at 25°C when using a 5 volt power source and a 2.4576 MHZ crystal. Batteries can be used as the primary power source as well as the secondary backup source.

* Trademark Digital Equipment Corporation

HARDWARE / SOFTWARE ENGINEERING

System Design • Microcomputer Applications • Product Development

SPECIFICATIONS

MICROPROCESSOR

- . IM 6100 (INTERSIL)/HM 6100 (HARRIS) STATIC CMOS
- . EXECUTES DEC PDP-8E INSTRUCTION SET (Table 2)
- . PDP-8/E COMPATIBLE I/O INTERFACE
- . I/O COMMAND TO ADDRESS 64 DEVICES
- . DIRECT SELECTION SIGNALS FOR
 - MEMORY
 - CONTROL PANEL MEMORY
 - DEVICE I/O
 - SWITCHES IN
- . WORD SIZE OF 12 BITS FOR DATA AND ADDRESSING ALLOWING MEMORY ACCESSES TO 4096 WORDS AND SEPARATE CONTROL PANEL ACCESSES TO 4096 WORDS WITHOUT EXTERNAL FIELD REGISTER
- . CONTROLS FOR
 - DIRECT MEMORY ACCESS (Request and Grant)
 - RUN AND HALT
 - INTERRUPTS (Request and Grant)
 - RESET (Unconditional)
 - WAIT (For Slow Memory or Device)
 - READ/WRITE (Input/Output)
 - CO, C1, C2 I/O CONTROL
 - SKIP

BUS AND I/O CONTROL

- . BUS DISABLE disables
 - ADDRESS STROBE (LXADR)
 - MEMORY SELECTION (MEMS/)
 - DEVICE SELECTION (DEVS/)
 - READ/WRITE (WE/)
- . SKIP-INTERRUPT SIGNAL GENERATION
- . C1, C2 SIGNAL GENERATION
- . MASKABLE CHAINED PRIORITY INTERRUPTS
- . INPUT STROBE TO TAKE DATA FROM INPUT LATCH
- . EXTERNAL INPUT STROBE
- . OUTPUT STROBE TO PUT DATA IN OUTPUT LATCH OR TIMER LATCH
- . EXTERNAL OUTPUT STROBE
- . FOUR SENSE INPUTS SOFTWARE PROGRAMMABLE TO LEVEL OR EDGE INPUTS (Utilized by interrupts and/or SKIP commands)
- . TWO LATCHED SINGLE BIT OUTPUTS FOR EXTERNAL USE
- . TWO LATCHED SINGLE BIT OUTPUTS TO CONTROL TIMER AND 12 BIT OUTPUT LATCH
- . STRAPPABLE DEVICE SELECT CODE FOR I/O PORTS

RAM/ROM MEMORY

- . 256 x 12 BITS OF RAM
- . RAM SELECT SIGNAL STRAPPABLE FOR SIGNAL FROM ROM OR OFF BOARD
- . BI-DIRECTIONAL WITH DIRECT CONNECTION TO BUS
- . 18 PIN SOCKET FOR 6312 ROM

PROGRAMMABLE INTERVAL TIMER

- . SOFTWARE SELECTABLE TIME INTERVAL WHERE TIME INTERVAL = $T_{RC} \times 2^n$ or $T_{RC} \times 2^{n+8}$ with n SELECTABLE FROM 0 to 15
- . T_{RC} of 220 μs STANDARD - OTHER VALUES OPTIONAL BY COMPONENT CHANGES
- . STRAPPABLE SERVICE REQUEST PRIORITY

TWELVE BIT INPUT PORT

- . LATCHED 12 BIT INPUT
- . EXTERNAL LOAD CONTROL
- . STRAPPABLE INTERRUPT/SKIP REQUEST
- . 18 PIN DUAL IN-LINE CONNECTOR SOCKET

TWELVE BIT OUTPUT PORT

- . LATCHED 12 BIT OUTPUT
- . EXTERNAL TRI-STATE OUTPUT CONTROL
- . STRAPPABLE INTERRUPT/SKIP REQUEST
- . 18 PIN DUAL IN-LINE CONNECTOR

CONNECTOR

- . 60 PIN EDGE CONNECTOR (0.100 X 0.200 inch centers)
- . MATING CONNECTORS - EDAC 345-060, SAE 7000-060
- . COMMON MULTIPLEXED BUS FOR MEMORY OR I/O DATA AND ADDRESS INFORMATION
- . UNASSIGNED PINS FOR STRAPPABLE INTERCONNECT SIGNALS

PHYSICAL CHARACTERISTICS

Height - 5.0 inches
Width - 4.0 inches
Depth - .55 inches
Weight - 3.75 oz.

DC POWER - TYPICALLY LESS THAN 8MA at 5V $\pm$ 10% at 25°C

OPERATING TEMPERATURE - 40°C to +85°C (Other ranges - see Table 1)

FEATURES

- 1K X 12 CMOS RAM
- SIMULATES 6312 ROM
- MAIN OR 'CP' MEMORY SELECTION
- WRITE PROTECT SWITCH
- BATTERY BACKUP (OPTIONAL)
- LP-12 COMMON BUS INTERFACE

CONFIGURATION

The LP-12D is a 1024 X 12 CMOS RAM module implemented using twelve 6518 (1024 X 1) components. The board measures 4" X 5" and interfaces with the LP-12 common bus via a 60-pin edge-board connector.

SELECTABLE OPTIONS

On-board switches cause the LP-12D to respond to MEMSEL/, CPSEL/ or the logical "OR" of these two signals from the LP-12 Computer. This allows the board to be configured as main memory, "CP" memory or both. On-board straps permit the assignment of the module to one of four 1K memory blocks starting at address 0000.

DATA PROTECT/RETENTION

Write-protect capability is provided by an on-board switch. Optional on-board batteries and power off switching logic are available to provide power off data retention.

ROM SIMULATION

Strap-programmed decoding is provided on the board to enable the generation of a RSEL/ signal such as provided by the 6312 ROM to enable external RAM. This allows the LP-12D to be used as a 6312 ROM simulator for prototyping.

SPECIFICATIONS

WORD SIZE:	12 bits
MEMORY SIZE:	1024 words
ACCESS TIME:	750 ns at 5v (see Note)
INTERFACE:	All address, data and control signals are CMOS compatible. Data lines are tri-state and bidirectional. Eighteen signals have same pinout as LP-12 module; six of the unassigned bus connector contacts may be strapped for variations of selection.
ADDRESS SELECTION:	RAM block assignment and RSEL/ assignment are strappable. RAM block starting locations can be assigned to 0000 _h , 2000 _h , 4000 _h , 6000 _h . RSEL/ starting assignments can be any modulo 256 location.
CONNECTOR:	60-pin double-sided PC edge connector with 0.100-inch contact centers. Mating connectors — EDAC 345-060 SAE 7000-060
PHYSICAL CHARACTERISTICS:	Height — 5.0 in. Width — 4.0 in. Depth — .55 in. without batteries — .6 in. with batteries Weight — 3.5 oz. without batteries — 5.0 oz. with batteries
DC POWER:	4 to 7 volt operating range 25ma max. 10ma typ. at 5 volts 10v (see Note) With battery backup add 5 ma charge current.
OPERATING TEMPERATURE:	LP 12D 0° to 75°C LP-12D/AI -40° to +85°C LP-12D/AM -55° to +125°C
BATTERY BACKUP OPTION:	Allows data retention 3.6v rechargeable battery pack Trickle charged from main supply with 5ma charge current Source power-down cutover detection.

NOTE: Consult the factory for specifications on faster extended voltage range LP-12D/A plus extended temperature range LP-12D/AI and LP-12D/AM modules.

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INCORPORATED

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FEATURES

- Interfaces LP-12 computer to teletype, other terminals
- Supplied with 20mA current loop TRANSMIT and RECEIVE modules (RS232 module optional)
- Provision for READER RUN control
- Second I/O port for control signals and CMOS serial I/O
- Ten pin flat wire header connectors for each I/O port
- RUN-HALT and RESET switches, LED RUN indicator
- Optional multiple BAUD RATE selection

The LP-12F terminal interface plugs directly into the LP-12 computer system bus and provides a complete interface to asynchronous serial devices such as teletypes and CRT terminals. Switches for RESET, RUN/HAULT, PIE ADDRESS, PARITY, STOP BIT, CHARACTER LENGTH, and BAUD RATE (optional) permit hardware control of these functions. A strapping socket with 7 lines connected to unassigned bus lines allows the user to convey clock, baud rate, or other signals between components plugged into the LP-12 bus. Nine control lines from the LP-12 bus to the PIE establish priorities, skips or interrupts, direct data to and from the selected I/O port, implement edge or level sensitivity of skip/interrupt signals from peripherals and perform other control functions.

The LP-12F MR option allows the user to select one of several different baud rates for each of the two I/O ports. Rates from 50 to 9600 baud are selected by operating dip switches on the board. Control circuits are included to direct each baud rate to the appropriate I/O port in response to program commands.

SPECIFICATIONS

I/O PORT #1:	Supplied with 20mA TRANSMIT and RECEIVE modules for standard teletypes. Optional RS232 or special plugable modules built on 16 pin plug in carriers permit program control of teletype reader (READER RUN) or custom interface to other terminals
I/O PORT #2:	Independant READ and WRITE signals 2 latched single bit FLAG outputs 1 single bit READER RUN output 2 single bit edge or level sensitive SKIP or INTERRUPT inputs Program control of edge/level sensitivity, SKIP or INTERRUPT selection WRITE signal active high or low CMOS SERIAL INPUT and OUTPUT at second selected baud rate with port 1 disabled under program control.
MULTIPLE BAUD RATE: (OPTIONAL)	Baud rates of 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, and 9600 independently selectable by dip switch for I/O ports 1 and 2 Strap option for 19,200 baud.
HARDWARE CONTROL, SELECTION FEATURES:	RUN-HALT, RESET pushbuttons RUN indicator (LED) PIE address established by dip switch Word length, stop bit, and parity established by dip switches Maskable chained priority interrupts External or internal clock
POWER REQUIREMENT:	45mA max @ 5V using 20mA TTY LOOP
OPERATING TEMPERATURE:	0° to 75°C Standard
MECHANICAL:	Dimensions: 5"H x 4"W x 0.7"D Weight: 4 oz. Bus connector: 60 pin edge (card plugs into LP-12 bus which uses EDAC 345-060, SAE 7000-060 or other with 0.1 x 0.2 inch centers) Port connectors: 3M type 3491 header

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LP-12 Low Power 12-Bit Computer Board

LP-12J(CP) Control Panel Module

LP-12F-MR Terminal Interface Board

LP-12D 1K RAM Module

INTRODUCTION

2

HM-6100 MICROPROCESSOR

At the time Harris Semiconductor made its July 1967 decision to focus on the industrial integrated circuits market place, the company already possessed a foundation of state-of-the-art technology based on nearly a decade of developing hi-rel circuits for demanding military applications.

A natural vehicle for extending high performance into the industrial market was CMOS where the Harris process of self-aligned silicon gates promised speed/performance products several times that offered in the early 70's. The Harris CMOS process provides 1024 bits of self-aligned silicon gate memory where only 256 bits would be available with metal gate design. And, in speed, CMOS now rivals bipolar technology.

The broad Harris product base supports the HM-6100 microprocessor with specific microprocessor peripheral devices and a full complement of general purpose circuits. These include CMOS memories from 64 through 1024 bits, PROM's from 256 through 4096 bits, all major CMOS logic families, and linear interface circuits, such as keyboard encoders, analog switches, D/A's and comparators.

The HM-6100 is a single address, fixed word length, parallel transfer microprocessor using 12-bit, two's complement arithmetic. The processors recognize the instruction set of Digital Equipment Corporation's PDP8/E minicomputer. The internal circuitry is completely static and is designed to operate at any speed between DC and the maximum operating frequency. Two pins are available to allow for an external crystal thereby eliminating the need for clock generators and level translators. The crystal can be removed and the processor clocked by an external clock generator. A 12-bit memory-accumulator ADD instruction, using a +5 volt supply, is performed in 5 μ sec by the HM-6100, in 6 μ sec by the HM-6100C and in 2.5 μ sec by the HM-6100A using a +10 volt supply. The device design is optimized to minimize the number of external components required for interfacing with standard memory and peripheral devices.

FEATURES

DESIGN

- Silicon Gate Complementary MOS
- Fully Static-0 to 8 MHz
- Single Power Supply
 - HM-6100/C $V_{cc}=5$ volts
 - HM-6100A $V_{cc}=10$ volts
- Crystal Controlled On Chip Timing
- Low Power Dissipation < 10 mW @ 4 MHz @ 5 volts
- Single Power Supply $4V \leq V_{cc} \leq 11V$
- TTL Compatible at 5 Volts
- Excellent Noise Immunity
- -55°C to $+125^{\circ}\text{C}$ Operation

INTERFACE

- Memory—Any Speed
- Control Panel
- Switch Register
- Asynchronous CPU—Memory and CPU—Device Communication
- 64 I/O Devices with PDP-8/E Compatible Interface
- Device Controlled Input-Output
- All Control Signals Produced By The CPU
- Power-on Initialize

ARCHITECTURAL

- Executes PDP-8/E, Instruction Set
- Direct, Indirect, and Autoindexed Memory Addressing
- 12-Bit Memory Accumulator ADD Instruction
 - HM-6100 $5\mu\text{sec}$ @ $+5$ volts/4.0 MHz
 - HM-6100A $2.5\mu\text{sec}$ @ $+10$ volts/8.0 MHz
 - HM-6100C $6\mu\text{sec}$ @ $+5$ volts/3.3 MHz
- Input-Output Instruction
 - HM-6100 $8.5\mu\text{sec}$ @ $+5$ volts/4.0 MHz
 - HM-6100A $4.25\mu\text{sec}$ @ $+10$ volts/8 MHz
 - HM-6100C $10.2\mu\text{sec}$ @ $+5$ volts/3.3 MHz
- Single-Clock, Single-Instruction Capability
- Direct Memory Access (DMA)
- Interrupt
- Dedicated Control Panel Features

APPLICATIONS

- Intelligent Computer Terminals
- POS Terminals
- Portable Terminals
- Aerospace/Satellite System
- Automotive Systems
- Remote Data Acquisition Systems
- Process Control
- Instrumentation
- Medical Electronics
- Displays
- Traffic Control
- Navigation

PIN ASSIGNMENTS

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PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1	V _{cc}		Supply voltage
2	RUN	H	The signal indicates the runstate of the CPU and may be used to power down the external circuitry
3	DMAGNT	H	Direct Memory Access Grant—DX lines are three state
4	DMAREQ	L	Direct Memory Access Request—DMA is granted at the end of the current instruction. Upon DMA grant, the CPU suspends program execution until the DMAREQ line is released.
5	CPREQ	L	Control Panel Request—a dedicated interrupt which bypasses the normal device interrupt request structure
6	RUN HLT	L	Pulsing the Run/Halt line causes the CPU to alternately run and halt by changing the state of the internal RUN HLT flip flop
7	RESET	L	Clears the AC and loads 7777 into the PC. CPU is halted
8	INTREQ	L	Peripheral device interrupt request
9	XT ₁	H	External coded minor cycle timing—signifies input transfers to the HM-6100

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
10	LXMAR	H	The Load External Address Register is used to store memory and peripheral address externally
11	WAIT	L	Indicates that peripherals or external memory is not ready to transfer data. The CPU state gets extended as long as WAIT is active. The CPU is in the lowest power state with clocks running
12	XT ₂	H	External coded minor cycle timing—signifies output transfers from the HM-6100
13	XT _c	H	External coded minor cycle timing—used in conjunction with the Select Lines to specify read or write operations
14	OSC OUT		Crystal input to generate the internal timing (also external clock input)
15	OSC IN		See Pin 14—OSC OUT (also external clock ground)
16	DX ₀		DataX—multiplexed data in, data out and address lines
17	DX ₁		See Pin 16—DX ₀
18	DX ₂		See Pin 16—DX ₀
19	DX ₃		See Pin 16—DX ₀
20	DX ₄		See Pin 16—DX ₀

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
21	DX ₅		See Pin 16—DX ₀
22	DX ₆		See Pin 16—DX ₀
23	DX ₇		See Pin 16—DX ₀
24	DX ₈		See Pin 16—DX ₀
25	DX ₉		See Pin 16—DX ₀
26	GND		Ground
27	DX ₁₀		See Pin 16—DX ₀
28	DX ₁₁		See Pin 16—DX ₀
29	LINK	H	Link flip flop
30	DEVSEL	L	Device Select for I/O transfers
31	SWSEL	L	Switch Register Select for the OR THE SWITCH REGISTER INSTRUCTION (OSR). OSR is a Group 2 Operate Instruction which reads a 12 bit external switch register and OR's it with the contents of the AC.
32	C	L	Control line inputs from the peripheral device during an I/O transfer (Table 5).

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
33	C	L	See Pin 32—C
34	C	L	See Pin 32—C
35	SKP	L	Skips the next sequential instruction if active during an I/O instruction
36	IFETCH	H	Instruction Fetch Cycle
37	MEMSEL	L	Memory Select for memory transfers
38	CPSEL	L	The Control Panel Memory Select becomes active, instead of the MEMSEL, for control panel routines. Signal may be used to distinguish between control panel and main memories.
39	INTGNT	H	Peripheral device Interrupt Grant
40	DATAF	H	Data Field pin indicates the execute phase of indirectly addressed AND, TAD, ISZ and DCA instructions so that the data transfers are controlled by the Data Field, DF, and not the Instruction Field, IF, if Extended Memory Control hardware is used to extend the addressing space from 4K to 32K words

SPECIFICATIONS

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage

HM-6100-C -4.0V to +7.0V

HM-6100A -4.0V to +11.0V

GND 0.3V to V_{CC} -0.3V

-65°C to +125°C

Operating Temperature Range

Commercial

Industrial

Military

0°C to +70°C

-40°C to +85°C

-55°C to +125°C

Input or Output Voltage Applied

Storage Temperature Range

DC CHARACTERISTICS

$V_{CC} = 5.0 \text{ V} \pm 10\%$ (HM-6100)

$V_{CC} = 10.0 \text{ V} \pm 10\%$ (HM-6100A)

$V_{CC} = 5.0 \text{ V} \pm 5\%$ (HM-6100C)

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (HM-6100-9/6100A-9)

$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ (HM-6100-2/6100A-2)

$T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ (HM-6100C-5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		70% V_{CC}			V
Logical "0" Input Voltage	V_{IL}				20% V_{CC}	V
Input Leakage (HM-6100/6100A) (HM-6100-5)	I_{IL}	$0 \text{ V} \leq V_{IN} \leq V_{CC}$	-1.0 -10.0		1.0 10.0	μA
Logical "1" Output Voltage	V_{OH2}	$I_{OUT} = 0$	$V_{CC} - 0.01$			V
Logical "1" Output Voltage	V_{OH1}	$I_{OH} = -0.2 \text{ mA}$	2.4			V
Logical "0" Output Voltage	V_{OL2}	$I_{OUT} = 0$			GND + 0.01	V
Logical "0" Output Voltage	V_{OL1}	$I_{OL} = 1.6 \text{ mA}$			0.45	V
Output Leakage (HM-6100/6100A) (HM-6100C)	I_O	$0 \text{ V} \leq V_O \leq V_{CC}$	-1.0 -10.0		1.0 10.0	μA
Supply Current (HM-6100) (HM-6100A) (HM-6100C)	I_{CC}	$V_{CC} = 5.0 \text{ volts}^1$ $V_{CC} = 10.0 \text{ volts}^1$ $V_{CC} = 5.0 \text{ volts}^1$			2.5 10.0 5.0	mA
Input Capacitance	C_{IN}			5.0		pF
Output Capacitance	C_O			8.0		pF

NOTE 1: I_{CC} measured at $C_L = 50 \text{ pF}$. F_{CLOCK} = Operating Frequency; $T_A = +25^\circ\text{C}$

ORDERING INFORMATION Circuit marking and product code explanation

HM1-6100A-2

Temperature Range

-2: -55°C to $+125^\circ\text{C}$

-9: -40°C to $+85^\circ\text{C}$

-5: 0°C to $+75^\circ\text{C}$

Version

A: 10.0V

C or Blank: 5.0V nominal

Specific Type

Package Code

HARRIS

ARCHITECTURE

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The HM-6100 has 6 twelve bit registers, a programmable logic array, an arithmetic and logic unit and associated gating and timing circuitry. A block diagram of the HM-6100 is shown in Figure 1.

FIGURE 1

ACCUMULATOR (AC)

The AC is a 12-bit register with which arithmetic and logical operations are performed. Data words may be fetched from memory to the AC or stored from the AC into memory. Arithmetic and logical operations involve two operands, one held in the AC and the other fetched from the memory. The result of the operation is left in the AC. The AC may be cleared, complemented, tested, incremented or rotated under program control. The AC also serves as an input-output register. All programmed data transfers pass through the AC.

LINK (L)

The Link is a 1-bit flip-flop that serves as a high-order extension of the AC. It is used as a carry flip-flop for 2's complement arithmetic. A carry out of the ALU complements the Link. Link can be cleared, set, complemented and tested under program control and rotated as part of the AC.

MQ REGISTER (MQ)

The MQ is a 12-bit temporary register which is program accessible. The contents of AC may be transferred to the MQ for temporary storage. MQ can be OR'ed with the AC and the result stored in the AC. The contents of the AC and the MQ may also be exchanged.

MEMORY ADDRESS REGISTER (MAR)

While accessing memory, the 12-bit MAR register contains the address of the memory location that is currently selected for reading or writing. The MAR is also used as an internal register for microprogram control during data transfers to and from memory and peripherals.

PROGRAM COUNTER (PC)

The 12-bit PC contains the address of the memory location from which the next instruction is fetched. During an instruction fetch, the

PC is transferred to MAR and the PC is then incremented by 1. When there is a branch to another address in memory, the branch address is set into the PC. Branching normally takes place under program control. However, during an input-output operation, a device may specify a branch address. A skip (SKP) instruction increments the PC by 1, thus causing the next instruction to be skipped. The SKP instruction may be unconditional or conditional on the state of the AC and/or the Link. During an input-output operation, a device can also cause the next sequential instruction to be skipped.

ARITHMETIC AND LOGICAL UNIT (ALU)

The ALU performs both arithmetic and logical operations—2's complement binary addition, AND, OR and complement. The ALU can perform a single position shift either to the left or to the right. A double rotate is implemented in two single bit shifts. The ALU can also shift by 3 positions to implement a byte swap in two steps. The AC is always one of the inputs to the ALU. However, under internal microprogram control, AC may be gated off and all one's or all zero's gated in. The second input may be any one of the other registers under internal microprogram control.

TEMPORARY REGISTER (TEMP)

The 12-bit TEMP register latches the result of an ALU operation before it is sent to the destination register to avoid race conditions. The TEMP is also used as an internal register for microprogram control.

INSTRUCTION REGISTER (IR)

During an instruction fetch, the 12-bit IR contains the instruction that is to be executed by the CPU. The IR specifies the initial step of the microprogram sequence for each instruction and is also used as an internal register to store temporary data for microprogram control.

MULTIPLEXER (DX)

The 12-bit Input/Output Multiplexer handles data, address and instruction transfers, into and out of, the CPU, from or into, the main memory and peripheral devices on a time-multiplexed basis.

MAJOR STATE GENERATOR AND THE PROGRAMMED LOGIC ARRAY (PLA)

During an instruction fetch the instruction to be executed is loaded into the IR. The PLA is then used for the correct sequencing of the CPU for the appropriate instruction. After an instruction is completely sequenced, the major state generator scans the internal priority network. The state of the priority network decides whether the machine is going to fetch the next instruction in sequence or service one of the external request lines.

PLA OUTPUT LATCH

The PLA Output Latch latches the PLA output thereby permitting the PLA to be pipelined; it fetches the next control sequence while the CPU is executing the current sequence.

MEMORY AND DEVICE CONTROL, ALU AND REG TRANSFER LOGIC

The Memory and Device Control Unit provides external control signals to communicate with peripheral devices (DEVSEL), switch register (SWSEL), memory (MEMSEL) and/or control panel memory (CPSEL). During I/O instructions this unit also modifies the PLA outputs depending on the states of the four device control lines (SKP, C₀, C₁, C₂). The ALU and Register Transfer Logic provides the control signals for the internal register transfers and ALU operation.

TIMING AND STATE CONTROL

The HM-6100 generates all the timing and state signals internally. A crystal is used to control the CPU operating frequency. The CPU divides the crystal frequency by two. With a 4MHz crystal, the internal states will be of 500ns duration. The major timing states are described in Figure 2.

T₁ For memory reference instructions, a 12-bit address is sent on the DataX, DX, lines. The Load External Address Register, LXMAR, is used to clock an external register to store the address information externally, if required. When executing an Input-Output I/O instruction, the instruction being executed is sent on the DX lines to be stored externally. The external address register then contains the device address and control information.

Various CPU request lines are priority sampled if the next cycle is an Instruction Fetch cycle. Current state of the CPU is available externally.

T₂ Memory/Peripheral data is read for an input transfer (READ). WAIT controls the transfer duration. If WAIT is active during input transfers, the CPU waits in the T₂ state. The wait duration is an integral multiple of the crystal frequency—250ns for 4MHz.

For memory reference instructions, the Memory Select, MEMSEL, line is active. For I/O instructions the Device Select, DEVSEL, line is active. Control lines, therefore, distinguish the contents of the external register as memory or device address.

External device sense lines, C₀, C₁, C₂, and SKP, are sampled if the instruction being executed is an I/O instruction.

Control Panel Memory Select, CPSEL, and Switch Register Select, SWSEL, become active low for data transfers between the HM-6100 and Control Panel Memory and the Switch Register, respectively.

T₃, T₄, T₅ ALU operation and internal register transfers.

T₆ This state is entered for an output transfer (WRITE). The address is defined during T₁. WAIT controls the time for which the Write data must be maintained.

FIGURE 2

HM-6100 TIMING AND STATE SIGNALS

AC CHARACTERISTICS (T_A = 25°C), Derate 0.30%/°C

PARAMETER	SYMBOL	HM-6100 V _{CC} = 5.0 f _c = 4MHz		HM-6100A V _{CC} = 10.0 f _c = 8 MHz		HM-6100C V _{CC} = 5.0 f _c = 3.3MHz		UNITS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Major State Time	T _s	500		250		600		ns
Address Setup Time	t _{AS}	50		30		80		ns
Address Hold Time	t _{AH}							ns
Access Time From LXMAR	t _{AL}	500		250		600		ns
Read Pulse Width	t _{RP}	700		350		800		ns
Write Pulse Width	t _{WP}							ns
Data Setup Time	t _{DS}	240		120		280		ns
Data Hold Time	t _{DH}			50		160		ns

MEMORY AND PROCESSOR INSTRUCTIONS

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The HM-6100 instructions are 12-bit words stored in memory. The HM-6100 makes no distinction between instructions and data; it can manipulate instructions as stored variables or execute data as instructions when it is programmed to do so. There are three general classes of HM-6100 instructions. They are referred to as Memory Reference Instruction (MRI), Operate Instruction (OPR) and Input/Output Transfer Instruction (IOT).

Before proceeding further, we will discuss the Specific Memory Organization with which the HM-6100 interfaces.

MEMORY ORGANIZATION

The HM-6100 has a basic addressing capacity of 4096 12-bit words. The addressing capacity may be extended by Extended Memory Control hardware. The memory system is organized in 4096 word blocks, called MEMORY FIELDS. The first 4096 words of memory are in Field 0. If a full 32K of memory is installed, the uppermost Memory Field will be numbered 7. In any given Memory Field every location has a unique 4 digit octal (12 bit binary) address, 0000₈ to 7777₈ (0000₁₀ to 4095₁₀). Each Memory Field is subdivided into 32 PAGES of 128 words each. Memory Pages are numbered sequentially from Page 00₈, containing addresses 0000-0177₈, to Page 37₈, containing addresses 7600₈-7777₈. The first 5 bits of a 12-bit MEMORY ADDRESS denote the PAGE NUMBER and the low order 7 bits specify the PAGE ADDRESS of the memory location within the given Page.

MEMORY ORGANIZATION

During an instruction fetch cycle, the HM-6100 fetches the instruction pointed to by the PC. The contents of the PC are transferred to the MAR. The PC is incremented by 1. The PC now contains the address of the 'next' sequential instruction. The MAR contains the address of the 'current' instruction which must be fetched from memory. Bits 0-4 of the MAR identify the CURRENT PAGE, that is, the Page from which instructions are currently being fetched and bits 5-11 of the MAR identify the location within the Current Page. (PAGE ZERO (0), by definition, denotes the first 128 words of memory, 0000₈-0177₈.)

MEMORY REFERENCE INSTRUCTIONS (MRI)

The Memory Reference Instructions operate on the contents of a memory location or use the contents of a memory location to operate on the AC or the PC. The first 3 bits of a Memory Reference Instruction specify the operation code, or OPCODE, and the low order 9 bits, the OPERAND address, as shown in Figure 3.

FIGURE 3

MEMORY REFERENCE INSTRUCTION FORMAT

Bits 5 through 11, the PAGE ADDRESS, identify the location of the OPERAND on a given page, but they do not identify the page itself. The page is specified by bit 4, called the CURRENT PAGE OR PAGE 0 BIT. If bit 4 is a 0, the page address is interpreted as a location on Page 0. If bit 4 is a 1, the page address specified is interpreted to be on the Current Page.

For example, if bits 5 through 11 represent 123₈, and bit 4 is a 0, the location referenced is the absolute address 0123₈. However, if bit 4 is a 1 and the current instruction is in a memory location whose absolute address is 4610₈, the page address 123₈ designates the absolute address 4723₈, as shown below.

$$4610_8 = 100\ 110\ 001\ 000 = \text{PAGE } 10\ 011 = \text{PAGE } 23,$$

Location 4610₈ is in PAGE 23. Location 123₈ in PAGE 23, CURRENT PAGE, will be:

$$10\ 011, 1\ 010\ 011 = 100\ 111\ 010\ 011 = 4723_8$$

PAGE NUMBER 23, PAGE ADDRESS 123₈

By this method, 256 locations may be directly addressed, 128 on PAGE 0 and 128 on the CURRENT PAGE. Other locations are addressed by utilizing bit 3. When bit 3 is a 0, the operand address is a DIRECT ADDRESS. An INDIRECT ADDRESS (pointer address) identifies the location that contains the desired address (effective address). To address a location that is not directly addressable, not in PAGE 0 or in the CURRENT PAGE, the absolute address of the desired location is stored in one of the 256 directly addressable locations (pointer address). Upon execution, the MRI will operate on the contents of the location identified by the address contained in the pointer location.

It should be noted that locations 0010₈-0017₈ in PAGE 0 are AUTOINDEXED. If these locations are addressed indirectly, the contents are incremented by 1 and restored before they are used as the operand address. These locations may, therefore, be used in indexing applications.

Table 1 lists the mnemonics for the five memory reference instruction, their OPCODE, the operations they perform, the number of states and the execution time at +5.0V and +10.0V, assuming a crystal frequency of 3.3MHz, 4MHz and 8MHz or a state time period of 600ns, 500ns and 250ns, respectively.

It should be noted that the data is represented in Two's Complement Integer notation. In this system, the negative of a number is formed by complementing each bit in the data word and adding "1" to the complemented number. The sign is indicated by the most significant bit. In the 12-bit word used by the HM-6100, when bit 0 is a "0", it denotes a positive number and when bit 0 is a "1", it denotes a negative number. The maximum number ranges for this system are 3777₈ (+2047) and 4000₈ (-2048).

Notations applied in Table 1, are defined as follows:

- () Denotes the contents of the register or location within the parenthesis. (EA) is read as "... the contents of the Effective Address".
- (()) Denotes the contents of the location pointed to by the contents of the location within the double parenthesis. ((PA)) is read as "... the contents of the location pointed to by the contents of the Pointer Address."

← Denotes "... is replaced by ..."

^ Denotes, logical AND operation

∨ Denotes, logical OR operation

TABLE 1

MNE- MONIC	OP CODE	OPERATION	NUMBER OF STATES	EXECUTION TIME (μs)		
				HM-6100 +5.0V 4MHz	HM-6100A +10.0V 8MHz	HM-6100C +5.0V 3.3MHz
AND	0	LOGICAL AND DIRECT (I = 0) Operation: (AC) ← (AC) & (EA) Description: Contents of the EA are logically AND'ed with the contents of the AC and the result is stored in AC.	10	6.0	2.50	6.0
		LOGICAL AND INDIRECT (I = 1, PA ≠ 0010-0017) Operation: (AC) ← (AC) & ((PA))	15	7.5	3.75	9.0
		LOGICAL AND AUTOINDEX (I = 1, PA = 0010-0017) Operation: (PA) ← (PA) + 1; (AC) ← (AC) & ((PA))	16	8.0	4.00	9.6
TAD	1	BINARY ADD DIRECT (I = 0) Operation: (AC) ← (AC) + (EA) Description: Contents of the EA are ADD'ed with the contents of the AC and the result is stored in the AC; carry out complements the LINK. If AC is initially cleared, this instruction acts as LOAD from Memory.	10	5.0	2.50	6.0
		BINARY ADD INDIRECT (I = 1, PA ≠ 0010-0017) Operation: (AC) ← (AC) + ((PA))	15	7.5	3.75	9.0
		BINARY ADD AUTOINDEX (I = 1, PA = 0010-0017) Operation: (PA) ← (PA) + 1; (AC) ← (AC) + ((PA))	16	8.0	4.00	9.6
ISZ	2	INCREMENT AND SKIP IF ZERO DIRECT (I = 0) Operation: (EA) ← (EA) + 1; if (EA) = 0000, PC ← PC + 1 Description: Contents of the EA are incremented by 1 and restored. If the result is zero, the next sequential instruction is skipped.	16	8.0	4.00	9.6
		INCREMENT AND SKIP IF ZERO INDIRECT (I = 1, PA ≠ 0010-0017) Operation: ((PA)) ← ((PA)) + 1; if ((PA)) = 0000, PC ← PC + 1	21	10.5	5.25	12.6
		INCREMENT AND SKIP IF ZERO AUTOINDEX (I = 1, PA = 0010-0017) Operation: (PA) ← (PA) + 1; ((PA)) ← ((PA)) + 1; if ((PA)) = 0000, PC ← PC + 1	22	11.0	5.50	13.2
DCA	3	DEPOSIT AND CLEAR THE ACCUMULATOR DIRECT (I = 0) Operation: (EA) ← (AC); (AC) ← 0000 Description: The contents of the AC are stored in EA and the AC is cleared.	11	5.5	2.75	6.6
		DEPOSIT AND CLEAR THE ACCUMULATOR INDIRECT (I = 1, PA ≠ 0010-0017) Operation: ((PA)) ← (AC); (AC) ← 0000	16	8.0	4.00	9.0
		DEPOSIT AND CLEAR THE ACCUMULATOR AUTOINDEX (I = 1, PA = 0010-0017) Operation: (PA) ← (PA) + 1; ((PA)) ← (AC); (AC) ← 0000	17	8.5	4.25	10.2
JMS	4	JUMP TO SUBROUTINE DIRECT (I = 0) Operation: (EA) ← (PC); (PC) ← EA + 1 Description: The contents of the PC are stored in the EA. The PC is incremented by 1. Immediately after every instruction fetch: The contents of the EA now point to the next sequential instruction following the (return address). The next instruction is taken from EA + 1.	10	6.0	2.50	6.0
		JUMP TO SUBROUTINE INDIRECT (I = 1, PA ≠ 0010-0017) Operation: ((PA)) ← PC; (PC) ← ((PA)) + 1	15	7.5	3.75	9.0
		JUMP TO SUBROUTINE AUTOINDEX (I = 1, PA = 0010-0017) Operation: (PA) ← (PA) + 1; ((PA)) ← PC; (PC) ← ((PA)) + 1	16	8.0	4.00	9.6
JMP	5	JUMP DIRECT (I = 0) Operation: (PC) ← EA Description: The next instruction is taken from the EA.	10	5.0	2.50	6.0
		JUMP INDIRECT (I = 1, PA ≠ 0010-0017) Operation: (PC) ← ((PA))	15	7.5	3.75	9.0
		JUMP AUTOINDEX (I = 1, PA = 0010-0017) Operation: (PA) ← (PA) + 1; (PC) ← ((PA))	16	8.0	4.00	9.6

OPERATE INSTRUCTIONS

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The Operate Instructions, which have an OPCODE of 7₄ (111), consists of 3 groups of microinstructions. Group 1 microinstructions, which are identified by the presence of a 0 in bit 3, are used to perform logical operations on the contents of the accumulator and link. Group 2 micro instructions, which are identified by the presence of a 1 in bit 3 and a 0 in bit 11, are used primarily to test the contents of the accumulator and then conditionally skip the next sequential instruction. Group 3 microinstructions have a 1 in bit 3 and a 1 in bit 11 and are used to perform logical operations on the contents of the AC and MQ.

The basic OPR instruction format is shown in Figure 4.

Operate microinstructions from any group may be microprogrammed with other operate microinstructions of the same group. The actual code for a microprogrammed combination of two, or more, microinstructions is the bitwise logical OR of the octal codes for the individual microinstructions. When more than one operation is microprogrammed into a single instruction, the operations are performed in a prescribed sequence, with logical sequence number 1 microinstructions performed first, logical sequence number 2 microinstructions performed second, logical sequence number 3 microinstructions performed third and so on. Two operations with the same logical sequence number, within a given group of microinstructions, are performed simultaneously.

FIGURE 4

GROUP 1 MICROINSTRUCTIONS

Figure 5 shows the instruction format of a group 1 microinstruction. Any one of bits 4 to 11 may be set, loaded with a binary 1, to indicate a specific group 1 microinstruction. If more than one of these bits is set, the instruction is a microprogrammed combination of group 1 microinstructions, which will be executed according to the logical sequence shown in Figure 5.

Table 2 lists commonly used group 1 microinstructions, their assigned mnemonics, octal number, instruction format, logical sequence, the operation they perform, the number of states and the execution time at +5.0V and +10.0V, assuming a crystal frequency of 3.3MHz, 4MHz and 8MHz or a state time period of 600ns, 500ns and 250ns, respectively. The same format is followed in Table 3 and 4 which correspond to group 2 and 3 microinstructions, respectively.

FIGURE 5

GROUP 1 MICROINSTRUCTION FORMAT

TABLE 2

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	OPERATION	NUMBER OF STATES	EXECUTION TIME (μ s)		
					HM-6100 +5.0V 4MHz	HM-6100A +10.0V 8MHz	HM-6100C +5.0V 3.3MHz
NOP	7000	1	NO OPERATION—This instruction causes a 10 state delay in program execution, without affecting the state of the HM-6100. It may be used for timing synchronization or as a convenient means of deleting an instruction from a program.	10	5.0	2.50	6.0
IAC	7001	3	INCREMENT ACCUMULATOR—The content of the AC is incremented by one (1) and carry out complements the Link (L).	10	5.0	2.50	6.0
RAL	7004	4	ROTATE ACCUMULATOR LEFT—The contents of the AC and L are rotated one binary position to the left. AC(0) is shifted to L and L is shifted to AC(1).	15	7.5	3.75	9.0
RTL	7006	4	ROTATE TWO LEFT—The contents of the AC and L are rotated two binary positions to the left. AC(1) is shifted to L and L is shifted to AC(10).	15	7.5	3.75	9.0
RAR	7010	4	ROTATE ACCUMULATOR RIGHT—The contents of the AC and L are rotated one binary position to the right. AC(11) is shifted to L and L is shifted to AC(0).	15	7.5	3.75	9.0
RTR	7012	4	ROTATE TWO RIGHT—The contents of the AC and L are rotated two binary positions to the right. AC(10) is shifted to L and L is shifted to AC(1).	15	7.5	3.75	9.0
BSW	7002	4	BYTE SWAP—The right six (6) bits of the AC are exchanged or SWAPPED with the left six (6) bits. AC(11) is swapped with AC(0), AC(10) with AC(5), etc. L is not affected.	15	7.5	3.75	9.0
CML	7020	2	COMPLEMENT LINK—The content of the link is complemented.	10	5.0	2.50	6.0
CMA	7040	2	COMPLEMENT ACCUMULATOR—The content of each bit of the AC is complemented, having the effect of replacing the content of the AC with its one's complement.	10	5.0	2.50	6.0
CIA	7041	2,3	COMPLEMENT AND INCREMENT ACCUMULATOR—The content of the AC is replaced with its two's complement. Carry out complements the LINK.	10	5.0	2.50	6.0
CLL	7100	1,4	CLEAR LINK—The link is loaded with binary 0.	10	5.0	2.50	6.0
CLL RAL	7104	1,4	CLEAR LINK—ROTATE ACCUMULATOR LEFT.	15	7.5	3.75	9.0
CLL RTL	7106	1,4	CLEAR LINK—ROTATE TWO LEFT.	15	7.5	3.75	9.0
CLL RAR	7110	1,4	CLEAR LINK—ROTATE ACCUMULATOR RIGHT.	15	7.5	3.75	9.0
CLL RTR	7112	1,4	CLEAR LINK—ROTATE TWO RIGHT.	15	7.5	3.75	9.0
STL	7120	1,2	SET THE LINK—The LINK is loaded with a binary 1 corresponding with a microprogrammed combination of CLL and CML.	10	5.0	2.50	6.0
CLA	7200	1	CLEAR ACCUMULATOR—The accumulator is loaded with binary 0.	10	5.0	2.50	6.0
CLA IAC	7201	1,3	CLEAR ACCUMULATOR—INCREMENT ACCUMULATOR.	10	5.0	2.50	6.0
GLT	7204	1,4	GET THE LINK—The AC is cleared, the content of L is shifted into AC(11), and L is shifted into L(1). This is a microprogrammed combination of CLA and RAL.	15	7.5	3.75	9.0
CLA CLL	7300	1	CLEAR ACCUMULATOR—CLEAR LINK.	10	5.0	2.50	6.0
STA	7240	1,2	SET THE ACCUMULATOR—Each bit of the AC is set to 1 corresponding to a microprogrammed combination of CLA and CMA.	10	5.0	2.50	6.0

GROUP 1 OPERATION MICROINSTRUCTIONS

OPERATE INSTRUCTIONS CONTINUED

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GROUP 2 MICROINSTRUCTIONS

Figure 6 shows the instruction format of group 2 microinstructions. Bits 4—10 may be set to indicate a specific group 2 microinstruction. If more than one of bits 4—7 or 9—10 is set, the instruction is a microprogrammed combination of group 2 microinstructions, which will be executed according to the logical sequence shown in Figure 6.

Skip microinstructions may be microprogrammed with CLA, OSR, or HLT microinstructions. Skip microinstructions which have a 0 in bit 8, however, may not be microprogrammed with skip microinstructions which have a 1 in bit 8. When two or more skip microinstructions are microprogrammed into a single instruction, the resulting condition on which the decision will be based is the logical OR of the individual conditions when bit 8 is 0, or, when bit 8 is 1, the decision will be based on the logical AND.

FIGURE 6

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	1	CLA	SMA SPA	SZA SNA	SNL SZL	0 1	OSR	HLT	0

LOGICAL SEQUENCES:
 1 (Bit 8 is Zero) — SMA or SZA or SNL
 (Bit 8 is One) — SPA and SNA and SZL
 2 — CLA
 3 — OSR, HLT

GROUP 2 MICROINSTRUCTION FORMAT

TABLE 3

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	OPERATION	NUMBER OF STATES	EXECUTION TIME (μs)		
					HM-6100 +5.0V 4MHz	HM-6100A +10.0V 8MHz	HM-6100C +5.0V 3.3MHz
NO	7400		NO OPERATION—NO MICROINSTRUCTIONS	10	5.0	2.50	6.0
HLT	7402	3	HALT—Program stops at the conclusion of the current machine cycle. If HLT is combined with others in OPR 2, the other operations are completed before the end of the cycle.	10	5.0	2.50	6.0
OSR	7404	3	OR WITH SWITCH REGISTER—The content of the Switch Register (SR) is ORed with the content of the AC. The result is loaded into the AC. This is equivalent to a microprogrammed combination of CLA and OSR.	15	7.5	3.75	9.0
SKP	7410	1	SKIP—The content of the PC is incremented by 1, to skip the next sequential instruction.	10	5.0	2.50	6.0
SNL	7420		SKIP ON NON-ZERO LINK—The content of L is sampled, the next sequential instruction is skipped if L contains a 1. If L contains a 0, the next instruction is executed.	10	5.0	2.50	6.0
SZL	7430	1	SKIP ON ZERO LINK—The content of L is sampled, the next sequential instruction is skipped if L contains a 0. If the L contains a 1, the next instruction is executed.	10	5.0	2.50	6.0
SZA	7440		SKIP ON ZERO ACCUMULATOR—The content of the AC is sampled, the next sequential instruction is skipped if the AC has all ones (i.e., if the AC is 1). If the AC is 0, the next instruction is executed.	10	5.0	2.50	6.0
SNA	7450	1	SKIP ON NON-ZERO ACCUMULATOR—The content of the AC is sampled, the next sequential instruction is skipped if the AC has any bits which are not 0. If every bit in the AC is 0, the next instruction is executed.	10	5.0	2.50	6.0
SZA SNL	7460		SKIP ON ZERO ACCUMULATOR OR SKIP ON NON-ZERO LINK OR BOTH	10	5.0	2.50	6.0
SNA SZL	7470	1	SKIP ON NON-ZERO ACCUMULATOR AND SKIP ON ZERO LINK	10	5.0	2.50	6.0
SMA	7500		SKIP ON MINUS ACCUMULATOR—The content of AC (0) contains a 1, indicating that the AC contains a negative two's complement number, the next sequential instruction is skipped. If AC (0) contains a 0, the next instruction is executed.	10	5.0	2.50	6.0
SPA	7510	1	SKIP ON POSITIVE ACCUMULATOR—The contents of AC (0) are sampled. If AC (0) contains a 0, indicating that the AC contains a positive two's complement number, the next sequential instruction is skipped. If AC (0) contains a 1, the next instruction is executed.	10	5.0	2.50	6.0
SMA SNL	7520		SKIP ON MINUS ACCUMULATOR OR SKIP ON NON-ZERO LINK OR BOTH	10	5.0	2.50	6.0
SPA SZL	7530	1	SKIP ON POSITIVE ACCUMULATOR AND SKIP ON ZERO LINK	10	5.0	2.50	6.0
SMA SZA	7540		SKIP ON MINUS ACCUMULATOR OR SKIP ON ZERO ACCUMULATOR OR BOTH	10	5.0	2.50	6.0
SPA SNA	7550	1	SKIP ON POSITIVE ACCUMULATOR AND SKIP ON NON-ZERO ACCUMULATOR	10	5.0	2.50	6.0
SMA SZA SNL	7560		SKIP ON MINUS ACCUMULATOR OR SKIP ON ZERO ACCUMULATOR OR SKIP ON NON-ZERO LINK OR ALL	10	5.0	2.50	6.0
SPA SNA SZL	7570	1	SKIP ON POSITIVE ACCUMULATOR AND SKIP ON NON-ZERO ACCUMULATOR AND SKIP ON ZERO LINK	10	5.0	2.50	6.0
CLA	7600		CLEAR ACCUMULATOR—The AC is loaded with binary 0.	10	5.0	2.50	6.0
LAS	7604	1,3	LOAD ACCUMULATOR WITH SWITCH REGISTER—The content of the AC is loaded with the content of the SR, bit for bit. This is equivalent to a microprogrammed combination of CLA and OSR.	15	7.5	3.75	9.0
SZA CLA	7640	1,2	SKIP ON ZERO ACCUMULATOR THEN CLEAR ACCUMULATOR	10	5.0	2.50	6.0
SNA CLA	7650	1,2	SKIP ON NON-ZERO ACCUMULATOR THEN CLEAR ACCUMULATOR	10	5.0	2.50	6.0
SMA CLA	7700		SKIP ON MINUS ACCUMULATOR THEN CLEAR ACCUMULATOR	10	5.0	2.50	6.0
SPA CLA	7710	1,2	SKIP ON POSITIVE ACCUMULATOR THEN CLEAR ACCUMULATOR	10	5.0	2.50	6.0

GROUP 3 MICROINSTRUCTIONS

Figure 7 shows the instruction format of group 3 microinstructions which requires bits 3 and 11 to contain a 1. Bits 4, 5 or 7 may be set to indicate a specific group 3 microinstruction. If more than one of the bits is set, the instruction is a microprogrammed combination of group 3 microinstructions following the logical sequence listed in Figure 7.

FIGURE 7

GROUP 3 MICROINSTRUCTION FORMAT

TABLE 4

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	OPERATION	NUMBER OF STATES	EXECUTION TIME (μ s)		
					HM-6100 +5.0V 4MHz	HM-6100A +10.0V 8MHz	HM-6100C +5.0V 3.3MHz
NOF	7401	1	NO OPERATION—See Group 1 Microinstructions.	10	5.0	2.50	6.0
MQL	7421	2	MQ REGISTER LOAD—The content of the AC is loaded into the MQ, the AC is cleared and the original content of the MQ is lost.	10	5.0	2.50	6.0
MOA	7501	2	MQ REGISTER INTO ACCUMULATOR—The content of the MQ is OR'ed with the content of the AC and the result is loaded into the AC. The original content of the AC is lost but the original content of the MQ is retained. This instruction provides the program with an included OR operation.	10	5.0	2.50	6.0
SWP	7521	3	SWAP ACCUMULATOR AND MQ REGISTER—The content of the AC and MQ are interchanged accomplishing a microprogrammed combination of MOA and MQL.	10	5.0	2.50	6.0
CLA	7601	1	CLEAR ACCUMULATOR	10	5.0	2.50	6.0
CAM	7621	3	CLEAR ACCUMULATOR AND MQ REGISTER—The content of the AC and MQ are loaded with binary 0's. This is equivalent to a microprogrammed combination of CLA and MQL.	10	5.0	2.50	6.0
AC	7701	1	CLEAR ACCUMULATOR AND LOAD MQ REGISTER INTO ACCUMULATOR—This is equivalent to a microprogrammed combination of CLA and MQL.	10	5.0	2.50	6.0
CLA SWP	7721	3	CLEAR ACCUMULATOR AND SWAP ACCUMULATOR AND MQ REGISTER—The content of the AC is cleared. The content of the MQ is loaded into the AC and the MQ is cleared.	10	5.0	2.50	6.0

GROUP 3 OPERATE MICROINSTRUCTIONS

FIGURE 8

OSR INSTRUCTION TIMING

INPUT/OUTPUT TRANSFER INSTRUCTIONS (IOT)

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The input/output transfer instructions, which have an OPCODE of 6_h, are used to initiate the operation of peripheral devices and to transfer data between peripherals and the HM-6100. Three types of data transfer may be used to receive or transmit information between the HM-6100 and one or more peripheral I/O devices. PROGRAMMED DATA TRANSFER provides a straightforward means of communicating with relatively slow I/O devices, such as Teletypes, cassettes, card readers and CRT displays. INTERRUPT TRANSFERS use the interrupt system to service several peripheral devices simultaneously, on an intermittent basis, permitting computational operations to be performed concurrently with the data I/O operations. Both Programmed Data Transfers and Program Interrupt Transfers use the accumulator as a buffer, or storage area, for all data transfers. Since data may be transferred only between the accumulator and the peripheral, only one 12 bit word at a time may be transferred. DIRECT MEMORY ACCESS, DMA, transfers variable-size blocks of data between high-speed peripherals and the memory with a minimum of program control required by the HM-6100.

IOT INSTRUCTION FORMAT

The Input/Output Transfer Instruction format, the number of states and the execution time at +5.0V and +10.0V, assuming a crystal frequency of 3.3MHz, 4MHz and 8MHz or a state time period of 600ns, 500ns and 250ns, respectively is represented in Figure 9.

The first three bits, 0-2, are always set to 6_h (110) to specify an IOT instruction. The next six bits, 3-8, contain the device selection code that determines the specific I/O device for which the IOT instruction is intended and, therefore, permit interface with up to 64 I/O devices. The last three bits, 9-11, contain the operation specification code that determines the specific operation to be performed. The nature of this operation for any given IOT instruction depends entirely upon the circuitry designed into the I/O device interface.

PROGRAMMED DATA TRANSFER

Programmed Data Transfer is the easiest, simplest, most convenient and most common means of performing data I/O. For micro-processor applications, it may also be the most cost effective

approach. The data transfer begins when the HM-6100 fetches an instruction from the memory and recognizes that the current instruction is an IOT. This is referred to as IFETCH and consists of five (5) internal states. The HM-6100 sequences the IOT instruction through a 2-cycle execute phase referred to as IOT_A and IOT_B. Bits 0-11 of the IOT instruction are available on DX 0-11 at IOT_A · LXMAR. These bits must be latched in an external address register. DEVSEL is active low to enable data transfers between the HM-6100 and the peripheral device(s). Input-Output Instruction Timing is shown in Figure 10. The selected peripheral device communicates with the HM-6100 through 4 control lines—C₀, C₁, C₂ and SKP. In the HM-6100 the type of data transfer, during an IOT instruction, is specified by the peripheral device(s) by asserting the control lines as shown in Table 5.

The control line SKP, when low during an IOT, causes the HM-6100 to skip the next sequential instruction. This feature is used to sense the status of various signals in the device interface. The C₀, C₁, and C₂ lines are treated independently of the SKP line. In the case of a RELATIVE or ABSOLUTE JUMP, the skip operation is performed after the jump. The input signals to the HM-6100, DX 0-11, C₀, C₁, C₂, and SKP, are sampled at IOT_A during DEVSEL · XT_C. The data from the HM-6100 is available to the device(s) during DEVSEL · XT_C. IOT_B cycle is internal to the HM-6100 to perform the operations requested during IOT_A. Both IOT_A and IOT_B consist of six (6) internal states.

In summary, Programmed Data Transfer performs data I/O with a minimum of hardware support. The maximum rate at which programmed data transfers may take place is limited by the HM-6100 instruction execution rate. However, the data rate of the most common, used peripheral devices is much lower than the maximum rate at which programmed transfers can take place in the HM-6100. The major drawback associated with Programmed Data Transfer is that the HM-6100 must hang up in a waiting loop while the I/O device completes the last transfer and prepares for the next transfer. On the other hand, this technique permits easy hardware implementation and simple, economical interface design. For this reason, almost all devices except bulk storage units rely heavily on programmed data transfer for routine data I/O.

FIGURE 9

IOT INSTRUCTION FORMAT

NUMBER OF STATES	EXECUTION TIME (μs)		
	HM-6100 +5.0V 4MHz	HM-6100A +10.0V 8MHz	HM-6100C +5.0V 3.3MHz
17	8.5	4.25	10.2

IOT NUMBER OF STATES/EXECUTION TIME

TABLE 5

CONTROL LINES C ₀ C ₁ C ₂	OPERATION	DESCRIPTION
H H H	DEV ← AC	The content of the AC is sent to the device.
L H H	DEV ← AC.CLA	The content of the AC is sent to a device and then the AC is cleared.
H L L	AC ← DEV	Data is received from a device, OR'ed with the data in the AC and the result is stored in the AC.
L L H	AC ← DEV	Data is received from a device and loaded into the AC.
H L L	PC ← PC + DEV	Data from the device is added to the contents of the PC. This is referred to as a RELATIVE JUMP.
L L L	PC ← DEV	Data is received from a device and loaded into the PC. This is referred to as an ABSOLUTE JUMP.

*Don't Care

PROGRAMMED I/O CONTROL LINES

FIGURE 10

INPUT-OUTPUT INSTRUCTION TIMING

INTERRUPT TRANSFER

PROGRAM INTERRUPT TRANSFERS

The program interrupt system may be used to initiate programmed data transfers in such a way that the time spent waiting for device status is greatly reduced or eliminated altogether. It also provides a means of performing concurrent programmed data transfers between the HM-6100 and the peripheral devices. This is accomplished by isolating the I/O handling routines from the mainline program and using the interrupt system to ensure that these routines are entered only when an I/O device status is set, indicating that the device is actually ready to perform the next data transfer, or that it requires some sort of intervention from the running program.

The interrupt system allows certain external conditions to interrupt the computer program by driving the INTREQ input to the HM-6100 Low. If no higher priority requests are outstanding and the interrupt system is enabled, the HM-6100 grants the device interrupt at the end of the current instruction. After an interrupt has been granted, the Interrupt Enable Flip-Flop in the HM-6100 is reset so that no more interrupts are acknowledged until the interrupt system is re-enabled under program control.

DEVICE INTERRUPT GRANT TIMING

The current content of the Program Counter, PC, is deposited in location 0000_h of the memory and the program fetches the instruction from location 0001_h. The return address is available in location 0000_h. This address must be saved in a software stack if nested interrupts are permitted. The INTGNT, Figure 11, signal is activated by the HM-6100 when a device interrupt is acknowledged. This signal is reset by executing any IOT instruction as shown in Figure 12. The INTGNT signal is necessary to implement the Extended Memory Control hardware when more than 4K of memory is required. The INTGNT is also useful in implementing an External Vectored Priority Interrupt network.

The user program controls the interrupt mechanism of the HM-6100 by executing the processor IOT instructions listed in Table 6. Several of these interrupt IOT instructions are also used if the memory is extended beyond 4K words.

FIGURE 11

DEVICE INTERRUPT GRANT TIMING

FIGURE 12

DEVICE INTERRUPT GRANT RESET TIMING

INPUT/OUTPUT TRANSFER INSTRUCTIONS CONTINUED

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TABLE 6

MNE-MONIC	OCTAL CODE	OPERATION
SKON	6000	SKIP IF INTERRUPT ON—The interrupt system is enabled after the next sequential instruction is executed. The interrupt system is disabled after the next sequential instruction is executed.
ION	6001	INTERRUPT TURN ON—The internal interrupt acknowledge system is enabled. The interrupt system is enabled after the CPU executes the next sequential instruction. The INTERRUPT ENABLE TIMING is shown in Figure 13.
IOF	6002	INTERRUPT TURN OFF—The interrupt system is disabled after the next sequential instruction is executed.
SRQ	6003	SKIP IF INT REQUEST—The next sequential instruction is skipped if the INT request bus is low.
GET	6004	GET FLAGS—The following machine states are read into the indicated bits of AC: Bit 0—Link Bit 1—INT request bus Bit 2—Interrupt Enable Bit 3—Interrupt Enable FF When this instruction is executed, the interrupt system is disabled.
RTF	6005	RETURN FLAGS—Link is restored from AC (0). Interrupt system is enabled after the next sequential instruction is executed. All AC bits are available externally to restore external states. (ex. Extended memory control)
CA	6007	CLEAR ALL FLAGS—All flags are cleared.

PROCESSOR IOT INSTRUCTIONS

FIGURE 13

INTERRUPT ENABLE FF ON (ION)

CONTROL PANEL INTERRUPT TRANSFER

The HM-6100 control panel is implemented in software. The software implementation of the control panel need not use any part of the main memory or change the processor state. This is an important feature since the final version of the system may not have a control panel and the system designer would like to use the entire capacity of the main memory for the specific system application.

The control panel communicates with the HM-6100 with the Control Panel Request, CPREQ, line. The CPREQ is functionally similar to the INTREQ with some important differences. The CPREQ is granted even when the machine is in the HALT state. The HM-6100 is temporarily put in the RUN state for the duration of the panel routine. The HM-6100 reverts back to its original processor state after the panel routine has been executed.

The CPREQ bypasses the interrupt enable system and the processor IOT instructions. ION and IOF, are ignored while the HM-6100 is in the Control Panel Mode. Once a CPREQ is granted, the HM-6100 will not recognize any DMAREQ or INTREQ until CPREQ has been fully serviced.

When a CPREQ is granted, Figure 14, the PC is stored in location 0000₆ of the Panel Memory and the HM-6100 resumes operation at location 7777₆ of the Panel Memory. The Panel Memory would be organized with RAM's in the lower pages and PROM's in the higher pages. The control panel service routine would be stored in the higher pages in the nonvolatile PROM's, starting at 7777.

FIGURE 14

CONTROL PANEL INTERRUPT GRANT TIMING

A Control Panel Flip-Flop, CNTRL FF, which is internal to the HM-6100, is set when the CPREQ is granted. The CNTRL FF prevents further CPREQ's from being granted.

As long as the CNTRL FF is set, the Control Panel Memory Select, CPSEL, is active instead of the Memory Select, MEMSEL, for memory references. The CPSEL signal may, therefore, be used to distinguish the Control Panel Memory from the Main Memory. However, during the Execute phase of indirectly addressed AND, TAD, ISZ or DCA instructions, the MEMSEL is made active. The instructions are always fetched from the control panel memory. The operand address for indirectly addressed AND, TAD, ISZ or DCA refers first to the control panel memory for an effective address, which, in turn, refers to a location in the main memory. A main memory location may, therefore, be examined and changed by indirectly addressed TAD and DCA instructions, Figure 15, respectively. Every location in the main memory is accessible to the control panel routine.

FIGURE 15

"DCA INDIRECT" IN CONTROL PANEL ROUTINE

Exiting from the control panel routine is achieved by executing the following sequence with reference made to Figure 16.

ION

JMP I 0000, (Loc 0000, in CPMEM)

The ION, 6001_h, instruction will reset the CP FF after executing the next sequential instruction. The ION will not affect the interrupt system since the CNTRL FF is still active. Location 0000_h of the CPMEM contains either the original return address deposited by the HM-6100 when the CP routine was entered, or it may be a new starting address defined by the CP routine, for example, by activating the LOAD ADDRESS SWITCH. CPREQ's are normally generated by the manual actuation of the control switches. If the CPU registers must be displayed in real-time, the CPREQ's must be generated by a timer at fixed intervals.

The designer may also make use of the control panel features to implement Bootstrap loaders in the CP Memory so that the loader will be "transparent" to the main memory. Programs will be loaded by DCA I POINTER instruction, the pointer being developed in the CP RAM to point to the main memory location to be loaded.

Approximately 64 P ROM locations are sufficient to implement all the functions of the PDP8/E Control Panel. The HM-6100 provides for a 12 bit switch register which can be read by the HM-6100 under program control with the OR THE SWITCH REGISTER, OSR, instruction even without a control panel.

An RTF, 6005_h, instruction also resets the internal CNTRL FF. Exiting from a panel routine can be achieved by activating the RESET line since RESET has a higher priority than CPREQ as shown in Figure 18. If the RUN/HLT line is pulsed while the HM-6100 is in the panel mode, it will 'remember' the pulse(s) but defer any action until the HM-6100 exits from the panel mode.

FIGURE 16

"ION; JMP I 0000," IN CONTROL PANEL ROUTINE

INPUT/OUTPUT TRANSFER INSTRUCTIONS CONTINUED

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DIRECT MEMORY ACCESS (DMA)

Direct Memory Access, sometimes called data break, is the preferred form of data transfer for use with high-speed storage devices such as magnetic disk or tape units. The DMA mechanism transfers data directly between memory and peripheral devices. The HM-6100 is involved only in setting up the transfer; the transfers take place with no processor intervention on a "cycle-stealing" basis. The DMA transfer rate is limited only by the bandwidth of the memory and the data transfer characteristics of the device.

The device generates a DMA Request when it is ready to transfer data. The HM-6100 grants the DMAREQ by activating the DMAGNT signal at the end of the current instruction as shown in Figure 17. The HM-6100 suspends any further instruction fetches until the DMAREQ line is released. The DX lines are tri-stated, all SEL lines are high, and the external timing signals XT_A, XT_B, and XT_C are active. The device which generated the DMAREQ must provide the address and the necessary control signals to the memory for data transfers. The DMAREQ line can also be used as a level sensitive "pause" line.

FIGURE 17

DIRECT MEMORY ACCESS (DMA)

INTERNAL PRIORITY STRUCTURE

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After an instruction is completely sequenced, the major state generator scans the internal priority network as shown in Figure 18. The state of the priority network decides the next sequence of the HM-6100.

The request lines, RESET, CPREQ, RUN/HLT, DMAREQ and INTREQ, are sampled in the last cycle of an instruction execution, at time T₁. The worst case response time of the HM-6100 to an external request is, therefore, the time required to execute the longest instruction preceded by any 6-state execution cycle. For the HM-6100, this is an autoindexed ISZ, 22 states, preceded by any 6-state execution cycle instruction. The worst case response time is, therefore, 28 states, 14 μ s at 5 volts.

When the HM-6100 is initially powered up, the state of the timing generator is undefined. The generator is automatically initialized with a maximum of 68 clock pulses. The request inputs, as the HM-6100 is powered on, must span at least 92 clock pulses to be recognized, 68 clocks for the counter to initialize and a maximum of two HM-6100 cycles (20 to 24 clocks) for the state generator to sample the request lines.

The internal priority is RESET, CPREQ, RUN/HLT, DMAREQ, INTREQ, and IFETCH.

IFETCH

If no external requests are pending, the HM-6100 fetches the next instruction pointed to by the contents of the PC. The IFETCH line is active during the cycle in which the instruction is fetched. External devices can monitor DX, 0-2, during IFETCH-X_T, to determine the functional class of the current instruction. For example, the external memory extension hardware must know when JMP or JMS instructions are fetched to implement the Extended Memory Control.

The Programmable Logic Array, PLA, in the HM-6100 sequences the HM-6100 to execute the fetched instruction. All INDIRECT and AUTOINDEX Memory Reference Instructions go through a common state sequence to generate the Effective Address, EA, of the operand. The subsequent sequence, referred to as the EXECUTE phase, is controlled by the functional class of the instruction. The EXECUTE phase of AND, TAD, DCA, JMS, JMP and OPR Group 3 Microinstruction consists of only one cycle. ISZ and IOT have a 2-cycle EXECUTE phase. OPR Group 1 and Group 2 Microinstructions have an optional second cycle, depending on the microcoding of the OPR instructions. An HM-6100 cycle consists of 5 states, T₁, T₂, T₃, T₄, and T₅, with an optional sixth state, T₆, for Output Transfers (WRITE).

The state sequence for internal (processor) and external IOT instructions are identical. The Device Address and Control bits are available in the External Address Register for internal IOT instructions. External hardware, for example Extended Memory Control, can control the C-lines for data transfers to implement Get Flags (GTF), Return Flags (RTF), and Clear All Flags (CAF) instructions. External Control of the C-lines is necessary to implement these internal IOT instructions since the flag bits may be distributed both inside and outside the HM-6100.

FIGURE 18

INTERNAL PRIORITY STRUCTURE CONTINUED

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RESET

The Reset initializes all internal HM-6100 flags and clears the AC and the LINK. The machine is halted.

The HM-6100 remains in the Reset state as long as the Reset line is low as shown in Figure 19. The DX lines are three stated. The HM-6100 continues to provide the external timing signals XT_A, XT_B, and XT_C. All SEL lines are high.

The PC is set to 7777_h. In most applications, the higher memory locations utilize P ROM's or ROM's. Therefore, a power-up routine starting at the highest memory location can be used to initialize the system.

FIGURE 19

RESET TIMING

RUN/HALT

RUN/HLT changes the state of the HM-6100's RUN/HLT flip-flop. Pulsing the line low causes the HM-6100 to alternately run and halt as shown in Figure 20. The RUN/HLT line is normally high. The HM-6100 recognizes the positive transition of the signal.

The RUN/HLT flip-flop can be put in the halt state under program control by executing the HLT, 7402_h, instruction. when the HM-6100 is halted, RUN/HLT is functionally identical to the CONTINUE switch of the PDP8/E control panel.

If the HM-6100 is in the halt state, the RUN signal is low. The RUN signal can be used to power down external circuitry for a low power system.

The RUN/HLT can also be used to make the HM-6100 execute or instruction at a time as shown in Figure 21. The RUN/HLT combines the functional features of STOP, CONTINUE, and SINGLE INSTRUCTION as defined by the PDP8/E Control Panel.

FIGURE 20

RUN/HALT TIMING

FIGURE 21

"SINGLE STEP" WITH RUN/HLT

PDP-8/E COMPATIBILITY

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The HM-6100 and the PDP-8/E* of Digital Equipment Corporation are software compatible. The basic PDP-8/E paper-tape software system supplied by Digital Equipment Corporation will operate properly with the HM-6100. This basic software package includes Binary Loaders, PAL III Assembler, Symbolic Editor, Dynamic Debugging Technique (DDT), Octal Debugging Technique (ODT), 23 Bit Floating Point Package and FOrmula CALculator (FOCAL)*. The HM-6100 will execute the complete set of CPU diagnostics for PDP-8/E.

Since the bus structure of the HM-6100 can be adapted to provide a subset of the PDP-8/E OMNIBUS* signals, as shown in Figure 22, all programmed I/O interfaces for the PDP-8/E, for example, Teletype, Papertape Reader/Punch, etc., will operate with the HM-6100 without any hardware or software modification.

The Direct Memory Access, DMA, structure of the HM-6100 and PDP-8/E are different, the HM-6100 DMA structure is similar to the PDP-8 1-CYCLE BREAK, but not compatible.

The HM-6100 handles 4K words of memory directly. Like the PDP-8/E, an external Extended Memory Control element can be used to extend the addressing space up to 32K. All necessary control and timing signals to implement the memory extension controller are generated by the HM-6100.

The Extended Arithmetic Element, EAE, and the User Flag, UF, processor options of the PDP-8/E cannot be used with the HM-6100. The EAE is used for hardwired Multiply/Divide and the UF for timesharing.

The HM-6100 treats the Control Panel as a programmed I/O device with certain special features. The Control Panel has a dedicated INT request line to the HM-6100 and the control panel program can reside in a separate memory, distinct from the normal program memory. The control panel service routine can be made transparent to the user and the user program can occupy the entire 4K of main memory. The bootstrap routines may also reside in the dedicated control panel memory. Unlike the PDP-8/E, the HM-6100 bootstrap routines and the loaded user programs, can, therefore, share common address space.

FIGURE 22

EXAMPLE OF A PDP-8/E PROGRAMMED I/O PERIPHERAL INTERFACE

APPLICATIONS

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ALL CMOS SYSTEM

The HM-6100 microprocessor family provides for the capability of building an all CMOS system with no additional support components. The CMOS RAM devices are organized 1024 x 1 (HM-6506/18), or 256 x 4 (HM-6551/6561). They have internal address latches and operate synchronously with an address strobe. A 1024 x 12 bit mask programmable CMOS ROM (HM-6312) is also provided. The HM-6402/6403 is an industry standard UART with the option of operating directly from a high fre-

quency crystal. The HM-6101, Parallel Interface Element (PIE), provides all the signals necessary to communicate with an external device including a vectored priority interrupt chain. For example, a parallel Teletype interface can be designed with only two logic elements—the HM-6101 for control and the HM-6403 for data handling. The dynamic power dissipation of the CMOS system will be less than 60mW at +5 volts. (Figure 23.)

FIGURE 23

GENERAL PURPOSE HM-6100 SYSTEM

A few auxiliary circuits are necessary to permit the HM-6100 to be operational in a general purpose environment. They include transceivers (DM8833) to buffer the DX lines, address latches

(SN74174) and buffers for control lines. The HM-6100 requires only 6 additional packages to interface with standard bipolar or MOS RAM's, P ROM's or FPLA's. (Figure 24.)

FIGURE 24

256 × 12 RAM, 2K × 12 PROM MEMORY SYSTEM

A low power nonvolatile memory system with extremely low standby power requirements can be constructed as shown below. A 256 × 12 RAM, 2K × 12 P ROM organization seems to be sufficient for typical microprocessor applications. Provisions are made, however, to expand the RAM-P ROM capacity up to 4K words. The PROM devices are power strobed with HD-6605's. The CMOS RAM's have extremely low quiescent power requirements, less than

300 μ W for a 256 × 12 array, and they can be made nonvolatile with an inexpensive battery backup. The system designer can reduce memory power dissipation considerably with CMOS RAM's and power strobed P ROM's since the memory utilization of microprocessors is typically less than 30%. The power dissipation of the system shown below is less than 0.5watts at 5 volts. (Figure 25.)

FIGURE 25

TRANSPARENT CONTROL PANEL

A unique feature of the HM-6100 is the provision for a dedicated completely independent control panel with its own memory separate from the main memory. The concept of a "transparent" control panel is an important one for microprocessors since microprocessor based production systems normally do not have a full fledged panel and the system designer would like to use the entire capacity of the main memory for the specific system applications. A number of panel options which can greatly increase the usefulness, flexibility and

reliability of the system, such as test, maintenance and diagnostic routines, bootstrap loaders, etc., can be incorporated just by increasing the size of the panel memory to handle more software. The panel can be considered as a portable device which can be plugged into a socket on the CPU board, whenever the panel functions are needed, and disconnected, when not needed, without disturbing any part of the user program. (Figure 26.)

FIGURE 26

APPLICATIONS CONTINUED

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HM-6100 TO CMOS RAM INTERFACE

The HM-6100 provides all the control signals to interface directly with standard CMOS RAM's. Since the CMOS RAM's have internal address latches, the address information on the DX lines is latched

internally with the address strobe. Address, Data-in and Data-out can be multiplexed on the DX lines without any degradation in performance. (Figure 27.)

FIGURE 27

Harris reserves the right to make changes in the information contained herein at any time without notice to the user. Information contained herein bearing on specific or potential applications is presented solely for general guidance. Harris assumes no responsibility for user's specific designs or applications, or for infringement of property rights of others in such designs or applications.

FEATURES

- IM6100 Compatible
- Low Power — typ $< 5.0 \mu\text{W}$ standby
- 4-11V Supplies
- High Speed
- Static Operation

PRELIMINARY CMOS PARALLEL INTERFACE ELEMENT IM6101/6101A

GENERAL DESCRIPTION

The IM6101 and IM6101A Parallel Interface Elements (PIE) are high speed low power silicon gate CMOS general purpose devices which provide addressing, interrupt and control for a variety of peripheral functions such as UARTs, FIFOs, Keyboards, etc. The PIE is designed to eliminate external logic. Data transfers between the Intersil IM6100 CMOS Microprocessor and the IM6101 are via IOT instructions.

tions, control lines and DX bus. Data transfers between peripheral devices and the DX bus are controlled by the PIE via 2 read, 2 write, 4 sense and 4 flag functions. The A and B registers program write polarities, sense polarities, sense levels or edges, flag values and interrupt enables. The vector register has 10 bits writeable from the IM6100 and 2 bits indicating the highest priority SENSE input that generated the interrupt.

INSTRUCTIONS (DX 8, 9, 10, 11)

1000 - READ2	0000 - READ1
1001 - WRITE 2	0001 - WRITE1
1010 - SKIP3	0010 - SKIP1
1011 - SKIP4	0011 - SKIP2
1100 - WVR	0100 - RCRA
1101 - WCRB	0101 - WCRA
1110 - SFLAG3	0110 - SFLAG1
1111 - CFLAG3	0111 - CFLAG1
6007 - CAF (Internal IOT)	
clears interrupt requests	

FUNCTIONAL DIAGRAM

PACKAGE DIMENSIONS

DL 40 Pin DIP

ORDERING INFORMATION

REGISTER BIT ASSIGNMENTS

DX	0	1	2	3	4	5	6	7	8	9	10	11
CONTROL REGISTER A	FL4	FL3	FL2	FL1	WP2		WP1		IE4	IE3	IE2	IE1
CONTROL REGISTER B	SL4	SL3	SL2	SL1	SP4	SP3	SP2	SP1				
INTERRUPT VECTOR REGISTER												SPRI
INSTRUCTION REGISTER												

- FL - Flag
- WP - Write Polarity
- IE - Interrupt Enable
- SL - Sense Level
- SP - Sense Polarity
- SPRI - Sense Priority

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		Operating Temperature Range	
IM6101	+8.0V	Industrial	-40°C to 85°C
IM6101A	+12.0V	Military	-55°C to 125°C
Applied Input or Output Voltage	GND -0.3V to V _{CC} +0.3V	Operating Voltage Range	
		IM6101	4V to 7V
Storage Temperature Range	-65°C to 150°C	IM6101A	4V to 11V

DC CHARACTERISTICS V_{CC} = Operating Voltage Range T_A = Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V _{IH}		70% V _{CC}			V
Logical "0" Input Voltage	V _{IL}				20% V _{CC}	V
Input Leakage	I _{IL}	0V ≤ V _{IN} ≤ V _{CC}	-1.0		1.0	μA
Logical "1" Output Voltage	V _{OH2}	I _{OUT} = 0	V _{CC} - 0.01			V
Logical "1" Output Voltage	V _{OH1}	I _{OH} = -0.2 mA	2.4			V
Logical "0" Output Voltage	V _{OL2}	I _{OUT} = 0			GND + 0.01	V
Logical "0" Output Voltage	V _{OL1}	I _{OL} = 2.0 mA			0.45	V
Output Leakage	I _O	0V ≤ V _O ≤ V _{CC}	-1.0		1.0	μA
Supply Current	I _{CC1}	V _{IN} = V _{CC}		1.0		μA
	I _{CC2}	V _{CC} = 5V f _{IM6100} = 4 MHz		1.0		mA
Input Capacitance	C _I			5	7	pf
Output Capacitance	C _O			8	10	pf
Input/Output Capacitance	C _{ID}			8	10	pf

AC CHARACTERISTICS T_A = 25°C C_L = 50pf

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Delay from DEVSEL to READ	t _{DR}	IM6101 V _{CC} = 5V IM6101A V _{CC} = 10V		150 75		ns ns
Delay from DEVSEL to WRITE	t _{DW}	IM6101 V _{CC} = 5V IM6101A V _{CC} = 10V		150 75		ns ns
Delay from DEVSEL to FLAG	t _{DF}	IM6101 V _{CC} = 5V IM6101A V _{CC} = 10V		200 100		ns ns
Delay from DEVSEL to C1, C2	t _{DC}	IM6101 V _{CC} = 5V IM6101A V _{CC} = 10V		200 100		ns ns
Delay from DEVSEL to SKP/INT	t _{DI}	IM6101 V _{CC} = 5V IM6101A V _{CC} = 10V		200 100		ns ns
Delay from DEVSEL to DX	t _{DA}	IM6101 V _{CC} = 5V IM6101A V _{CC} = 10V		200 100		ns ns
LXMAR pulse width	t _{LXMAR}	IM6101 V _{CC} = 5V IM6101A V _{CC} = 10V		200 100		ns ns
Address setup time	t _{ADDs}	IM6101 V _{CC} = 5V IM6101A V _{CC} = 10V		50 25		ns ns
Address hold time	t _{ADDH}	IM6101 V _{CC} = 5V IM6101A V _{CC} = 10V		100 50		ns ns
Data setup time	t _{DS}	IM6101 V _{CC} = 5V IM6101A V _{CC} = 10V		200 100		ns ns
Data hold time	t _{DH}	IM6101 V _{CC} = 5V IM6101A V _{CC} = 10V		50 25		ns ns

TIMING DIAGRAM

Timing for a typical IOT transfer is shown below. During IFETCH the processor obtains from memory an IOT instruction of the form 6XXX. During the IOTA the processor places that instruction back on the DX lines ③ and pulses LXMAR transferring address and control information for the IOT transfer to all peripheral devices. A low going pulse on DEVSEL while XTC is high ④ is used by the addressed PIE along with decoded control

information to generate C1, C2, SKP and controls for data transfers to the processor. Control outputs READ1 and READ2 are used to gate peripheral data to the DX lines during this time. A low going pulse on DEVSEL while XTC is low ⑤ is used to generate WRITE1 and WRITE2 controls. These signals are used to clock processor accumulator instruction data into peripheral devices.

All PIE timing is generated from IM6100 signals LXMAR, DEVSEL, and XTC. No additional timing signals, clocks, or one shots are required. Propagation delays, pulse width, data setup and hold times are specified for direct interfacing with the IM6100.

PIE ADDRESS AND INSTRUCTIONS

The IM6100 communicates with the PIE and with peripherals through the PIE via IOT commands. During the IOTA cycle (See Figure 1) an instruction of the form 6XXXX is loaded into all PIE instruction registers. The bits are interpreted as shown below.

The 5 address bits (3-7) are compared with the select inputs SEL3, SEL4, SEL5, SEL6, SEL7 to address 1 of 31 possible PIE's. Address zero is reserved for IOT's internal to the IM6100. The four control bits are decoded to select one of 16 instructions.

CONTROL	MNEMONICS	ACTION
0000	READ1	The READ instructions generate a pulse on the appropriate read outputs. This signal is used by the peripheral device to gate data onto the DX bus to be "OR'ed" with the IM6100 accumulator data. The IM6100 accumulator is cleared prior to reading peripheral data when CO is asserted low.
1000	READ2	
0001	WRITE1	The WRITE instructions generate a pulse on the appropriate write output. This signal is used by peripherals to load the IM6100 accumulator data on the DX lines into peripheral data registers. The IM6100 AC is cleared after the write operation when the CO input is asserted low.
1001	WRITE2	
0010	SKIP1	The SKIP instructions test the state of the sense flip flops. If the input conditions have set the sense flip flop, the PIE will assert the SKP/INT output causing the IM6100 to skip the next program instruction. The sense flip flop is then cleared. If the sense flip flop is not set, the PIE does not assert the SKP/INT output and the IM6100 will execute the next instruction.
0011	SKIP2	
1010	SKIP3	
1011	SKIP4	
0100	RCRA	The Read Control Register A instruction gates the contents of CRA onto the DX lines during time (4) to be "OR" transferred to the IM6100 AC.
0101	WCRA	The Write Control Register A, Write Control Register B and Write Vector Register instructions transfer IM6100 AC data on the DX lines during time (5) of IOTA into the appropriate register.
1101	WCRB	
1100	WVR	
0110	SFLAG1	The SET FLAG instructions set the bits FL1 and FL3 in control register A to a high level. PIE outputs FLAG1 and FLAG3 follow the data stored in bits FL1 and FL3 of CRA.
1110	SFLAG3	
0111	CFLAG1	The CLEAR FLAG instructions clear the bits FL1 and FL3 in control register A to a low level.
1111	CFLAG3	
(6007) ₈	CAF	IM6100 internal IOT instruction CLEAR ALL FLAGS clears the interrupt requests by clearing the sense flip flops.

PRIORITY FOR VECTORED INTERRUPT

A hardware priority network uniquely selects a PIE to provide a vectored address. The first IOT command of any type, after the IM6100 signal INTERRUPT GRANT goes high, resets the line INTGNT to a low level. The signal INTGNT is used to freeze the priority network and enable vector generation. The highest priority PIE has PIN tied

to V_{CC}. The lowest priority PIE is the last one on the chain. The vector address generated by the PIE consists of 10 bits from the vector register and two bits that indicate the sense input within the highest priority PIE that generated the interrupt.

VPRI	Conditions
00	SENSE1
01	SENSE2 and not SENSE1
10	SENSE3 and not (SENSE2 or SENSE1)
11	SENSE4 and not (SENSE3 or SENSE2 or SENSE1)

I/O CONTROL LINES (C1 and C2)

The type of input-output transfer is controlled by the selected PIE by activating the C1, C2 lines as shown below. These outputs are open drain.

C1	C2	
H	H	DEV/PIE ← AC Write
L	H	AC ← AC V DEV/PIE "OR" Read
L	L	PC ← VECTOR ADDRESS Vectored Interrupt

INTERRUPT/SKIP (INT/SKP)

Interrupt and skip information are time multiplexed on the same lines. Since the IM6100 samples skip and interrupt data at separate times (see Figure 1) there is no degradation in system performance. The PIE samples the sense flip flops and generates an interrupt request for enabled bits on the rising edge of XTC. Interrupt requests are asserted by driving the INT/SKP line low. During IOTA of SKIP instructions the INT/SKP reflects the SENSE flip flop data.

If the SENSE flip flop is set, the INT/SKP line is driven low to cause the IM6100 to skip the next instruction. This output is open drain.

CONTROL REGISTER A (CRA)

The CRA can be read and written by the IM6100 via the RCRA and WCRA commands. The format and meaning of control bits are shown below.

FL(1-4) Data on FLAG outputs corresponds to data in FL (1-4). Changing the FL bits in CRA changes the corresponding FLAG output.

WP(1,2) A high level on WRITE POLARITY bits causes positive pulses at the WRITE outputs (see Figure 1).

IE(1-4)

A high level on INTERRUPT ENABLE enables interrupts.

CONTROL REGISTER B

The CRB can be written by the IM6100 via the WCRB instruction. It has no read back capability. The format and meaning of control bits are shown below.

0	1	2	3	4	5	6	7
SL4	SL3	SL2	SL1	SP4	SP3	SP2	SP1

SL(1-4) A high level on the SENSE LEVEL bits causes the SENSE inputs to be level sensitive. A low level on the SL bits causes the SENSE inputs to be edge sensitive.

SP(1-4) A high level on the SENSE POLARITY bits causes the sense flip flop to be set by a high level or positive going edge. A low level causes the sense flip flop to be set by a low level or negative going edge.

PERIPHERAL INTERFACE LINES

SENSE (1-4) The sense inputs are used to set the flip flops SENSE FF. Conditions for setting SENSE FF, levels or edges and positive or negative polarities, are set by control bits SL and SP in CRB. The SENSE FF's are sampled on the rising edge of XTC. Interrupt requests are generated when the sense flip flops are set and interrupts are enabled (SENSE FF and IE). Sense flip flops are reset on two conditions.

1. Vectored interrupt resets highest priority SENSE FF on selected PIE.
2. SKIP instruction resets corresponding SENSE FF if set.

READ (1,2) The READ outputs are activated by the read instructions and are used by peripheral devices to gate data onto the DX lines for transfer to the IM6100 (see Figure 1). READ lines are active low.

WRITE (1,2) The WRITE outputs are activated by the write instructions and are used by peripheral devices to load IM6100 AC data from the DX lines into peripheral data registers (see Figure 1). Output polarity is controlled by the WRITE POLARITY bits of CRA. A logic one causes pulses to be positive while a logic zero causes pulses to be negative.

FLAG (1-4) The FLAG's are general purpose outputs that can be set and cleared under program control. FLAG1 follows bit FL1 in CRA and etc. FLAG's can be changed by loading new data into CRA via the WCRA commands. In addition, FLAG1 and FLAG3 can be set and cleared directly by the commands SFLAG1, CFLAG1, SFLAG3 and CFLAG3.

PIN DEFINITIONS

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1	VCC		+5 volts
2	INTGNT	H	A high level on INTERRUPT GRANT inhibits recognition of new interrupt requests and allows the priority chain time to uniquely specify a PIE.
3	PRIN	H	A high level ON PRIORITY IN and an interrupt request will select a PIE for vectored interrupt.
4	SENSE 4	PROG	The SENSE input is controlled by the SL (sense level) and SP (sense polarity) bits of control register B. A high SL level will cause the sense flip flop to be set by a level while a low SL level causes the sense flip flop to be set by an edge. A high SP level will cause the sense flip flop to be set by a positive going edge or high level. A high IE (interrupt enable) level generates an interrupt request whenever the sense flip flop is set.
5	SENSE 3	PROG	See pin 4 - SENSE 4
6	SENSE 2	PROG	See pin 4 - SENSE 4
7	SENSE 1	PROG	See pin 4 - SENSE 4

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
8	SEL 3	TRUE	Matching SELECT(3-7) inputs with PIE addressing on DX(3-7) during IOTA selects a PIE for programmed input/output transfers.
9	SEL 4	TRUE	See Pin 8 - SEL 3
10	LXMAR	H	A positive pulse on LOAD EXTERNAL ADDRESS REGISTER loads address and control data from DX(3-11) into the address register.
11	SEL 5	TRUE	See Pin 8 - SEL 3
12	SEL 6	TRUE	See Pin 8 - SEL 3
13	XTC	H	The XTC input is a timing signal produced by the microprocessor. When XTC is high a low going pulse on DEVSEL initiates a "read" operation. When XTC is low, a low going pulse on DEVSEL initiates a write operation.
14	SEL 7	TRUE	See Pin 8 - SEL 3
15	DX 0	TRUE	Data transfers between the microprocessor and PIE take place via these input/output pins.
16	DX 1	TRUE	See Pin 15 - DX 0
17	DX 2	TRUE	See Pin 15 - DX 0
18	DX 3	TRUE	See Pin 15 - DX 0
19	DX 4	TRUE	See Pin 15 - DX 0
20	DX 5	TRUE	See Pin 15 - DX 0

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
21	DX 6	TRUE	See Pin 15 - DX 0
22	DX 7	TRUE	See Pin 15 - DX 0
23	DX 8	TRUE	See Pin 15 - DX 0
24	DX 9	TRUE	See Pin 15 - DX 0
25	DX 10	TRUE	See Pin 15 - DX 0
26	DX 11	TRUE	See Pin 15 - DX 0
27	GND		
28	DEVSEL	L	The DEVSEL input is a timing signal produced by the microprocessor during IOT instructions. It is used by the PIE to generate timing for controlling PIE registers and "read" and "write" operations.
29	FLAG 4	PROG	The FLAG outputs reflect the data stored in control register A. Flags (1-4) can be set or reset by changing data in CRA via a WRA (write control register A) command. FLAG1 and FLAG3 can be controlled directly by PIE commands SFLAG1, CFLAG1, SFLAG3 and CFLAG3.
30	FLAG 3	PROG	See Pin 29 - FLAG 4
31	FLAG 2	PROG	See Pin 29 - FLAG 4
32	FLAG 1	PROG	See Pin 29 - FLAG 4
33	C1	L	The PIE decodes address, control and priority information and asserts outputs C1 and C2 during the IOTA cycle to control the type of data transfer. These outputs are open drain for bussing and require a pullup register to VCC. C1(L), C2(L) - vectored interrupt C1(L), C2(H) - READ1, READ3 or RRA commands C1(H), C2(H) - all other instructions

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
34	C2	L	See Pin 33 - C1
35	READ1	PROG	Outputs READ1 and READ2 are used to gate data from peripheral devices onto the DX bus for input to the IM6100. Note the data does not pass through the PIE.
36	WRITE1	PROG	Outputs WRITE1 and WRITE2 are used to gate data from the IM6100 DX bus into peripheral devices. Data does not pass through the PIE.
37	READ2	PROG	See Pin 35 - READ1
38	WRITE2	PROG	See Pin 36 - WRITE1
39	SKP/INT	L	The PIE asserts this line low to generate interrupt requests and to signal the IM6100 when sense flip flops are set during SKIP instructions. This output is open drain.
40	POUT	H	A high level on priority out indicates no higher priority PIE interrupt requests are outstanding. This output is tied to the PIN input of the next lower priority PIE in the chain.

APPLICATION

INTRODUCTION

The IM6101, Parallel Interface Element (PIE), provides a universal means of interfacing industry standard LSI devices and peripheral equipment controllers to the IM6100 Microprocessor.

The IM6100 configures each PIE for a specific interface during system initialization by programming the control registers within the PIE for write enable polarities, sense polarities, sense edges or levels, flag values and interrupt enables.

The data transfer between the IM6100 and the peripheral devices does not take place through the PIE. The Parallel Interface Element provides the steering signals for data transfers. This approach was chosen since all the standard LSI elements such as Keyboard chips, UARTs, FIFOs, etc. have internal storage latches and they require only control signals to take data from the bus or to put data on the bus. If some user defined peripheral interfaces do not have these built-in storage elements, discrete CMOS or low power Schottky latches, or flip-flops, must be provided to store the data from the IM6100 until the peripheral device is ready to accept it and to latch data from the peripheral devices until the IM6100 asks for it.

INTERRUPT HANDLING WITH PIE'S

The PIEs provide for a vectored priority interrupt scheme. Up to 31 PIEs may be chained to obtain 124 interrupt lines. The microprocessor will recognize, identify and start servicing the highest priority interrupt request within 30.5 μ s at 4 MHz.

The INTREQ lines from all PIEs are wire-ANDed together. A PIE generates an interrupt request, if any one of its four sense lines, which are interrupt enabled, become active by driving the INTREQ line to the IM6100 low. If no higher priority requests are outstanding (RESET, CPREQ, HLT or DMAREQ), the IM6100 will grant the request at the end of the current instruction. The content of the Program Counter is deposited in location 0000g of the memory and the program fetches the next instruction from location 0001g. The return address is hence available in location 0000g. This address must be saved in a software stack if nested interrupts are allowed.

The IM6100 activates the INTGNT signal high when an INTREQ is acknowledged. The INTGNT is reset by executing any IOT instruction. The PIEs use the INTGNT signal to freeze the priority network and to uniquely specify the PIE with the highest priority interrupt request. The PIE with the highest priority request sends a unique vector address to the IM6100 when the processor executes the first IOT instruction after the INTGNT. It is recommended that the internal processor instruction, Interrupt Off (IOF - 6002g) be used for vectoring. IOF, in this context, is a NOP since the interrupt system is automatically disabled after an interrupt grant.

The 12-bit vector address generated by the PIE consists of 10 high order bits from the vector register, defined by the user during system initialization, and two low order bits which indicate the sense input that generated the interrupt. Therefore, if the instruction in location 0001g is IOF - 6002g, the processor will branch to 1 of 4 locations, depending on which of the sense lines within a PIE generated the request. Each one of these locations must contain a Jump instruction pointing to the specific service routine for the corresponding sense input. The 30.5 μ s interrupt acknowledge time at 4 MHz consists of 14 μ s (max) to recognize an interrupt request, 3 μ s to grant an interrupt request, 8.5 μ s to execute the IOF for vectoring and 5.0 μ s to execute a Jump instruction to a specific service routine.

PIN INSTRUCTION FORMAT

The IM6100 communicates with the PIEs using the Input-Output Transfer (IOT) instructions. The first three bits, 0-2, are always set to 6g (110) to specify an IOT instruction. The standard DEC* convention is to set the next 6 bits, 3-8, to specify 1 of 64 I/O devices and then to control the operation of the selected I/O device by using bits 9-11. However, the DEC interfaces are not standardized since a specific pattern of bits 9-11 could specify completely different operations in different I/O devices. For example, the pattern 000 in bits 9-11 could mean a read operation for Interface A, a write operation for Interface B, a skip instruction for Interface C and so on since the operation for any IOT instruction depends entirely upon the circuitry designed into the I/O device interface.

The IOT instruction format for the PIE is different from that used by DEC interfaces. The first three bits are, as usual, set to 6g to indicate an IOT instruction. The next 5 bits, 3-7, specify 1 of 31 PIEs and then the operation of the selected PIE is controlled by bits 8-11 in 16 uniquely specified ways. For example, the specific pattern 0000 in bits 8-11 means exactly the same operation for all PIEs, namely activate READ1 line.

Of the 32 possible combinations of bits 3-7, the pattern 00000 is reserved for internal Processor IOT instructions and hence not available as a PIE address. The 6900 Prototyping System assigns bit patterns 00001 and 00010 for the PDP-8/E^T compatible Teletype interface and these two addresses also must not be used for PIEs if the 6900 System is used for prototyping.

* Digital Equipment Corporation, Maynard, MA

^T Registered Trademark, Digital Equipment Corporation

The IM6402/03 Universal Asynchronous Receiver/Transmitter is a general purpose programmable serial device for interfacing an asynchronous serial data channel to a parallel synchronous data channel. The receiver converts a serial word with start, data, parity and stop bits to a parallel data word and checks for parity, framing and data overrun errors. The transmitter section converts a parallel data word into a serial word with start, data, parity and stop bits. The data word length may be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The number of stop bits may be 1 or 2 or 1½ when transmitting a 5 bit code.

The IM6204/03 can be used in a wide variety of applications including interfacing modems, Teletypes^T and remote data acquisition systems to the IM6100 microprocessor. The IM6403 makes provisions for a crystal oscillator and internal divider chain to specify the data transfer rate. In the IM6402 the data transfer rate is controlled by an external timing source, for example, a Baud Generator.

A functional block diagram of the PIE/UART/IM6100 interface is shown below. The UART is configured, in this specific example, to interface with an ASR-33 Teletype which has a data format that consists of 11 bits – a start bit, 8 data bits and 2 stop bits. The UART is clocked at 16X the data rate. For the 10 character per second ASR-33, the UART clock frequency would be 1.76 KHz. The configuration shown is compatible with the DEC BIN and RIM paper tape formatting.

An 8-bit data word from the IM6100 Accumulator is loaded into the Transmitter Buffer Register via inputs TBR8-TBR1 when the Transmit Buffer Register Load (TBRL) signal makes a zero to one transition. A high level on Transmit Buffer Register Empty (TBRE) indicates that the buffer is ready to accept a new character for transmission. The microprocessor checks the status of TBRE via SENSE2 before it transmits a new character to the UART by pulsing WRITE1. The start bit, data bits and stop bits appear serially at the Transmit Register Output (TRO).

A serial data stream on the Receiver Register Input (RRI) is clocked into the Receive Buffer Register. A high level on Data Received (DR) indicates that a character has been received. The contents of Receiver Buffer Register appear on the outputs RBR8-RBR1 when a low level is applied to Receiver Register Disable (RRD) input. The RBR outputs are tristated when RRD is high. A low level on Data Received Reset (DRR) clears the DR flag. RRD and DRR may be tied together to clear DR as the register data is being read. The microprocessor monitors the status of the DR flag via SENSE1 to see if a new character has been received before it reads the information stored in the buffer register by pulsing READ1 low.

The UART interface uses only the low order 8 bits of the IM6100 data bus (DX) to receive and transmit characters.

^T Registered trademark for Teletype Corporation

SELECT CODE:
 SEL3 = 0
 SEL4 = 1
 SEL5 = 1
 SEL6 = 1
 SEL7 = 0

110 BAUD SERIAL PORT

110 BAUD SERIAL PORT

PI = 1 No Parity
CLS1 = CLS2 = 1 8 Data Bits
SBS = 1 2 Stop Bits
RRC = TRC = 1.76 KHz 110 Baud Rate

SYSTEM 330X: ULTRA-LOW NOISE, WIDE DYNAMIC RANGE SQUID SYSTEM

SHE has recently developed a series of modifications to the Model 330 SQUID Electronics and TSQ SQUID Sensor which reduces the noise energy of the system by nearly one order of magnitude. This has been accomplished with absolutely no change in any other specification making it possible to directly substitute a low noise system for a standard system. The low noise System 330X is available either as an extra cost option at the time of original purchase, or as a modification to a standard System 330.

Each System 330X has its noise level checked over a wide range of frequencies and is carefully adjusted for maximum sensitivity. SHE guarantees the noise level of each System 330X to be less than 5×10^{-29} J/Hz, a level substantially lower than any other commercially available SQUID System. This is the lowest noise SQUID System ever built operating at a bias frequency below 100 MHz. The typical sensitivity of the 330X is 4×10^{-29} J/Hz, but noise levels as low as 2×10^{-29} J/Hz have been measured. It should be pointed out that this record breaking sensitivity is required by only the most demanding applications; the sensitivity of the standard System 330 (which previously had the lowest noise of any commercially available SQUID system) is more than adequate for most measurements.

A list of important system specifications is given in Table 1 for both the 330 and 330X. Note that the noise level of the 330X has been reduced without reducing the size of the maximum signal that it can handle. This gives it a larger dynamic range, a feature which may be more useful than low noise for some applications. For example, if a SQUID System 330 were being used as a magnetometer with 10^{-9} gauss/ $\sqrt{\text{Hz}}$ sensitivity, substitution of the 330X could provide either of the following improvements:

1. Without changing the magnetometer pick-up coils, the system sensitivity could be increased to about 3×10^{-10} gauss/ $\sqrt{\text{Hz}}$.
2. By reducing the size of the magnetometer pick-up coils by a factor of three, as well as changing to the 330X SQUID System, a sensitivity of 10^{-9} gauss/ $\sqrt{\text{Hz}}$ will be maintained but the size of the maximum signal that can be tracked will be increased by a factor of three. This will also increase the slew-rate of the system by a factor of three and reduce the physical size of the system due to the use of smaller coils.

If you have questions concerning the 330X or would like to find out how it can be used to improve the sensitivity of your measurements, call or write SHE. A member of our technical staff will be happy to discuss it with you in detail.

TABLE 1

	330X	330
Maximum equivalent input current noise, I_0 (rms A/ $\sqrt{\text{Hz}}$).	7×10^{-12}	2×10^{-11}
Input coil inductance, L (μH).	2	2
Guaranteed energy sensitivity, $\frac{1}{2}LI_0^2$ (Joules/Hz).	5×10^{-29}	4×10^{-28}
Maximum input signals without resetting output, I_m (p-p A).	10^{-4}	10^{-4}
Dynamic range, I_m/I_0 ($\sqrt{\text{Hz}}/2\sqrt{2}$).	1.4×10^7	5×10^6

APPENDIX C

SHE MAGNETOMETER SYSTEM

APPENDIX C

SHE Magnetometer System

A Model GMS-45 (Modified) Geophysical Magnetometer System is available to be used with the EM Receiver. Included here is a specification sheet, a calibration and test report, and a brief general description of the SHE squid system. The 3-axis magnetometer and system 330 operating manuals are included with the system under separate cover.

MODEL GMS-45 (MODIFIED) GEOPHYSICAL MAGNETOMETER SYSTEM

1. Custom designed, flexible helium transfer tube.
2. Three sets of Model 330X SQUID Electronics (data sheets enclosed).
3. Three 100 meter interconnecting cables.
4. Model LPD-25 dewar with built-in helium level gauge and aguaranteed operating time between helium refills of 21 days when the dewar is stationary.
5. Model GMP Probe with the following specifications:
 - a.) Magnetic orthogonality between axes better than .01 radian.
 - b.) Relative sensitivity between axes measured to better than 1%.
 - c.) Absolute calibration of sensitivity to better than 1%.
 - d.) Built-in roll-off with -3dB frequency greater than 60 Hz.
 - e.) Switchable sensitivity (with probe at room temperature) between two customer selected noise levels (N). N may be chosen to be any two values between $2 \times 10^{-5} \gamma$ and $5 \times 10^{-4} \gamma$ in a one hertz bandwidth (rms). For magnetotelluric measurements, N is normally chosen to be $1.2 \times 10^{-4} \gamma$ and $4 \times 10^{-5} \gamma$.
 - f.) Maximum slew rate greater than 3×10^9 N/sec.
 - g.) Full scale range of $\pm 6 \times 10^6$ N.
 - h.) Linearity better than 10 ppm.
 - i.) Output drift due to temperature changes of the rf head of less than $0.2 \text{ N}/^\circ\text{C}$.
 - j.) Output drift due to temperature changes of the control unit of less than $\pm (2N + 5 \times 10^{-6} \text{ reading})/^\circ\text{C}$ with smallest output gain ($200\text{V}/\text{N}$) or less than $\pm (0.1 \text{ N} + 10^{-4} \text{ reading})/^\circ\text{C}$ with largest output gain ($2 \times 10^4 \text{ V}/\text{N}$).
6. Two complete sets of operating manuals.
7. Electronic helium level gauge monitor with capability for either 115 Vac or built-in battery operation.

1. DESCRIPTION AND SPECIFICATIONS

1.1 INTRODUCTION

The SHE 3-axis geophysical magnetometer system consists of a fiberglass helium dewar with built-in helium level gauge, a 3-axis magnetometer probe, and 3 sets of SQUID electronics (Model 330). Separate manuals are enclosed for the level gauges, SQUID electronics and dewar which give details of these components that are not included in this combined system manual. Some of the instructions in these more detailed sub-system manuals may appear to conflict with the instructions contained herein. If so, this manual is the correct one to use.

1.2 MEASURED SPECIFICATIONS OF THE 3-AXIS MAGNETOMETER

A) -3 dB point of built-in eddy current roll-off shield:

X Axis	Y Axis	Z Axis
103 Hz	103 Hz	91 Hz

The complete frequency response curve, normalized to the magnetometer's dc sensitivity is given in Fig. 1.1.

B) Orthogonality between axes:

Constructed to be better than 1° between all axes.

C) Output voltage corresponding to one flux quantum (ϕ_0) in sensor or one "field quantum" (H_0) at input:

SENS.	X	Y	Z
$\times 1$	0.0226 V	0.0219 V	0.0220 V
$\times 10$	0.226 V	0.219 V	0.220 V
$\times 100$	2.26 V	2.19 V	2.20 V

D) The "field quantum" H_0 , defined as the input field required to change the flux in the sensor by one flux quantum:

	X	Y	Z
Shunted	1.59 γ	1.71 γ	1.49 γ
NOT Shunted	0.29 γ	0.30 γ	0.29 γ

INPUT ROLL-OFF

Fig. 1.1

E) Magnetometer noise level, all axes:

Shunted	$1.1 \times 10^{-4} \gamma/\sqrt{\text{Hz}}$
NOT Shunted	$2.1 \times 10^{-5} \gamma/\sqrt{\text{Hz}}$

Typically white from 0.01 Hz to 5 kHz, increasing as $1/f^{1/2}$ below 0.01 Hz.

F) Magnetometer Sensitivity:

SHUNTED			
SENS.	X	Y	Z
×1	0.014 V/γ	0.013 V/γ	0.015 V/γ
×10	0.14 V/γ	0.13 V/γ	0.15 V/γ
×100	1.4 V/γ	1.3 V/γ	1.5 V/γ

NOT SHUNTED

SENS.	X	Y	Z
×1	0.078 V/γ	0.074 V/γ	0.075 V/γ
×10	0.78 V/γ	0.74 V/γ	0.75 V/γ
×100	7.8 V/γ	7.4 V/γ	7.5 V/γ

1.3 GENERAL SPECIFICATIONS

The following specifications are often given in terms of H_0 which is defined as the magnetic field required to change the flux in the sensor by one flux quantum (ϕ_0). This quantity is a function of the pick-up coil and sensitivity shunt in use. It is measured for each probe and its values are given in Section 1.2.

RANGE: 3 sensitivity ranges selected by pushbuttons. Table gives input current and equivalent flux change for full-scale deflection (FSD). Relative accuracy of scale factor is $\leq 2\%$ of nominal value.

Sensitivity Range	Input Field for FSD	Sensor Flux for FSD
×1	$\pm 500 H_0$	$\pm 500 \phi_0$
×10	$\pm 50 H_0$	$\pm 50 \phi_0$
×100	$\pm 5 H_0$	$\pm 5 \phi_0$

ϕ_0 is the flux quantum: $\phi_0 = 2.07 \times 10^{-15} \text{ Wb} = 2.07 \times 10^{-7} \text{ G cm}^2$

S.H.E. CORPORATION CRYOGENIC INSTRUMENTS AND SYSTEMS

SQUID Probe Calibration and Test Report

Customer Westinghouse/Farstad

Model No. GMP-45 X Serial No. GMP-121, X-Axis

Sensor Test

Resistance of RF Shunt across Input Terminals 2 Ω

Equivalent rms noise at input coil (nominal inductance, 2 μ H)

<u>Frequency</u>	<u>Equivalent Current Noise</u>	<u>Equivalent Energy Noise</u>
0.5 Hz	<u>5.3</u> $\times 10^{-12}$ A/ $\sqrt{\text{Hz}}$	<u>2.8</u> $\times 10^{-29}$ J/Hz
50	<u>6.3</u>	<u>4.0</u>
5000	<u>8.4</u>	<u>7.1</u>

Flux Sensitivity. 0.97 $\times 10^{-7}$ A/ ϕ_0

or 22.6 mV/ ϕ_0 (sens. $\times 1$)

Current Sensitivity 4.3 $\times 10^{-9}$ A/mV (sens. $\times 1$)

Probe Test

Low Temperature RF Tuning Capacitor 200 pF

DC Voltage Mode

Voltage Gain ($V_{\text{out}}/V_{\text{in}}$). NA $\times 10^8$ (1% accuracy)

Input Voltage Equivalent Noise (input shorted) NA $\times 10^{-13}$ V rms

AC Impedance Mode

Standard Mutual Inductor NA μ H (1% accuracy)

Physical Tests

Upper Housing Leak Tight, Leak Rate $< 2 \times 10^{-5}$ std. cm^3 of $^4\text{He}/\text{sec.}$ NA

Sealed SQUID Holder Leak Tight, Leak Rate $< 2 \times 10^{-7}$ std. cm^3 of $^4\text{He}/\text{sec.}$. . NA

Checked by: Ken Miller
Ken Miller

Date: September 22, 1978

Approved by: Richard T. Johnson
Richard T. Johnson

Date: September 22, 1978

S.H.E. CORPORATION CRYOGENIC INSTRUMENTS AND SYSTEMS

SQUID Probe Calibration and Test Report

Customer Westinghouse/Farstad

Model No. GMP-45 X Serial No. GMP-121, Y-Axis

Sensor Test

Resistance of RF Shunt across Input Terminals 2 Ω

Equivalent rms noise at input coil (nominal inductance, 2 μ H)

Frequency	Equivalent Current Noise	Equivalent Energy Noise
0.5 Hz	<u>4.0</u> $\times 10^{-12}$ A/ $\sqrt{\text{Hz}}$	<u>1.6</u> $\times 10^{-29}$ J/Hz
50	<u>5.4</u>	<u>2.9</u>
5000	<u>7.4</u>	<u>5.5</u>

Flux Sensitivity. 0.98 $\times 10^{-7}$ A/ ϕ_0

or 21.9 mV/ ϕ_0 (sens. $\times 1$)

Current Sensitivity 4.5 $\times 10^{-9}$ A/mV (sens. $\times 1$)

Probe Test

Low Temperature RF Tuning Capacitor 220 pF

DC Voltage Mode

Voltage Gain ($V_{\text{out}}/V_{\text{in}}$). NA $\times 10^8$ (1% accuracy)

Input Voltage Equivalent Noise (input shorted) NA $\times 10^{-13}$ V rms

AC Impedance Mode

Standard Mutual Inductor NA μ H (1% accuracy)

Physical Tests

Upper Housing Leak Tight, Leak Rate $< 2 \times 10^{-5}$ std. cm^3 of $^4\text{He}/\text{sec.}$ NA

Sealed SQUID Holder Leak Tight, Leak Rate $< 2 \times 10^{-7}$ std. cm^3 of $^4\text{He}/\text{sec.}$ NA

Checked by: Ken Miller
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S.H.E. CORPORATION CRYOGENIC INSTRUMENTS AND SYSTEMS

SQUID Probe Calibration and Test Report

Customer Westinghouse/Farstad

Model No. GMP-45 X Serial No. GMP-121, Z-Axis

Sensor Test

Resistance of RF Shunt across Input Terminals 2 Ω

Equivalent rms noise at input coil (nominal inductance, 2 μ H)

<u>Frequency</u>	<u>Equivalent Current Noise</u>	<u>Equivalent Energy Noise</u>
0.5 Hz	<u>4.0×10^{-12} A/$\sqrt{\text{Hz}}$</u>	<u>1.6×10^{-29} J/Hz</u>
50	<u>6.0</u>	<u>3.6</u>
5000	<u>7.9</u>	<u>6.3</u>

Flux Sensitivity. 0.98 $\times 10^{-7}$ A/ ϕ_0

or 22.0 mV/ ϕ_0 (sens. $\times 1$)

Current Sensitivity 4.5 $\times 10^{-9}$ A/mV (sens. $\times 1$)

Probe Test

Low Temperature RF Tuning Capacitor 180 pF

DC Voltage Mode

Voltage Gain ($V_{\text{out}}/V_{\text{in}}$). NA $\times 10^8$ (1% accuracy)

Input Voltage Equivalent Noise (input shorted) NA $\times 10^{-13}$ V rms

AC Impedance Mode

Standard Mutual Inductor NA μ H (1% accuracy)

Physical Tests

Upper Housing Leak Tight, Leak Rate $< 2 \times 10^{-5}$ std. cm³ of ⁴He/sec. NA

Sealed SQUID Holder Leak Tight, Leak Rate $< 2 \times 10^{-7}$ std. cm³ of ⁴He/sec. NA

Checked by: Ken Miller
Ken Miller

Date: September 22, 1978

Approved by: Richard T. Johnson
Richard T. Johnson

Date: September 22, 1978

SHE CORPORATION

Invented in the early 1960's, the superconducting quantum interference device (commonly known by the acronym SQUID) remained a laboratory curiosity for many years. SHE pioneered the development of practical measurement systems based on this remarkable device. The first commercially available SQUID and associated electronics was introduced in 1970 by SHE, and our apparatus is now used routinely by hundreds of scientists and engineers in laboratories around the world. We continue to play a leading role in advancing the basic technology and in developing many new SQUID-based instruments. Representative SQUID systems designed and built by SHE include:

- Ultrasensitive superconducting magnetometers and gradiometers used for geophysical exploration and research, magnetic anomaly detection and studies of biomagnetic fields;
- Variable temperature small sample magnetometers and susceptometers;
- Instruments for measuring electric and magnetic properties of materials at very low temperatures; and
- A high gain, low impedance dc amplifier with a 10^{-4} K noise temperature.

The SQUID is the most sensitive magnetic flux detector known today. It has often been referred to as a cryogenic or superconducting magnetometer, and indeed the measurement of extremely small magnetic fields is one of its most important applications. However, the scope of the SQUID's usefulness extends far beyond simple field measurements. Almost any low frequency electric or magnetic signal that can be converted into a corresponding magnetic flux signal will be detected at a greater level of sensitivity with a SQUID than with any other instrument. Applications of SQUID systems have ranged from the investigation of magnetic and electronic properties of materials to the search for geothermal energy sources, from studies of paleomagnetism to biomagnetic research, and from the measurement of millikelvin temperatures to the detection and characterization of subsurface magnetic structures on land and at sea.

A simple SQUID system for making external magnetic field measurements is shown schematically in Fig. 1. The principal components are identified on the figure. The SQUID sensor and its associated input circuitry must be operated at very low cryogenic temperatures. As illustrated in Fig. 1, the most common means to provide the necessary cryogenic environment is to immerse the SQUID and input circuitry directly in liquid helium which boils at 4.2 K under normal atmospheric pressure. Liquid helium containers, or dewars, specifically designed for SQUID use are now available from SHE with evaporation rates and capacities sufficient to operate the SQUID for weeks or even months between refills (see Data Sheet on liquid

helium dewars). A low thermal conductivity rf transmission line connects the SQUID sensor to the room temperature electronics, which consists of an rf head located at the helium dewar and a separate control unit where the output signal is obtained.

The SHE Series 300 SQUID systems are based on the remarkably successful TSQ sensor and on a new generation of control and readout electronics designed specifically to complement the TSQ's outstanding capabilities. Both the sensor and electronics, which culminate nearly two years of intensive development and testing effort, advance the state-of-the-art in a number of significant ways. The TSQ sensor is described below. The accompanying Data Sheets present detailed information on the other components and contain complete specifications for various systems and standard measuring instruments based on the SQUID.

Fig. 2. The TSQ encapsulated SQUID sensor photographed approximately 2 $\times$ full size. Superconducting connections to the input coil are readily made using the niobium screw terminals. The two pins opposite the input terminals attach to the rf transmission line.

Fig. 1. Schematic drawing of a typical SQUID system for sensing external magnetic fields.

THE TSQ SENSOR

The TSQ sensor is shown in Fig. 2. The SQUID itself is hermetically sealed inside a protective casing to prevent possible damage from moisture condensation, ice, freezing air, or excessively fast temperature changes. The two coils required for rf excitation and for introducing the signal are permanently installed inside the SQUID. The niobium screw terminals shown at one end of the TSQ package are provided to facilitate making a superconducting connection to the input coil.

The TSQ sensor features an entirely new type of weak link which we have incorporated into an optimum toroidal SQUID geometry. The ruggedness and reliability of this new SQUID sensor are unsurpassed, and yet it retains the low noise, exceptionally low drift, and freedom from small, subquantum flux jumps that was available in the past only from comparatively

delicate point-contact devices. The toroidal geometry improves the coupling to external pickup coils, giving a greater *usable* sensitivity (see below), and it protects the weak link from exposure to ambient and to signal magnetic fields. The response of the TSQ sensor is extremely linear (better than 0.1 ppm) over an enormous dynamic range, not only at dc but also when operating near the very high slew-rate limits of our Model 330 electronics. Furthermore, the TSQ is about an order of magnitude less sensitive to temperature than other commercially available SQUIDS, and can be operated equally well from 5 K down to 0 K without loss of performance.

The basic response of a SQUID is to magnetic flux, and it is often convenient, though sometimes misleading, to specify noise and performance of the device in terms of the flux quantum, $\phi_0 = 2 \times 10^{-7}$ G-cm² = 2×10^{-15} Wb. (The relationship between flux noise in the SQUID and sensitivity of a particular instrument — a magnetometer, for example — is pointed out in the appropriate Data Sheets.) Intrinsic noise of the TSQ SQUID is very small and at least partially masked by electronic noise. When measured with a SHE Model 330 SQUID electronics, the total noise from the TSQ sensor and the electronics is essentially "white" over the range 0.05 Hz to 5 kHz, and expressed in terms of equivalent flux noise in the sensor is typically about 1.5 to $1.7 \times 10^{-4} \phi_0$ rms per root hertz of measuring bandwidth.

We *guarantee* for every Series 300 SQUID system that the total shorted input noise from both sensor and electronics will not exceed $2 \times 10^{-4} \phi_0$ rms/ $\sqrt{\text{Hz}}$ in the range 0.1 Hz to 5 kHz. This result will be obtained without the requirement for unusual precautions, such as careful regulation of the helium bath temperature or pressure, cancellation of the earth's field prior to cooldown, or use of an electromagnetically screened room.

When comparing different SQUIDS and their associated electronics it is most important to note that a low flux noise in the sensor itself is of little value if an efficient means is not provided to couple in an external signal. The only meaningful quantity for comparison is the signal-to-noise ratio that can be obtained at the input terminals; this involves the input coil inductance and its coupling to the SQUID (mutual inductance) as well as the flux noise in the SQUID. An appropriately combined measure of all these quantities is the energy sensitivity δE_i at the sensor input:

$$\delta E_i = \frac{L_i I_N^2}{2} = \frac{L_i}{2} \left(\frac{\phi_N}{M} \right)^2$$

where ϕ_N is the rms equivalent flux noise in the SQUID, M is the mutual inductance between the input coil and the SQUID, $I_N = \phi_N/M$ is the equivalent input coil noise current corresponding to ϕ_N , and L_i is the in situ self inductance of the input coil.

For the TSQ sensor, as measured with a Model 330 SQUID electronics operating in the flux-locked loop mode, the values for these quantities are:

$$L_i = 2 \mu\text{H}$$

$$M = 20 \text{ nH (corresponds to } 0.1 \mu\text{A}/\phi_0)$$

$$\phi_N = 4 \times 10^{-19} \text{ Wb (max.) in a 1 Hz bandwidth}$$

$$I_N = \phi_N/M = 2 \times 10^{-11} \text{ A (max.) in a 1 Hz bandwidth}$$

Therefore, the guaranteed maximum equivalent input noise energy for the TSQ sensor is

$$\delta E_i = (1/2) (2 \times 10^{-6}) (2 \times 10^{-11})^2 = 4 \times 10^{-28} \text{ J/Hz}$$

The actual measured value obtained under quiet conditions is typically about 40% less than this figure.

Figure 3 presents the results of a computer analysis of the "shorted input" noise spectrum from a TSQ sensor taken under laboratory conditions over a 16-hour period.* The sensor input was shorted with a 2Ω resistor rather than a superconductor in order to avoid pickup of any very low frequency flux noise from the external magnetic shields. The extra flux noise generated by Johnson noise currents in this resistor is indicated in the figure. The significant feature to note from Fig. 3 is that the onset of the characteristic $1/f$ behavior of the noise spectrum is at a very low frequency, about 0.01 Hz. While regulation of the helium bath temperature might decrease the $1/f$ contribution, this is clearly unnecessary for most applications.

Fig. 3. Computer analysis of the low frequency noise spectrum from a TSQ sensor and Model 330 SQUID electronics. The rf bias frequency is 19 MHz. Total noise output (curve A) contains a contribution of 1.2×10^{-28} J/Hz due to a 2Ω resistor connected across the sensor input terminals while the measurements were being taken. Curve B is the residual "white" noise attributed to the SQUID and electronics.

*We are grateful to Prof. J. Clarke of the University of California, Berkeley, for making these low frequency noise spectrum measurements in his laboratory and for permission to present the results here.

Figure 4 shows a representative recorder tracing of the output from a TSQ SQUID and Model 330 electronics over a 16 hour period. In this case, the measurements were taken in our plant without any special shielding precautions or temperature regulation. Our normal activities, including electric arc welding in an adjacent room, continued as usual. Note the complete absence of flux jumps and the extremely small zero drift. This unprecedented performance is routinely achieved with the new Series 300 SQUID system.

Fig. 4. Recorder tracing of a typical SHE SQUID system drift test performed in an open laboratory environment without special temperature regulation or electromagnetic shielding. The sensor was cooled (and operated) in the earth's field by direct immersion in a liquid helium dewar which was freely vented to atmospheric pressure. Total drift, measured from maximum to minimum excursion, over the 16 hour period shown was $4 \times 10^{-4} \phi_0$. These tests have been extended to as long as 3 days during which the total excursion does not exceed $6 \times 10^{-4} \phi_0$.

COMPLETE SYSTEMS

Among the complete SQUID systems offered by SHE are

- magnetometers for single- and multiple-component vector field measurements,
- magnetic field gradiometers with uniform field rejection as good as 0.1 ppm, and
- magnetometers for the measurement of small magnetic moments and/or susceptibilities from cryogenic temperatures to well above room temperature.

Accessories are also available to permit making extremely sensitive voltage measurements from low impedance sources at cryogenic temperatures and for ac bridge measurements of tiny susceptibilities and resistances. These systems and accessories are described in the data sheets and brochures contained in our catalog, or the information and specifications may be obtained separately on request from SHE. We are also publishing a continuing series of Technical Notes which explain the basic principles behind these remarkable instruments and how the SQUID can be applied to a number of different types of measurement problems.

While a number of "standard" designs for various systems are available, SHE is prepared to offer design suggestions and technical assistance to tailor any system to your particular requirement. If you are not certain of the feasibility of a given measurement, we urge you to discuss it with our technical staff.

SHE CORPORATION

MODEL 30

SQUID CONTROL

FEATURES

- Fully remote operation of SQUID system
- Simple, fast initial set up without auxiliary test equipment
- Exceptionally low drift
- Insensitive to variable thermal and group loop potentials
- Very low cross talk in multi-channel systems
- Three stability/maximum slew rate modes
- Unique noise rejection circuit
- 20 kHz bandwidth, response to 200 kHz
- Built-in notch and low-pass output filters
- Three sensitivity ranges
- Virtually unlimited dynamic range

The Model 30 SQUID Control unit is the most versatile, easiest to use SQUID control available. It has a number of unique and important new features that dramatically improve SQUID system performance, both in the laboratory and under the most difficult field conditions. The operational characteristics of the Model 30 are described here assuming it is used with a Model 300 rf head and a standard SHE SQUID probe. Detailed system specifications are presented on the SQUID System Specifications sheets and also in the complete instruments brochures.

GENERAL DESCRIPTION

The Model 30 control unit contains all the low frequency electronics needed to operate the SQUID system in a "flux-locked loop." The operating controls, system checkout circuitry and outputs are part of the control unit. It is designed to operate from line power or from batteries, and a ruggedized portable version is available with a built-in rechargeable battery pack. A tilt-bail and carrying handle are provided with the standard unit. For easy rack mounting, the Model 30 housing can be fastened to other half-rack width SHE instruments, including another Model 30 control unit when multiple SQUIDs are being used. Detachable rack mount fittings are available.

REMOTE SET UP AND OPERATION

To facilitate the operation of the SQUID system at locations remote from the rf head, all set up controls are located at the control unit. The SET 1 and SET 2 functions activate special internal test circuits* and convert the panel meter into a sensitive tuning indicator. The initial set up adjustments are made quickly and precisely, and the whole procedure is entirely self-contained, so no auxiliary test equipment is needed. Once the controls have been set properly for a given measuring configuration, no further adjustments are required, even if the probe and sensor are warmed to room temperature and then recooled to operating temperature. If the input circuitry or other parameters of the system are changed, the internal set up functions make it easy to re-establish the optimum operating conditions.

One of the most important benefits of the tuning circuitry contained in the Model 30 is that the optimum settings can be established even in the presence of relatively large input signals or noise. For example, a magnetometer having an ultimate sensitivity of 10^{-9} G can be put into operation when there is as much as 0.5 mG of 60 Hz interference. This corresponds to a slew rate of $10^4 \phi_0/\text{sec}$, more than most other SQUID systems will be able to track at all, much less permit adjustment for peak performance. This capability, available only from SHE, is essential when the SQUID is used for sensitive magnetometry in an unshielded environment, and it removes a serious limitation for many other applications.

Standard length for the cable connecting the Model 30 to the rf head is 6 m (20 ft). A longer 100 m (328 ft) cable is available as an option, and other cable lengths can be supplied on request. Cables much longer than 100 m may be used, but there will be some loss of slew rate and high frequency response.

LOW DRIFT AND IMMUNITY TO GROUND LOOP VOLTAGES

The long-term drift and stability characteristics of a SQUID system become an important consideration when dc measurements near the limits of resolution are made over extended periods of time, especially when constant supervision is not available. Recognizing that none of the previously existing SQUID systems were sufficiently stable and free of long-term drift to be very useful for such measurements, an intensive effort was made to identify the principal sources of drift and to systematically eliminate them from the SQUID system. This effort, which influenced the design of every major component of the system, was enormously successful. A unique feedback scheme* is employed for the first

time in Model 30 to reduce by two or three orders of magnitude the dc drifts due to changing thermal emfs or ground loop potentials generated between the rf head and control unit. These stray emfs may vary with changes in ambient temperature and humidity, position of the sun (for outdoor measurements), the switching on and off of nearby electrical apparatus, etc. No periodic readjustments are required to maintain the full system performance under these changing conditions.

We have also controlled the various drifts caused by the slight increase of probe resistance as the helium level drops in the dewar. An added benefit of the Model 30 circuitry is that interaction between several SQUID systems sharing a common ground link is effectively eliminated. This is quite a significant development for multiple-axis magnetometers and other systems of similar complexity where interchannel cross talk can seriously degrade performance.

MULTIPLE SLEW RATE SELECTION

For many applications the most significant feature of the Model 30 control unit is the availability of three locked-loop operating modes, SLOW, MED and FAST, each characterized by a different slew rate response. To understand the critical importance of selectable slew rate response for SQUID systems we must examine the technique used to obtain a large linear dynamic range from an rf-biased SQUID. The rf-biased SQUID has an intrinsically periodic response to magnetic flux, the period being the flux quantum ϕ_0 , which is equal to 2.07×10^{-15} Wb. To obtain an output that is a linear rather than periodic function of the input flux signal, a negative feedback flux is applied to the SQUID such that the sum of the flux change due to the input signal plus that produced by the feedback is always very nearly equal to zero. This is called a flux-locked loop. The voltage required to produce the feedback is a highly linear measure of the input signal and is read as the output of the system. If the input signal to the SQUID changes at a greater rate than the feedback loop can follow, the output will exhibit occasional discontinuities, or flux jumps. These jumps result in a distorted reproduction of the input signal and produce a permanent offset in the dc level.

The maximum speed with which the output can accurately follow a quickly changing input signal is called the slew rate limit of the system. The slew rate limit, when referred to the SQUID input, is given as the maximum number of flux quanta per second (ϕ_0/sec) that can be followed without flux jumping. Maximum slew rates for simple SQUID systems are typically about $10^3 \phi_0/\text{sec}$. In 1971 SHE developed the first fast slewing SQUID system that could track signals up to nearly $10^5 \phi_0/\text{sec}$. Now, with the standard Model 30 in the FAST mode, one can track full scale ($10^3 \phi_0$ p-p).

*pat. pend.

sinusoidal signals at frequencies up to at least 100 Hz. This corresponds to a maximum slew rate in excess of $3 \times 10^5 \phi_0/\text{sec}$, and modifications are possible for special applications to increase this to nearly $10^6 \phi_0/\text{sec}$.

It is important to realize that although the user may not intend to observe or measure signals requiring such a large slew rate capability, there may arise situations where ambient noise (line-frequency interference, for example) rather than the desired signal itself, determines the slew rate requirements for the system. To recover small signals from a noisy background by filtering the noise from the output, it is first necessary that the SQUID system be able to accurately track *all* signals present at the input, including the noise. Although occasional flux jumps may be tolerable, frequent jumps can completely obscure and prevent recovery of the desired signal. Thus a large reserve slew rate capability is often the deciding factor in performing a given measurement successfully.

When the system response is speeded up to handle very fast input signals, sensitivity to rf noise bursts and to spurious nonmagnetic electrical transients is also increased; and this too can result in undesirable flux jumping. Sources of transient interference, which include arcing from electric motors or switches, radio transmissions, and even distant lightning strokes, are present for nearly all applications. It is therefore important to have a selection of different performance characteristics to closely match the slew rate requirement to the measuring situation and thus minimize sensitivity to spurious transients. Ability to remain locked while subjected to strong electrical transients is greatest in the SLOW mode; ability to track rapidly varying magnetic signals is greatest in the FAST mode.

UNIQUE NOISE REJECTION CIRCUIT*

To enhance the system stability in all modes, we have devised a novel noise rejection circuit for the Model 30 control unit. The effect of this circuit is to selectively discriminate against transients that have entered the system but could not have been caused by proper magnetic input signals. As a result, the SQUID system remains locked, even in the FAST mode, under conditions that were previously impossible to handle. The SLOW mode, which still maintains a maximum slew rate of about $1.5 \times 10^3 \phi_0/\text{sec}$ (typical), has the greatest stability in the presence of electrical transients of any SQUID system we know of.

FREQUENCY RESPONSE AND OUTPUT FILTERS

The frequency response of the system is essentially flat from dc to 20 kHz (-3 dB point) in the FAST mode. A separate high frequency output with response extending beyond 200 kHz is provided for signal amplitudes less than $0.5 \phi_0$ p-p. To assist in removing unwanted noise from the output, the Model 30 control unit has five low-pass filters with 12 dB/octave rolloff commencing at 100 Hz, 10 Hz, 1 Hz, and 0.1 Hz respectively, and a powerline frequency notch filter which can be switched in or out independently of the low pass filters. The filter capacitors always track the output voltage to minimize long charging transients when a new filter is switched into use. Dc stability is only very slightly decreased when the filters are used.

*pat. pend.

VERSATILE RESET CIRCUITRY

The Model 30 output may be reset to zero or to any other point in the operating range of the instrument by depressing a front panel pushbutton or by applying a TTL signal to the System Interface connector. It can also be reset automatically whenever the output exceeds any preselected level between ± 1 V and ± 10 V (full scale).

The total dynamic range of the system can be extended almost indefinitely by using the versatile automatic reset circuitry. For example, when the system is operating on the $\times 100$ range, with a deflection factor of $2 \text{ V}/\phi_0$, the full scale limit without resetting is $\pm 5 \phi_0$. If the automatic reset controls are adjusted to reset the output to zero each time it reaches a full scale deflection, either $+5 \phi_0$ or $-5 \phi_0$, the dynamic range can be extended almost indefinitely by simply counting the number of resets, each of which will correspond to a $5 \phi_0$ change in the output. TTL compatible signals containing the reset information are available at the rear panel System Interface connector to automatically keep track of the reset operation with an up/down counter.

Activating the reset circuitry causes the output to change (reset) to a new "lock point" separated by an *exactly* integral number of flux quanta from its previous value. Since the change in output voltage corresponding to one flux quantum can be measured easily and very precisely, it is a simple matter to know the number of quanta jumped by the reset operation and thus to know precisely the consequent shift in output voltage. This feature is very powerful when used to effectively extend the dynamic range of a recorder connected to the output. For example, the full-scale recorder sensitivity may be set to $\pm 1 \phi_0$ (i.e., ± 2 V on the $\times 100$ range) and the Model 30 adjusted to reset automatically whenever the output reaches $\pm 1 \phi_0$. The recorder will then never go off-scale; and, if the resets are not too frequent, it is a simple matter to reconstruct the actual system output from the record.

When the system output is reset to "zero," it will lock onto a definite symmetry point in the periodic response pattern of the SQUID. This symmetry point may not correspond to exactly zero volts output, but it cannot be further away than $\pm \phi_0/2$ from zero. In order that the voltage may be set precisely to zero (or to any other voltage in the ± 10 V range of the instrument), the Model 30 has a highly stable 10-turn offset control with a resolution of $10^{-3} \phi_0$. This resolution and stability is especially needed when it is desired to examine very small (subquantum) signals on a sensitive recorder.

TECHNICAL DATA

Technical data pertaining solely to the Model 30 is given here. A detailed set of performance specifications is given on the SQUID System Specifications sheets.

Dimensions	3.4 in H $\times$ 8.5 in W $\times$ 13.2 in D (87 mm H $\times$ 215 mm W $\times$ 336 mm D)
Weight	8.0 lb (3.6 kg)
Power Requirements	115 Vac (75 mA) or 230 Vac (37 mA), 48 – 400 Hz; or ± 24 Vdc (150 mA). Power requirements for rf head are included in these figures.
Enclosure	Sturdy cast aluminum frame with vinyl clad aluminum covers, tilt-bail and carrying handle. Two Model 30 control units or one Model 30 plus one other SHE half-rack instrument can be fastened together into a single rack-mountable unit. Rack mount adapters available for full or half-rack installation.
Rear Panel Connectors	HF OUT — special output for high frequency signals outside normal bandwidth, response to 200 kHz. EXT FB — used when flux feedback cannot be supplied via rf coil (e.g. for picovoltmeter or ultralinear magnetometer applications). TEST IN (for injecting test signal into SQUID), rf DETECTOR output, 50 kHz modulation SYNC — all used for checking system performance. SYSTEM INTERFACE connector — Inputs: reset, ± 24 Vdc, electrical ground. Outputs: autoreset, reset sign, floating signal output, external feedback, rf detector, modulation sync, high frequency output.
Options	Rack mount adapters for half or full rack width. Ruggedized field version of Model 30. Rechargeable battery pack and connecting cable.

SHE CORPORATION

MODEL 300 RF

FEATURES

- Low noise, low drift
- Highly stable against large changes in ambient temperature
- Fully remote operation including all setup adjustments
- Insensitive to rf interference

The compact Model 300 rf head attaches directly to the SQUID transmission line through a type N connector. Its function is to provide the 19 MHz SQUID bias and to amplify and detect the rf response from the SQUID. The rf head may be located up to 100 meters from the control unit without any loss of performance. Longer separations are possible with some sacrifice in the maximum slew-rate and in the high frequency response. The rf bias level and input tuning adjustments of the rf head are made by means of control voltages generated at the control unit; there are no setup or operating adjustments to be made at the rf head itself. This feature is especially important for applications requiring long separations between the control and rf units.

The Model 300 rf unit is extremely stable against changes in ambient temperature. When used with a standard SHE SQUID probe and a Model 30 control unit, on the most sensitive range, the system output drifts by less than 4 ppm/°C (referred to full scale) as a function of ambient temperature at the rf head. This drift is reduced in direct proportion to the sensitivity on the less sensitive ranges. A full 10°C temperature change at the rf head is required just to cause the system output to drift by an amount equal to the rms system noise per unit bandwidth. It is thus possible to make dc measurements of extremely high sensitivity in environments where the ambient temperature changes over rather wide limits.

Although the standard carrier frequency for the Series 300 SQUID system is 19 MHz, operation at higher frequencies (e.g., 25 or 30 MHz) may be specified as an option. In general, the 19 MHz carrier is preferred because there is less interference at this frequency. For systems employing more than one SQUID, it is advisable to operate each SQUID at a slightly different frequency to avoid mutual interference. For such applications the rf unit may be ordered with suitably spaced frequencies, typically 0.2 MHz separation.

TECHNICAL DATA

Rf Bias Frequency	19 MHz $\pm$ 0.1, crystal controlled (other frequencies up to 30 MHz available on special order)
Rf Injection	0 – 100 μ V via 3 pf, adjusted from control unit
Temperature Coefficient of rf Level	0.2%/°C
Overall Gain	83 dB nominal gain, rf input through detector (dc output/rms input)
Carrier Level for Linear Operation	20 μ V – 250 μ V
Bandwidth	$\pm$ 150 kHz at carrier frequency
Noise	< 2 nV/ $\sqrt$ Hz referred to input
Tuning Capacitance at Input	35 – 85 pf, adjusted from control unit
System Output Drift	< $2 \times 10^{-5} \phi_0$ /°C at any point in range 0°C to 40°C (for TSQ sensor and Model 30 control unit)
Power Requirements	Approximately 3 watts, provided by SQUID control unit
Dimensions	37 mm $\times$ 76 mm $\times$ 95 mm (1½ in. $\times$ 3 in. $\times$ 3¾ in.)
Weight	0.5 kg (1 lb)

Complete performance specifications for the systems using the Model 300 rf head are given on the separate SQUID System Specifications sheets.

APPENDIX D

ELECTROMAGNETIC INDUCTION BY A VERTICAL MAGNETIC DIPOLE ON A HOMOGENEOUS EARTH

APPENDIX D

ELECTROMAGNETIC INDUCTION BY A VERTICAL MAGNETIC DIPOLE ON A HOMOGENEOUS EARTH

1.0 INTENSITIES OF FIELD COMPONENTS

This report summarizes a preliminary calculation estimating the intensities of the electromagnetic field components generated by a vertical magnetic dipole (a horizontal loop) at the surface of a homogeneous earth. The fields are calculated for earth conductivities of 10^{-3} , 10^{-1} and 10 siemens/m at frequencies of 10^{-3} to 10^3 Hz; over a range of source-receiver spacings from 100 meters to 10 kilometers.

The original development for electromagnetic induction in a homogeneous earth by a vertical magnetic dipole (a horizontal loop of wire) was presented in a series of papers by Wait (1951, 1952, 1953, 1954, 1955) and except for sign correction in H_z and E_θ pointed out by Bhattacharya (1959), these are the expressions used below.

The case to be considered is that illustrated in Figure 1, namely a vertical dipole created by a loop of wire having a dipole strength IdA ; I being the electric current in amperes (multiplied by the number of turns if a multi-turned source is used) and dA is the cross-sectional area in meters-squared. All units are in MKSA. As shown in Figure 1, the observer is at a radial distance ρ from the center of the source which also serves as the origin of our coordinate system. We assume the conductivity of the atmosphere is zero, but that dielectric effects are still finite. Moreover, we assume that the permittivity, ϵ_0 , and permeability, μ_0 , everywhere take on the values of free-space.

It is useful to compare the expressions presented by subsequent workers (Bhattacharya, 1959; Ward, 1967) in order to allay any question regarding misprints, sign errors and algebraic manipulation. Bhattacharya (1959) presents the expressions using the propagation constant of air as $\gamma_0^2 = -\omega^2 \mu_0 \epsilon_0$ and the propagation constant of the earth as $\gamma_1^2 = i\omega \mu_0 \sigma - \omega^2 \mu_0 \epsilon_0$. In this case

$$H_z = \frac{IdA}{2(\gamma_0^2 - \gamma_1^2)\rho^5} \left[(9 + 9\gamma_0\rho + 4\gamma_0^2\rho^2 + \gamma_0^3\rho^3)e^{-\gamma_0\rho} - (9 + 9\gamma_1\rho + 4\gamma_1^2\rho^2 + \gamma_1^3\rho^3)e^{-\gamma_1\rho} \right]$$

Figure 1

and

$$E_{\theta} = \frac{i\omega\mu IdA}{2\pi(\gamma_0^2 - \gamma_1^2)} \frac{1}{\rho^4} \left[3 + 3\gamma_0\rho + \gamma_0^2\rho^2 e^{-\gamma_0\rho} \right. \\ \left. - (3 + 3\gamma_1\rho + \gamma_1^2\rho^2) e^{-\gamma_1\rho} \right]$$

Ward (1967) presents the expressions using

$$c = -i\omega\mu IdA/4\pi,$$

where the implicit time dependence is $e^{-i\omega t}$ and the propagation constant is

$$k^2 = \omega^2\mu\epsilon + i\omega\mu\sigma.$$

Assuming that electric diffusion effects dominate displacement field effects in the conducting earth, $k_1^2 = i\omega\mu\sigma_1$, and the fields have solutions of the form: $\exp(ikr)$.

In this case

$$H_z = \frac{-2c}{i\omega\mu k_1^2} \frac{1}{\rho^5} \left[9 - (9 - 9ik_1\rho - 4k_1^2\rho^2 + ik_1\rho^3) e^{ik_1\rho} \right]$$

and

$$E_{\theta} = \frac{2c}{k_1^2 \rho^4} \left[3 - \{3 - 3ik_1\rho - k_1^2\rho^2\} e^{ik_1\rho} \right]$$

Upon noting that Ward's (1967) time dependence is $\exp(-i\omega t)$ whereas that of Bhattacharya (1959) is $\exp(i\omega t)$, we take the complex conjugate of Ward's expressions, after which $(k^2)^* = -i\omega\mu\sigma$ or $(k^2)^* = -\gamma^2$.

Hence, Ward's expressions become:

$$H_z = \frac{-IdA}{2\pi\gamma_1^2} \frac{1}{\rho^5} \left[9 - (9 + 9\gamma_1\rho + 4\gamma_1^2\rho^2 - \gamma_1\rho^3) e^{-\gamma_1\rho} \right]$$

and

$$E_{\theta} = \frac{-i \text{IdA}}{2\pi\gamma_1^2} \frac{1}{\rho^4} \left[3 - \{3 + 3\gamma_1\rho + \gamma_1^2\rho^2\}e^{-\gamma_1\rho} \right]$$

both of which agree with Bhattacharya's (1959) development, except for the term $\gamma_1\rho^3$ in Ward's expression for H_z . This is obviously a misprint.

In the following discussion, we will use Wait's (1952) expressions for H_z and E_{θ} with the appropriate sign correction noted by Bhattacharya (1959).

The calculations for E_{θ} and H_z involve only complex exponentials, and are readily performed by a variety of computers. However, the calculation for H_{ρ} involves Bessel functions of the second kind having complex arguments. Since packaged programs for these functions are not always readily available, at this stage of our analysis we will go directly to their far-field asymptotic form. This appears to be the most useful limit to consider since we are primarily interested in the design specification of the minimum expected values for H_{ρ} .

The present system design is for a peak current of 50A (100A p-p). Assuming a loop 300m on a side can be deployed consisting of, say, 10 turns of wire, a maximum dipole moment of 10^8 Ampere-turns meter-squared can be generated. Each field strength on the accompanying table can then be multiplied by a factor of 10^8 .

Assuming reference oscillators are available with a stability of better than 1ppm, then the limiting factor on extracting signal from noise will apparently be the finite number of bits available from the A-D converters. For a 12 bit digitizer the resolution is approximately 1 part in 4000. Assuming amplitudes have to be determined with a precision of better than 2.5% (1 part in 40), we have a restriction that the noise to signal ratio has to be less than 100:1 (pp; 50:1 peak).

Magnetometer Considerations

The cryogenic magnetometer has a dynamic range specification of 140db (1:10⁷ amplitude). If it is designed for a #100 γ full-scale sensitivity, it has a lower-limit resolution of 10 microgammas/ $\sqrt{\text{Hz}}$ rms.

Natural noise in the band around 1 Hz has a level on the order of 0.1 to 1.0 milligamma/ $\sqrt{\text{Hz}}$ or is 10 to 100 times stronger than the intrinsic magnetometer noise.

Since we would expect that local thunderstorm activity would raise the level of natural noise by a factor of 100 to 1000, one might expect an rms noise level of 0.1 to 1.0 gammas during a period of high natural activity. According to the above reasoning, a 3 milligamma (p-p) signal can be extracted from 0.3 gammas (p-p) of noise with a resolution of 2.5%.

In summary, magnetic signal levels have to be greater than 3 milligammas (p-p) and noise has to be less than 100 times as great (0.3 gammas, p-p).

3.0 ELECTRIC FIELD CONSIDERATIONS

Generally broad-band natural telluric noise will be less than 10 mV/km peak to peak. If one uses a 100m electrode liner, this noise is reduced to 1 mV (p-p). Presumably a signal 100 times as weak (10 microvolts) can be extracted from this background noise.

Prefiltering in the band around 1 Hz should reduce natural noise to less than 0.1 mV/km, or upon using a 100 meter electrode liner, to a level of 10 microvolts. Since this is still larger than the electronic noise level intrinsic to the better instrument amplifiers, it appears that the system will be limited by natural noise sources rather than internal noise sources.

Therefore, natural noise levels of 0.1 mV/km should be expected, and signals greater than 1 microvolt/km must be available for adequate measurements.

4.0 SUMMARY

From the above considerations of noise and the inspection of the attached calculations, it appears that even in worst-case situations at least one, and generally two, field components can be detected at source-receiver spacings of up to 5 km.

Moreover, in comparing signals at 100m⁸ with those at 5km, one should anticipate a dynamic range of up to 10⁸.

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