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SILICON-ON CERAMIC PROCESS

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Silicon Sheet Growth and Device Development for the Large-Area Silicon Sheet
Task of the Low-Cost Solar Array Project

Quarterly Report No. 15 for April 1—June 30, 1980

By
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Quarterly Report No. 15

by

**A. B. Whitehead, J. D. Zook, B. L. Grung,
K. McHenry, S. B. Schuldt, and P. W. Chapman**

Period Covered: 4/1/80 – 6/30/80

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SUMMARY

The objective of this research is to investigate the technical feasibility of producing solar-cell-quality sheet silicon which could meet the DOE cost goals. The Honeywell approach is to coat one surface of carbonized ceramic substrates with a thin layer of large-grain polycrystalline silicon from the melt. Results and accomplishments which occurred during the quarter can be summarized as follows:

- Two major problems associated with SCIM-coating wide (10-cm) substrates were identified and solved.
- The longitudinal temperature profile in SCIM-II has been improved to prevent substrate warping, buckling, and cracking.
- The transverse temperature profile in SCIM II has been improved to produce more uniform coatings.
- A strategy to eliminate effects of thermal stress has been developed.
- The best SOC cell has a total-area conversion efficiency of 10.5% (AM1, AR), for a cell area of 5 cm².
- A number of experiments are being investigated for improving cell efficiency. Significant improvements were obtained using a slow cooldown after the phosphorus diffusion.
- For the slow-cooldown experiment, the average efficiency of 29 AR-coated cells was 9.9%, with a standard deviation of 0.3%.
- Encouraging results were obtained on SOC material that had been treated in a hydrogen plasma at Sandia.
- Thermal modeling has proven to be beneficial in designing modifications for SCIM II.

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INTRODUCTION

This research program began on 21 October 1975. Its purpose is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by coating inexpensive ceramic substrates with a thin layer of polycrystalline silicon. The coating methods to be developed are directed toward a minimum-cost process for producing solar cells with a terrestrial conversion efficiency of 11% or greater.

By applying a graphite coating to one face of a ceramic substrate, molten silicon can be made to wet only that graphite-coated face and produce uniform, thin layers of large-grain polycrystalline silicon; thus, only a minimal quantity of silicon is consumed. A dip-coating method for putting silicon on ceramic (SOC) has been shown to produce solar-cell-quality sheet silicon. This method and a continuous-coating process also being investigated have excellent scale-up potential which offers an outstanding, cost-effective way to manufacture large-area solar cells. The dip-coating investigation has shown that as the substrate is pulled from the molten silicon, crystallization continues to occur from previously grown silicon. Therefore, as the substrate length is increased (as would be the case in a scaled-up process), the expectancy for larger crystallites increases.

A variety of ceramic materials have been dip-coated with silicon. The investigation has shown that mullite substrates containing an excess of SiO_2 best match the thermal expansion coefficient of silicon and hence produce the best SOC layers. With such substrates, smooth and uniform silicon layers 23 cm^2 in area have been achieved with single-crystal grains as large as 4 mm in width and several cm in length. The thickness of the coating and the size of the crystalline grains are controlled by the temperature of the melt and the rate at which the substrate is withdrawn from the melt.

The solar-cell potential of this SOC sheet silicon is promising. To date, solar cells with areas from 1 to 10 cm^2 have been fabricated from material with an as-grown surface. Conversion efficiencies, η , of about 10% with anti-reflection (AR) coating have been achieved. Such cells typically have open-circuit voltages, V_{oc} , and short-circuit current densities, J_{sc} , of 0.57 V and 23 mA/cm^2 , respectively.

The SOC solar cell is unique in that its total area is limited only by device design considerations. Because it is on an insulating substrate, special consideration must be given to electrical contact to the base region. The preferred method uses slots in the substrate perpendicular to the crystalline growth direction. Electrical contact to the base region is made by metallizing the silicon exposed through the slots on the back side of the substrate. Smooth, continuous coatings have been obtained on substrates which were slotted in the green state prior to high-temperature firing. The best slotted-cell results to date indicate a 10.5% conversion efficiency (AR-coated) on a 5-cm² (total area) cell.

The best experimental coated layers have been produced by dipping the substrate into the melt. However, the dipping process has two limitations if scaled up to a production method: 1) The melt becomes progressively contaminated by the mullite substrate. 2) The coating throughput in terms of area per unit time is limited. For these reasons, an alternative method of applying the silicon is being developed, which is termed SCIM (for Silicon Coating by Inverted Meniscus). The first SCIM-coating facility has successfully coated 5-cm-wide mullite sheets with uniform silicon layers by passing the sheets, carbonized surface down, over a trough of molten silicon. The current objective of this task is to uniformly coat slotted substrate sheets 5 inches wide. An improved SCIM coater has been designed and built to meet the coating throughput goals of the contract.

TECHNICAL DISCUSSION

CONTINUOUS COATING (D. Zook, E. Masterson, F. Schmidt,
R. Hegel, V. Harris, H. Burke, and
H. Wolner)

During the past quarter, two major problems associated with SCIM-coating wide (10-cm) substrates were identified and solved. The problems were: (1) buckling and breaking of the substrates, particularly at low speeds, and (2) nonuniform coating across the width of the substrate. Both problems have been considerably reduced by modifications of the heater elements and other carbon parts. The modifications at the same time have resulted in simpler or fewer parts in the machine.

It has been possible to make the modifications in a timely and effective manner because of three factors: (a) the observations and suggestions of D. Heaps, who is working on the developments of SCIM coating under a SERI program, (b) the theoretical modeling of the longitudinal temperature distribution by S. Schuldt, and (c) availability of help from the machine shop. Although further fine-tuning of temperature profiles is required, the modifications to date have made dramatic improvements, and have increased our understanding of and confidence in the SCIM-coating technique.

Thermal Stresses - Longitudinal Temperature Profiles

The most obvious problem during the initial operation of SCIM II (in March, 1980) was the buckling and/or breakage of the coated substrates. Experiments were performed without silicon in the system to clarify the situation. Initial experiments quickly showed that at high speed (15 cm/min) there was only minor buckling, but at lower speeds the buckling became more severe, and below 6 cm/min the substrates broke. The results were qualitatively the same regardless of the silicon coating and regardless of whether one side of the substrate was carbon-coated.

The original design of the entrance and exit tunnels was on the basis of engineering intuition and the thermal modeling done by S. Schuldt (see Quarterly Report No. 13, Feb. 1980). The design speed was 15 cm/min, which

is the 1980 program goal. The most interesting result is that at this high speed there has been little warping and no cracking of any substrates. This is true of the original design as well as all subsequent modifications.

The problem is that without forced convective cooling or use of any asymmetric growth mode, there is no chance of getting the desired silicon thickness at the high speed. The thickness is needed to demonstrate slot coverage and cell performance. Thus, we want to do initial coatings in the range of 4 to 6 cm/min. At these lower speeds, the substrates have warped, buckled, or cracked. The proposed explanation is that the longitudinal temperature profile must be the cause of the problem. At high speeds the longitudinal profile is smoother than at low speeds because the heat capacity of the substrate causes a temperature lag (see the thermal modeling referenced above). Thus, the purpose of the changes in tunnel design has been to linearize the temperature profile. Fortunately, this has reduced the problem at low speeds, and has not created any problem at high speeds.

The explanation in terms of thermal stresses caused by longitudinal temperature gradients is the same as that proposed by Surek for EFG ribbon growth.¹ The origin of thermal stresses can be understood in terms of Fig. 1 which shows schematically the effect of the temperature distribution along a central section of the substrate. We consider the substrate to be divided into two strips. If there is no temperature gradient, there is no stress. If the temperature gradient is constant (linear temperature profile), there is also no stress, as discussed by Boley and Weiner.² Figure 1(a) shows this case with the width of the two strips tapering uniformly. Since the inner edges fit together perfectly, zero force is required to maintain the edges in contact.

Figure 1(b) shows the case of a nonlinear temperature profile with $d^2T/dx^2 > 0$. In this case, the inner edges do not fit smoothly together. They could be forced together by forces pushing in at the center of the outside edge, but we are considering only thermal stresses, so edge forces are not allowed. The inner edges can be straightened and matched by applying tension at the inside edges and compression on the outside edges, as shown by the arrows in Fig. 1(b). This type of force is allowed if the forces are applied

¹A.D. Morrison, et al., "Large-Area Silicon Sheet by EFG," Mobile Tyco Energy Corporation Annual Progress Report, September 15, 1976.

²B.A. Boley and J.H. Weiner, Theory of Thermal Stress, John Wiley and Sons, New York, 1960.

Figure 1. Thermal stress in a rectangular plate. (a) A linear temperature profile produces no thermal stress because adjacent elements of the plate fit together. (b) If $\frac{d^2T}{dx^2} > 0$, tensile stress at the inside edges and compressive stress at the outside edges of each element are required to make adjacent elements fit. (c) The sign of the stresses changes if the sign of $\frac{d^2T}{dx^2}$ changes.

by the sections of the substrate at the two ends of the section shown. Thus, the substrate is under tension at the center and compression at the edges. The opposite situation is shown in Fig. 1(c).

As discussed by Surek,¹ the equation for the stress is

$$\sigma_{xx} = \frac{\alpha_E b^2}{6} \left(1 - \frac{3y^2}{b^2} \right) \frac{d^2T}{dx^2} \quad (1)$$

in the case where only the second derivative of the temperature is significant. Here, α is the expansion coefficient, E is Young's modulus, and b is one-half the substrate width. The solution is positive at the center ($y = 0$) and negative at the edges ($y = \pm b$), indicating tension and compression, respectively, when $\frac{d^2T}{dx^2}$ is positive. At the ends of the substrate the solution is not valid, since $\sigma_{xx} = 0$. Thus, in the vicinity of the end, there are σ_{yy} and σ_{xy} stresses which can also be derived analytically.¹

It is obvious that the temperature profile cannot be entirely linear in any substrate which is heated and then cooled and that both types of nonlinearities must be encountered, as shown in Fig. 2. Thus, thermal stress must always exist. However, there is a strategy which, at least in principle, can reduce the residual thermal stress to zero.¹ This strategy is detailed in Fig. 2. The idea is to have the concave portions of the profile in regions with high yield stress, and to maintain d^2T/dx^2 sufficiently low that $(\sigma_{xx})_{max}$ does not exceed the yield stress. Thus, thermal stresses do exist, but they result only in elastic deformation so that when the sample is again in a $d^2T/dx^2 = 0$ region, the residual thermal stress is zero. The predicted residual stress pattern is shown in Fig. 3, which is taken from Boley and Weiner.²

Figure 2. Strategy to eliminate effects of thermal stress. In the high-temperature regions, the ceramic can deform without buckling or cracking, and stress in the silicon is annealed as it is generated. At low temperatures, only elastic deformation occurs. The intermediate temperature ranges is critical, and the temperature profile must be linear.

At sufficiently high temperatures, the yield strength of both the ceramic and the silicon is low so that the sample can undergo plastic deformation with no buckling or cracking. Stress relaxation studies in silicon¹ show that at 1000°C the stress relaxation time is a few seconds. The assumption is that the plastic flow occurs by diffusion-controlled climb of disloca-

Figure 3. Theoretical thermal stress pattern and the corresponding residual stress pattern. This figure is taken from Boley and Weiner,² page 538. Their calculation actually applies to a different case, but the equations are identical to our case. In this figure, $\bar{x}$ is the coordinate axis along the width of the sample.

tions, and that the presence of the dislocations is not deleterious to the solar cell performance.¹ Thus, in the vicinity of the trough and especially of the liquid-solid interface, the presence of large nonlinearities in the temperature gradient will not have harmful effects.

In summary, the strategy is to consider the problems in terms of three temperature zones. The following strategy applies to both the heating and cooling zones:

- a) The high zone ($T \geq 1000^{\circ}\text{C}$) can tolerate large nonlinearities in the temperature profile.
- b) The intermediate zone ($1000^{\circ}\text{C} \geq T \geq 500^{\circ}\text{C}$) must have a very linear profile.
- c) The low temperature zone ($500^{\circ}\text{C} \geq T$) can tolerate large nonlinearities such that the thermal stress does not exceed the elastic limit of silicon or ceramic.

Modification of Longitudinal Temperature Profiles

A number of changes have been made in the entrance and exit tunnels to improve the temperature profile. The technique of temperature measurement has also been modified. The original profiles are shown in Fig. 4. These were measured with a fully sheathed thermocouple inserted into the slots in place of the substrate. The thermocouple was moved 2 cm and then the temperature was allowed to stabilize for 20 seconds. The transverse temperature profile could be obtained by pivoting the thermocouple from side to side in the tunnel. Generally, the measurements made by pivoting were in qualitative agreement with the three thermocouple readings under the entrance tunnel (A_1 , A_2 , and A_3) and the three thermocouples under the trough (T_1 , T_2 , and T_3).

During the course of the quarter, the following changes were made, all of which are judged to have been beneficial:

- The carbon felt was removed from the front half of the entrance tunnel and the back half of the exit tunnel, to promote cooling these regions.

Figure 4. Initial temperature profile. Both tunnels were fully insulated, and the tunnel heaters were at the position shown. A₁, A₂, and A₃ are the three trough thermocouple readings and T₁, T₂ and T₃ are the trough thermocouple readings.

- The halves of the tunnels were grooved in the same regions where the felt was removed. The purpose was to reduce the thermal conductance and make these regions cooler. This was not found to be as effective as removing the insulation.
- The entrance tunnel heaters were redesigned to move the maximum in the temperature profile closer to the trough. With this design the side heaters do not appear to be necessary.

The result of these changes is the temperature profile shown in Fig. 5. It is clear that significant improvement in the linearity of the profile has

Figure 5. Temperature profile as of 6/27/80. The curves are direct tracings of the thermocouple chart record, so that the temperature scale is non linear. The arrows indicate the direction of the thermocouple movement.

been achieved and that the temperature maximum is closer to the trough as desired. The data in Fig. 5 were obtained by direct recording of the output of a moving thermocouple. For the profile shown, the velocity was 4.8 cm/min, which was the speed planned for the silicon coating experiments. The thermocouple was driven by the same rollers used to transport the substrate. The thermocouple was not sheathed, and the measurements were made without silicon in the trough, in an N_2 atmosphere. We note that there is considerable hysteresis in the measurements, and that there is not perfect agreement between the entrance and exit tunnel measurements. Clearly, measurements at lower speeds will give more accurate measurements of the actual carbon temperature, whereas measurements of the actual substrate speed give more of an indication of the actual temperature profiles in the substrate.

The results of the improvement in the longitudinal temperature profiles have been very positive. In brief, substrates without silicon can go through the system at speeds from 3 to 30 cm/min. At the high speeds, there is no evidence

of buckling, warping, or breakage. At the lower speeds, some buckling still occurs but no breakage. An exception is a substrate coated with silicon at 4.8 cm/min which split down the middle as described below.

Modification of Transverse Temperature Profile

A primary area of concern at the beginning of the quarter was the uniformity of the temperature in the trough during coating. This has been a long-standing problem in SCIM I, and initially the uniformity was just as bad in SCIM II. The problem is evident in the nonuniformity of the coatings. Fortunately, during the past quarter we feel we have identified the sources of the temperature gradient and have corrected the problem for the most part.

The basic problem is in the asymmetry of the trough heater. One end is connected to the water-cooled copper electrode. At first it was believed that the major problem is in the asymmetry of the radiation environment, and some measures were taken to correct this with insulation. However, more thinking about the problem suggested that thermal conduction to the water-cooled electrode could be the major factor, and that these losses, in principle, are easily compensated.

The strategy is to choose a region of the heater next to the heater support but beyond the end of the fused-quartz trough, in which extra heat will be generated to supply the heat conducted down the supports. It is desired that the temperature of this region be near the melting point of silicon. Thus, the radiation losses from this region will be about the same (per unit area) as those from the rest of the trough heater. The conduction losses are then calculated, and the cross section of the region is reduced so that additional I^2R losses are generated.

The calculation is slightly complicated by the fact that the thermal conductivity of graphite is quite temperature-dependent. An approximate formula, derived by S. Schuldt, is

$$K(T) = 2 \left(\frac{300}{T} \right)^{0.0592} \text{ W/cm } ^\circ\text{C} \quad (2)$$

or more generally:

$$K(T) = K_0 \left(\frac{T_0}{T} \right)^n \quad (3)$$

The heat flux

$$J = K(T) \frac{dT}{dx} \quad (4)$$

is assumed to be constant if the cross section of the supports is constant. The temperature distribution along the support can be obtained by integrating Eq. (4):

$$\int_{x_0}^{x_1} dx = \frac{1}{J} \int_{T_0}^{T_1} K(T) dT \quad (5)$$

The integration gives the result

$$\begin{aligned} J &= \frac{K_0}{1-n} \frac{T_1}{L} \left[\left(\frac{T_0}{T_1} \right)^n - \frac{T_0}{T_1} \right] \\ &= K_e \frac{T_1 - T_0}{L} \end{aligned} \quad (6)$$

where $L = x_1 - x_0$ is the length of each support leg and K_e is an effective thermal conductivity. Using the specific numbers appropriate to graphite, with $T_1 = 1700K$ and $T_0 = 300K$, we get an effective conductivity of graphite of 1.08 W/cm K.

The calculated amount of heat lost by conduction is compared with the amount of heat dissipated per unit length along the heater, and the cross section is then reduced proportionately. By machining an L-shaped cross section, the cross section can be reduced without significantly weakening the structure and without changing the radiating area.

The above calculations were made for the trough heater, the machining was done, and the results were very gratifying. The temperature difference between the inner and outer trough thermocouples (T_1 and T_3 in Figs. 4 and 5) reduced from 150 to 250°C to about 10°C, as measured when no silicon was in the trough, the temperature gradient increased by more than 50°C, and nonuniform coatings were still produced. This led us to a less obvious cause of transverse temperature gradients, associated with the liquid silicon.

The presence of liquid silicon makes a significant change in the radiation losses, and can result in significant temperature gradients between the regions of the trough that contain silicon and those that do not. The reason for this is the low emissivity (0.30) of molten silicon as compared with the emissivity of carbon (0.9). The Stefan-Boltzmann law gives σT^4 losses of 47 W/cm² when $T = 1700\text{K}$. Thus, an emissivity difference of 0.6 results in a difference in thermal losses of 28 W/cm² for the liquid. If the trough heater has a uniform cross section, the I^2R heat being generated is uniform, but the losses are lower in the portion of the trough containing molten silicon. To compensate for this, the temperature of the trough heater under the molten silicon must rise, balancing the losses by increasing T^4 .

Clearly, the strategy to correct this situation is to design a nonuniform trough heater that generates additional heat in the region beyond the end of the quartz trough. The quartz troughs must always be of the same length, and must be filled all the way to the end with molten silicon to ensure uniform trough temperature.

This strategy has been implemented and appears to be successful. After the trough is filled with silicon, the current is lowered so that the liquid is closer to the freezing point. In one experiment, the temperature of the trough was gradually lowered to the freezing point, and freezing started at the edge of the trough rather than at the observer end. The freezing was not uniform along the edge, and the nonuniformity gives a direct measurement of the isotherm in the trough. This information can then be used to further correct transverse temperature nonuniformities in the trough.

Results of Coating

A number of coating runs were made during the quarter. At first there were operational problems associated with the breakage of substrates due to thermal stress, and with mechanical alignment of the system. As the thermal stress problem was improved, the fraction of the coated areas on each substrate was increased. However, buckling of the substrates in the coating zone can create deformations that propagate back to the coating zone. The deformations can be so severe that they cause the meniscus to pull away from the edge, so that the full width is not coated.

By the end of this quarter, the thermal stress and transverse temperature gradient problems had been improved to the point that continuous coating of successive substrates could be achieved. The results of recent runs are shown in Fig. 6. Five substrates were coated at speeds of 4.8 to 30 cm/min. The high-speed runs produce coatings that are extremely thin, as expected. This run was not optimal because of two factors:

- 1) The quartz trough did not properly fit into the heater, so that one end of the trough was raised 2 mm from being in contact with the heater, and the silicon was frozen at that end. The problem can be readily avoided in the future.
- 2) Insufficient power was available for the entrance tunnel heaters so that the substrate was not above 1300°C on coming in contact with the silicon, as indicated in Fig. 5. This problem can also be readily solved.

Because of these two factors, the trough was maintained at a higher temperature than desirable (thermocouple reading 1410°C), which tended to give thin coatings. On the positive side we note that:

- Five substrates were fully coated with no meniscus breaks or instabilities.
- There were no detectable effects of thermal stress at the high speeds. In fact, at the higher speeds, the coating process seemed smoother and easier.

Figure 6. Five recent large-area SOC substrates. The top substrate was coated at 4.8 cm/min; the bottom substrate at 30 cm/min.

On the negative side we note that:

- The substrate coated at 4.8 cm/min did crack down the center. The crack initiated at the end, propagated back into the cooling zone, and continued to propagate as the coating proceeded. There was no visible deformation extending back into the coating region, however, and the coating continued even as the crack propagated.
- At all speeds, there is evident dendrite formation near the edges of the substrate. During coating, the dendrites are visible from the back as bright fingers extending downstream at the dendrites. In these respects the dendrites are similar to those obtained in dip-coating. Unfortunately, we still do not understand the causes of dendrite formation in dip-coating although a number of hypotheses have been tested.

Problem and Concerns

An operational problem relates to the shut-down procedure of SCIM II. On several occasions we have had breakage of the crucible holder and crucible heater. The problem may simply have been insufficient clearance between the crucible and the crucible holder, and this will be corrected. We are also planning to try to freeze the crucible from the bottom using He gas cooling, an idea based on the Heat-Exchanger Method (HEM) of crystal growth.³ Two other operational problems concern delivery of the temperature controllers for SCIM II and delivery of large slotted substrates. It will be very difficult to meet our goal for delivery of slotted substrates to JPL in early September because substrates will not be available until late August.

The near-term objective of SCIM II is to eliminate the dendrites and produce uniform layers that will be thick enough to bridge 1-mm-wide slots in the substrates and be used for solar cells. We hope that this can be achieved by controlling the temperature of the substrate as it comes into contact with

³C.P. Khattak and F. Schmid, "Low-Cost Conversion of Polycrystalline Silicon into Sheet by HEM and FAST," 14th Photovoltaic Specialists Conference, San Diego, 1980, p. 484.

the molten silicon. We also are attempting to have the radiative environment approximate that which occurs in dip-coating. In this way we should be able to produce growth conditions in the SCIM-coater that duplicate dip-coating.

In order to achieve our throughput goal ($350 \text{ cm}^2/\text{min}$), we need to coat at 14 cm/min or more. This is most likely achievable using the "fast-growth mode." At this point, however, fast-growth has not been attempted in SCIM-coating. The most promising approach appears to be the "cold-substrate mode" using a hot shoe on the silicon side and a cold shoe on the substrate side. We plan to implement this scheme in SCIM II.

DIP-COATING (K.D. McHenry and D. Sauve)

Dip-Coating results for the second quarter of 1980 are summarized in Table 1. Runs 252 through 255 were performed in the old production dip-coater; runs 469 through 473, in the experimental dip-coater. During the past quarter, the responsibility for dip-coating production has been transferred to the experimental dip-coater. The design of the experimental dip-coater permits the flexibility of performing both production and experimental runs.

Several problems were encountered during the reporting period which reduced the number of runs performed. One problem was intermittent power outages and an interruption of the water supply to the experimental dip-coater. These led to several aborted runs. In addition, the interruption of the water supply did some damage to the dip-coater. Several O-rings and gaskets were melted and two SCRs in the power supply required replacement.

The other major problem was availability of substrates. Because of production difficulties, Coors Porcelain Co. was unable to supply any type "O" substrates for the last month of the quarter. As a result of this delay, old type "Q" and type "K" substrates were used in runs 471 and 472. These substrates did not work as well and there were problems with dendrite formation and substrates cracking.

With an adequate supply of type "O" substrates now in hand, it is possible to resume production and experimental dip-coating. The first experiment to be performed will be the resumption of fast-growth with an afterheater in place.

Table 1. Dip-Coating Production^a

Run No. Run No.	Number Dipped	Comments
252	12	Substrates 1 and 2 cracked.
253	12	100% yield.
254	11	91% yield.
255	12	"Q" substrates cracked. "O" substrates good.
469	11	Dendritic formation on first five substrates.
470	12	Video-taped the dipping of first three substrates..
471	18	Problems with dendrite formation and open slots.
472	11	Dendritic formation on first five substrates.
473	14	All substrates type "O". 1 substrate froze in the melt. 1 substrate broke on cooling.

^aAll SOC substrates were grown at 3.60 cm/min and were boron-doped at $5 \times 10^{16}/\text{cm}^3$.

CELL DEVELOPMENT (B. Grung, T. Heisler, and S. Znameroski)

Currently, the best SOC cell has a total-area conversion efficiency, η , of 10.48% (AM1, AR), for a cell area of 5 cm^2 . The primary characteristics of this cell are given in Tables 2 and 3, along with the corresponding characteristics of 87 recent SOC cells. The average efficiency of 51 AR-coated cells is 9.6%, with a standard deviation of 0.6%. Very recent results indicate a significant improvement in SOC cell performance for cells fabricated using a slow cooldown after the phosphorus diffusion, as described below. For the slow-cooldown SOC cells, the average efficiency of 29 AR-coated cells is 9.9%, with a standard deviation of 0.3%.

Table 2. Conversion efficiencies of recent slotted-substrate SOC cells.

item	Cell Number	Base Doping (atoms/cc)	Dip Speed (cm/sec)	RA Product (ohms-sqcm)	Base Sheet Resistance (ohms/□)	Total Area Conversion Efficiencies	
						Before	After
						AR (%)	AR (%)
1	205 - 3-111	1.0e+016	0.06	0.9	90.0	6.33	
2	205 - 3-211	1.0e+016	0.06	1.0	90.0	6.57	
3	206 - 3-111	1.0e+016	0.06	1.0	86.0	7.09	10.15
4	206 - 3-211	1.0e+016	0.06	1.0	86.0	6.94	10.26
5	212 - 1-111	1.0e+016	0.06	1.2	66.0	4.99	
6	212 - 1-211	1.0e+016	0.06	1.1	66.0	3.28	
7	226 - 3-111	4.7e+016	0.06	0.7	24.0	6.45	9.28
8	226 - 3-211	4.7e+016	0.06	0.8	24.0	6.93	9.62
9	238 - 8-111	5.0e+016	0.06	1.0	29.0	6.95	9.56
10	238 - 8-211	5.0e+016	0.06	0.8	29.0	5.95	8.51
11	239 - 1-111	5.0e+016	0.06	0.8	27.0	5.76	
12	239 - 1-211	5.0e+016	0.06	0.8	27.0	5.06	
13	241 - 4-111	5.0e+016	0.06	0.7	29.0	6.40	8.77
14	241 - 4-211	5.0e+016	0.06	0.8	29.0	5.57	8.17
15	244 - 3-111	5.0e+016	0.06	0.6	18.0	5.73	8.40
16	244 - 3-211	5.0e+016	0.06	0.8	18.0	7.15	9.75
17	244 -11-111	5.0e+016	0.06	0.7	22.0	6.03	8.43
18	244 -11-211	5.0e+016	0.06	0.8	22.0	7.08	9.79
19	244 -12-111	5.0e+016	0.06	0.7	21.0	6.70	9.42
20	244 -12-211	5.0e+016	0.06	0.8	21.0	5.71	8.50
21	246 - 7-111	5.0e+016	0.06	1.3	34.0	4.68	
22	246 - 7-211	5.0e+016	0.06	2.4	34.0	4.63	
23	248 - 1-111	5.0e+016	0.06	0.6	25.0	5.92	8.61
24	248 - 1-211	5.0e+016	0.06	0.8	25.0	6.82	9.62
25	248 - 2-111	5.0e+016	0.06	0.7	24.0	6.71	9.42
26	248 - 2-211	5.0e+016	0.06	1.0	24.0	3.93	6.60
27	248 - 4-111	5.0e+016	0.06	0.7	30.0	6.81	9.41
28	248 - 4-211	5.0e+016	0.06	0.9	30.0	7.02	9.94
29	249 - 7-111	5.0e+016	0.06	0.7	20.0	7.07	10.07
30	249 - 7-211	5.0e+016	0.06	0.8	20.0	5.24	8.39
31	249 - 8-111	5.0e+016	0.06	1.0	28.0	6.62	
32	249 - 8-211	5.0e+016	0.06	0.6	28.0	6.59	
33	250 - 2-111	1.0e+018	0.06	0.7	1.0	3.27	
34	250 - 2-211	1.0e+018	0.06	0.7	1.0	3.87	
35	250 - 5-111	1.0e+018	0.06	0.6	1.0	4.83	5.85
36	250 - 5-211	1.0e+018	0.06	0.7	1.0	3.67	5.69
37	250 - 6-111	1.0e+018	0.06	0.7	1.0	4.60	6.66
38	250 - 6-211	1.0e+018	0.06	0.7	1.0	3.19	5.10
39	250 - 9-111	1.0e+018	0.06	0.5	1.0	3.17	
40	250 - 9-211	1.0e+018	0.06	0.4	1.0	1.70	
41	251 - 3-111	5.0e+016	0.06	0.9	15.0	7.06	9.90
42	251 - 3-211	5.0e+016	0.06	0.9	15.0	6.28	9.12
43	251 - 5-111	5.0e+016	0.06	1.2	22.0	4.27	
44	251 - 8-111	5.0e+016	0.06	0.8	21.0	6.48	9.26
45	251 - 8-211	5.0e+016	0.06	0.7	21.0	6.81	9.78
46	252 - 3-111	5.0e+016	0.06	0.8	14.0	6.89	9.56

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Table 2. Conversion efficiencies of recent slotted-substrate SOC cells (concluded).

item	Cell Number	Base Doping (atoms/cc)	Dip Speed (cm/sec)	RA Product (ohms-sqcm)	Base Sheet Resistance (ohms/[J])	Total Area Conversion Efficiencies	
						Before AR (%)	After AR (%)
47	252 - 3-211	5.0e+016	0.06	0.7	14.0	6.61	9.78
48	252 - 4-111	5.0e+016	0.06	0.8	19.0	6.92	9.87
49	252 - 4-211	5.0e+016	0.06	0.9	19.0	7.06	9.96
50	252 - 6-111	5.0e+016	0.06	0.7	21.0	7.11	9.80
51	252 - 6-211	5.0e+016	0.06	0.7	21.0	7.26	10.12
52	252 - 7-111	5.0e+016	0.06	0.6	25.0	7.00	9.96
53	252 - 7-211	5.0e+016	0.06	0.7	25.0	6.59	9.48
54	252 - 9-111	5.0e+016	0.06	0.8	19.0	7.05	9.80
55	252 - 9-211	5.0e+016	0.06	0.9	19.0	7.16	10.22
56	252 -10-111	5.0e+016	0.06	0.7	20.0	6.86	
57	252 -10-211	5.0e+016	0.06	0.8	20.0	6.77	
58	252 -11-211	5.0e+016	0.06	0.8	18.0	6.67	
59	253 - 1-111	5.0e+016	0.06	1.8	15.0	6.82	
60	253 - 3-111	5.0e+016	0.06	0.7	18.0	7.22	10.42
61	253 - 3-211	5.0e+016	0.06	0.7	18.0	7.17	10.38
62	253 - 4-111	5.0e+016	0.06	0.8	22.0	7.19	9.97
63	253 - 4-211	5.0e+016	0.06	1.0	22.0	7.22	9.82
64	253 -10-111	5.0e+016	0.06	0.9	26.0	6.47	
65	253 -10-211	5.0e+016	0.06	1.2	26.0	6.05	
66	254 - 1-111	5.0e+016	0.06	1.4	21.0	6.62	9.15
67	254 - 1-211	5.0e+016	0.06	0.6	21.0	6.92	9.97
68	254 - 6-111	5.0e+016	0.06	0.7	21.0	6.78	10.19
69	254 - 6-211	5.0e+016	0.06	0.7	21.0	6.98	10.11
70	254 - 9-111	5.0e+016	0.06	0.6	26.0	7.08	10.03
71	254 - 9-211	5.0e+016	0.06	0.6	26.0	6.85	9.96
72	255 - 2-111	5.0e+016	0.06	0.6	21.0	6.90	9.58
73	255 - 2-211	5.0e+016	0.06	0.6	21.0	7.09	9.82
74	255 - 5-111	5.0e+016	0.06	0.6	22.0	7.08	9.87
75	255 - 5-211	5.0e+016	0.06	0.7	22.0	7.58	10.21 (10.48)*
76	255 - 6-111	5.0e+016	0.06	0.8	26.0	6.73	
77	255 - 6-211	5.0e+016	0.06	0.8	26.0	6.43	
78	255 - 7-111	5.0e+016	0.06	0.6	27.0	6.97	9.91
79	255 - 7-211	5.0e+016	0.06	0.7	27.0	6.92	10.03
80	470 - 1-111	5.0e+016	0.06	0.7	19.0	7.17	
81	470 - 1-211	5.0e+016	0.06	0.7	19.0	7.04	
82	470 - 2-111	5.0e+016	0.06	0.7	35.0	6.57	
83	470 - 2-211	5.0e+016	0.06	0.7	35.0	6.46	
84	470 - 5-111	5.0e+016	0.06	0.7	29.0	6.39	
85	470 - 5-211	5.0e+016	0.06	0.9	29.0	5.68	
86	470 - 8-111	5.0e+016	0.06	1.1	38.0	5.03	
87	470 - 8-211	5.0e+016	0.06	0.7	38.0	3.34	

*See text and Figs. 7, 8, and 9.

Table 3. Characteristics of recent slotted SOC cells and their corresponding single-crystal control cells.

Item	Cell Number	Total-Area				
		Isc (mA)	Voc (V)	Fill Factor	Jsc (mA/sqcm)	Eff. (%)
1	205 - 3-111-0	85.40	0.526	0.705	17.00	6.33
2	205 - 3-211-0	85.30	0.521	0.739	17.06	6.57
3	206 - 3-111-0	89.70	0.535	0.739	17.94	7.09
3	206 - 3-111-1	127.20	0.552	0.723	25.44	10.15 (AR)
4	206 - 3-211-0	87.40	0.534	0.743	17.48	6.94
4	206 - 3-211-1	130.30	0.553	0.712	26.06	10.26 (AR)
5	212 - 1-111-0	89.20	0.474	0.590	17.84	4.99
6	212 - 1-211-0	84.40	0.463	0.419	16.88	3.28
7	226 - 3-111-0	80.40	0.551	0.728	16.08	6.45
7	226 - 3-111-1	114.80	0.570	0.709	22.96	9.28 (AR)
8	226 - 3-211-0	83.70	0.554	0.747	16.74	6.93
8	226 - 3-211-1	117.30	0.570	0.719	23.46	9.62 (AR)
9	238 - 8-111-0	82.60	0.556	0.757	16.52	6.95
9	238 - 8-111-1	114.10	0.570	0.735	22.82	9.56 (AR)
10	238 - 8-211-0	82.10	0.546	0.664	16.42	5.95
10	238 - 8-211-1	114.20	0.560	0.665	22.84	8.51 (AR)
11	239 - 1-111-0	79.60	0.536	0.675	15.92	5.76
12	239 - 1-211-0	79.00	0.511	0.627	15.80	5.06
13	241 - 4-111-0	78.40	0.554	0.737	15.68	6.40
13	241 - 4-111-1	107.40	0.566	0.721	21.48	8.77 (AR)
14	241 - 4-211-0	77.70	0.536	0.669	15.54	5.57
14	241 - 4-211-1	110.00	0.551	0.674	22.00	8.17 (AR)
15	244 - 3-111-0	81.50	0.552	0.673	16.30	5.73
15	244 - 3-111-1	114.20	0.559	0.658	22.84	8.40 (AR)
16	244 - 3-211-0	82.30	0.563	0.772	16.46	7.15
16	244 - 3-211-1	114.90	0.565	0.751	22.98	9.75 (AR)
17	244 -11-111-0	81.60	0.557	0.663	16.32	6.03
17	244 -11-111-1	110.70	0.568	0.670	22.14	8.43 (AR)
18	244 -11-211-0	83.00	0.562	0.759	16.60	7.08
18	244 -11-211-1	113.60	0.572	0.753	22.72	9.79 (AR)

continued next page

Table 3. Characteristics of recent slotted SOC cells and their corresponding single-crystal control cells (continued).

item	Cell Number	Isc (mA)	Voc (V)	Fill Factor	Total-Area	
					Jsc (mA/sqcm)	Eff. (%)
19	244 -12-111-0	79.60	0.560	0.752	15.92	6.70
19	244 -12-111-1	117.20	0.565	0.711	23.44	9.42 (AR)
20	244 -12-211-0	81.10	0.552	0.638	16.22	5.71
20	244 -12-211-1	117.90	0.560	0.644	23.58	8.50 (AR)
21	246 - 7-111-0	72.10	0.531	0.611	14.42	4.68
22	246 - 7-211-0	66.80	0.536	0.647	13.36	4.63
23	248 - 1-111-0	81.00	0.546	0.669	16.20	5.92
23	248 - 1-111-1	111.20	0.561	0.690	22.24	8.61 (AR)
24	248 - 1-211-0	82.40	0.550	0.753	16.48	6.82
24	248 - 1-211-1	113.90	0.567	0.745	22.78	9.62 (AR)
25	248 - 2-111-0	79.40	0.556	0.760	15.88	6.71
25	248 - 2-111-1	115.50	0.568	0.718	23.10	9.42 (AR)
26	248 - 2-211-0	79.60	0.526	0.469	15.92	3.93
26	248 - 2-211-1	116.50	0.548	0.517	23.30	6.60 (AR)
27	248 - 4-111-0	81.30	0.550	0.761	16.26	6.81
27	248 - 4-111-1	111.50	0.563	0.750	22.30	9.41 (AR)
28	248 - 4-211-0	83.50	0.552	0.761	16.70	7.02
28	248 - 4-211-1	115.80	0.566	0.758	23.16	9.94 (AR)
29	249 - 7-111-0	84.10	0.560	0.753	16.62	7.07
29	249 - 7-111-1	121.10	0.575	0.723	24.22	10.07 (AR)
30	249 - 7-211-0	78.50	0.540	0.618	15.70	5.24
30	249 - 7-211-1	120.00	0.560	0.624	24.00	8.39 (AR)
31	249 - 8-111-0	83.10	0.551	0.723	16.62	6.62
32	249 - 8-211-0	78.40	0.554	0.759	15.68	6.59
33	250 - 2-111-0	69.70	0.451	0.520	13.94	3.27
34	250 - 2-211-0	70.20	0.522	0.528	14.04	3.87
35	250 - 5-111-0	65.00	0.550	0.676	13.00	4.83
35	250 - 5-111-1	93.20	0.570	0.551	18.64	5.85 (AR)
36	250 - 5-211-0	68.80	0.547	0.487	13.76	3.67
36	250 - 5-211-1	99.20	0.572	0.506	19.64	5.69 (AR)
37	250 - 6-111-0	69.00	0.555	0.609	13.60	4.60

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Table 3. Characteristics of recent slotted SOC cells and their corresponding single-crystal control cells (continued).

item	Cell Number	Isc (mA)	Voc (V)	Fill Factor	Total-Area	
					Jsc (mA/sqcm)	Eff. (%)
37	250 - 6-111-1	95.50	0.574	0.607	19.10	6.66 (AR)
38	250 - 6-211-0	65.50	0.458	0.532	13.10	3.19
38	250 - 6-211-1	95.10	0.514	0.522	19.02	5.10 (AR)
39	250 - 9-111-0	65.80	0.523	0.461	13.16	3.17
40	250 - 9-211-0	66.70	0.245	0.521	13.34	1.70
41	251 - 3-111-0	84.40	0.566	0.739	16.88	7.06
41	251 - 3-111-1	120.20	0.575	0.716	24.04	9.90 (AR)
42	251 - 3-211-0	84.80	0.560	0.661	16.96	6.28
42	251 - 3-211-1	121.10	0.570	0.661	24.22	9.12 (AR)
43	251 - 5-111-0	83.50	0.538	0.475	16.70	4.27
44	251 - 8-111-0	80.00	0.564	0.718	16.00	5.48
44	251 - 8-111-1	120.40	0.568	0.677	24.08	9.26 (AR)
45	251 - 8-211-0	81.60	0.563	0.741	16.32	6.81
45	251 - 8-211-1	122.70	0.567	0.703	24.54	9.78 (AR)
46	252 - 3-111-0	80.20	0.566	0.759	16.04	6.89
46	252 - 3-111-1	117.30	0.572	0.713	23.44	9.56 (AR)
47	252 - 3-211-0	80.10	0.562	0.734	16.02	6.61
47	252 - 3-211-1	120.20	0.570	0.714	24.04	9.78 (AR)
48	252 - 4-111-0	82.30	0.569	0.739	16.46	6.92
48	252 - 4-111-1	118.40	0.575	0.725	23.68	9.87 (AR)
49	252 - 4-211-0	82.90	0.565	0.754	16.48	7.06
49	252 - 4-211-1	120.10	0.571	0.726	24.02	9.96 (AR)
50	252 - 6-111-0	83.50	0.569	0.748	16.70	7.11
50	252 - 6-111-1	119.50	0.579	0.708	23.90	9.80 (AR)
51	252 - 6-211-0	83.80	0.567	0.764	16.76	7.26
51	252 - 6-211-1	119.40	0.578	0.733	23.88	10.12 (AR)
52	252 - 7-111-0	80.70	0.566	0.767	16.14	7.30
52	252 - 7-111-1	120.50	0.577	0.716	24.10	9.96 (AR)
53	252 - 7-211-0	80.20	0.558	0.736	16.04	6.59
53	252 - 7-211-1	120.00	0.570	0.693	24.00	9.48 (AR)
54	252 - 9-111-0	82.60	0.570	0.749	16.52	7.05
54	252 - 9-111-1	116.20	0.580	0.727	23.24	9.80 (AR)

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Table 3. Characteristics of recent slotted SOC cells and their corresponding single-crystal control cells (continued).

Item	Cell Number	Isc (mA)	Voc (V)	Fill Factor	Total-Area	
					Jsc (mA/sqcm)	Eff. (%)
55	252 - 9-211-0	83.60	0.570	0.751	16.72	7.16
55	252 - 9-211-1	122.30	0.578	0.723	24.46	10.22 (AR)
56	252 -10-111-0	83.10	0.569	0.725	16.62	6.86
57	252 -10-211-0	81.60	0.566	0.733	16.32	6.77
58	252 -11-211-0	80.00	0.561	0.743	16.00	6.67
59	253 - 1-111-0	82.70	0.565	0.730	16.54	6.82
60	253 - 3-111-0	81.80	0.565	0.754	16.96	7.22
60	253 - 3-111-1	123.60	0.573	0.736	24.72	10.42 (AR)
61	253 - 3-211-0	81.80	0.564	0.750	16.96	7.17
61	253 - 3-211-1	125.10	0.572	0.725	25.02	10.38 (AR)
62	253 - 4-111-0	81.30	0.563	0.757	16.86	7.19
62	253 - 4-111-1	117.10	0.578	0.724	23.82	9.97 (AR)
63	253 - 4-211-0	84.80	0.560	0.760	16.96	7.22
63	253 - 4-211-1	121.10	0.574	0.706	24.22	9.82 (AR)
64	253 -10-111-0	82.40	0.553	0.710	16.48	6.47
65	253 -10-211-0	84.10	0.556	0.647	16.82	6.05
66	254 - 1-111-0	80.30	0.560	0.736	16.06	6.62
66	254 - 1-111-1	113.20	0.569	0.680	23.64	9.15 (AR)
67	254 - 1-211-0	79.00	0.563	0.778	15.80	6.92
67	254 - 1-211-1	117.10	0.570	0.734	23.82	9.97 (AR)
68	254 - 6-111-0	83.40	0.564	0.721	16.68	6.78
68	254 - 6-111-1	119.40	0.572	0.746	23.88	10.19 (AR)
69	254 - 6-211-0	81.40	0.562	0.763	16.28	6.98
69	254 - 6-211-1	117.40	0.567	0.760	23.48	10.11 (AR)
70	254 - 9-111-0	82.70	0.565	0.758	16.54	7.08
70	254 - 9-111-1	117.90	0.580	0.733	23.58	10.03 (AR)
71	254 - 9-211-0	80.90	0.561	0.755	16.18	6.85
71	254 - 9-211-1	119.30	0.575	0.726	23.86	9.96 (AR)
72	255 - 2-111-0	80.20	0.564	0.763	16.04	6.90
72	255 - 2-111-1	112.80	0.573	0.741	22.56	9.58 (AR)

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Table 3. Characteristics of recent slotted SOC cells and their corresponding single-crystal control cells (continued).

item	Cell Number	Isc (mA)	Voc (V)	Fill Factor	Total-Area	
					Jsc (mA/sqcm)	Eff. (%)
73	255 - 2-211-0	82.80	0.565	0.758	16.56	7.09
73	255 - 2-211-1	114.70	0.573	0.747	22.94	9.82 (AR)
74	255 - 5-111-0	82.30	0.569	0.756	16.46	7.08
74	255 - 5-111-1	119.50	0.575	0.718	23.90	9.87 (AR)
75	255 - 5-211-0	86.00	0.571	0.772	17.20	7.58
75	255 - 5-211-1	120.60	0.579	0.731	24.12	10.21 (AR) (10.48)*
76	255 - 6-111-0	80.60	0.567	0.736	16.12	6.73
77	255 - 6-211-0	78.10	0.560	0.735	15.62	6.43
78	255 - 7-111-0	81.70	0.565	0.755	16.34	6.97
78	255 - 7-111-1	116.50	0.571	0.745	23.30	9.91 (AR)
79	255 - 7-211-0	82.10	0.563	0.748	16.42	6.92
79	255 - 7-211-1	116.70	0.573	0.750	23.34	10.03 (AR)
80	470 - 1-111-0	83.40	0.567	0.758	16.68	7.17
81	470 - 1-211-0	82.90	0.566	0.750	16.58	7.04
82	470 - 2-111-0	77.20	0.560	0.760	15.44	6.57
83	470 - 2-211-0	79.80	0.555	0.729	15.96	6.46
84	470 - 5-111-0	81.10	0.547	0.720	16.22	6.39
85	470 - 5-211-0	78.30	0.526	0.689	15.66	5.68
86	470 - 8-111-0	79.70	0.518	0.609	15.94	5.03
87	470 - 8-211-0	80.80	0.491	0.421	16.16	3.34
(Single-Crystal)						
88	R45B- 0-111-0	102.70	0.568	0.755	20.54	8.81
89	R45B- 0-211-0	103.90	0.571	0.755	20.78	8.96
90	R47A- 0-111-0	98.20	0.564	0.757	19.64	8.38
91	R47A- 0-211-0	98.60	0.565	0.745	19.72	8.30
92	R47B- 0-111-0	103.60	0.576	0.764	20.72	9.12

*See text and Figs. 7, 8, and 9.

continued next page

Table 3. Characteristics of recent slotted SOC cells and their corresponding single-crystal control cells (concluded).

Item	Cell Number	Isc (mA)	Voc (V)	Fill Factor	Total-Area	
					Jsc (mA/sqcm)	Eff. (%)
93	R47B- 0-211-0	104.00	0.574	0.756	20.80	9.03
94	R48 - 0-111-0	102.00	0.571	0.756	20.40	8.81
95	R48 - 0-211-0	99.80	0.570	0.762	19.96	8.67
96	R49 - 0-111-0	102.00	0.577	0.763	20.40	8.98
97	R49 - 0-211-0	101.70	0.578	0.760	20.34	8.94
98	R50 - 0-111-0	102.50	0.577	0.754	20.50	8.92
99	R50 - 0-211-0	103.10	0.580	0.765	20.62	9.15
100	R51 - 0-111-0	98.90	0.569	0.733	19.78	8.25
101	R52 - 0-111-0	104.60	0.576	0.752	20.92	9.06
102	R52 - 0-211-0	104.20	0.576	0.744	20.84	8.93
103	R54 - 0-111-0	101.20	0.581	0.762	20.24	8.96
104	R54 - 0-211-0	99.30	0.581	0.757	19.86	8.74
105	R55 - 0-111-0	96.80	0.564	0.748	19.36	8.11
106	R55 - 0-211-0	96.50	0.564	0.755	19.30	8.22
107	R56 - 0-111-0	98.70	0.574	0.741	19.74	8.40
108	R56 - 0-211-0	100.40	0.575	0.745	20.08	8.60
109	R57 - 0-111-0	97.40	0.569	0.642	19.48	7.12
110	R57 - 0-211-0	98.20	0.575	0.728	19.64	8.22

For the just-given averages, five cells were omitted. One cell (no. 248-2-211) was broken and had a cell efficiency of 6.6%. Four other cells were very heavily doped to determine the upper limit for the base doping concentration and all had efficiencies less than 7% with AR coating. Since those low efficiencies are understandable, these results are justifiably omitted from the above averages.

The current-voltage (I-V) characteristics for the 10.48% SOC cell are given in Figs. 7, 8, and 9. The first two figures show four efficiency values measured consecutively. The first efficiency value of 7.58% was measured before the AR coating. The corresponding I-V curve shows that $V_{oc} = 0.58$ V, $FF = 0.77$, and $J_{sc} = 17.2$ mA/cm². These values are all rather high and (with our typical AR coating) an efficiency greater than 10.5% was possible. The second efficiency value of 10.21% was measured after AR coating. The corresponding I-V curve indicated that the AR coating produced undesirable shunting, probably due to some water vapor in the AR coating system. The third efficiency value of 10.26% was measured after baking the AR coating for 10 minutes at 100°C. The shunting was improved but the J_{sc} decreased, indicating that the heat treatment converted some of the SiO to SiO₂. The fourth and final efficiency value of 10.48% was obtained by removing the initial AR coating with 50-50 mixture of HF and DI water and by depositing a second AR coating. For the final AR coating, the shunting was negligible, as shown in Fig. 9. Figure 8 shows that $V_{oc} = 0.57$ V, $J_{sc} = 24.2$ mA/cm², and $FF = 0.76$ for the 10.48% SOC cell.

To improve cell performance, a number of experiments are being investigated and the principal ones are listed in Table 4. Experiments 1 through 5 are completed; experiments 6 through 9 are currently being investigated; and experiments 10 through 12 are being started. Some of the experiments were discussed in Quarterly Report No. 14 (April 1980) and these results will be partially repeated here for completeness. More recent results will be discussed below, with reference to Table 5. Group A of this table corresponds to control SOC cells that were fabricated using our unmodified standard SOC process.

Figure 7. Current-voltage characteristics of SOC cell no. 255-5-211. The lower curve corresponds to measurements before AR coating; the upper two curves, to measurements after AR coating.

Figure 8. Current-voltage characteristics of the same cell as Fig. 7. For this curve the initial AR coating was removed and a new AR coating deposited.

Figure 9. Dark I-V characteristics of SOC cell no. 255-5-211. This characteristic was measured after the second AR coating.

Table 4. Experiments for increasing cell performance.

Experiment	Objective	Results	Status
1) Melt Current	Reduce Impurities	No effect	Completed
2) No Doping	Determine the Rate of Contamination	Graph of ρ vs N	
3) Al Doping	Determine if Al doping improves J_{sc}	Reduces J_{sc}	
4) Heavy Doping	Determine Effect of Heavy Doping	Reduces J_{sc}	
5) Carbon Substrate	Measure Melt Quality	Poor Structure	
6) Ion-implantation	Increase J_{sc}	Preliminary Results	Working on
7) Hydrogenation	Increase J_{sc}	Some Improvements	
8) Two-Step	Increase J_{sc}	Some Improvements	
9) Slow Cool	Increase J_{sc}	Significant Improvements	
10) Etching	Increase J_{sc}	-----	Starting
11) Gas Ambient	Increase J_{sc}	-----	
12) PN Cells	Comparison	-----	

1) Melt-Current Experiment--Eight SOC cells were fabricated to determine the effect of an electric current through the melt during dip-coating. It was hoped that this current might reduce melt contamination by influencing the transport of impurities from the substrate into the melt. Based on the results of the eight cells, an electric current does not seem to have an effect on melt contamination. Group B of Table 5 gives recent results for the melt-current experiment. The main results were given in Quarterly Report No. 14.

2) No-Doping Experiment--Four SOC cells were fabricated to determine the effects of progressive melt contamination on the sheet resistance of the dip-coated SOC material. For the ninth and twelfth substrates dipped in run no. 228, the sheet resistance was 770 and 550 $\Omega/\square$, respectively. Cells fabricated using these SOC substrates had efficiencies in

Table 5. Some results from experiments in Table 4.

CONTROL CELLS:

ITEM	CELL NUMBER	EFFICIENCY	
		BEFORE AR	AFTER AR
9	238 - 8-111	6.95	9.56
10	238 - 8-211	5.95	8.51
11	239 - 1-111	5.76	
12	239 - 1-211	5.06	
13	241 - 4-111	6.40	8.77
14	241 - 4-111	5.57	8.17
15	244 - 3-111	5.73	8.40
16	244 - 3-211	7.15	9.75
17	244 -11-111	6.03	8.43
18	244 -11-211	7.08	9.79
19	244 -12-111	6.70	9.42
20	244 -12-211	5.71	8.50
23	248 - 1-111	5.92	8.61
24	248 - 1-211	6.82	9.62
27	248 - 4-111	6.81	9.41
28	248 - 4-211	7.02	9.94
29	249 - 7-111	7.07	10.07
30	249 - 7-211	5.24	8.39
31	249 - 8-111	6.62	
32	249 - 8-211	6.59	
43	251 - 5-111	(4.27)*	
52	252 - 7-111	7.00	9.96
53	252 - 7-211	6.59	9.48
58	252 -11-211	6.67	

GROUP A

Average $\overline{6.37}$ $\overline{9.15}$
Standard Deviation ± 0.63 ± 0.66

*OMITTED FROM AVERAGE

MELT CURRENT EXPERIMENT:

ITEM	CELL NUMBER	EFFICIENCY	
		BEFORE AR	AFTER AR
7	226 - 3-111	6.45	9.28
8	226 - 3-211	6.93	9.62

GROUP B

Average $\overline{6.69}$ $\overline{9.45}$
Standard Deviation ± 0.34 ± 0.24

Table 5. Some results from experiments in Table 4
(continued).

HEAVY DOPING EXPERIMENT:

ITEM	CELL NUMBER	EFFICIENCY		
		BEFORE AR	AFTER AR	
33	250 - 2-111	(3.27)*		GROUP C
34	250 - 2-211	(3.87)*		
35	250 - 5-111	4.83	5.85	
36	250 - 5-211	3.67	5.69	
37	250 - 6-111	4.60	6.66	
38	250 - 6-211	3.19	5.10	
39	250 - 9-111	(3.17)*		
40	250 - 9-211	(1.70)*		
Average		$\overline{4.07}$	$\overline{5.83}$	
Standard Deviation		± 0.77	± 0.64	

*OMITTED FROM AVERAGE

TWO STEP DIFFUSION:

ITEM	CELL NUMBER	EFFICIENCY		
		BEFORE AR	AFTER AR	
1	205 - 3-111	6.33		GROUP D
2	205 - 3-211	6.57		
3	206 - 3-111	7.09	10.15	
4	206 - 3-211	6.94	10.26	
5	212 - 1-111	(4.99)*		
6	212 - 1-211	(3.28)*		
25	248 - 2-111	6.71	9.42	
26	248 - 2-211	(3.93)*	(6.60)*	
21	246 - 7-111	(4.68)*		GROUP E
22	246 - 7-211	(4.63)*		
72	255 - 2-111	6.90	9.58	GROUP F
73	255 - 2-211	7.09	9.82	
74	255 - 5-111	7.08	9.87	
75	255 - 5-211	7.58	10.21	
76	255 - 6-111	6.73		
77	255 - 6-211	6.43		
78	255 - 7-111	6.97	9.91	
79	255 - 7-211	6.92	10.03	
Average		$\overline{6.87}$	$\overline{9.92}$	
Standard Deviation		± 0.33	± 0.28	

*OMITTED FROM AVERAGE

Table 5. Some results from experiments in Table 4
(concluded).

SLOW COOL EXPERIMENT:

ITEM	CELL NUMBER	EFFICIENCY		
		BEFORE AR	AFTER AR	
44	251 - 8-111	6.48	9.26	GROUP G
45	251 - 8-211	6.81	9.78	
48	252 - 4-111	6.92	9.87	
49	252 - 4-211	7.06	9.96	
50	252 - 6-111	7.11	9.80	
51	252 - 6-211	7.26	10.12	
62	253 - 4-111	7.19	9.97	
63	253 - 4-211	7.22	9.82	
66	254 - 1-111	6.62	9.15	
67	254 - 1-211	6.92	9.97	
68	254 - 6-111	6.78	10.19	
69	254 - 6-211	6.98	10.11	
80	470 - 1-111	7.17		
81	470 - 1-211	7.04		
56	252 -10-111	6.86		GROUP H
57	252 -10-211	6.77		
59	253 - 1-111	6.82		
60	253 - 3-111	7.22	10.42	
61	253 - 3-211	7.17	10.38	
70	254 - 9-111	7.08	10.03	
71	254 - 9-211	6.85	9.96	
41	251 - 3-111	7.06	9.90	GROUP J
42	251 - 3-211	6.28	9.12	
54	252 - 9-111	7.05	9.80	
55	252 - 9-211	7.16	10.22	
64	253 -10-111	6.47		
65	253 -10-211	6.05		
Average		$\overline{6.90}$	$\overline{9.89}$	
Standard Deviation		± 0.30	± 0.36	

ETCHING EXPERIMENT:

46	252 - 3-111	6.89	9.56	GROUP G
47	252 - 3-211	6.61	9.78	
82	470 - 2-111	6.57		
83	470 - 2-211	6.46		
84	470 - 5-111	6.39		
85	470 - 5-211	(5.68)*		
86	470 - 8-111	(5.03)*		
87	470 - 8-211	(3.34)*		
Average		6.58	9.67	
Standard Deviation		± 0.19	± 0.16	

*OMITTED FROM AVERAGE

the range from 4.3 to 6.1% (AM1, no AR). This indicates that the mullite progressively contaminated the melt with a p-type dopant, shown to be aluminum in earlier experiments. Such contamination is a basic problem for the dip-coating technique. A similar problem should not exist for the SCIM-coating technique, since the mullite will not be in direct contact with the silicon melt. The main results of the no-doping experiment were given in Quarterly Report No. 14.

- 3) Aluminum-Doping Experiment--Eleven SOC cells were fabricated to determine if aluminum doping could produce higher values of J_{sc} for a given doping concentration. The highest J_{sc} is 14.68 mA/cm^2 (AM1, no AR) for an aluminum-doping concentration of $2.2 \times 10^{16}/\text{cm}^3$. This value is low compared with an average value of 17 mA/cm^2 for boron-doped samples. Thus, aluminum doping does not produce high values of J_{sc} . The main results of the aluminum-doping experiment were given in Quarterly Report No. 14.
- 4) Heavy-Doping Experiment--Eight solar cells were fabricated using SOC material with a boron doping concentration of $10^{18}/\text{cm}^3$, as compared with the normal concentration of $5 \times 10^{16}/\text{cm}^3$. Our objective was to extend the experimental results given in Fig. 4 of Quarterly Report No. 14 in order to determine the upper limit for the base doping concentration. The fabricated cells were of poor quality and only the J_{sc} results were of value. The most interesting result was that the average J_{sc} was 19 mA/cm^2 as compared with 21 mA/cm^2 value associated with the linear regression line shown in Fig. 4 of the just-noted report. The 19 mA/cm^2 value indicates that Auger recombination begins to limit the performance of SOC cells for base doping concentration greater than $10^{18}/\text{cm}^3$, as expected. Group C of Table 5 gives recent results for the heavy-doping experiment. The main results were given in Quarterly Report No. 14.

- 5) Carbon-Substrate Experiment--Several carbon substrates were dipped first in a run in order to learn more about melt contamination from the ceramic substrate. We planned to make photodiodes on the resulting silicon layers and to compare the performance of these diodes with the performance of corresponding diodes on SOC material. Unfortunately, the grain structure of the silicon layers on the carbon substrates was rather poor and, as a result, we did not complete this experiment.
- 6) Ion-Implant Experiment--Eight SOC cells were fabricated using ion implantation and thermal anneal to form the n^+ emitter region. Arsenic was used as the dopant. For one set of SOC cells, the annealing temperature was 850°C for 60 minutes, which are the same conditions used for our phosphine diffusion. The emitter sheet resistance was $\sim 32 \Omega/\square$ and the efficiency of one ion-implant/anneal cell was 5.6%, as compared with the 6.7% efficiency of a corresponding cell used for a control. More work needs to be done to determine the proper annealing conditions. The main results for the ion-implant experiment were given in Quarterly Report No. 14.
- 7) Hydrogenation Experiment--Results for this experiment are discussed in the material evaluation section of this and other recent reports.
- 8) Two-Step Experiment--Eighteen solar cells (Groups D, E, and F in Table 5) were fabricated to determine the effects of a two-step diffusion process. The best two-step cell had a total-area conversion efficiency of 10.26% (AM1, AR) for a cell area of 5 cm^2 . For Group D, the two-step process was similar to the process described by DiStefano and Cuomo [Applied Phys. Lett. 30, 351 (1977)], as well as by Lindmayer (13th IEEE Photovoltaic Specialists Conference, p. 1096). This two-step diffusion process basically is as follows. First, a low-temperature phosphorus diffusion is used to diffuse phosphorus atoms down grain boundaries using a spin-on diffusion source and diffusion conditions of 600°C

for 60 minutes. Second, the initial diffusion source is then removed and the normal high-temperature phosphorus diffusion is used to form the p-n junction.

For Group E, the initial spin-on source was used for both the low- and high-temperature diffusion. Group F was same as Group E except that the order of the two diffusions was interchanged. The latter process seems to produce the highest efficiencies but more work must be done to determine if this is so.

- 9) Slow-Cooldown Experiment--Twenty-seven SOC cells were fabricated using a slow cooldown after the phosphorus diffusion. Typically, the cooling rate was $\sim 3^{\circ}\text{C}/\text{min}$ from the diffusion temperature of 850°C to 700°C . The slow cooldown seems to produce a significant increase in cell performance, as shown in Table 5. As a result, we have recently fabricated 12 SOC cells with efficiencies greater than 10%. For Group G, the cooling rate was $3^{\circ}\text{C}/\text{min}$ for the first 1.5 hours; then it was $3^{\circ}\text{C}/\text{min}$ until the temperature was less than 700°C . For Group J, the cooling rate was $6^{\circ}\text{C}/\text{min}$ from 850°C to 700°C . Table 5 shows that there is no significant difference between cell fabricated with cooling rates in the range from 1 to $6^{\circ}\text{C}/\text{min}$.
- 10) Etching Experiment--Eight cells were fabricated from SOC material that was etched in KOH before the phosphorus diffusion. For future cells, we will also use CP4 etching as well as plasma etching. The main idea of the etching experiment is to determine if cell performance is limited by impurities that segregate to the silicon surface during growth. The best etched cell has a conversion efficiency 6.9%, without an AR coating. This value is typical of non-etched cells and indicated that no performance improvement was obtained for the preliminary etching experiment.

MATERIAL EVALUATION (J.D. Zook, R. Hegel, C. Wensman,
and S. Kempf)

During the quarter, a number of SOC cells were evaluated by the LBIC (light-beam-induced current) technique. Very encouraging results were obtained on the material that had been treated in a hydrogen plasma at Sandia, as

described in previous reports. The results on one of the diodes are shown in Fig. 10. The photo at the top shows the diode with the grain boundaries approximately vertical and a horizontal LBIC scan line. The lower traces show the spectral response, S_λ , before and after the hydrogen treatment, at three different wavelengths. The 0.54- μm scans are similar to the LBIC scans done at Sandia. A paper showing early LBIC scans and some preliminary results was recently published.⁴

Several conclusions can be drawn from Fig. 10, which are also typical of the results on other diodes. Most of the grain boundaries are passivated to a considerable extent. However, some grain boundaries are not affected by the passivation, namely the boundary at the 1.8-mm mark of the scan. It is also interesting that the spectral response within grains also improved, implying an increase in the bulk-diffusion length. This result is surprising, since the hydrogen was thought to improve only the grain boundaries. It is possible, however, that the temperature annealing itself could have had a beneficial effect on the bulk-diffusion length. The annealing was at 350°C for 64 hours, and this could have affected the boron-oxygen or boron-carbon centers that appear to be limiting diffusion length.

Apart from the hydrogen treatment studies, the purpose of LBIC studies is to determine the effects of processing on diffusion length, L_n , and the relative importance of structure versus chemistry in limiting L_n in SOC material. Recent scans on moderately boron-doped ($\sim 5 \times 10^{16}/\text{cm}^3$) material have shown qualitative differences from lightly boron-doped (2×10^{15} to $10^{16}/\text{cm}^3$) material. The qualitative feature is that there are few "grains" having the maximum L_n , and there are a number of "grains" that have a very low diffusion length, even though no apparent grain boundaries are evident as viewed from the top surface. This raises the question of subsurface structure.

To examine the question of structure, a substrate showing a number of good grains with poor diffusion length was selected and then carefully sectioned so that the final polished cross section cut through the scan line. The result is shown in Fig. 11. The grinding and polishing was done very slowly

⁴C.H. Seagek, D.S. Ginley, and J.D. Zook, "Improvement of Polycrystalline Silicon Solar Cells With Grain-Boundary Hydrogenation Techniques," Appl. Phys. Lett. **36**, 831 (1980).

Figure 10. LBIC results for SOC photodiode no. 210-1 before (curve B) and after (curve A) hydrogen plasma treatment at Sandia.

Figure 11. Correlation of LBIC scan with structure. A solar cell was scanned and then cross-sectioned through the scan line. The LBIC scan (upper trace) is at the same magnification as the cross-section (middle photo) and the front surface view (bottom photo). The letters, such as L1 and LV, correspond to minima in the trace. The numbers correspond to maxima. The distance between the 10.0 and 8.0 markers is 2.0 mm. In the cross-section view, the ceramic is on top and the top surface below it is rougher because of inevitable chipping during polishing.

so as to do the least possible damage to the sample. The surface was etched in Wright's etch to reveal dislocations, twins, stacking faults, and grain boundaries.

It is clear from Fig. 11 that this sample has a considerable amount of substructure. This sample is somewhat thicker than most, having a thickness of 330 to 360 μm . The increased thickness may be correlated with the unusual amount of structure. At any rate, this a good sample in which to examine the relationship between diffusion length and structure. The structure is difficult to see at the low magnification so higher-magnification photos were taken at selected areas. These are shown in Figs. 12 through 15. These figures show that dislocations play an apparent role in determining diffusion length in these samples. Regions that are highly twinned tend to have low dislocation density ($< 5 \times 10^5 \text{ cm}^{-2}$) and good LBIC response. Regions with high dislocation densities ($> 2 \times 10^6 \text{ cm}^{-2}$), especially with stacking faults heavily decorated with dislocations, tend to have poor LBIC response. The effect of dislocations has been observed in other sheet silicon material, but we have not had direct observation of the effects of dislocations in SOC material previously.

In summary, both grain boundaries and dislocations have detrimental effects on solar cell performance of SOC material. The effect of hydrogen treatment is to reduce recombination at grain boundaries and to make the response within grains more uniform. The mechanism may be that hydrogen treatment reduces recombination at grain boundaries. Since the hydrogen treatment also includes a long thermal anneal, it is important to identify the specific benefits of hydrogen.

THERMAL MODELING FOR SCIM II (S. Schuldt)

Thermal stresses have continued to be a problem in the substrate heating and cooling chambers of SCIM II, but a combined experimental and theoretical approach is making good progress toward solving the problem. In order to minimize these stresses in general, an attempt is made to keep both substrate heating and substrate cooling temperature profiles as nearly linear as possible. As predicted in the previous analysis (reported in Quarterly Report No. 13, Feb. 1980, the heating problems are more severe at low substrate speeds, owing to the rapid initial temperature rise as the substrate enters the heating tunnel. This is evidenced by tendencies to warping and cracking at low speeds.

Figure 12. A magnified view of section near minimum L1 in Fig. 11. The region to the right of L1 shows good LBIC response, whereas the region to the left shows poor LBIC response and has a high density of dislocations as seen above. The density of dislocations is low in the twinned region and in the lower part of the untwinned region on the right.

Figure 13. A magnified view of section near maximum 14 in Fig. 11. This is a region of good LBIC response and consists of a heavily twinned region with twin boundaries perpendicular to the surface. The horizontal line at the bottom is a microcrack attributed to sample preparation.

Figure 14. A magnified view of section near maximum 13 in Fig. 11. This region has few dislocations but has a grain boundary parallel to the surface about 200 μm from the surface.

The previous thermal models were modified and extended, as follows, to account for design modifications which seemed appropriate means of coping with the problem:

- The amount of insulation used in the entrance and exit tunnels can be varied. In the previous versions the amounts were fixed. Adjusting insulation may be the quickest and easiest way to set up for different substrate speeds.
- The far ends of the exit tunnel guides have tended to reach excessively high temperatures in both theory and practice. The theoretical model includes an optional heat sink at these ends.
- "Standby" versions of the models have been provided. These represent entrance and exit tunnels with heaters active but no substrate present. The main purpose for these versions is to calibrate the models against temperature measurements, which are normally taken with the tunnels empty.

Only longitudinal temperature profiles are being analyzed, since these are believed to be associated with warping and breakage. Transverse temperature variations also occur and are discussed elsewhere. The main problem caused by transverse variations is coating nonuniformity, and this is being successfully attacked by heater redesign.

The physical relationships upon which the thermal models are based will next be summarized. All temperature profiles are assumed to be one-dimensional; thus, variations in the transverse direction are ignored. Several thermal elements interact with one another (Fig. 16) so that as many as five coupled heat equations must be solved. Basically, the electrical input produces heat in the resistive heaters (h), and this heat spreads along both entrance tunnel guides (c) by thermal conduction. In the steady state, the heated guides release part of this energy by radiation to the entering substrate (s) and the rest is lost by radiation and conduction to the ambient. The model includes a convective heat transfer coefficient, but this has been set equal to zero in the calculations reported here. A significant portion of the heat loss takes place from insulated surfaces due to the limited thicknesses of carbon felt. The substrate (s) acquires heat from the guides so that its temperature increases from approximately ambient at the left to the coating temperature (1420°C).

Figure 15. A magnified view of section near maximum 12 in Fig. 11. This region has a higher density of dislocations and stacking faults that are especially evident from the dislocation clustered at the stacking fault on the left side.

Figure 16. Side view of SCIM II showing hypothetical arrangement of various thermal elements. h = resistive heater; c = carbon (guide); i = insulation; w = heat sink (when present).

In the exit tunnel, the process is essentially reversed. The substrate is progressively cooled by radiation to the exit tunnel guides and by conduction in the downstream direction. Because of the heat-shield effect, the cooling efficiency occurs at the far (right) end because thermal conduction within the guides tends to elevate the temperature at that end. This effect can be greatly relieved by heat-sinking (w).

End effects are found to be significant and are included both at the external ends facing the cool environment, and the internal ends facing the coating chamber. Not only the actual end surfaces are affected but also parts of the internal surfaces close to the ends. The moving substrate is not completely cooled when it emerges from the exit tunnel. It is important that enough cooling has taken place at this point in order to avoid a further precipitous temperature drop outside of the tunnel. In the numerical calculations, a practical approximation is required for the boundary condition at infinity. We use $T = T_0$ (room temperature) at a point some distance (a few cm) beyond the tunnel end. Over this distance the radiation environment is assumed to be at temperature T_0 . It is easily verified that the approximate boundary condition does not affect the numerical solutions for the temperatures within the tunnel. Figure 17 shows calibration of model against the data.

The finite-difference grid for the entrance tunnel represents 1-cm increments in longitudinal position, or 41 points for a 40-cm tunnel. Since there are five coupled layers (two heater-insulation layers, two guides, and one

Figure 17. Calculated exit guide temperatures (curve) together with measured data. No substrate in tunnel.

substrate), there are $5 \times 41 = 205$ model equations which are solved by a direct-inversion method for sparse matrices. The matrix has a bandwidth of 11 and is asymmetric due to the moving substrate. Since the radiation law is nonlinear and thermal conductivities are temperature-dependent, the equations are resolved iteratively with updated coefficients for the nodal equations. Convergence occurs in about 20 iterations.

For the exit tunnel, a finer grid (0.33 cm) is used, but heater-insulation layers are not required.

Entrance Tunnel Results

Calculated temperature profiles are shown in Fig. 18 for two substrate speeds. The solid curve gives the substrate temperature and the dashed curve gives the mean guide temperature. (The two guides may differ up to 20°C from each other at any x position.) The dotted curve represents mean guide temperature under standby conditions--the same electrical input but no substrate. The high-speed substrate profile is nearly linear, indicating optimum design for

Figure 18. Entrance tunnel profiles corresponding to slow and fast operation. Guides are 0.5 inch thick and the channel height is 0.5 inch. Solid profile corresponds to the substrate; dashed, to the guides under operating conditions; and dotted, to guides in standby conditions with same electrical input.

high speed. Electrical input is 135 W/cm of width, of which 92 W/cm heats the substrate, the rest being absorbed by the ambient environment. The standby profile is considerably elevated because the entire 135 watts is wasted to the environment, thus requiring a higher average radiation temperature.

The low-speed profile demonstrates some of the difficulties encountered in trying to optimize the basic tunnel design for a range of substrate speeds. With all the insulation in place, the initial temperature rise in the substrate is extremely rapid. This is moderated by removing all of the insulation, giving the indicated profile, which is still somewhat too steep and has excessive curvature. The curvature is initially convex but becomes concave in the middle due to the large radiation losses from the guides. It becomes convex once again in the heater region at the end. The electrical input, 198 W/cm, is almost totally wasted, with only 12 W/cm required to heat the substrate. As discussed in Quarterly Report No. 13, the theoretical profile for the low-speed case is best improved by increasing the thermal resistance of the guides--for example, reducing their thickness. A compromise solution is being investigated experimentally; carbon has been removed in transverse grooves at the ends of the guides.

Exit Tunnel Results

The substrate temperature distribution in the exit tunnel should satisfy three requirements: (1) a large initial gradient to carry off the latent heat of fusion of the grown silicon layer; (2) a nearly constant gradient where there is no plastic stress relief ($< 200^{\circ}\text{C}$) at the end. These requirements are difficult to satisfy simultaneously in a short tunnel. The location of the insulation is critical; since the cooling curve has the greatest curvature at high temperatures, the insulation should be placed fairly close to the beginning of the tunnel. On the other hand, the first requirement demands a fast initial cooling, and this dictates leaving a finite uninsulated gap at the very beginning. A 1-cm gap was found to be sufficient to retain the full initial cooling rate. The next ~ 18 cm of both guides are insulated for present experimental work, and the same insulation interval (1 to 19 cm) was used in the numerical calculations plotted in Fig. 20. The effects of this insulation are readily observed by comparison with Fig. 19 which represents the uninsulated case.

Figure 19. Exit tunnel profiles for slow and fast operation. No insulation. Carbon guides not heat-sunk. Solid profile corresponds to substrate; dashed profile corresponds to guides under operating conditions; and dotted profile corresponds to guides in standby conditions.

Figure 20. Exit tunnel profiles as in previous figure but with insulation located as indicated (Carbon guides not heat-sunk).

As discussed above, the high exit temperatures are intolerable. A water-cooled heat sink was recently added at each guide end, and according to calculations (Fig. 21), a substantial lowering of the exit temperature was expected. As discussed below, this was indeed the result.

Figure 21. Exit tunnel profiles with carbon guides terminated at heat sink.

CONCLUSIONS AND RECOMMENDATIONS

CONCLUSIONS

- Modifications of SCIM II have reduced substrate buckling and breaking, particularly at low speeds.
- The modifications have also improved coating uniformity in SCIM-coated material.
- The SCIM-II modifications were based on a combined experimental and theoretical approach.
- The slow-cooldown experiments have significantly increased the conversion efficiencies of SOC cells.
- The best SOC cells have a total-area conversion efficiency of 10.5% (AM1, AR), for a cell area of 5 cm².

RECOMMENDATIONS

- A slow cooldown should be used for the fabrication of all future SOC cells.

PROJECTION OF FUTURE ACTIVITIES

With regard to future SOC activities, we plan:

- To improve our shut-down procedure for SCIM II to prevent breakage of the crucible holder and crucible heater.
- To implement the cold-substrate mode in SCIM II using a hot shoe on the silicon side and a cold shoe on the substrate side.
- To resume experiments of fast growth in the experimental dip coater.
- To optimize the diffusion parameters using a slow cooldown after the phosphorus diffusion.
- To continue the etching experiments to determine if cell performance is limited by impurities that segregate to the silicon surface during growth.
- To continue investigations of subsurface structure to examine the relationship between structure and diffusion length.

PROGRAM STATUS UPDATE

Updated versions of the Program Plan, Program Labor Summary, and Program Cost Summary are presented in Figs. 22, 23 and 24, respectively.

Figure 22. Updated program plan (sheet 1 of 2).

Figure 22. Updated program plan
(sheet 2 of 2).

Figure 23. Updated program labor summary.

Figure 24. Updated program cost summary.