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DEVELOPMENT OF POLYCRYSTAL GaAs SOLAR CELLS

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ABSTRACT

This is the first quarterly report of a research program, "Development of High Efficiency Polycrystal GaAs Solar Cells." This program is being carried out jointly by Rockwell International, Cornell University, Howard University and North Carolina A & T State University. The objective of this program is to develop a thin film GaAs solar cell technology with the potential of yielding cells with 12-15% efficiency and to develop thin film growth techniques which are compatible with the low cost production goal of \$500/KW-peak.

During the first quarter, we have completed our study of junction formation in large grain polycrystal GaAs; begun characterization of the electronic properties of polycrystal GaAs grown by MBE on low cost foreign substrates; worked on optimizing the structure of AlGaAs-GaAs heterojunction Schottky barrier solar cells; and carried out a variety of grain boundary measurements, including Scanning Light Microscopy (SLM), Deep Level Transient Spectroscopy (DLTS), SIMS and temperature dependent resistivity.

1.0 INTRODUCTION

Progress in the development of high efficiency single crystal GaAs solar cells has been phenomenal over the past three years. Over this period, GaAs cell efficiencies have gone from 16% up to nearly 25%, the highest value for any solar cell, and approaching the theoretical limit for a single cell structure. Numerous systems studies of various solar cell options suggest that the lowest, long term solar electric generating costs will be achieved by very low cost, polycrystal or amorphous thin film devices. The major difference between single and polycrystal materials is the occurrence of grain boundaries in the polycrystal material. The successful reduction of the adverse effects of grain boundaries could lead to polycrystal solar cells with efficiencies of more than 15%. The realization of 10% conversion efficiency in a thin film polycrystal structure is the goal of this program.

During the past quarter we have begun to correlate the electronic properties with the growth conditions of polycrystal GaAs grown by MBE on low cost substrates including graphite, W and Mo. We have completed our series of measurements of the forward I-V characteristics of Al Schottky barriers grown on large grain polycrystal GaAs and have made important strides in optimizing the performance of AlGaAs-GaAs heterostructure Schottky barrier solar cells. Preliminary measurements on MOS solar cells fabricated with a "spin-on" oxide have been encouraging in terms of performance and stability.

2.0 MATERIALS DEVELOPMENT

Materials growth at the participating institutions has been aimed at two goals. The first is to provide a continuing supply of material for ongoing characterization projects; the second is to grow relatively large grained polycrystal GaAs on foreign substrates.

2.1 MBE Growths (Rockwell)

During the first quarter, MBE has been used to make GaAs layers for several applications in this program. GaAs epilayers have been grown on n^+ single- and polycrystal substrates used for solar cell fabrication at the Science Center and Howard University. A number of layers have been grown consisting of GaAs with a thin (20Å-300Å) $Al_{0.3}Ga_{0.7}As$ layer, for investigation of the suitability of this modified Schottky barrier structure for polycrystal solar cells. Results of measurements on these structures are reported in Section 3.1.

Layers have been grown by MBE on Union Carbide Highly Ordered Pyrolytic Graphite (HOPG), commercial pyrolytic graphite and on polycrystal Fe, Mo and W. Growths on all forms of graphite (Carbone Lorraine 5890/PT graphite, commercial pyrolytic graphite, and HOPG) are essentially identical, leading to grain structure at the surface of the layer approximately equal in size to the layer thickness, with a strong (111) preferred orientation. Growths on Carbone Lorraine graphite contain a number of holes, due to large pits and voids in the graphite surface which cannot be removed by polishing

(see previous reports). Growths on the pyrolytic graphites have fewer holes, especially on HOPG, but exhibit a network of cracks due to the thermal expansion mismatch between the GaAs and graphite, as seen in Fig. 1.

Growths on W sheets appear very similar in grain size and orientation to growths on graphite. The W was rolled, commercial foil, degreased, electropolished, rinsed, then argon ion bombarded in the MBE chamber prior to growth of the GaAs. Apparently the GaAs grows without significant reaction with the W, similar to growth on graphite. Growth on Mo shows smaller grains than on W or graphite, with a more random grain orientation. This suggests that the GaAs reacts with Mo during the initial stages of growth.

Electrical measurements have been made on metal diodes deposited on these GaAs layers. This data is reported in Section 2.2.

Ga very heavily doped with Sn was also grown on graphite and sent to Cornell U. for SIMS imaging of Sn at grain boundaries. The sensitivity to Sn was not sufficient to accomplish this, as is reported in Section 2.3.

Discussions at the SERI Polycrystalline GaAs Solar Cell Contractor's meeting, 28-29 March, prompted us to renew investigations of nucleation of GaAs on graphite by MBE, at very small thicknesses. The motivation is to understand the mechanism by which grain growth occurs, and hopefully to gain insight into processes by which grain size might be improved. Initial studies were done of GaAs deposited onto carbon-coated mica. The carbon was deposited by vacuum deposition, using a standard carbon coater normally used for TEM work. The idea was to float the GaAs plus carbon off the mica onto an

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Fig. 1 Growth of GaAs by MBE on highly ordered pyrolytic graphite (HOPG).

electron microscope grid and study nuclei orientation, crystallinity, and coalescence at very small thicknesses using a transmission electron microscope. The first step was to determine whether GaAs deposited on carbon-coated mica behaved at large thicknesses ($\sim 2 \mu\text{m}$) similarly to GaAs grown on graphite, so that nucleation information would be relevant to the case of GaAs on graphite. It was found that growth on carbon-coated mica was very different from growth on graphite. The layers were smooth and featureless (either nearly single crystal or extremely small crystallites) and cracked badly and peeled off the mica substrate at about 1000Å thickness. Self-supporting carbon layers predeposited on TEM grids will be used for future experiments.

2.2 CCLPE Growth (N.C.A. & T.)

It has been found necessary to design, machine, and vacuum bake a new graphite and boron nitride boat/slider structure for the CCLPE system. The electrical contact configuration has been modified to reduce the Joule heating which occurred in the previous design. Also, the boat assembly was modified in order to permit sequential growths by CCLPE and normal LPE during the same process cycle.

During the inoperative period of the CCLPE system, considerable time was devoted to developing methods for polishing graphite and molybdenum for use as substrates. As might be expected, the grainy nature of the graphite substrate material (Carbone Lorraine, or POCO DFP) limits the ultimate surface finish.

The following procedure was found to yield the best observed surface morphology:

- a) Lap both sides of graphite substrate to within 5 mils of desired thickness using a $3\mu\text{m}$ alumina/water slurry on a glass plate.
- b) Ultrasonically clean graphite in DI- H_2O to remove abrasive and graphite particles from the surfaces.
- c) Wax three substrates to a stainless steel lapping disk.
- d) Mix a solution of $0.3\mu\text{m}$ alumina powder, 200 ml DI- H_2O , 15 ml Breck shampoo, and 30 ml household Clorox; pour into lapping tray with glass lap.
- e) Place tray and disk on Mazur lapping/polishing machine. At a medium speed the process removes about 0.5 mils/hour. After desired thickness is achieved, the dull graphite surface is wiped with a soft tissue and cleaned ultrasonically.

A photomicrograph of the results of the above polishing process on a Carbone Lorraine substrate is shown in Fig. 2.

100 μm

Fig. 2. Photomicrograph of polished graphite surface.

No success has been achieved in attempts to chemically polish molybdenum substrates. The $\text{NH}_4\text{OH}-\text{H}_2\text{O}_2-\text{H}_2\text{O}$ etch described by K. Pander, et al,⁽¹⁾ does not result in a smooth surface suitable for CCLPE.

Growth of GaAs on graphite substrates was attempted at 750°C and 700°C by using either CCLPE or LPE or a combination of the two. All attempts were unsuccessful. Growth was also attempted on Ge coated graphite substrates [1000Å and 700Å of Ge evaporated on graphite (5890/PT) substrates using the E-Beam evaporator]. These growths were also successful resulting in dissolution of Ge in the Ga melt during the growth run.

In conclusion, all attempts to grow GaAs on graphite and Ge coated graphite substrates were unsuccessful. It therefore seems unlikely that LPE and/or CCLPE can be used for growing GaAs on graphite substrates.

After all possibilities of growing GaAs on graphite were exhausted, our attention was focused on growing GaAs on molybdenum substrates. Growth took place by passing 20 A/cm² across the substrate melt interface for a period of 30 minutes. While passing current the melt was step cooled by approximately 10°C in order to speed up the growth rate and reduce melt back of the Mo substrate.

The scanning electron microscope (SEM) was used to study the surface morphology of the layers grown by CCLPE on molybdenum substrates. The layers appeared fairly uniform and the grain size varied from 3µm to 40µm. Two samples were mailed to Rockwell Science Center for X-ray microprobe analysis in order to determine whether the grown layer is GaAs or recrystallized Mo.

2.3 SIMS Characterization (Cornell)

The emphasis of the SIMS solar cell program has been the characterization of GaAs samples for several parts of the project. Two samples from NCA&T were studied to determine the nature of unusual features which occurred during preparation. Imaging of segregation to grain boundaries still remains to be realized. Impurities were determined and depth profiles taken for a Cornell GaAs sample and a Rockwell GaAs on graphite sample.

One NCA&T GaAs sample showed black and shiny areas after an HCl etch. Both areas were mass scanned for positive and negative secondary ions. The results for both areas were the same. Optical microscopy revealed a difference in roughness between the areas. This is the most likely cause of the observed reflectivities.

The second NCA&T sample contained a grain boundary for imaging. No segregation was seen for elements which had high enough signals to image (Na, Al). As with the first sample, major impurities included the alkali metals, Al and Cl. Optical microscopy showed the grain boundary to be like a crack in the epilayer. Several other cracks were also observed in this sample.

A profile was taken of Rockwell sample MBA 242 (Fig. 3). The grain size was quite small and the surface was too rough for good depth resolution. Sn could not be seen in the sample, and the small grain size ($\sim 5 \mu\text{m}$), approximately the image resolution of the SIMS instrument, made Sn imaging impossible. Mass scans showed an extremely high level of impurities in the sample including the alkali metals, Ca, Al and many possible hydrocarbon ions.

Fig. 3. SIMS profile of polycrystal Sn-doped GaAs grown by MBE on graphite

A GaAs sample was prepared by Ken Wagner at Cornell in an attempt to profile (profiling has a much better spatial resolution compared to imaging) through the grain boundary. The sample was cut from a larger sample of GaAs, to make a grain boundary with an $\sim 5^\circ$ angle to the surface.

Mass scans showed Cr, Cu and In impurities. The Cr and Cu signals were too low to image and the In proved to be homogeneous. A profile from the top, through the grain boundary would have only given a depth resolution of $10\text{ }\mu\text{m}$ due to the 5° angle of the boundary. An In profile in this direction showed no anomalies.

Work on solving the high oxygen background of the instrument is still in progress. A cold finger for the sample chamber has been designed and is currently being machined. A system for a hydrogen leak onto the sample is now ready to operate and will be tested within the next month. It is hoped that the hydrogen will compete with oxygen for surface sites and thereby reduce the oxygen background.

3.0 INVESTIGATIONS OF GRAIN BOUNDARIES

Investigations of grain boundaries are in progress at Rockwell, Cornell and N.C.A.&T. Efforts include measurements to determine transport parameters in the vicinity of a grain boundary; junction formation in polycrystalline material, and attempts to identify and modify the chemical properties of grain boundaries.

3.1 Junction Formation in Polycrystal GaAs (Rockwell)

During the first quarter we have completed the series of measurements characterizing the forward bias I-V characteristics of in-situ Schottky barriers formed on n-GaAs (Sn-doped) grown by MBE on n^+ -polycrystal GaAs substrates. We have found that some (but not all) of the diodes grown on top of grain boundaries contain a leakage component in the forward current; that the magnitude of this current increases and its temperature dependence decreases with increasing doping concentration.

The samples measured were all grown in Rockwell's MBE apparatus which operates at a background pressure in the mid 10^{-10} torr range. The substrates used were n^+ -polycrystal GaAs ($N_D - N_A \cong 10^{18} \text{ cm}^{-3}$) with a visible grain size ranging from $\sim 10^2 \mu\text{m}$ to several mm. The substrate temperature was held at $580^\circ \pm 20^\circ\text{C}$ and a 2-3 μm MBE layer was grown at a rate of 1 $\mu\text{m}/\text{hour}$. The morphology of the MBE layer mirrored that of the substrate. Upon completion of the growth, the substrate heater was turned off and when the sample temperature fell below 50°C , a 2000A thick aluminum layer was grown on the

surface. The sample was removed from the MBE chamber and the indium which had been used to mount the n^+ -substrate to the holder was used as an ohmic contact. 10 mil Schottky diodes were isolated photolithographically in the aluminum and the sample and a thin film platinum resistance thermometer were mounted on a square of molybdenum. A photograph of the surface of a typical sample is shown in Fig. 4 and a schematic of an edge view is shown in Fig. 5.

The initial characterization we performed consisted of measurements of the current as a function of both forward bias and temperature. The cryostat used was basically a copper pedestal mounted in an aluminum and styrofoam can which was cooled with cold nitrogen gas. The diodes were contacted by a thin tungsten probe. We carried out measurements over a range of temperatures between 120K and room temperature with a temperature stability of $\pm 1K$.

The diodes characterized fell into three categories: (i) those which were located entirely within a single grain, (ii) those which straddled a grain boundary but whose electrical characteristics were indistinguishable from the single crystal diodes, and (iii) those which straddled a grain boundary and whose forward I-V characteristics contained a leakage component. Although the statistics are not extensive enough to be conclusive, it appears that the majority of grain boundaries do not contribute to the decrease in open circuit voltage observed in polycrystal solar cells as compared to single crystal cells. This observation raises hopes that those grain boundaries which do exhibit significant leakage current may be "modified" to minimize their detrimental effect on solar cell performance.

79-3878

MBA 175

MBA 164

Fig. 4 In-situ Schottky barrier arrays on polycrystal samples with dopings of 3×10^{16} (MBA 164) and 8×10^{16} (MBA 175).

Fig. 5. Schematic of sample used in Schottky barrier study.

Figure 6 shows the I-V characteristic of two diodes from a sample whose doping was $N_D - N_A = 3 \times 10^{16} \text{ cm}^{-3}$. The data from both diodes can be fit to the formula

$$I = I_{01} [\exp^{(eV/n_1 kT)} - 1] + I_{02} [\exp^{(eV/n_2 kT)} - 1]$$

As can be seen, the diode located within a single grain exhibits ideal, one component behavior ($n_1 = 1.04$; $I_{02} = 0$) while the diode straddling the grain boundary contains an extra leakage current with $n_2 = 2.0$. The data (i.e., $n_2 = 2$) are suggestive that at this doping the leakage current is dominated by generation-recombination processes in the space charge region. The observation was also made that those diodes which exhibited leakage currents did so with $n_2 \approx 2$ and I_{02} which scaled with the length of the grain boundary which intercepted the 10 mil dot.

Figure 7 shows the I-V characteristics of "leaky" diodes from samples with dopings of 3×10^{16} , 8×10^{16} , and $4 \times 10^{17} \text{ cm}^{-3}$ superimposed on ideal behavior. Again, these curves are characteristic of virtually all of the data at their respective doping levels. As the doping is increased, the magnitude of the leakage (I_{02}) increases while the voltage and temperature dependence decreases (i.e., n_2 increases).

The decrease in voltage and temperature dependence is suggestive of an increasing dominance of tunneling as the leakage mechanism as the doping is

Fig. 6. I-V characteristics of single crystal and grain boundary diodes on samples with $N_D - N_A = 3 \times 10^{16} \text{ cm}^{-3}$

Fig. 7. Forward I-V characteristics of grain boundary diodes as function of doping density.

increased. This behavior can be correlated with the observation made by us, and others, of band bending at grain boundaries.

For a number of possible reasons, the plane of a grain boundary is expected to be highly conducting. The possible reasons include (i) metallic delocalization of the 2-D density of states at the interface; (ii) a continuum of defects states in the gap, and (iii) a bandgap shrinkage due to bond dilation at the interface. The band bending at the grain boundary apparently prevents the grain boundary from being a complete short by reflecting the majority carriers away from the high conductivity region. Under bias, however, the carriers can reach the grain boundary where they are shunted to the metal counterelectrode. As the depletion width "protecting" the grain boundary decreases with increasing doping, the possibility of tunneling to the grain boundary improves, increasing the leakage current.

Upon completion of the measurements, the samples, together with a copy of our cryostat, were forwarded to Cornell for DLTS analysis. In the coming quarter, we plan to check the dopant dependence of the above results, to correlate our results with any DLTS results and to begin analysis of "modified" material.

3.2 I-V Measurements on GaAs Grown on W, Mo, and Graphite Substrates (Rockwell)

Current-voltage characteristics of metal-GaAs structures have been measured for GaAs grown by MBE on several different types of substrates. These substrates were Union Carbide Highly Ordered Pyrolytic Graphite (HOPG),

and sheet Mo and W. The HOPG was prepared by heating in vacuum; the Mo and W sheets were electropolished and rinsed, then vacuum degreased. This was followed by argon ion bombardment. The growth morphology and grain size of GaAs grown on W was very similar to growths on HOPG or other types of graphite, except no cracking of the GaAs was observed with W substrates. Growths on Mo substrate had smaller grain sizes and did not appear to be as highly ordered (111) as on graphite.

Au dot contacts (0.010 in. diam.) were evaporated through a shadow mask directly onto the as-grown surface of the GaAs layers. The substrate was used as the back contact. Current-voltage characteristics were qualitatively similar for all the substrates reported here, with $I \propto V^n$, $1.6 \leq n \leq 3.1$ over a limited range of bias. This behavior is due to the small grained GaAs itself, rather than barriers at the Au contacts or at the substrate-GaAs interface, and is similar to the behavior observed in small-grained CdS-CuS₂ cells. The bias-dependent resistivity of the material is largest in lightly doped smaller-grained material (no substrates), and decreases dramatically with more heavily doped, larger grained material (WOG substrates). Current at low voltages (< 0.5 V), i.e., "leakage," also increases rapidly as the doping of the layer increases.

Figure 8 shows the behavior of these diodes, with the I-V characteristic of a single crystal Al Schottky barrier diode plotted for comparison. Notice that for small bias (≤ 0.4 V), the lightly doped material shows currents in excess of the ideal characteristic by about $1 \mu\text{A}$. This is about the magnitude of excess current observed for this size contact in the

Fig. 8. I-V characteristics of polycrystal GaAs grown by MBE on various foreign substrates.

"leakiest" of the in-situ Al Schottky diodes fabricated on heavily doped large grain polycrystal GaAs. Since the leakage component in those diodes decreased relatively less rapidly with bias than the "ideal" forward bias Schottky diode current, it is possible that the amount of leakage seen here in the low doping density layers (labeled 200, 237, 240, in Fig. 9) would not lower the V_{OC} of a solar cell excessively. For the heavily doped layer (labeled 215 in Fig. 9), the leakage greatly exceeds a reasonable I_{SC} ($30 \mu A$ for this size device) even at 0.1 V forward bias, and such solar cells would exhibit extremely low V_{OC} 's.

Whereas "leakage" in these diodes does not necessarily predicate disaster in solar cells made from this material, the bias-dependent resistance of the layer does. Cells made from this material would probably have very poor fill factors, and also probably poor I_{SC} due to grain boundaries running parallel to the GaAs surface. Some encouragement is found, however, in preliminary measurements on layers doped heavily for the first micron of GaAs growth, followed by about a micron of undoped GaAs. These combine relatively low leakage with less layer resistance at a given bias. Further measurements will be made on samples of this type in the future.

3.3 SLM Characterization of Polycrystal GaAs (Cornell)

The SLM investigations have centered around three areas: 1) The understanding in detail of the electronic structure of grain boundaries in GaAs; 2) The use of internal photoemission to probe local variations of barrier height across the surface of a solar cell or Schottky barrier; and 3) The development of a method for measuring local variations of minority carrier diffusion lengths beneath a semitransparent Schottky barrier.

Our study of internal fields associated with grain boundaries has to date been confined to bulk polycrystalline specimens because these behave in a manner amenable to interpretation. These investigations will aid us in understanding the more complex behavior of epitaxial layers associated with realistic solar cell structures. Since the last quarter, new specimens have been fabricated and one was sent to the Science Center for EBIC measurements. Current-voltage measurements as a function of temperature have revealed that the grain boundary barrier height is quite large (~ 800 mV). Our previous measurements of an apparent barrier height of only ~ 30 mV made by scanned photocurrent under bias can be understood when one takes into account the fields associated with the normally depleted surface. These fields sweep holes to the surface and electrons into the bulk. Since only lateral fields are measured in the experiment, the holes (at the surface) are presented with a very small (negative) barrier at the grain boundary, while electrons (in the bulk) are presented with the full barrier. The lateral fields at the surface (experienced only by holes) are those measured in the experiment.

The equipment to measure internal photoemission on Science Center Schottky dot specimens has been assembled and a specimen holder allowing back-surface illumination has been constructed. Measurements have been held up by the failure of our Nd:YAG laser, which is now being repaired. Work for the next quarter will emphasize these scanned internal photoemission measurements.

We are progressing steadily in our effort to implement a reverse-biased Schottky barrier method for measuring lateral variations in minority carrier diffusion lengths. Work this quarter has focused on obtaining good

ideal Schottky barrier behavior with thin (semitransparent) metallizations. To date good success has been achieved with chromium barriers. This work will continue next quarter with increased emphasis as our Krypton ion laser and electron-beam evaporator come back on line.

Measurements on a number of N.C.A.&T. State University specimens have been made this quarter. We have found that we are unable to detect lateral fields in polycrystalline epilayers grown on n^+ substrates by SLM, presumably because the photocurrent is shunted by the conducting substrate. Future SLM studies of these specimens will have to make use of the perpendicular rather than lateral internal fields.

3.4 Grain Boundary Neutralization (N.C.A.&T.)

An apparatus has been set to study the intentional diffusion of impurities in grain boundaries. The equipment includes a bag connected to a diffusion pump and nitrogen gas tank. Quartz tubes are used for the evacuated ampules which contain the GaAs sample coated with a thin layer of sodium in a graphite boat. The diffusion process will be carried out after characterization measurements have been completed. Since the grain boundary diffusion coefficient is expected to be much greater than for the bulk, bulk diffusion will be minimized by carrying out the experiments at low $T(\approx 150^\circ\text{C})$. A control sample, cut from the same wafer, will be used to observe any changes in grain boundary characteristics due to bulk diffusion.

3.5 DLTS Measurements (Cornell)

During this quarter, work has concentrated on setting up a cryostat for use with the DLTS apparatus. Our goal is to be able to probe Science Center MBE "in situ" Schottky dots on grain boundary epilayers without having to cut or bond the specimens. With this equipment, it should be possible to correlate DLTS measurements with I-V and C-V measurements done at the Science Center.

4.0 POLYCRYSTAL SOLAR CELL DEVELOPMENT

Our goal in this task is to develop solar cell structures which can be used with polycrystal materials. In the following sections, we describe our progress in developing metal-oxide-GaAs and metal-AlGaAs-GaAs structures and theoretical models of solar cell performance.

4.1 Barrier Height Enhancement in Heterojunction Schottky Barrier Solar Cells (Rockwell)

Schottky barriers are a more attractive alternative than p-n junctions for low cost polycrystalline solar cells, not only because of their simplicity but also because the p-n junction devices are not compatible with polycrystalline semiconductors due to high reverse saturation currents. The principal disadvantage of Schottky barrier solar cells are their smaller barrier height resulting in a lower open circuit voltage and reduced power conversion efficiency. Prior efforts at barrier height enhancement have concentrated on the use of a thin native or deposited oxide layer between the metal and semiconductor.⁽²⁾ One of the main problems with the MOS structure is the instability of the oxide layer which causes the degradation of solar cell performance.

An alternate approach is to replace the thin oxide with a thin layer of a wide bandgap semiconductor. The wide bandgap layer provides a higher barrier height which increases open circuit voltage. In this quarter we report the barrier height enhancement using an AlGaAs/GaAs heterojunction

Schottky barrier structure. The physical structure of the solar cell is shown in Fig. 9. It is believed that the thin AlGaAs layer may be more stable than the thin oxide which may degrade the solar cell performance under relatively high temperature for a relatively long period of time. Due to the properties of $n\text{Al}_x\text{Ga}_{1-x}\text{As}/n\text{GaAs}$ heterojunctions, a barrier to holes appears in the valence band at the junction when the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer thickness is near to or greater than the Schottky barrier depletion width. The band diagram is shown in Fig. 10. The presence of this barrier degrades the collection efficiency for the photo-generated electron-hole pairs in the GaAs layer. The barrier, when under short circuit condition, will reduce the short circuit current density. This hole barrier height will become even higher under forward bias. A solar cell with a hole barrier will decrease the current much faster than that without a barrier during the forward bias increasing, resulting in a poorer fill factor. Since it is very important to maintain the short circuit current density as well as the fill factor, during the enhancement of the open circuit voltage, the hole barrier should be removed.

A theoretical study of this heterojunction Schottky structure has been done by Y. D. Shen in his Ph.D dissertation.⁽³⁾ His analysis indicated that the hole barrier height was essentially controlled by three factors: (I) the thickness of AlGaAs layer: The thicker the AlGaAs layer the higher the hole barrier. When the AlGaAs thickness is much less than the depletion width, the barrier in the valence band is only a few tenths of kT which is essentially flat for holes at room temperature. (II) The $\text{Al}_x\text{Ga}_{1-x}\text{As}$ composition: The higher x the higher the band gap of AlGaAs, thus increasing

Fig. 9. Schematic of AlGaAs-GaAs heterojunction Schottky barrier solar cell

Fig. 10. Schematic of band structure of AlGaAs-GaAs heterojunction Schottky barrier solar cell

the hole barrier. (III) The carrier concentration in the GaAs layer. For a fixed AlGaAs carrier concentration, the lower the carrier concentration in the GaAs layer the higher the hole barrier height. The increment of the hole barrier height is larger under increasing forward bias for lower carrier concentration in the GaAs layer.

On the basis of the above theoretical analysis, a series of experiments have been performed at Rockwell on single crystalline substrates. The purpose of these experiments was to try to optimize the characteristics of this heterojunction Schottky barrier structure and to apply this structure and technique to the fabrication of polycrystal solar cells.

In the first series of experiments, the short circuit current density and fill factor variation against the carrier concentration variation in GaAs layer for constant AlGaAs composition and thickness were investigated. Most of the cells were fabricated by liquid phase epitaxy. The thickness of the AlGaAs layer was about 200-300Å, and the Al composition was 30%. The carrier concentration N_d in the GaAs layer ranged from $7 \times 10^{17} \text{ cm}^{-3}$ to $3 \times 10^{16} \text{ cm}^{-3}$. Molecular beam epitaxy has been used to achieve even lower doping levels in the GaAs layer.

Fabrication of this cell is similar to that of MOS-type GaAs solar cells, except for the interfacial layer. Instead of growing a thin oxide layer, a thin AlGaAs layer was grown on the GaAs epilayer which was grown on an n^+ GaAs substrate ($N_d \approx 10^{18} + 10^{19} \text{ cm}^{-3}$). The back ohmic contact is evaporated Ge-doped gold sintered in H_2 at 480°C for 2 min. The

semitransparent gold film which forms the Schottky barrier is evaporated to a thickness of $\sim 70\text{\AA}$. A thicker gold collecting grid contact is evaporated on the top layer.

The differential capacitance method was used to determine the carrier concentration (N_d) in the GaAs layer at room temperature. The thickness and composition of the AlGaAs layer was determined with a sputtered Auger depth profile. Photoluminescence was used on thicker layers. Illuminated I-V characteristics of solar cells were measured using an ELH lamp solar simulator with 100 MW/cm^2 input power. Results of the measurements are shown in Table I.

The short circuit current density increases as N_d in the GaAs layer decreases. The fill factor essentially shows no degradation when the N_d is not less than $3 \times 10^{16}\text{ cm}^{-3}$. This fact means that the hole barrier was still not high enough to block the minority carrier collection within the above range of N_d in the GaAs layer. In the theoretical analysis, it was predicted that the N_d in the GaAs layer should be as high as 1×10^{18} to prevent the fill factor degradation, but the experiment result showed that the N_d requirement is much lower. The discrepancy between theoretical and experimental results is presumably due to the difference between the assumed N_d in AlGaAs as well as the transition region and the actual value. It was assumed in the theoretical analysis that the mobility and diffusion length are independent of N_d but in actual cases, lower N_d should result in higher mobility and diffusion length. From the experimental results, the lower N_d limit should be preferred for enhanced carrier collection. Since the mobility and junction

Table I

No.	Growth	AlGaAs Thickness	Al %	GaAs N_d	V_{oc}	J_{sc}	FF
1	LPE	(200-300Å)	(30)	7×10^{17}	605	13.5	0.76
2	LPE	(200-300Å)	(30)	3.5×10^{17}	675	14.3	0.59
3	LPE	(200-300Å)	(30)	1×10^{17}	617	14.6	0.76
4	LPE	(200-300Å)	(30)	5.3×10^{16}	640	15.2	0.79
5	LPE	(200-300Å)	(30)	3×10^{16}	660	15.9	0.80
6	MBE	(200Å)	(35)	8×10^{14}	640	14.4	0.42

abruptness of MBE layers are different from those of LPE layers, it is not appropriate to compare the current between cells made with these two different techniques. In Fig. 11 the illuminated curve had almost identical shape as its dark curve. But in Fig. 12, the illuminated I-V curve showed a strain as the forward bias increased. This was because the hole barrier height increment was too high under forward bias and increased when N_d in the GaAs layer was too low.

The scatter in the open circuit voltage from cell to cell was presumably due to both the variation of the Al% and the surface condition of the AlGaAs layer, both of which were hard to control. Overall, the open circuit voltage of those cells was higher than that of pure GaAs Schottky barrier cells which usually have an open circuit voltage of less than 500 MV.

Short circuit current density increases with increasing N_d in the GaAs layer without degrading the fill factor as long as the N_d was kept above $3 \times 10^{16} \text{ cm}^{-3}$. This value is much lower than the theoretical predicted value for which may have a shorter diffusion length in the GaAs layer. As the N_d in the GaAs layer became much lower, the hole barrier increment was fast enough to strain the illuminated I-V curve, hence degrade the fill factor of the cell performance. Even before optimization, the open circuit voltage was already enhanced by putting a thin layer of AlGaAs on top.

The preliminary results, are very encouraging. More experiments have been planned for the next period.

Fig. 11 Dark and illuminated I-V characteristics of cell 5, table I.

Fig. 12 Dark and illuminated I-V characteristics of cell 6, table I.

4.2 Neutral - Beam Sputtering/Milling System (Howard)

During this quarter a neutral beam ion system was used in an attempt to fabricate MIS cells using various foreign oxides. However, problems were found in the ion sputtering system when it was used to fabricate gold Schottky barrier diodes, because the Schottky devices exhibited severely degraded electrical characteristics. When using oxide coated wafer pieces to replace the target in the neutral beam ion system, it was found that the area covered by the ion beam at the target position appeared to be larger than the area of the target itself. Thus, inadvertent sputtering of the target-holder material (made of stainless steel) was apparently occurring. In addition, it was also discovered (after a number of trial depositions) that the vendor-supplied shutter system malfunctioned repeatedly due to the fact that it was flimsy, poorly designed, and consequently totally unreliable.

As a result of the two problems referred to above, work on the sputtered foreign oxides was severely hampered during this quarter. Several modifications of the system are planned to solve the above two problems. It is believed that reasonable progress will be made in the next quarter to fabricate MIS cells using sputtered oxides. The two modifications in process are (1) the fabrication of a smaller diameter final aperture to reduce the ion beam area at the target, and (2) the re-design and fabrication of the substrate shutter assembly.

4.3 Spin-On Oxide (Howard)

Preliminary investigations were started in the past two months of a spin-on oxide yielding a 25 Å film of 1.4% gallium oxide in silicon dioxide. The inability of the Ion Milling machine to work satisfactorily prevented the study of foreign oxides produced by this technique from getting underway, the effort therefore concentrated on determining the reproducibility of solar cells resulting from the spin-on oxide approach. It can safely be said that these initial efforts have been fairly successful and a patent disclosure is intended.

Fabrication at this point starts with the GaAs epitaxial wafers soaked in concentrated HCl, rinsed in D.I. water and gold-germanium mixture evaporated on back. The Au-Ge is next alloyed at 450°C in forming gas; the wafer is then resoaked in HCl and the gallium oxide-silica solution diluted with methyl alcohol is spun on at 3000 rpm to yield a film of 25 Å thickness. These wafers were then baked at 180°C for 45 minutes, coated with 60 Å of gold, and a collecting grid is e-beam evaporated to a thickness of 2000 Å through a metal mask. The individual cells are separated by photolithography and chemical etching.

To determine if it was indeed the gallium oxide solution giving us the test data, two controls were run along with the spin coated wafer, all being taken from the same epitaxial wafer. The first was etched, rinsed, etc., and 60 Å of Au along with the grid was applied, the second chip uncoated was baked along with the spin coated chip at 180°C for 45 minutes. The

baseline Schottky barrier cell exhibited $I_{SC} = 0.28$ mA and $V_{OC} = 0.44$ V while the spin-on oxide cell had $I_{SC} = 0.37$ mA and $V_{OC} = 0.53$ V.

Note that no attempt was made to optimize the fabrication. It was felt that a systematic study of the process was necessary including such parameters as concentration of Ga_2O_3 vs electrical performance, oxide film thickness vs electrical characteristics, surface preparation technology vs electrical parameters, etc.

At present using the spin-on approach for the oxide, cells of open circuit voltages of 700 mV or better are regularly obtained with little change due to shelf age. The reasoning behind this approach is as follows - one of the components of the native oxide is gallium oxide which by itself is unstable and extremely hydrophilic but when combined with SiO_2 to form a glass, the stability is enhanced because SiO_2 does not absorb water in the amorphous state. In addition a relatively low processing temperature (180°) and short time (45 minutes) seem to minimize the formation of surface states.

While the exact reason for the success of gallium oxide in the test results is not known, a systematic study may give an answer that will suggest better oxides in spin-on technology for use with gallium arsenide, and the technique can be later extrapolated to polycrystalline GaAs.

4.4 Modeling (N.C.A.&T.)

During the reporting period numerical results were realized from our grain boundary modeling of polycrystalline GaAs. The results of our initial

calculations indicate two important features of medium to high angle grain boundaries which are of both theoretical and experimental importance:

- 1) for the same bulk donor density N_D , the depletion width W decreases with increasing tilt angle θ ;
- 2) the depletion width (at donor density $N_D > 10^{17} \text{ cm}^{-3}$) is approximately independent of the tilt angle.

As reported earlier, our grain boundary model is an extended Read model. Read's formulism was applied to dislocations in GaAs in our previous investigations. However, the simple Read theory is valid only for single isolated (non-interacting) dislocations. But for medium ($1^\circ < \theta < 5^\circ$) to high angle ($\theta > 5^\circ$) grain boundaries, which dislocation overlap is of primary importance, the Read theory is not applicable. Since such grain boundaries are common in polycrystalline GaAs, a new theory is needed. We refer to our theory as the Extended Read Model. The results from our initial computations using this new model are shown in Fig. 13.

Curve (A) shows the space charge depletion width W for a tilt grain boundary ($\theta = 5^\circ$) as a function of bulk donor density N_D . With $\theta = 5^\circ$, the planar density of dangling bond acceptor levels introduced at the grain boundary is $\sigma_a = 5.5 \times 10^{13} \text{ cm}^{-2}$. As can be seen, the space charge depletion width decreases from $6.4 \mu\text{m}$ at $N_D = 10^{14} \text{ cm}^{-3}$ to $0.28 \mu\text{m}$ at $N_D = 10^{17} \text{ cm}^{-3}$. Curve (B) shows the results when the tilt angle is increased. For $\theta = 25^\circ$,

Fig. 13. Grain boundary depletion width as a function of tilt angle for small angle (A: $\Theta = 5^\circ$) and large angle (B: $\Theta = 25^\circ$)

the planar density of acceptor levels is increased to $\sigma_a = 2.7 \times 10^{14} \text{cm}^{-2}$. With $N_D = 10^{17} \text{cm}^{-3}$ the depletion width $W = 3.3 \mu\text{m}$ while for $N_D = 10^{17} \text{cm}^{-3}$, $W = 0.27 \mu\text{m}$.

Two important grain boundary characteristics are predicted from the model. First, for the same bulk donor density, the depletion width decreases with increasing tilt angle. This is somewhat surprising since the density of acceptor levels increases with tilt angle. However, the increase in donor acceptor density at the interface is more than compensated by the reduction in the occupational probability for a given core site due to the strong core - core interaction of the closely space dislocation cores.

Secondly, we note that for high bulk donor density $N_D > 10^{17} \text{cm}^{-3}$ the depletion width is nearly independent of tilt angle. This fact is very important both theoretically and experimentally. Theoretically it means that a precise tilt angle determination may not be needed in the modeling of grain boundaries in highly doped GaAs. This is very important since numerous grain boundaries of different orientation often occur in a single polycrystalline sample. Experimentally, it means that all grain boundaries ($\theta > 1^\circ$) in a single highly doped sample should have approximately the same measured depletion width.

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