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Model 516 LSI- 1 Six-Channel Scaler

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MODEL 516
LSI-11 SIX-CHANNEL SCALER

by

S. Bourret, T. W. Crane, G. W. Eccleston,
S. Johnson, and R. Slice

ABSTRACT

The LSI-11 scaler module has six separate counting channels, each with a 24-bit capacity. The scaler is located in the backplane of the computer and operated using software programs. This report describes the scaler, shows how to operate and test it, and provides listings of the scaler software control programs.

1. DESCRIPTION

1.1 General

The six-channel scaler is constructed on a multiwire module (Fig. 1) and connects directly into the Q-Bus of an LSI-11 microcomputer. The scaler module consists of six separate channels, each having a 24-bit capacity enabling up to 16 777 215 decimal counts to be recorded. The scaler inputs are (TTL) compatible, and a count is registered on the transition of a pulse from a low to a high state. Operation of the scaler module is controlled by software.

1.2 Basic Function

The scaler module employs a ripple-counting circuit to record information. Input connections to the unit are supplied using LEMO connectors, which provide dense packing when compared to BNC coaxial connectors. Scaler operation is controlled by software executed with the LSI-11 microcomputer. A universal clear strobe is used to zero all the channels simultaneously. Individual

Fig. 1.
Scaler board pictorial.

channels are operated by a control status register (CSR) that allows any channel to be enabled, disabled, or read. An additional test feature enables scalers to be incremented by a software command and enables the counting and readout functions of each channel to be checked automatically.

1.3 Console Control Commands

The LSI-11 microcomputer contains a set of on-line debugging technique (ODT) commands that allow peripherals and memory to be read and altered from the console keyboard. The scaler board is a peripheral device to the LSI-11 and has a switch-selectable address. The recommended address settings for the scaler are 177340 to 177346. With ODT commands, all the scaler functions can be readily exercised and checked. Detailed examples using ODT to check the scaler are provided in Secs. 4.2 and 6.2.

1.4 FORTRAN Control Commands

An assembly-language software driver has been written to allow communication between a FORTRAN program and the scaler module. This driver permits all the module functions to be controlled using the following four FORTRAN calls:

```
CALL CSCAL
CALL ESCAL(OCTAL)
CALL RSCAL(N,COUNT)
CALL TSCAL( INC)
```

The clear scaler call (CSCAL) requires no input parameters, and all channels are zeroed simultaneously. The enable scaler (ESCAL) command requires an octal pattern (OCTAL) to specify the channels to be enabled (1) and disabled (0). For example, octal value 35, which is binary (011 101), will enable scalers 0, 2, 3, and 4 and disable scalers 1 and 5. The read scaler call (RSCAL) obtains the count from one channel specified by N (N = 0, 1, 2, 3, 4, or 5) per call, and the channel count is stored in COUNT, which must be specified in double-integer format (INTEGER*4). Scaler testing is accomplished with the test scaler call (TSCAL). The integer number INC specifies the number of times the channels are to be incremented. The TSCAL call functions only on a disabled channel. To test all channels simultaneously, we must first disable them by an ESCAL call with OCTAL = 0.

2. SPECIFICATIONS

The model 516 six-channel scaler is housed in the main frame of the LSI-11 microcomputer. This module connects directly to the microcomputer's Q-Bus, which supplies power for the scaler. All signals into the scaler channels are on the edge strip and require LEMO connectors.

Performance Data

Pulse width	:	>50 ns
Polarity	:	TTL level requiring logic transition from 0.8 to 3.4 V for count to be registered
Impedance	:	50 Ω
Pulse pair resolution:		50 ns

Power requirements : 1.7 A at 5 V
Operating temperature: 0 to 50 C
Counting speed : 20 MHz

3. INSTALLATION

3.1 General

The scaler module, which contains no internal power supply, obtains all operating power from the computer power supply. We recommend that the computer be turned off when the module is inserted or removed from the Q-Bus.

Input pulses to the module may come from any source of logic pulses. The input impedance to each channel is approximately 50- Ω . Some care must be taken to prevent reflections in the driving transmission cable. Reflections can be avoided by using a standard 50- Ω impedance cable. Depending on the impedance mismatch, pulse duration, and cable length, the mismatch may present problems in actual operation.

3.2 Address Selection

The memory address selection (A3 through A12) for the scaler module is switch selectable. Refer to Fig. 2 for the address positions on the switches. The recommended memory address setting of 177340 allows the scaler to be used with the LSI-11, LSI-11/2, LSI-11/23, and LSI-11/24 microcomputers.

Addresses 177340 through 177346 are selected by setting switches 5B and 6B (Table I). The remaining locations 3 through 8 on switch 6B apply to the vector address and are not used by the scaler module. These positions should be switched off.

3.3 Clock or Scaler Selection

The scaler module contains six individual scalers (0 through 5). The last channel (5) can be used to receive external inputs or to provide clock pulses of a fixed frequency when the scaler is enabled for counting. Refer to Fig. 3 and locate the clock, labeled QT4, and jumper selections FF1, FF2, and FF3. An external input for counting is completed by connecting FF1 to FF2. The clock selection is completed by connecting FF3 to FF2.

4. OPERATING PROCEDURES

4.1 General

Connection of external TTL signals is made and properly terminated at the scaler module. A FORTRAN program, which contains one or more subroutines with calls to the scaler module, must be compiled and debugged to ensure proper operation. After a complete software control package is composed by linking the scaler software driver with the FORTRAN program, the completed binary program is loaded into the computer memory and executed by the LSI-11 microcomputer.

4.2 Scaler Operation Using ODT

The scalers can be operated and checked directly by using ODT commands at the computer keyboard console. The computer is placed into ODT by striking the BREAK key on the console. After the @ symbol is printed the system waits

Fig. 2.
Six-channel scaler bus interface.

TABLE I
SCALER BOARD ADDRESS SETTING OF 177340

<u>Address</u>	<u>Switch</u>	<u>Switch Position</u>
A 3	5B-1	OFF
A 4	5B-2	OFF
A 5	5B-3	ON
A 6	5B-4	ON
A 7	5B-5	OFF
A 8	5B-6	ON
A 9	5B-7	ON
A10	5B-8	ON
A11	6B-1	ON
A12	6B-2	ON

for input of ODT commands. Functions that can be exercised on the six-channel scaler are

- (1) zeroing the contents of all scalers,
- (2) enabling/disabling scalers to counting,
- (3) incrementing selected scalers, and
- (4) reading the contents of a scaler.

All functions are controlled by addressing memory locations occupied by the scaler. The memory addresses and their contents using the settings in Table I are

177340	control-status register,
177342	low-order scaler 12 bits,
177344	high-order scaler 12 bits, and
177346	scaler increment test/zero.

The 18 bit addressing capability of the LSI-11/23 and -11/24 microcomputers requires the above memory address (177XXX) to be specified as 177XXX when using ODT. Before collecting counts, each of the six scalers, 0, 1, 2, 3, 4, and 5, must be enabled by setting its appropriate bits to a value of 1 in the CSR. The enable-bit locations for each scaler are shown in Fig. 4. The bit pattern of Fig. 4 will enable scalers 1, 2, and 5 and disable scalers 0, 3, and 4 to counting.

Scalers must be read individually by setting the appropriate output bit to 0 in the CSR. If more than one scaler is set for output, false data may be generated. In addition, the scaler must be disabled before reading, or incorrect data may result. The bit locations to place scaler data on the output lines are shown in Fig. 5. The bit pattern of Fig. 5 has scalers 0, 1, 2, 4, and 5 enabled for counting. Scaler 3 is disabled, and its output line is set to 0 to permit reading.

This bit pattern is placed by ODT in the CSR by typing the address (177340) followed by a slash (/) to open the memory location. The contents

(XXXXXX) of the CSR then are printed. Typing the octal value (6767) corresponding to the enable- and output-bit locations of Fig. 5, followed by a carriage return (RET), loads the value into the CSR. The console command line appears as

```
@ 177340/XXXXXX 6767 RET
```

```
@ 177340/006767 RET
```

Fig. 4.
Enable scaler-bit locations in the CSR.

Fig. 5.
Output-scaler specification bits in the CSR.

The command's second line checks to ensure that the information is correctly stored in the CSR.

The capacity of each scaler is 24 bits, which are stored in two 12-bit memory addresses. The low-order 12 bits are at address 177342, and the high-order 12 bits are at address 177344. To read the data, the address followed by a slash is typed at the console. For example, if scaler 0 contains 5191 decimal counts (an octal value of 12107), these data can be read by disabling the count bit for scaler 0 and enabling the output bit. If we want to leave scalers 1 through 5 enabled for counting, the bit pattern in the CSR is first set, then the scaler data are read. The instruction sequence is:

```
@ 177340/XXXXXX 7676 RET
```

```
@ 177340/7676 RET
```

```
@ 177342/2107 RET
```

```
@ 177344/1 RET
```

The contents of all scalers can be cleared by writing to address 177346. Writing data at this address results in a clear strobe that zeros all the contents of all scalers. Scalers cannot be individually cleared; to clear all scalers, type:

```
@ 177346/XXXXXX 1 RET
```

A hardware increment feature, built into the six-channel scaler board, enables software to check the scalers for proper counting and to check whether any scalers are dropping bits or functioning improperly. To increment a scaler with the hardware test feature, all scalers first must be disabled from counting. Each time the address 177346 is read, all scalers will be incremented. For example, to test all scalers and initially read the contents of scaler 4, disable all scalers to counting by setting the enable bits to zero. At the same time, set the scaler 4-output bit for reading. Next, the scalers will be zeroed and then incremented twice by using the following instructions:

```
@ 177340/XXXXXX 57 RET      DISABLE, READ 4
@ 177340/57      RET
@ 177346/XXXXXX 1 RET      ZERO
@ 177346/XXXXXX RET      INCREMENT
@ 177346/XXXXXX RET      INCREMENT
@ 177342/000002 RET      low-order 12 bits
@ 177344/000000 RET      high-order 12 bits
@
```

Electronics details of the hardware and control signals are discussed in Sec. 6.

4.3 Example FORTRAN Program

The following listing is a FORTRAN program that can operate the scalers. This program makes a series of calls to another routine that communicates at the assembly-language level with the scaler board. A listing of the assembly-language scaler driver is provided in Appendix A. A call to read a scaler results in the driver packing the low- and high-order 12 bits of data into the specified INTEGER*4 address. These data then can be translated to a floating point word using the AJFLT function provided in the System Subroutine Library (SYSLIB).

```
REAL*4 CNT
INTEGER*4 COUNT, ARRAY
COMMON COUNT(6), CNT(6), ARRAY(6)

C  CLEAR THE SCALERS
CALL CSCAL
```

```

C  ENABLE SCALERS 1,3,5  OCTAL = 52(101 010)
   CALL ESCAL ("52)

C  WAIT 10 SECONDS TO COLLECT CNTS
   CALL ISLEEP (0,0,10,0)

C  STOP SCALERS
   CALL ESCAL ("0)

C  READ SCALER 3 INTO COUNT(3)
   CALL RSCAL (3, COUNT(3))

C  CONVERT TO A FLOATING POINT
   CNT(3) = AJFLT(COUNT(3))

STOP
END

```

Appendix B lists a complete FORTRAN program to test and check the scalers, and Appendix A lists the RT-11 assembly language scaler driver.

5. CIRCUIT DESCRIPTION

5.1 General

In the diagrams in Figs. 2, 6, and 7, locate these four areas: the six scalers on the left side of the print, the CSR in the center, the test circuit in the upper right, and the address control signal on the lower right.

There are six address control signals derived from four base addresses, 177340, 177342, 177344, and 177346. Each of the four base addresses has an input and an output signal. This arrangement gives a range of eight control signals, of which six are used. RSTAT, the input, and SETCREG, the output of base address 177340, are used to read and write the CSR. The input of SELDEV2, BYTE1, is used to strobe the low-order 12-bit set of data from the selected scaler. The SELDEV2 output is not used. SELDEV4, BYTE2, input is used to strobe the high-order 12-bit set of data, but the output is not used. Both the input and output of SELDEV6 are used. The output control signal clears all the scalers. The input is the TEST signal that increments the scalers when their ENBL(0-5) signals are disabled.

Each of the six ($N = 0,5$) scalers has several control signals. COUNT(N) is the external input pulse from the LEMO connector. ENBL(N) allows the signal to enter the counting register. CNTR(N) selects the scaler to be read. BYTE1 reads the low-order 12 bits and BYTE2 reads the high-order 12 bits. SELDEV6 input clears the scaler.

The CSR, a 12-bit register that can be read and written with SELDEV0, is composed of two sections, ENBL(0-5) and CNTR(0-5). We emphasize that the ENBL signals are 1 true and the CNTR signals are 0 true. Only one scaler can be read at a time.

The test circuit will put one count in each scaler if and only if all the ENBLs are false, meaning all are set to 0, and the SELDEV6 input signal is given. For more details, see Sec. 6.2.

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Fig. 7

The signal-flow block diagram corresponding to one of the six scales.

5.2 Q-Bus Interface

The DEC Q-Bus transfers signals between the LSI-11 CPU, memory, and the interfaces. The Q-Bus bus is bidirectional and has 16 data/address lines and 18 control/synchronization signal lines. Details of the Q-Bus description are found in the DEC Microcomputer Handbook.¹

6. MAINTENANCE

6.1 Preparation for Troubleshooting

To prepare the scaler board for testing, use a test pulser, a scope, an extender board, Figs. 2, 3, and 6, a DEC Microcomputer Handbook, and become familiar with the LSI-11's ODT (Sec. 4.2).

6.2 Scaler Check-out

To test the CSR, observe the ENBL(0-5) signal outputs from the LEDs on the back of the scaler board. The CNTR(0-5) can be seen with a scope or by reading the scalers with the software. For example, to enable counters 1 and 3 to count and to set up counter 1 to be read (Fig. 8), use ODT,

```
@ 177340/XXXXX 1275 RET (X represents data output from ODT) (RET
                           represents the carriage return key on the
                           console).
```

@

This operation will enable scalers 1 and 3 to count, should turn on their respective LEDs, and also should set up scaler 1 to be read. Only one scaler can be read at a time because the output data share the computer Q-Bus lines.

The scalers can be incremented two ways. One, use an external pulse source, feed it into the desired LEMO connector, and enable the associated scaler. Two, set all the scaler ENBL(0-5) bits to false; that is, to 0, then give a SELDEV6 output. Use ODT,

```
@ 177340/XXXXX 00XX RET (disables all ENBL bits)
```

```
177346/XXXXX RET (increments all scalers by 1)
```

```
177346/XXXXX RET (increments all scalers by 1 again)
```

@

To read a scaler, the CSR must have the selected CNTR bit set and then must issue the BYTE1 command for the low-order 12 bits and BYTE2 for the high-order 12 bits of data. As an example, read scaler number 4. With ODT,

```
@ 177340/XXXXX 5757 RET (set CNTR4 to be read)
```

```
@ 177342/ddddd RET (read low-order 12 bits of data)
```

Fig. 8.
Control status register

@ 177344/ddddd RET (read high-order 12 data bits)

To clear the scaler, issue the SELDEV6 output command. For example,

@ 177346/XXXXX 1 Return

@

The number after the XXXXX could be any number from 0 through 7.

Putting the above commands into one program to test the primary operations will yield the following. First, clear the scalers, read scaler 1, increment all the scalers by one, read scaler 1, increment again, read scaler 1 again, and then clear all scalers and read scaler 1 again.

@ 177346/XXXXX 1 RET (clear all scalers)

@ 177340/XXXXX 0075 RET (set scaler 1 to be read)

@ 177342/00000 RET (read low-order 12 data bits of scaler 1)

@ 177344/00000 RET (read high-order 12 data bits of scaler 1)

@ 177346/XXXXX RET (increment all scalers by 1)

@ 177342/000001 RET (low-order 12 bits of scaler 1 data)

@ 177344/000000 RET (high-order 12 bits of scaler data)

@ 177346/XXXXX RET (increment all scalers)

@ 177342/000002 RET (read scaler low-order 12 bits)

@ 177344/000000 RET (read scaler high-order 12 bits)

@ 177346/XXXXX 1 RET (clear all scalers)

@ 177342/00000 RET (read scaler low-order 12 bits)

@ 177344/00000 RET (read scaler high-order 12 bits)

6.3 Troubleshooting Suggestions

If the scaler board is suspected of malfunctioning, try the following. Turn off the computer. Remove the cables from the scaler board. Place the scaler board on an extender board. Power up the computer. Check the +5 V on the scaler board. The testing instructions in Sec. 6.2, Table II, and Figs. 2, 3, and 6 should provide assistance in isolating trouble.

TABLE II
TROUBLESHOOTING SUGGESTIONS

Symptom	Suggestions
None of the scalers function.	(1) Check +5 V on board. (2) Check address control signals with scope and ODT. (3) Check control register circuitry. (4) Use test program routine in Sec. 6.2. (5) Use pulser on scaler input and trace signal path using print and scope. (6) Check Q-Bus control circuitry.
Address control signals do not respond.	(1) Check device decoder signals by putting computer in a loop using program. (2) Check pin Z11, which should be pulsing. If not, trace backward until missing signal is found.
One scaler does not work.	(1) Check the scaler's ENBL and CNTR signals. (2) With a pulser and scope (following the schematic), trace forward in circuit for the missing signal.

Two simple looping programs, which can be entered and run with ODT, will pulse the selected address control signal by inserting the appropriate address number in program address 1002. The first program is used for checking input control signals such as RSTAT(177340), BYTE1(177342), BYTE2(177344), and CLEAR(177346). The second program is for output-control signals SETCREG(177340) and TEST(177346). With ODT,

Program 1:

```

@ 1000/13700 RET      MOV @ #177340, R0 ; Input RSTAT
@ 1002/177340 RET
@ 1004/775           BR.-3           ; Loop back
@ 1000G              ; Go

```

Program 2:

```

@ 1000/10037 RET      MOV R0, @ #177340 ; Set control key
@ 1002/177340 RET
@ 1004/775           RET          BR.-3           ; Loop back
@ 1000G              ; Go

```

REFERENCE

1. Digital Microcomputer Handbook (DEC, Maynard, Massachusetts, 1976).

APPENDIX A

FORTRAN CALLABLE ASSEMBLY-LANGUAGE SCALER PROGRAM


```

1          LIST TTM
2          ;*****
3          ; SCALER.MAC
4          ;
5          ; LSI-11 6 CHANNEL FORTRAN CALLABLE SCALER DRIVER
6          ; LSI-11 FOUNDATION MODULE
7          ;
8          ;      GEORGE ECCLESTON  6-JUN-78
9          ;      REV. SSJ 17-JUL-80 1050
10         ;
11         ;      FOR RT-11 VERSION 3B
12         ;
13         ;      FORTRAN CALLS TO SCALERS:
14         ;
15         ;      CALL CSCAL          CLEAR ALL SCALERS 0,1,2,3,4,5
16         ;      CALL ESCAL(OCTAL)   OCTAL PATTERN TO ENABLE SCALERS
17         ;      OCTAL=25 010 101 SCALERS 0,2 AND 4 WILL BE ENABLED
18         ;      CALL RSCAL(I,DATA)  READ SCALER I DATA=INTEGER*4
19         ;      CALL TSCAL(N)       TEST ALL SCALERS BY INC N TIMES
20         ;
21         ;ADDRESSES FOR DEVICE CONTROL
22         ;
23         ;      177340          SET ENABLE AND COUNTER BITS
24         ;      177342          READ SCALER BITS 11-0
25         ;      177344          READ SCALER BITS 23-12
26         ;      177346          CLEAR SCALERS ON WRITE
27         ;      177346          TEST SCALERS ON READ
28         ;
29         ;*****
30         ;
31         ;
32         ;      LOW ORDER 6 BITS OF STATUS ARE COUNTER (0 TRUE)
33         ;      ANY COUNTER BIT WHICH IS ZERO WILL CAUSE THAT SCALER
34         ;      DATA TO BE AND'ED WITH ANY OTHER SCALERS IN THE READ
35         ;
36         ;      NEXT 6 BITS OF STATUS ARE ENABLE (1 TRUE)
37         ;      ANY ENABLE BIT WHICH IS 1 CAUSES THAT SCALER TO COUNT
38         ;
39         ;.TITLE SCALER
40         ;.GLOBL CSCAL,ESCAL,RSCAL,TSCAL
41
42 000000    .CSECT          ;RELOCATABLE CODE
43          177340    STATUS=177340    ;SET ENABLE AND COUNTER STATUS
44          177342    READ1=177342    ;READ LOW BITS 11-0
45          177344    READ2=177344    ;READ HIGH BITS 23-12
46          177346    CLEAR=177346    ;CLEAR ALL SCALERS - WRITE
47          177346    TEST=177346     ;TEST SCALERS - READ
48
49 000000    010037    CSCAL:  MOV     R0,@#CLEAR    ;CLEAR SCALERS - ANY WRITE WILL DO
50          177346
51          000004    000207    RTS     PC
52
53 000006    017500    ESCAL:  MOV     @2(R5),R0    ;LOAD SCALER ENABLE PATTERN(OCTAL)
54          000002
55 000012    000300    SWAB     R0                ;SHIFT LEFT 8 PLACES
56 000014    105100    COMB     R0                ;SET COUNTER BITS=1 (OFF)
57 000016    006200    ASR      R0                ;SHIFT RIGHT 2 PLACES

```

```

56 000020 006200      ASR    R0          ;ALIGNED AND SET
57 000022 010037      MOV    R0,@#STATUS ;SET ENABLE AND COUNTER BITS
177340
58 000026 010067      MOV    R0,STATE    ;SAVE STATE OF ENABLE AND COUNTERS
000116
59 000032 000207      RTS     PC
60
61 000034 017500 RSCAL: MOV    @2(R5),R0    ;LOAD I - SCALER TO READ
000002
62 000040 006300      ASL     R0          ;USE BYTES NOT WORDS (TIMES 2) AS INDEX
63 000042 062700      ADD     #SCATAB,R0    ;COMPUTE ADDRESS OF TABLE ENTRY
000156
64 000046 011000      MOV     (R0),R0      ;GET TABLE ENTRY FOR THIS SCALER
65 000050 016701      MOV     STATE,R1     ;GET PRESENT STATE OF ENABLE
000074
66 000054 040001      BIC     R0,R1       ;CLEAR ENABLE (OFF); CLEAR COUNTER (ON)
67 000056 010137      MOV     R1,@#STATUS  ;SET NEW STATE
177340
68 000062 013700      MOV     @#READ1,R0   ;LOW BITS 11-0 (IN LOWER 12)
177342
69 000066 013701      MOV     @#READ2,R1   ;HIGH BITS 23-12 (IN LOWER 12)
177344
70 000072 016737      MOV     STATE,@#STATUS ;RESET PREVIOUS STATE
000052
177340
71
72          ; CONFIGURE R1 AND R2 TO 16 BIT AND 8 BIT WORDS
73          ;
74 000100 010102      MOV     R1,R2       ;DUPLICATE BITS 23-12
75 000102 046702      BIC     MASKL,R2    ;ISOLATE BITS 23-16 IN MIDDLE 8
000044
76 000106 046701      BIC     MASKH,R1    ;ISOLATE BITS 15-12 IN BOTTOM 4
000042
77 000112 000301      SWAB    R1         ;BITS 15-12 TO UPPER BYTE
78 000114 006301      ASL     R1         ;SHIFT LEFT 4 MORE TIMES
79 000116 006301      ASL     R1
80 000120 006301      ASL     R1
81 000122 006301      ASL     R1         ;BITS 15-12 NOW IN UPPER FOUR
82 000124 060001      ADD     R0,R1       ;FORM 15-0 BITS
83 000126 006202      ASR     R2         ;SHIFT 23-16 TO LOWER BYTE
84 000130 006202      ASR     R2
85 000132 006202      ASR     R2
86 000134 006202      ASR     R2         ;HIGH 8 BITS POSITIONED
87 000136 016500      MOV     4(R5),R0    ;LOAD PTR TO DATA ADDRESS
000004
88 000142 010120      MOV     R1,(R0)+    ;PLACE INTO DATA(1)
89 000144 010210      MOV     R2,(R0)    ;PLACE INTO DATA(2)
90 000146 000207      RTS     PC
91          ;
92          ;
93 000150 000077 STATE: .WORD 77          ;STATE OF ENABLE AND COUNTER BITS
94 000152 170017 MASKL: .WORD 170017      ;ISOLATE MIDDLE 8 BITS
95 000154 177760 MASKH: .WORD 177760      ;ISOLATE LOWER 4 BITS
96          ;
97          ;SCALER TABLE ADDRESS FOR READING SELECTED SCALERS
98          ;
99 000156 000101 SCATAB: .WORD 0101      ;SCALER 0 000 001 000 001

```

```

100 000160 000202      .WORD 0202      ;SCALER 1 000 010 000 010
101 000162 000404      .WORD 0404      ;SCALER 2 000 100 000 100
102 000164 001010      .WORD 1010      ;SCALER 3 001 000 001 000
103 000166 002020      .WORD 2020      ;SCALER 4 010 000 010 000
104 000170 004040      .WORD 4040      ;SCALER 5 100 000 100 000
105
106                      ; ROUTINE TO INCREMENT ALL SCALERS -- CALL TSCAL(N)
107                      ;
108 000172 005725 TSCAL: TST      (R5)+      ;BUMP PTR TO ADDRESS OF N
109 000174 017500      MOV      @(R5),R0      ;LOAD N - NUMBER OF INCREMENTS
                      000000
110 000200 012737      MOV      #0,@#STATUS      ;DISABLE ALL SCALERS FOR TEST
                      000000
                      177340
111                      ;
112                      ; INCREMENT SCALERS N TIMES
113                      ;
114 000206 013701 CINC:  MOV      @#TEST,R1      ;INCREMENT SCALERS - JUST READ
                      177346
115 000212 005300      DEC      R0      ;COUNT DOWN INCREMENTS
116 000214 003374      BGT      CINC      ;CONTINUE INC IF POSITIVE
117 000216 000207      RTS      PC
118                      ;
119          000001      .END

```

APPENDIX B

SCALER FORTRAN TEST PROGRAM

```

C FORTRAN PROGRAM TO TEST SCALERS
      DIMENSION COUNT(6)
      INTEGER*2 OCTAL
      INTEGER*4 SDATA
      DATA IC/'103/,IE/'105/,IR/'122/,IT/'124/

C
10      TYPE 501
      CALL IPOKE('44','10000.OR.IPEEK('44))      !SET JSW
11      ICR=ITINR()      !READ CHAR
      IF(ICR.LT.0)GOTO 11
      CALL IPOKE('44','167777.AND.IPEEK('44))
      IF(ICR.EQ.IC)GOTO 100
      IF(ICR.EQ.IE)GOTO 101
      IF(ICR.EQ.IR)GOTO 102
      IF(ICR.EQ.IT)GOTO 103
      GOTO 9

C
100     CALL CSCAL      !CLEAR ALL SCALERS
      TYPE 600
      GOTO 10

C
101     TYPE 610      !ENABLE SCALERS
      READ(5,510)OCTAL      !INPUT OCTAL ENABLE PATTERN
      CALL ESCAL(OCTAL)
      GOTO 10

C
102     TYPE 620      !READ SCALERS 0-5
      DO 225 I=1,6
      N=I-1
      CALL RSCAL(N,SDATA)
      COUNT(I)=AJFLT(SDATA)
      WRITE(7,520)N,SDATA,COUNT(I)
225     CONTINUE
      GOTO 10

C
103     TYPE 630      !TEST SCALERS
      READ(5,530)NINC      !NUMBER OF SCALER INCREMENTS
      CALL TSCAL(NINC)
      GOTO 102      !READ SCALERS
      STOP

500     FORMAT(///' KEYBOARD COMMANDS TO TEST LSI-11 SCALER'/
1       ' C - CLEAR ALL SCALERS'/
2       ' E - ENABLE SCALERS  OCTAL 000 101 -> SCALERS 0 & 2' /
3       ' R - READ ALL SCALERS'/
4       ' T - TEST ALL SCALERS'///)

501     FORMAT(//$, ' INPUT COMMAND LFTTR')
600     FORMAT(// ' ALL SCALERS CLEARED')
610     FORMAT(///' ENABLE SCALERS'/$, ' INPUT OCTAL ENABLE PATTERN->')
510     FORMAT(016)
620     FORMAT(///' READ ALL SCALERS'/' SCALER')
520     FORMAT(I3,I24,F16.0)
630     FORMAT(///' TEST ALL SCALERS'/$, ' INPUT NUMBER OF INCREMENTS->')
530     FORMAT(I16)
      END

```


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