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REAL-TIME COMPUTER ANALYSIS
FOR NUCLEAR MATERIAL DETECTION
PART 3:
NUCLEAR INSTRUMENTATION INTERFACE

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MASTER

DECEMBER 1981

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Nuclear instrumentation interface.

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REAL-TIME COMPUTER ANALYSIS FOR NUCLEAR MATERIAL DETECTION

Part 3: Nuclear Instrumentation Interface

SUMMARY

An electronic interface between a Digital Equipment Corporation (DEC) LSI-11 microcomputer and a LeCroy Research Systems model 3001 "qvt" multichannel analyzer is described in detail. This interface provides for 16-bit parallel data transfer from the memory of the analyzer to the memory of the computer. An unusual feature of the interface is a provision that allows storage of counts of logic pulses (e.g., from radiation detector discriminators) in the first 16 channels of the analyzer's memory. A further provision allows use of a LeCroy printer and display interface that is designed specifically as a companion module to the qvt analyzer.

INTRODUCTION

For some time the Lawrence Livermore National Laboratory (LLNL) has possessed a nuclear instrument system for mobile detection and real-time analysis of nuclear radiation. This system, which is installed in the LLNL search and analysis van, has proven valuable for studying the problem of detecting and locating radioactive material when the source and detector are in motion relative to each other. In 1979 the collection and

analysis of nuclear data were put under computer control at LLNL.¹ Recently the data collection electronics were upgraded. Included in the upgrade were the design and construction of a nuclear instrumentation interface between a DEC LSI-11 microcomputer and a LeCroy Model 3001 "qvt" multichannel analyzer. This arrangement allows data to be acquired and buffered in the analyzer memory while freeing the microcomputer for analysis of previously acquired data.

This report is the third in a series of reports describing the computer-based detection and analysis system. The first report in this series¹ described the data analysis algorithms used, the first-generation data collection electronics, and field testing of the system. The second report in the series² is a detailed description of the computer program written to control the second-generation system and implement the data analysis algorithms. The present report is a detailed description of the nuclear instrumentation interface designed and constructed for the second-generation system.

Throughout this report, several items of hardware are mentioned repeatedly. The terms used to refer to this hardware are summarized and defined in Table 1.

Table 1. Terms and definitions used in this report.

Terms	Definitions
Detector logic pulse, detector logic input	The output pulse from a discriminator connected to a radiation detector (in our current application, ^3He neutron detectors)
LSI-11, microcomputer, computer	A Digital Equipment Corporation LSI-11 microcomputer
MCA, qvt, multichannel analyzer, analyzer	A LeCroy Research Systems model 3001 "qvt" multichannel analyzer
Nuclear instrumentation interface, NII	The nuclear instrumentation interface that is the subject of this report

REAL-TIME NUCLEAR DATA ACQUISITION AND ANALYSIS SYSTEM

The real-time system is based on a 16-bit microcomputer with 28K dynamic RAM, hardware fixed and floating point instructions and memory-mapped I/O. Also included in the computer chassis are a clock-calendar, programmable real-time clock, digital-to-analog converter (DAC), and various peripheral interface boards. Peripheral equipment includes a video terminal, dual floppy disk drive, strip chart recorders, and a nuclear data acquisition subsystem. Figure 1 is a block diagram of the system hardware.

The upper portion of Fig. 1 illustrates a rather conventional microcomputer system. At the heart of the nuclear data acquisition subsystem, illustrated in the lower portion of the figure, is a LeCroy qvt multichannel analyzer. This dual-width NIM

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Fig. 1. Real-time nuclear data acquisition and analysis system block diagram.

module is a 16-bit, 1024-channel instrument with horizontal and vertical outputs that allow its memory contents to be displayed on a monitor oscilloscope. A companion module to the MCA is the LeCroy model 3157 printer and display interface. This module provides both a decimal display of MCA memory contents and a hard-copy readout to a six-column line printer. The nuclear instrumentation interface joins these modules to the LSI-11 microcomputer. This interface also allows each of the first 16 channels of the MCA memory to be used as scaler memory registers. Thus, it is possible to use the MCA to acquire a gamma-ray spectrum, while simultaneously scaling the output of 16 other individual detectors. In our current application, two of the 16 scaler inputs are used for ^3He neutron detectors.

PHYSICAL DESCRIPTION OF THE NUCLEAR INSTRUMENTATION INTERFACE

The nuclear instrumentation interface is housed in a triple-width NIM module. Figure 2 shows a view of the front and rear panels of the interface. A meter at the top of the front panel displays MCA dead time as a percentage. This function is enabled by feeding the BUSY OUT signal from the MCA to the BUSY input BNC connector at the bottom of the front panel of the nuclear instrumentation interface. The rest of the front panel is occupied by a four-by-four array of BNC connectors for scaler inputs.

Front panel

Rear panel

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Fig. 2. Views of the front and rear panels of the nuclear instrumentation interface.

The NIM power connector is at the lower left-hand corner of the rear panel. Above this are two flat cable connectors (J1 and J2) for connection to a DRV11 general-purpose parallel line interface on the LSI-11 bus. To the right of these connectors are two 44-contact card-edge connectors for connection of the LeCroy printer and display interface (PTR) and the MCA (PHA).

Figure 3 is a view of the left side of the nuclear instrumentation interface chassis (with the side panel removed). The control logic card cage containing the interface circuitry is pictured at the center.

THEORY OF OPERATION

DRV11 Parallel Interface

As shown in Fig. 1, the nuclear instrumentation interface is joined to the LSI-11 bus with a DRV11 parallel line unit. An understanding of the salient features of the DRV11 is useful before proceeding to the discussion of the operation of the nuclear instrumentation interface.

The DRV11 is a general-purpose parallel interface configured on a dual-width LSI-11 circuit board. It is used for connecting parallel line TTL devices to the LSI-11 bus. The interface both provides LSI-11 bus interface and control logic for interrupt processing and vector generation and permits data transfers under program control. To the LSI-11 processor, the DRV-11 appears to

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Fig. 3. View of the left side of the nuclear instrumentation interface with the side panel removed. All circuitry is contained in the card cage at the center of the chassis. The functions of the individual cards are described in the section on Theory of Operation.

be three addressable registers: a control/status register (DRC SR), an input buffer (DRINBUF), and an output buffer (DROUTBUF). The addresses of these registers are in the memory-mapped I/O address space of the LSI-11 (upper 4K words) and are user-assigned by way of jumpers on the DRV11 circuit board.

Operation of the MCA, via the nuclear instrumentation interface, is accomplished under commands that load bits 0 and 1 of the DRC SR register. The four possible combinations of bit settings provide stop, reset, start, and read-out modes, as detailed in Table 2.

Table 2. DRV11 control settings for operation of the qvt multi-channel analyzer.

Mode	Control setting of DRC SR bits		Decimal equivalent of bits 0 and 1	Control function
	CSR1	CSR0		
Stop	0	0	0	Halts MCA data acquisition in progress. It is only in this mode that the MCA and printer and display interface are interconnected for normal manual operation
Reset	0	1	1	Clears MCA memory
Start	1	0	2	Begins data acquisition
Read-out	1	1	3	Enables read-out of the contents of the MCA memory into the LSI-11

Reading the contents of the MCA memory is accomplished by first putting the MCA in read-out mode. The contents of each memory location (channel) are then obtained as follows:

- The desired MCA memory address (channel number) is loaded into the DROUTBUF register.
- The value currently stored in the selected channel is presented to the output lines to be read into the DRINBUF. The DRINBUF is not a true buffer but a read-only register that comprises gated bus drivers that transfer data from the MCA onto the LSI-11 bus under program control.

Programming considerations are detailed in the Programmer's Guide section of this report. Program listings are in Appendix A. A more detailed description of the DRV11 can be found in Ref. 3.

Nuclear Instrumentation Interface

Four types of circuit boards have been designed to implement the functions of the nuclear instrumentation interface. All circuitry is contained in seven boards: one interface control board, two input buffer boards, and three bus buffer boards. A simplified block diagram showing the interrelationship of these boards is presented in Fig. 4. Detailed schematics of the individual boards are presented in this section, and a complete schematic of the interface showing the interrelationship of all of these boards is found in Appendix B.

Fig. 4. Nuclear instrumentation interface block diagram.

Interface Control Board

The interface control board provides the control logic for selection of the four MCA operating modes: stop, reset, start, and read-out. These functions are obtained by decoding the DRV11 control lines, CSR0 and CSR1, with a quad two-input OR gate. Figure 5 is a schematic diagram of the board.

Input Buffer Boards

Two input buffer circuit boards provide the means to receive detector logic pulses. Each buffer stores pulses from eight inputs in the dual flip-flop integrated circuits IC3 through IC6 (see Fig. 6). When a pulse is received and stored in a flip-flop, all other inputs on the board are inhibited by gates IC1 and IC2 until the value in the proper channel of MCA memory has been incremented. Integrated circuit IC7, an eight-input priority encoder, translates the flip-flop information into a three-bit address (A0, A1, and A2 out). A priority is assigned to each input of the encoder so that in the event that two or more inputs are simultaneously active, only the input with the highest priority is represented at the output. Input lines are numbered 0 through 7 with priority increasing with line number.

Two input buffer boards are required to scale 16 individual detectors. The enable out ($\overline{E_0}$) output from IC7 on the second input buffer is connected to the enable in ($\overline{E_1}$) input on IC7 of the first input buffer, extending the priority encoding across 16

Device No.	+5 V	Gnd
U1 thru U3	14	7

81/19181 05

Fig. 5. Interface control circuit board schematic diagram.

Fig. 6. Input buffer circuit board schematic diagram.

inputs. The $\overline{E}_O$ output from the second input buffer also forms the fourth address bit for the first 16 channels of MCA memory. Additionally, the $\overline{E}_O$ outputs of either board indicate the presence of a detector input pulse and start the timing sequence for storage of the event in the MCA.

Logic Control Board

The logic control board accepts both the three-bit addresses generated by each input buffer board and the enable out ($\overline{E}_O$) signal from the second input buffer board and uses them to form a four-bit address for storage events represented by logic inputs in the first 16 channels of the MCA memory. This board also provides the gating and timing signals necessary for storage of these events.

Figure 7 illustrates the quad two-input NAND gate (IC1) used to mix the three-bit active low binary address information from the two input buffer circuit boards. The outputs of IC1 are connected to one of the bus buffer circuit boards discussed in the following subsection. A quad two-input NOR gate (IC2) is used to provide gating signals necessary for starting the store sequence for a detector logic input and inhibiting further detector logic inputs until the sequence is complete. A dual four-input NAND buffer (IC3) is used where fan out is required. Integrated circuits 4, 5, and 6 are used for the store sequence. These are dual monostable multivibrators, level triggered, non-

Fig. 7. Logic control circuit board schematic diagram.

retriggerable integrated circuits. Each multivibrator has a negative transition triggered input. Once fired, the outputs are independent of further transition of the inputs and are a function of the timing circuits or of the overriding clear inputs.

The detector logic input storage sequence is shown schematically in Fig. 8. When a detector logic input occurs, the input signal at IC6 pin 9 has a negative transition starting the memory address (MAL) multivibrator which loads the appropriate address into the MCA address register via one of the bus buffer boards.

The negative transition of the MAL multivibrator starts the load register (LD) multivibrator which causes data at the addressed memory location in the MCA to be read into the MCA incrementing register.

The negative transition of the LD multivibrator starts the increment (INC) multivibrator which adds one to the value in the MCA incrementing register.

The negative transition of the INC multivibrator starts the write ($R/\bar{W}$) multivibrator which writes the contents of the MCA incrementing register back into its original memory location.

The negative transition of the ($R/\bar{W}$) multivibrator starts the reset multivibrator which resets the flip-flops in the input buffer readying the interface to accept a new detector logic input.

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Fig. 8. Timing sequence for scaling detector logic pulses from up to 16 individual inputs.

The gamma busy multivibrator is used in the process of storing a gamma-ray event. Such an event starts the gamma busy multivibrator which resets the memory address, load register, increment and write multivibrators and starts the reset multivibrator to reset any detector logic input that might be waiting to be processed.

Bus Buffer Boards

The three bus buffers provide the connections for driving the MCA bus for the MCA control, logic input stage, and data read out functions. The bus driver uses a quad tri-state bus buffer with high-true enable signal on pin 17 that energizes all the tri-state buffers. Figure 9 is a schematic diagram of a bus buffer board.

Controlling Data Acquisition Time

Control of data acquisition time must be done by a means external to the MCA. This can be easily accomplished using a suitable programmable real-time clock module for the LSI-11, such as the DEC model KQV11-A³ or the MDB Systems model MLSI-KWIIP.⁵

Fig. 9. Bus buffer circuit board schematic diagram.

EQUIPMENT INSTALLATION

Jumper Selection on the DRV11 Parallel Interface

Addresses for the control/status register (DRC SR), input buffer (DRINBUF), and output buffer (DROUTBUF) are assigned in the memory-mapped I/O portion of the LSI-11 address space using jumpers A3 to A12 on the DRV11 circuit board (see Fig. 10). We have chosen to use the standard address assignments given by the factory-installed jumper configuration. Table 3 summarizes these assignments and configurations.

Table 3. DRV11 standard address assignments and factory jumper configuration.

Standard address assignments			Factory jumper configuration	
Description	Mnemonic	Address	Jumper designation	Jumper state*
<u>Register:</u>			A3	R
Control and status	DRC SR	167770 ₈	A4	R
			A5	R
			A6	R
			A7	R
Output buffer	DROUTBUF	167772 ₈	A8	R
			A9	R
			A10	R
Input buffer	DRINBUF	167774 ₈	A11	R
			A12	I

*R = removed, I = installed.

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Fig. 10. Location of jumpers and connectors J1 and J2 on the DRV11 circuit board.

Connecting and Cabling

The connecting and cabling scheme for joining the nuclear data acquisition subsystem to the LSI-11 bus is shown schematically in Fig. 11.

The DRV11 is connected to the nuclear instrumentation interface with two ribbon cables with 26-pin connectors. First the connectors are joined to J1 and J2 on the DRV11 circuit board and the board is installed in the LSI-11 chassis. The free ends of the ribbon cables are then attached to their counterpart connectors (J1 and J2) on the rear panel of the interface.

A 44-conductor cable is used with mating connectors to connect the 44-contact card edge connector labeled PHA on the rear panel of the nuclear instrumentation interface to a similar edge connector (labeled J2) on the rear panel of the MCA.

A signal cable with BNC connectors is used to join the BUSY input on the front panel of the nuclear instrumentation interface to the BUSY OUT connector on the front panel of the MCA. This interconnection enables the dead-time meter on the front panel of the nuclear instrumentation interface.

Another 44-conductor cable is used to join the 44-contact card edge connector labeled PTR on the rear panel of the nuclear instrumentation interface to a similar edge connector (labeled J2) on the rear panel of the LeCroy printer and display interface.

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Fig. 11. Connecting and cabling scheme for joining the nuclear data acquisition subsystem to the LSI-11 bus.

Up to 16 detector logic inputs (e.g., discriminator outputs from proportional counters) may be connected to the 16 BNC connector array on the front panel of the nuclear instrumentation interface

A gamma signal cable from an appropriate shaping amplifier* is connected to the BNC V-input on the front panel of the MCA.

Two BNC cables are used to join the horizontal and vertical CRT outputs of the MCA to the X- and Y-inputs of a monitor display oscilloscope.

Finally, the six-column line printer is joined to the printer and display interface with the flat, multi-conductor, braided cable supplied.

PROGRAMMER'S GUIDE FOR CONTROL OF THE qVt MULTICHANNEL ANALYZER

Control of the MCA is achieved through the three DRV11 addressable registers: DRCSR, DRINBUF, and DROUTBUF. Reading from and writing to the registers is accomplished with the RT-11 FORTRAN callable external routines IPEEK and IPOKE.⁴

The mode of the qVt (see Table 2) is set with the IPOKE routine by loading the appropriate decimal equivalent of the control setting of DRCSR bits 0 and 1 in address 167770₈ (see Table 3). To examine the contents of one of the qVt's channels, the appropriate channel number is loaded in the DROUTBUF (address

*The qVt MCA requires a full-scale input of one volt or less.

167772_g) using the IPOKE routine. The contents of that channel can then be read from the DRINBUF (address 167774_g) using the IPEEK routine.

Two FORTRAN subroutines were written as modules of the RTAAP4 program² to control the qVt analyzer. The first, QVTON, resets the contents of all channels to zero and begins acquisition of a fresh spectrum. The second routine, QVTOFF, stops data acquisition and reads 256 channels of data into the memory of the LSI-11. Source code listings of these brief routines are included in Appendix A.

REFERENCES

1. T. B. Gosnell, G. A. Anzelon, G. W. Huckabay, and N. D. Bailey, "Real-Time Computer Analysis for Nuclear Material Detection--Nest-Pantex II Exercise" (U), Lawrence Livermore National Laboratory Rept. COVD-1976 (1980). (SRD)
2. T. B. Gosnell, G. A. Anzelon, and R. D. Myers, "Real-Time Computer Analysis for Nuclear Material Detection--Part 2: The RTAAP4 Computer Program" (U), Lawrence Livermore National Laboratory Rept. COVD-2046 (1980). (U)
3. Digital Equipment Corporation, Microcomputer Interfaces Handbook, Maynard, MA, 1981, pp. 261-281.
4. Digital Equipment Corporation, RT-11 Advanced Programmer's Guide, January 1976, pp. 4-47 to 4-48.
5. MDB Systems Inc., MLSI-KWIIP Programmable Real-Time Clock Instruction Manual, Orange, CA, 1978.

ANNOTATED BIBLIOGRAPHY OF MANUALS FOR THE LSI-11 MICROCOMPUTER
AND THE NUCLEAR DATA ACQUISITION SUBSYSTEM

LSI-11 Microcomputer

Hardware

1. Microcomputers and Memories, Digital Equipment Corporation, Maynard, MA, 1981. This manual describes all the processors and memories in the DEC LSI-11 family of products. Specifically, one can find detailed information on the LSI-11 bus and the LSI-11 processor.
2. Microcomputer Interfaces Handbook, Digital Equipment Corporation, Maynard, MA, 1981. This manual gives a detailed description of the DEC LSI-11 family of bus interface products. Of interest to readers of this report is the description of the DRV11 parallel line unit. Other interfaces used in the real-time system that are also described in this manual are the DLV11 serial line unit (video terminal interface) and the REV11-A RAM refresh, bootstrap ROM and bus terminator.

Software

3. PDP-11 FORTRAN Language Reference Manual, Digital Equipment Corporation, Maynard, MA, 1977. This document describes the FORTRAN IV language elements as implemented on the LSI-11 microcomputer.
4. RT-11/RSTS/E FORTRAN IV User's Guide, Digital Equipment Corporation, Maynard, MA, 1977. This document describes the operating procedures for the FORTRAN IV compiler for the RT-11 operating system and provides the information required to run a FORTRAN IV program under the operating system.
5. RT-11 Advanced Programmer's Guide, Digital Equipment Corporation, Maynard, MA, 1976. This manual provides information on useful external routines accessible from FORTRAN and assembly language programs.

Nuclear Data Acquisition Subsystem

6. NIM Model 3001 qVt Multichannel Analyzer, LeCroy Research Systems Corp., Spring Valley, NY. this manual contains detailed operating and maintenance information for the qVt MCA.
7. NIM Model 3157 Printer and Display Interface for qVt Multichannel Analyzer, LeCroy Research Systems Corp., Spring Valley, NY, 1977. This is an operating and maintenance manual for the qVt printer and display interface.
8. Miniature Digital Panel Printer, Model DPP-Q7, Datel Systems Inc., Mansfield, MA, 1978. This is a technical description of the six-column line printer used in conjunction with the qVt printer and display interface.
9. 604A Monitor with Options Instruction Manual, Tektronix, Inc., Beaverton, OR, 1978. This document is an operating and maintenance manual for a monitor display oscilloscope suitable for display of the contents of the qVt MCA memory.

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FORTRAN IV

RTAP4

0001

SUBROUTINE QVT0N

Author: Thomas B. Cosnell

Date: 18-Jun-80

Updated: 22-Aug-80

Purpose:

To clear memory and subsequently acquire a fresh
256-channel spectrum using a Lecroy "QVT" multi-channel
analyzer. Communication between the analyzer and the LSI-11
is via Ron Wood's Nuclear Instrumentation Interface and a
standard DPM1 general purpose parallel interface.

Type Declarations

INTEGER CSRADR, MEMADR, RESET, START

0002

Other Specification Statements

Constants for interface control

DATA CSRADR /167770/, MEMADR /167772/, RESET /1/, START /2/

0003

FORTRAN IV

VO2.5

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```

C
C
C *****
C ***** Definition of Identifiers *****
C *****
C
C Identifier  Type      Definition
C =====
C CSRADR      INTEGER    DPV11 contro /status register (CSR)
C                      address
C MEMADR      INTEGER    Address of DPV11 output buffer
C                      :DROUTBUF1. This buffer contains the
C                      qVt channel number
C RESET       INTEGER    Encodes CSR for clearing the analyzer
C START       INTEGER    Encodes CSR for acquisition of data
C =====
C *****
C ***** Executable Statements *****
C *****
C
C Clear analyzer memory
C =====
C
C Start at channel zero -----
0004 CALL IPOKE (MEMADR, 0)
C
C Clear (reset) memory -----
0005 CALL IPOKE (CSRADR, RESET)
C
C   While away about 100 msec to allow completion of reset -----
0006 DO 10 I = 1, 3000
0007 10 CONTINUE
C
C
C Start spectrum acquisition
C =====
C
0008 CALL IPOKE (CSRADR, START)
C
C
0009 RETURN
C
0 END

```

```

=====
RTAPPA
=====
SUBROUTINE DVI0FF
*****
Author: Thomas B. Gourel
Date: 18-Jun-80
Update: 21-Jul-80

Purpose:
To stop data acquisition and read out a 256-channel spectrum
from a Lecroy "QVt" multichannel analyzer. Communication
between the analyzer and the LSI-11 is via Rom word 5
Nuclear Instrumentation Interface and a standard DVI11
general purpose parallel interface.
=====
Type Declarations
*****
INTEGER CHANNEL, CSRADR, DATADP, MEMADR, FEED, SPCTRM, STOP
=====
***** Other Specifications *****
*****
COMMON /SORCE / SPCTRM(256)
DATA CSRADR /'167720/, DATADR /'167724/, MEMADR /'167722/,
* REED /3/, STOP /0/
=====

```

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```

C ***** Definition of Identifiers *****
C ****
C Identifier Type Definition
C =====
C CHANEL INTEGER Spectrum channel number (1-256)
C CSPADR INTEGER Address of DRV11 parallel interface control/status register (CSR)
C DATADR INTEGER Address of DRV11 data input register
C MEMADR INTEGER Address of DRV11 memory address register (contains channel number)
C REED INTEGER Encodes CSR for reading analyzer memory
C SPCTRM INTEGER Spectrum (256-channel array)
C STOP INTEGER Encodes CSR to stop analyzer
C =====
C ***** Executable Statements *****
C ****
C Stop the analyzer and read enable it
C =====
0005 CALL IPOKE (CSRADR, STOP)
0006 CALL IPOKE (CSRADR, REED)
C
C Read out the spectrum
C =====
0007 CHANEL = 0 ! For 8-bit (256-channel) reso-
! lution, the two least signif-
0008 DO 10 I = 1, 256 ! icant of the qVt's 10-bits are
0009 CALL IPOKE (MEMADR, CHANEL) ! dropped. Thus a 256-channel
0010 SPCTRM(I) = IPEEK(DATADR) ! spectrum is stored in every
0011 CHANEL = CHANEL + 4 ! fourth memory location in the
0012 10 CONTINUE ! analyzer.
C
0013 RETURN
0014 END
```

APPENDIX B

ENGINEERING DRAWINGS

NUCLEAR INSTRUMENTATION INTERFACE SCHEMATIC DIAGRAM

Fig. B1. Nuclear instrumentation interface schematic diagram (sheet 1 of 2)

Fig. B1. Nuclear instrumentation interface schematic diagram (sheet 2 of 2).

Fig. B2. Interconnection diagram.

NUCLEAR INSTRUMENTATION INTERFACE ASSEMBLY DRAWING

CIRCUIT BOARD ARTWORK

Fig. B4. Interface control board (sheet 1 of 4).

0	SEE SH 1						
REV	ZONE	DESCRIPTION (SEE REVISION SHEET FOR HISTORY)	DATE	DRAWN	APPROVED		
TITLE PRINTED BOARD - INTERFACE CONTROL LECROY / LSI-11 CONTROL							
ORIGINATOR LAWRENCE LIVERMORE LABORATORY ELECTRONICS ENGINEERING DEPARTMENT University of California, Livermore, California			GROUP LEA	BASIC PACKAGE NO. 80-1644	BUS 64	TYPE E	REV 0
CHECKED DATE			SCALE 2/1 TR 1/1 SHEET 2 of 4				
APPROVED DATE							

Fig. B4. Interface control board (sheet 2 of 4).

0	SEE SH 1					
REV	ZONE	DESCRIPTION (SEE REVISION SHEET FOR HISTORY)	DATE	DRAWN	APPROVED	
TITLE PRINTED BOARD - INTERFACE CONTROL LECROY / LSI-11 INTERFACE						
DESIGNED BY	DATE	LAWRENCE LIVERMORE LABORATORY ELECTRONICS ENGINEERING DEPARTMENT University of California / Livermore, California		GROUP	BASIC PACKAGE NO.	SUB TYPE REV
DRAWN	DATE			LEA	80-1644	64-E 0
CHECKED	DATE			SCALE 2/1 TRUE SHEET 3 OF 4		
APPROVED	DATE					

Fig. B4. Interface control board (sheet 3 of 4).

NOT TO SCALE

DO NOT USE AS DRILL TEMPLATE

ALL HOLES TO BE PLATED THRU
UNLESS OTHERWISE SPECIFIED
ALL HOLES TO BE .91
BASE MATERIAL DESCRIPTION
LED21895 GE-1.53-35/35-NAT
GENERAL PRODUCTION SPECIFICATION
PER LED21874
FAB ASSEMBLY REMARKS

DESIG	HOLE SIZE	QUAN	FAB ASSEMBLY REMARKS
A		A	
B		B	
C		C	
D		D	
E		E	
F		F	
H		H	
J		J	
K		K	

FABRICATION INFO

0	SEE SH 1				
REV	ZONE	DESCRIPTION (SEE REVISION SHEET FOR HISTORY)	DATE	DRAWN	APPROVED
<p>PRINTED BOARD- INTERFACE CONTROL LEAD 80/LSI-11 INTERFACE</p>					
<p>LAWRENCE LIVERMORE LABORATORY ELECTRONICS ENGINEERING DEPARTMENT University of California, Livermore, California</p>		<p>GROUP BASIC PACKAGE NO LEA 80-1644</p>	<p>SUB TYPE REV 64-E D</p>	<p>SCALE 2/1 TRUE SHEET 4 OF 4</p>	

Fig. B4. Interface control board (sheet 4 of 4).

Fig. B5. Input buffer board (sheet 1 of 3).

0	1st	SEE SHT 1			
REV / ZONE	DESCRIPTION	DATE	DESIGN	APPROVED	
TITLE PRINTED BOARD INPUT BUFFER LECROY/LSI-11 INTERFACE					
DESIGNED BY ERD/Z R. MOOD DATE 3/70	GROUP BASIC PROGRAMS LEA 80-1644	SIZE 24	TYPE E	REV 0	SCALE 2/1 TRUE
UNIVERSITY MICROFILMS INTERNATIONAL ELECTRONIC INFORMATION CENTER University of California, Los Angeles, California					

Fig. B5. Input buffer board (sheet 2 of 3).

SOLDER SIDE SHOWN

ALL DIMENSIONS IN MILLIMETERS
FABRICATION INFO

Doc No	ERD/7	FILE	PRINTED BOARD INPUT BUFFER, LECR07/LSI II INTERFACE	GROUP	BASIC	INCHARGE	NO	SUB	TYPE	DATE
PROJECTED BY	WOOD	DATE		EA	80	1544	24	4	E	
DESIGNED BY	W	DATE		SCALE	1:1					
IN CHARGE		DATE		LAWRENCE LIVERMORE LABORATORY ELECTRONIC ENGINEERING DEPARTMENT LIVERMORE, CALIFORNIA, CALIFORNIA, CALIFORNIA						
				SHEET 3 OF 3						

Fig. B5. Input buffer board (sheet 3 of 3).

Fig. B6. Logic control board (sheet 1 of 3).

Fig. B6. Logic control board (sheet 2 of 3).

RELEASED PER J/O 900944 DATE 10/1/80 BY [Signature]		E.P. [Signature] DATE 10/1/80 BY [Signature]	
TITLE PRINTED BOARD BUS BUFFER, LECROY/LSI-11 INTERFACE		GROUP BASIC PACKAGE NO. LEA 80-1644	
UNIVERSITY MICROFILMS INTERNATIONAL ELECTRONICS ENGINEERING DEPARTMENT University of California, Los Angeles, California		SUB TYPE REV 34 -E-B	
SCALE 2:1 TRUE		SHEET 1 OF 3	

Fig. B7. Bus buffer board (sheet 1 of 3).

ALL DIMENSIONS IN MILLIMETRES

DESIGNED ERD/Z CHECKED R. WOOD DATE DRAWN DATE DATE		SEE SHT 1 REV. ZONE DESCRIPTION PRINTED BOARD- BUS BUFFER, LECHROY/LSI-11 INTERFACE LANCELOTTS UNIVERSITY LABORATORY ELECTRONICS ENGINEERING DEPARTMENT University of California, La Jolla, California		DATE SEARCH APPROVED
GROUP BASIC PACKAGE NO. SUB TYPE REV.		SCALE 2:1 TRUE SHEET 2 OF 3		

Fig. B7. Bus buffer board (sheet 2 of 3).

NOT TO SCALE
DO NOT USE AS DRILL TEMPLATE

ALL HOLES TO BE PLATED THRU UNLESS OTHERWISE SPECIFIED
ALL HOLES TO BE .75

BASE MATERIAL DESCRIPTION
LEADWIS GF-1153-35/55-NAT
GENERAL PRODUCTION SPECIFICATION
PER LE021816

DRILLING	HOLE SIZE	QUANTITY	PAD ASSEMBLY REMARKS
A	2.55	1	A
B	3.20	1	B
C			C
D			D
E			E
F			F
G			G
H			H
I			I
J			J
K			K

ALL DIMENSIONS IN MILLIMETRES
FABRICATION INFO

REV	DATE	BY	DESCRIPTION	DATE	BY	DESCRIPTION
0	10/23	SEE SH 1				
<p>PRINTED BOARD - BUS BUFFER, LE020V/LSI-11 INTERFACE</p>						
<p>LEADWIS LAMINATE LABORATORY ELECTRONIC ENGINEERING DEPARTMENT University of California, Los Angeles, California</p>				<p>LEA 60-1644 34-E #</p>		

SCALE 2:1 SHEET 3 OF 3

Fig. B7. Bus buffer board (sheet 3 of 3).

REVISED PER J10 901579		DATE		APPROVED	
PRINTED BOARD CONTROL LOGIC INTERFACE CONNECTOR BOARD LECROY / LSI-11 INTERFACE					
LANCELOT ENGINEERING LABORATORY ELECTRONICS ENGINEERING DEPARTMENT University of California, Los Angeles, California		GROUP BASIC PACKAGE NO. LEA 80-1644		SCALE 2/1 TRUE	

Fig. B8. Connector board (sheet 1 of 4).

DATE	10-2	REV	1	SEE SHEET	12-84	DATE	10-84	DESIGN	APPROVED
PROJECT	10-2	PRINTED BOARD	CONTROL LOGIC INTERFACE CONNECTOR BOARD	LIBRARY / LIST INTERFACE					
DESIGNER	DAVE	10-2	10-2	10-2	10-2	10-2	10-2	10-2	10-2
CHECKED	DAVE	10-2	10-2	10-2	10-2	10-2	10-2	10-2	10-2
APPROVED	DAVE	10-2	10-2	10-2	10-2	10-2	10-2	10-2	10-2
LAWRENCE LIVINGSTON LABORATORY					SCALE 2/1 TRUE				
ELECTRONIC ENGINEERING DEPARTMENT					SHEET 2 OF 4				
UNIVERSITY OF CALIFORNIA, SAN DIEGO									

Fig. B8. Connector board (sheet 2 of 4).

A		SEE SHEET 1		15.84			
REV	DATE	BY	DESCRIPTION (SEE REVISION SHEET FOR HISTORY)	DATE	DRAWN	APPROVED	
<p>PRINTED BOARD CONTROL LOGIC INTERFACE CONNECTOR BOARD LEADY / LSI 11 INTERFACE</p>							
<p>DESIGNED BY: H. BODD CHECKED BY: C. WISSELL DATE: 5.80 APPROVED BY: [Signature] DATE: 6.80</p>				<p>LEAD 80-1644 44-F1A SCALE 2/1 TRUE SHEET 3 OF 4</p>			

Fig. B8. Connector board (sheet 3 of 4).

REV	DATE	DESCRIPTION (SEE REVISION SHEET FOR HISTORY)	DATE	DRAWN	APPROVED
1	11-11-60	PRINTED BOARD CONTROL LOGIC INTERFACE CONNECTOR BOARD LEADERS 11-11-60 35-35-547			
DRAWN BY: DATE: 11-11-60 CHECKED BY: DATE: 11-11-60 APPROVED BY: DATE:			GROUP: 11-11-60 BASIC PACKAGE NO: 11-11-60 SUB. TYPE: 11-11-60 SCALE: 2/1 TRUE SHEET 4 OF 4		

Fig. B8. Connector board (sheet 4 of 4).

Fig. B9. Mother board (sheet 1 of 4).

Fig. B9. Mother board (sheet 2 of 4).

REDUCE TO 127 DQ = 0.05 MM
ALL DIMENSIONS IN MILLIMETRES

REDUCE TO 15240 : 35 MI

D <u>4</u> <u>th</u> SEE SHEET 1		J 30 <u>10/10</u>	
NEW <u>1</u> <u>th</u> DESCRIPTION SEE REVISION SHEET FOR HISTORY		C-2 <u>10</u> <u>10/10</u> APPROVED	
TITLE PRINTED BOARD CONTROL LOGIC INTERFACE MOTHER BOARD LECROY / LSI-11			
SAN RAFAEL ERD / Z DESIGNER DATE 10/10/78 CHECKED BY R. RUSSELL 5.80 DATE 10/10/78 APPROVED BY DATE 10/10/78		UNIVERSITY MICROFILMS INTERNATIONAL ELECTRONICS ENGINEERING DEPARTMENT 300 N. ZEEB RD. ANN ARBOR MI 48106 GROUP BASIC PROGRAM NO. 16A00 - 1644 SUB TYPE NO. 54 - E SCALE 2/1 TRUE SHEET 3 OF 4	

Fig. B9. Mother board (sheet 3 of 4).

DATE	5-11-61	BY	W. WOOD
DESCRIPTION	PRINTED BOARD CONTROL LOGIC INTERFACE MOTHER BOARD LEADFORM / 151 11		
DESIGNED BY	C. RUSSELL	DATE	5-11-61
CHECKED BY	W. WOOD	DATE	5-11-61
APPROVED BY	W. WOOD	DATE	5-11-61
LAURENCE KIRKPATRICK LABORATORY ELECTRONICS ENGINEERING DEPARTMENT Presbyterian University, Lexington, California		GROUP	BASE PROCESS NO. 15A 8C - 1644
		SCALE	2 1/2" IN 1"
		BLK	54 - E-O
		TYPE	REV
		SHEET 4 OF 4	

Fig. B9. Mother board (sheet 4 of 4).

CHASSIS HARDWARE

Fig. B10. Front panel template.

REV		RELEASED PER JUD 256484		9-80	AWC	
REV		DESCRIPTION (SEE REVISION SHEET FOR HISTORY)		DATE	DESIGN	APPROVED
REV		FRONT PANEL SILKSCREEN, FRONT VIEW				
REV		LECROY / LSI-11 INTERFACE				
DESIGNER		GROUP		SILK PROGRAM NO.	SILK TYPE	REV
RON WOOD		LEA		80-1644	06	F 0
DATE		SILK PROGRAM DEPARTMENT		SCALE TRUE 1:1 SHEET 1 OF 2		
C. RUSSELL 4-80		SILK PROGRAM DEPARTMENT				
DATE		SILK PROGRAM DEPARTMENT				
APPROVED		SILK PROGRAM DEPARTMENT				
DATE		SILK PROGRAM DEPARTMENT				

Fig. B11. Front panel silkscreen (sheet 1 of 2).

J22 J18 J14 J10
J23 J19 J15 J11
J24 J20 J16 J12
J25 J21 J17 J13
J26

REV		DATE		DESCRIPTION AND REVISION SHEET FOR HISTORY		DATE	Drawn	Approved
1				FRONT PANEL SILKSCREEN INSIDE VIEW LECROY / LSI-11 INTERFACE				
DESIGNED BY		DATE		GROUP		BASIC PACKAGE NO.		REV
RON WOOD		4-80		LEA		80-1644		06
CHECKED BY		DATE		ELECTRONICS ENGINEERING DEPARTMENT		SCALE TRUE 1:1		SHEET 2 OF 2
C RUSSELL				University of California, Los Angeles, California				
APPROVED		DATE						

Fig. B11. Front panel silkscreen (sheet 2 of 2).

REAR VIEW

ALL CENTERS ☒ 000 DIA. ☐

REF. LBL DNG. NO. TX9053M-23. STORES STOCK 5975-47952

REF. USASI Y-14.5 AND LED 71-9314-02

REF LED T1-9018 COMPONENT PLACING CONFIGURATIONS

SIZE	DEPTH	QTY	DESCRIPTION
1/2	1/2	2	312 X 2.000 CUTOUT
1/2	1/2	2	125 X 3.000 CUTOUT
1/2	1/2	7	
1/2	1/2	4	4-40 UNC 2B THREAD THRU

LEASO-1644 02 TEMPLATE REAR PANEL, REAR VIEW.

A	RELEASED PER JPD 2564684	01/80	REAL	
B	RELEASED PER JPD 2564684	0-00	201	
FILE # (ONE OR MORE NUMBERS AND/OR LETTERS FOR HISTORY)		DATE	CLASS	APPROVED
REAR PANEL TEMPLATE REAR VIEW LECROY / LSI 11 INTERFACE				
SEARCHED INDEXED SERIALIZED FILED	JAN 17 1980 FBI - LOS ANGELES RUSSELL 9 30 DATE	RECEIVED JAN 18 1980 FBI - LOS ANGELES SCALE 1 DATE	BASIC PACKAGE SET 07-1-80 10-1-80 11-1-80	SIGNATURE [Signature] [Signature] [Signature]

Fig. B12. Rear panel template.

5.000 ± 0.0

J3

VD

SYMBOL		2		RELEASED PER J10 256684		F-00		DATE		APPROVED	
DESCRIPTION		ROM #300		REAR PANEL SILKSCREEN INSIDE VIEW		LEAD-1844 DESH-2, REAR PANEL SILKSCREEN REAR VIEW		COLOR WHITE			
DESIGNER		C. RUSSELL		DATE		4-80		SCALE		TRUE 1:1	
APPROVED		DATE		ELECTRONIC ENGINEERING DEPARTMENT		UNIVERSITY OF CALIFORNIA, LA JOLLA		SCALE		TRUE 1:1	
				LEA 80-1644		08-F-1		SHEET 2 OF 2			

Fig. B13. Rear panel silkscreen (sheet 2 of 2).

DO NOT SCALE THIS DRAWING				REV 1000 REVISION 256684				DATE 5-80		DRAWN ONE		APPROVED	
MATERIAL		UNLESS OTHERWISE SPECIFIED		DIMENSIONS		TOLERANCES		TITLE		GROUP/DATE/PAGE/NO		REV	
ALUMINUM 6061-T6 7535-11497		DIM ARE IN INCHES 3 PLACE DEC 3 PLACE DEC ANGLES 2.00 1.00 30° 30°		DIMENSIONS K MODE		DATE		FRAME MOUNTING BRACKET LEROY / LSI-11 INTERFACE		LEA 89-1644		09-A	
FINISH ALUMINE		DIMENSIONS AND TOLERANCES PER USAS 1 Y18 POSITIONAL AND FORM TOLERANCING APPLY AT RFS		DRAWN C. EYSSSEL 5-80		DATE		LAWRENCE LIVERMORE LABORATORY ELECTRONICS ENGINEERING DEPARTMENT University of California, Livermore, California		SCALE 1:1		SHEET 1 OF 1	
SURFACE TREATMENT PER SPEC LEAD 801 TYPE 2		SURFACE TREATMENT PER USAS 8461 MACHINE PER SPEC LEAD 801		CHECKED		DATE							
PAINT PER SPEC LEAD 802 COLOR		SHEET METAL PER SPEC LEAD 802		APPROVED		DATE							

Fig. B14. Frame mounting bracket.

DO NOT SCALE THIS DRAWING

MATERIAL 1/8" THK. PLAIN GLASS SPECT. PER. TRAN. RESIST PER. SPEC. LEST-1092 2550-48787		UNLESS OTHERWISE SPECIFIED DIM. ARE IN INCHES TOL. NO 3 PLACE DEC 3 PLACE DEC ANGLES 2.00 .010 3/4" 3/16"		ENVIRONMENT Z OPERATOR JIN HOGG		REV ZONE DESCRIPTION DATE DRAWN APPROVED	
COATING SURFACE TREATMENT PER SPEC LEST-1092 TYPE		DIMENSIONS AND TOLERANCING PER USAS 1145 POSITIONAL AND FORM TOLERANCING APPLY AT RPS		DRAWN DATE R. RUSSELL 7-80		TYPE CLI CARD SPACER MTS SKT LECROY / LSI 11 INTERFACE	
PAINT PER SPEC LEST-1092 COLOR		SURFACE FEATURE PER USAS 8481 MACHINE PER. SPEC LEST-1092 SHEET METAL PER. SPEC LEST-1092		APPROVED DATE		UNIVERSITY MICROFILMS INTERNATIONAL ELECTRONIC ENGINEERING DEPARTMENT University of California, Los Angeles, California	
				WORKING PLANS PACKAGE NO. LEA 80-1644		REV TYPE REV 10-F-0	
				SCALE 4X1		SHEET 1 OF 1	

Fig. B15. CLI card spacer mounting bracket.

LEA 80-1644 63-P Rev. 0

Interface Control Board

Component designation	Quantity required	Description
<u>Capacitors</u>		
C1	1	15 μ f, 20V, tant
C2	1	0.1 μ f, 50V, cerm, CK05 CK0513X104K
<u>Integrated Circuits</u>		
U1	1	SNLS32N, 2-input OR gate
U2	1	SN74LS00N, quad 2-input NAND gate
U3	1	SNLS04N, hex inverter
<u>Drawing List</u>		
LEA80-1644-61	Ref	Schematic diagram
-63	Ref	Parts list
-64	Ref	Printed board

LEA 80-1644 23-P Rev. 0Input Buffer Board

Component designation	Quantity required	Description
<u>Capacitors</u>		
C1	1	10 μ F, $\pm$ 10%, 20V, tant
C2	1	.1 μ F, $\pm$ 10%, 50V, cerm
<u>Integrated Circuits</u>		
1C1 & 1C2	2	74LS08, quad 2-input AND gate
1C3 through 1C6	4	74LS74, dual D-type, flip-flop
1C7	1	9318PC, 8-input priority encoder
<u>Resistors</u>		
R1 through R8	8	47 Ω , $\pm$ 5%, 1/4 W
<u>Drawing List</u>		
LEA80-1644-21	Ref	Schematic
-23	Ref	Parts list
-24	1	Printed board

LEA 80-1644 13-P Rev. 0

Logic Control Board

Component designation	Quantity required	Description
<u>Capacitors</u>		
C1	1	10 μ f, $\pm 10\%$, 20V, tant
C2	1	.1 μ f, $\pm 10\%$, 50V, cerm
C3 through C7	5	100pf, $\pm 10\%$ 200V, cerm
C8	1	1000pf, $\pm 10\%$ 200V, cerm
<u>Integrated Circuits</u>		
1C1	1	74LS00, quad 2-input NAND gate
1C2	1	74LS27, triple 3-input NOR gate
1C3	1	7440N, dual 4-input NAND buffer
1C4-1C6	3	74LS221, dual monostable multivibrator
<u>Resistors</u>		
R1	1	1K, $\pm 5\%$ 1/4 W
R2, R3, R5, R6, & R7	5	6.8K, $\pm 5\%$ 1/4 W
R4 & R8	2	10K, $\pm 5\%$ 1/4 W
<u>Drawing List</u>		
LEA80-1644-11	Ref	Schematic
-13	Ref	Parts list
-14	1	Printed board

LEA 80-1644 33-P Rev. 0

Bus Buffer Board

Component designation	Quantity required	Description
<u>Capacitors</u>		
C1	1	10 μ f $\pm$ 10%, 20V, tant
C2	1	.1 μ f $\pm$ 10%, 50V, ceram
<u>Integrated Circuits</u>		
IC1 through IC4	4	74LS126, quad tri-state bus buffer high-true enable
<u>Hardware</u>		
	1	Handle, control logic #183-163
	1	Screw, self-tapping, 3/8 x #4-40, black anodize
	1	Screw, gold ground CL1 #183-050
<u>Drawing List</u>		
LEA80-1644-31	Ref	Schematic
-33	Ref	Parts list
-34	1	Printed board

LEA 80-1644 03-P Rev. AChassis Assembly

Component designation	Quantity required	Description
<u>Connectors</u>		
XA1, XA2, & XA3	3	P.C. edge, 44 contacts pierce tail
XA4 & XA5	2	P.C. edge, 22 contacts pierce tail
J9	1	41 position, NIM module-mounted male
	3	Corner guide pin
	3	Corner guide socket
	1	Ground guide pin
	1	Ground guide socket
	1	Hood
	2	Pin, single wire
J10 through J26	17	Coaxial, BNC, jack receptacle pressurized No. UG657A/U
M1	1	Meter, 0-100 μ A 1800 Ω
VR1	1	Voltage regulator LM340T5
<u>Chassis Hardware</u>		
	1	NIM module, 8 3/4 triple wide
	1	Card frame assy 8 connector P/N P/N CFW-508
	2	End block

Misc. Hdw.

6	Screws, #4-40 x 1" long, binder HD., steel cad. plate
2	Screws, #4-40 x 5/8" long, binder hd., steel cad. plate
6	Standoffs, alum. 1/4" x F/=6
12	Spacers, nylon
6	Lock washers, split helical ring, steel, cad. plate, class A style 2, per spec. C-FF-W-84
6	Nuts, #4-40 steel cad. plate assembled washer, UNC/UNF, class B, per MEL-503600

Drawing List

LEA80-1644-01	Ref	Interconnection schematic
-03	Ref	Parts list
-05	1	Front panel template
-06	Ref	Front panel silkscreen (front view & inside view)
-07	1	Rear panel template
-08	Ref	Rear panel silkscreen (rear view & inside view)
-09	2	Card frame mtg. bracket
-10	2	CLI card spacer mtg. bkt.
-11	1	Control board (A3)
-13	Ref	Parts list, control board
-21	2	Input buffer board (A4 & A5)
-23	Ref	Parts list, input buffer board)
-31	2	Bus buffer board (A1 & A2)

-33	Ref	Parts list bus buffer board
-41	Ref	Logic interface connector board (refer to -01 schematic) (A7 & A8)
	Ref	(A3 refer to 03 parts list)
-44	2	P.C. art work, logic interface connector board
-51	Ref.	Logic interface mother board (refer to -01 schematic) (A6)
	Ref	(53 refer to -03 parts list)
-54	1	P.C. art work logic interface mother board equip