191 8/13/80 T.S.
LA-8255

Dn. 1629

MASTER

FPS Camera Sync and Reset Chassis

University of California

LOS ALAMOS SCIENTIFIC LABORATORY

Post Office Box 1663 Los Alamos, New Mexico 87545

FPS CAMERA SYNC AND RESET CHASSIS

by

George J. Yates

ABSTRACT

The sync and reset chassis provides all the circuitry required to synchronize an event to be studied, a remote free-running FPS data-acquisition TV camera, and a video signal recording system. The functions, design, and operation of this chassis are described in detail.

I. INTRODUCTION

The neutron TV pinex (for pinhole experiment) is a standard technique for analysis of underground nuclear weapons tests. Neutrons produced by the nuclear reactions are imaged through a pinhole onto a suitable scintillator that is viewed by data-acquisition TV cameras located downhole near the weapon. The cameras record a single field of data during the test. FPS cameras¹⁻⁷ (so called because focus projection and scanning are contained within the same vidicon element) were originally developed for use in such experiments. These cameras have features different from those of the TV cameras used previously,⁸ among the more notable being resettable sweeps, short field and line periods, high bandwidth, and large video output amplitude. These special features necessitated the development of a new system for recording the video output signals. One component of the new system is a sync and reset chassis, which synchronizes the FPS camera with the event to be viewed and the recording system with the FPS camera.

II. TV CAMERA-EVENT SYNCHRONIZATION

In some experiments, the data is collected by both FPS and non-FPS TV cameras. Because the non-

FPS cameras (usually 8-ms field-period cameras with magnetically focused and deflected vidicons) are difficult to reset at will, a circuit was designed to synchronize the event with the vertical sync interval of the non-FPS camera. This circuit is shown in the timing block diagram, Fig. 1. Composite video signals from two (for redundancy) non-FPS cameras are applied to sync strippers that remove the video information while retaining the sync waveforms. The sync waveforms enter the video coincidence trigger unit (VCTU) where they are ORed and applied to a cancelling circuit that selects every fourth vertical sync pulse. The wavetrain is amplified and transformer-coupled to produce a large amplitude (+60 V) 32-n.s.-period wavetrain (TV sync train). The TV sync train enters the timing and firing (T&F) circuitry where it is ANDed with a relay that is closed 200 ms after the countdown sequence's zero time, some 40 to 50 μ s before the event. The first TV sync train pulse to arrive after relay closure triggers the event, which in turn produces the fiducial signal (FIDU). Thus the event and FIDU are synchronized with the non-FPS camera's vertical sync interval. The FPS camera is synchronized with the event by FIDU through the reset-erase generator of the sync and reset chassis (see Sec. V).

With minor adjustments, this circuit can be used to synchronize the event with the TV camera when only FPS cameras are used (see Sec. V).

Fig. 1.

Block diagram of timing circuits that synchronize the event and the recorders with the TV cameras for experiments using both FPS and non-FPS cameras.

III. FPS CAMERA VIDEO RECORDING SYSTEM

The FPS camera video signals are recorded by both digital and analog recorders. Fast digitizers in the digital system record the signals in real time and store the digitized data in solid-state memory. The system, developed by EG&G Inc. for Group P-15 of Los Alamos Scientific Laboratory (LASL), is designed around LeCroy Research Systems Corp. digitizers and commercial dynamic memory.

Analog recording is normally provided by three independent systems; on certain occasions, a fourth system is also used.

The primary analog recorders are XY displays (Hewlett Packard Co. 1300 or 1311A CRTs) recorded on 4 by 5 in. Eastman Kodak Co. Royal-X Pan film by shuttered optical cameras. The XY displays are unblanked for a single TV field upon receipt of FIDU; the optical cameras are shuttered 0.5 s before

and after CRT unblanking upon receipt of a -1 s T&F signal.

The FPS camera video signals are also transmitted by microwave to analog disk recorders (Data Disc, Inc. model 6311) that record for a single revolution of the disk upon receipt of FIDU.

Frequently, the video signals are recorded on a laser scanner-film recorder (provided by EG&G Inc.) that records single-field video signals.

The above recording techniques provide intensity-modulated two-dimensional images of the single-field video signals. To see the video signals in conventional amplitude-modulated time-resolved format, the signals are recorded, upon receipt of FIDU, on a dual-channel oscilloscope (Hewlett Packard Co. model 81) at two different sweep speeds.

A typical system for distributing and recording the video signals from an FPS camera is shown in Fig. 2. The FPS camera produces large-amplitude video output signals (typically 10 times larger than

Fig. 2.

Typical FPS camera video signal distribution and recording system. R_1 through R_4 are 25 Ω , R_5 through R_{13} are 16.7 Ω , and R_T is 50 Ω .

conventional TV camera signals) that must be attenuated, rather than amplified, before being channeled to recording media. The distribution system is primarily passive with fan-out provided by commercial power dividers. The three-way dividers are Bishop Instruments, Inc. model 080-101; the two-way dividers are GenRad model 814-TPDL. (Note that the large video output amplitude of an FPS camera makes it possible to avoid the noise and distortion inherent in distribution amplifiers.) The calculated video amplitudes at the recorders and at the sync and reset chassis are also shown in Fig. 2.

IV. FPS CAMERA-RECORDING SYSTEM SYNCHRONIZATION

The sync and reset chassis synchronizes the remote free-running FPS camera with the event to be viewed and with the video signal recorders (other than the analog disk and the oscilloscope). The chassis provides precise reset timing and an erase function for the FPS camera, furnishes timing signals, deflection, and CRT unblanking for the XY displays and the laser scanner-film recorder, and supplies timing signals for the digital recorders. The unit was designed by LASL Group P-15 and fabricated by EG&G Inc. Special Measurements group. A block

diagram of the timing, sweep, and unblanking functions is shown in Fig. 3. The reset and erase functions are described in Sec. V.

The sync and reset chassis provides two sources of timing signals for synchronizing the remote FPS camera and the recorders: (1) a resettable sync generator, identical to the sync generator of the remote FPS camera, that can be reset to within ± 12.5 ns of the time at which the remote FPS camera itself is reset (Sec. IV.A); and (2) a sync-stripper circuit that extracts timing information from the composite video waveform of the FPS camera (Sec. IV.B). Factors influencing the choice of resettable sync generator or sync stripper as the sync source are discussed in Sec. IV.C. Timing signals from either sync source operate the sync, sweep, and unblanking circuits required by the various recorders (Sec. IV.E.).

A. Resettable Sync Generator

The resettable sync generator synchronizes the remote FPS camera and the recorders by synchronizing two independent identical sync generators. (It should be noted that this scheme of synchronizing two independent sync generators accomplishes a task usually performed by much more

Fig. 3.

Block diagram of the timing, sweep, and unblanking functions of the sync and reset chassis.

sophisticated circuitry, such as phase-locked loop systems or regenerating systems.) The two sync generators normally run free and are synchronized only as often as required. They are, of course, synchronized at event time by the concurrent application of FIDU. They can also be repetitively synchronized for static display, which is required, for example, when the camera is being focused.

The resettable sync generator has three distinct sections: (1) a precision delay circuit that provides a time period during which the remote FPS camera and the recorders are inhibited and after which both are reset; (2) a cable-delay compensator that corrects for the difference in times-of-arrival of FIDU at the remote FPS camera and at this sync generator (and hence at the recorders when the resettable sync generator is used as the sync source); and (3) the

sync generator circuits that generate timing pulses for sync, sweep, and unblanking.

1. Precision Delay Circuit. Triggered by FIDU, the precision delay circuit produces a time period, whose duration is accurate to within ± 12.5 ns, during which the FPS camera and the recorders are denied access to the data and after which both are synchronized for the data field that follows immediately. The ± 12.5 ns accuracy is provided by the 25 ns period of a 40 MHz crystal.

The delay period corresponds to an experimentally determined time during which transient disturbances, induced at event time, produce extreme amplitude modulations of the composite video waveform. Figure 4 shows a dry-run waveform and a typical disturbed waveform of the FPS camera. Extraction of useful information from such a disturbed

(a)

(b)

Fig. 4.

FPS camera video waveforms (a) during a dry run and (b) at event time with EMP-induced disturbances.

waveform is difficult. In addition, the disturbed waveform would cause flyback traces across the XY displays that would obviously degrade the data image.

Analysis indicates not only that the modulation affects the entire composite video waveform (rather than the individual sync, pedestal, and video components) but also that the modulation occurs after the components are mixed in the camera control chassis, thus placing the disturbance source outside the camera. It is believed that currents induced in the signal transmission cables by electromagnetic pulses (EMP) produce the disturbances.

Recent experiments show that fiber-optics transmission cables experience substantially less EMP-induced disturbance than do coaxial transmission cables. These experiments are being conducted by LASL Group WX-10* in cooperation with Group P-15.

The precision delay is generated by a circuit, part of the master oscillator circuit of the resettable sync generator shown in Fig. 5, that is effectively a digital oneshot. FIDU enters the master oscillator and, to eliminate false triggering by noise pulses or reflections of FIDU, is ANDed with the output of the oneshot IC-11A that effectively locks out future input pulses for the duration of its oneshot period. The output of IC-6 clears the J-K flip-flop IC-10A and enables the counters IC-2, -3, -4, and -5. When these

counters complete their counting sequence and after the cable delay period is added, to the $\bar{Q}$ output of IC-10A is clocked back to logic ZERO and the counters are disabled. The output of IC-10A thus appears to be a oneshot pulse triggered by FIDU.

The delay period is initiated through IC-11B, which upon receipt of FIDU loads the start coordinate preset by jumper connections on IC-5 or by a front panel switch. The duration of the delay can be varied from 100 to 1600 μ s in 100 μ s increments and is usually 500 μ s.

During the delay period, the FPS camera cathode-blanking circuitry disables the FPS vidicon, thus preventing access to the data just written. At the end of the delay period, the FPS camera sweep circuits are reset so that the next TV field is rastered from top to bottom of the vidicon, providing a line-sequential formatted picture uninterrupted by blanking intervals. Figure 6 shows the response of the sync generator (and of the FPS camera) to FIDU.

The EMP gate in the sync-stripper circuit (see Sec. IV.B) is also disabled during the precision-delay period (and for a period after the end of the precision-delay period by the EMP gate discussed in Sec. IV.B.2), preventing access of the FPS camera composite video signals to the sync-stripping circuitry and thus removing a possible source of error for that sync source. The error can arise because EMP-induced disturbances produce unpredictable

*Ralph Partridge is coordinating the WX-10 effort.

Fig. 5.

Schematic of the master oscillator of the resettable sync generator. The FPS camera contains an identical circuit with the exception of the cable-delay circuitry.

noise in the composite video signals that is difficult if not impossible to distinguish from the legitimate timing information contained in the undisturbed video signal.

2. Cable-Delay Compensator. Propagation delays ($\sim 2-8 \mu\text{s}$) in the long cables connecting the remote FPS camera and the resettable sync generator could produce a phase error between the camera and the XY displays or the laser scanner of $4 \pm 4 \mu\text{s}$, an appreciable fraction of the standard FPS camera scan line duration of $12.5 \mu\text{s}$. This phase error could produce a horizontal blanking bar almost

anywhere along the active portion of the displayed scan lines with the left half of the image (in the vertical plane) to the right of the bar and the right half to the left. Figure 7 illustrates correct phasing and the distortion caused by the phase error. Obviously, such a distorted image would create difficulties in data reduction and interpretation.

To correct for the phase error, a cable-delay trim circuit (IC-3' and others of Fig. 4) adds appropriate delay (again with $\pm 12.5 \text{ ns}$ accuracy) to the precision-delay period. The delay may be varied from 0.4 to $6.4 \mu\text{s}$ in $0.4 \mu\text{s}$ increments by preloading the synchronous counter IC-3' through jumper connections or by a front panel switch.

Fig. 6.

Response of the resettable sync generator to FIDU or other suitable input pulse. The delay period may be varied from 100 to 1600 μ s. The periods indicated for the remainder of the waveform are for the standard FPS camera scan rate.

(a)

(b)

Fig. 7.

Rasters depicting (a) correct phasing between camera and XY display and (b) the phase error caused by signal propagation delay.

The cable-delay trim circuitry of IC-3' allows the precision delay counters to operate (beyond the precision delay period) until the programmed cable delay is generated, after which the precision delay counters and the line and field counters are reset as follows. The carry outputs of IC-5 and IC-3 are logically ANDed by IC-9, inverted by IC-6, and used to clear the J-K flip-flop IC-10B. The $\bar{Q}$ output of IC-10B enables the clear input of counter IC-3', permitting it to be clocked by 400 ns clock pulses. The

IC-3' carry output then clocks the J-K flip-flop, bringing its $\bar{Q}$ back to logic zero and thus disabling the counter. The IC-3' carry output then resets the precision delay counters through IC-9 and the line and field counters through IC-6.

3. Sync Generator Circuits. The sync generator circuits shown in Fig. 8 run from the 40 MHz crystal. The FPS camera's standard horizontal line period of 12.5 μ s (256 active scan lines in an active field period of 3.2 ms) is 500 times the period of the 40 MHz (25 ns) crystal. This horizontal period is achieved using two distinct circuits, the clock frequency selector (IC-7 and -8 of Fig. 5) and the horizontal counter (IC-6, -9, and -10 of Fig. 8). Together, these two circuits constitute a variable-modulus counter that, when configured for the standard FPS camera scan rate, functions as a modulo-500 counter. (A modulo- m counter is a counter that resets after multiples of m .) The clock selector IC-8 selects one output of clock counter IC-7 for a chosen scan rate. For the standard rate, the QB output is selected, which effectively multiplies the 25-ns input crystal frequency by a factor of 4, producing a 100-ns clock period. The counters IC-6 and -10 form a cascaded modulo-125 counter by sensing with summing gate IC-9 the QA (2^0), QC (2^2), and QD (2^3) outputs of IC-6 and the QA (2^4), QB (2^5), and QC (2^6) outputs of IC-10. The binary outputs of these counters are decoded to produce the line-period pulse widths for sync, blanking, and drive.

Fig. 8.

Sync generator schematic. The FPS camera contains an identical circuit.

Counters IC-13 and IC-14 use the line rate as their clock frequency and count 256 lines per video field. The binary outputs of these counters are decoded to produce the field-period timing. These timing relationships are shown in Fig. 9 for the standard FPS camera line and field periods.

Minute differences exist between the crystal frequencies of the two sync generators, one providing sync for the FPS camera and the other for the XY displays. Therefore, the only lines that are locked in phase at both generators are the first horizontal scan lines to be generated after the delay period. All succeeding lines in the XY displays are slightly longer or shorter than those in the camera, thus producing raster skew.

The maximum raster skew is determined as follows. The 40 MHz crystal period is accurate (at

25°C) to within ± 0.000625 ns ($\pm 0.0025\%$) of the basic period of 25 ns. The greatest possible difference between the horizontal line periods of the FPS camera and of the XY displays is calculated by assuming a camera period corresponding to the maximum crystal frequency $[500(25 + 0.000625)$ ns] and an XY display period corresponding to the minimum crystal frequency $[500(25 - 0.000625)$ ns]. This maximum possible difference between the line periods of 0.625 ns and the fact that FPS camera fields contain 256 lines can produce a maximum phase difference of 160 ns between the last scan lines of the camera and of the XY displays. The maximum possible raster skew is thus 1.28% (160 ns $\div$ 12.5 μ s).

This is a negligibly small amount of skew. Skew is, of course, not a problem with the analog disk or the

Fig. 9.

Waveforms of the resettable sync generator. The times indicated are for the standard FPS camera format of 256 12.5- μ s scan lines. The times appropriate to scan rates twice (256 6.25- μ s scan lines), one-half (256 25- μ s scan lines), and one-fourth (256 50- μ s scan lines) the standard are obtained by multiplying the indicated times by 0.5, 2, and 4, respectively.

digital recorders but it is a problem with the laser scanner-film recorder, which also is a rastered system that depends on the timing signals supplied to deflect the laser beam.

Without the high tolerances of this design, the phase differences between the camera and the recorder could produce unacceptable skew in the displayed image as shown in Fig. 10.

B. Sync Stripper

The sync-stripper circuits in the sync and reset chassis are an alternative source of timing signals for synchronizing the remote FPS camera with the recorders by extracting the timing information contained in the FPS camera composite video waveform.

1. Circuits. The sync-stripper circuitry, shown in Fig. 11 and in block diagram form in Fig. 3, consists of four main sections: (1) an input differentiator and a clipper-clamper circuit that condition the composite video waveform; (2) an EMP gate that disconnects the input waveform from the remaining circuits during the EMP-disturbance interval; (3) a sync-stripper circuit that removes the video information from the composite video waveform while retaining the timing information; and (4) a sync-separator circuit that separates the vertical and horizontal components of the composite sync waveform.

a. Input Differentiator. The input RC coupling network functions as a differentiator for the longer period vertical components of the input waveform. Earlier designs used substantially larger RC time constants than those indicated in Fig. 11 to provide

Fig. 10.

Raster depicting skew caused by a difference between the horizontal periods of the FPS camera and the XY display.

effective coupling of the vertical pulse. Such large RC time constants can, however, cause problems when clamp circuits are used and when large transients (such as those shown in Fig. 4) are added to the normal signal.

Q_2 controls the clamp level at which the most negative portion of the input waveform is forced to reside. R_2 sets the reference clamp level; the range of clamp voltages is approximately 0 to +2 V dc. R_1 sets the reference clip level by biasing current source Q_1 . The range of clip voltages is approximately +1.15 to +3.30 V dc. Joint action of the clipper and clamper circuits restricts the input voltage swing to a maximum of ~3.3 V peak-to-peak. To insure that the clipped signal contains the sync component, due care must be taken to attenuate properly (16-40 dB) the large amplitude FPS camera's composite video output.

b. EMP Gate. The EMP gate of Fig. 11 disconnects the input signal from the remaining sync-stripper circuits. The gate, a solid-state relay (Teledyne 640-1), is normally closed but is opened just before the EMP-disturbance interval by FIDU through driver Q_4 for a time (usually ~200-500 μ s) determined by IC-7. When the sync stripper is used as the sync source, this interruption eliminates possible errors in the timing signals during the EMP-disturbance interval. These errors are due to EMP-induced noise in the video signal that, as noted before, is difficult if not impossible to distinguish from the legitimate timing information contained in the undisturbed video signal.

c. Sync Stripper. Q_3 and Q_6 (Fig. 11) of the two-stage network sync-stripper circuit operate as overdriven amplifiers providing saturated logic. The circuit effectively removes the video information from the composite video waveform and supplies logic-level composite sync at the collector of Q_6 .

d. Sync Separator. The sync-separator circuit uses a digital nonintegration scheme to achieve a response time (for vertical sync detection) that is an order of magnitude faster than that of conventional separator circuits. The circuit⁹ separates the composite sync waveform into vertical and horizontal

Fig. 11
Sync-stripper circuits.

components by detecting pulse durations longer than those of horizontal sync pulses.

The composite sync waveform at the input of the sync separator, pin 12 of IC-4 (G_1) in Fig. 11, exhibits a logic ZERO during the horizontal sync intervals, the equalizing pulse intervals, and the serration intervals. The waveform is applied simultaneously to the input of inverter IC-4 and cancel multivibrator IC-2. The period of the cancel multivibrator is set at $\sim 1.0 \mu s$, which is longer than the FPS camera horizontal sync (and equalizing pulse) intervals, but shorter than the vertical sync or serration intervals. The pulse generated at input 2 (pin 9) of G_2 each time the composite sync switches from logic ONE to logic ZERO acts as a cancel pulse that is 180° out of phase with the inverted composite sync pulse at input 1 of G_2 (pin 10). Thus all horizontal sync pulses (and all equalizing pulses, if present*) are cancelled.

However, when the vertical sync interval or the first serration interval is encountered, the cancel pulse cannot cancel it because the duration of these pulses is greater than $1.0 \mu s$. Therefore, at the end of the cancel pulse interval, both inputs of G_2 are at logic ONE and the gate is enabled, thus changing the output of G_2 from logic ONE to logic ZERO. Because this change occurs at a time greater than one horizontal sync pulse duration after the beginning of the first serration, G_2 is called the first serration detector. For sync waveforms without serrations, G_2 is called the vertical sync detector.

To compensate for the time jitter typical of monostable multivibrators, the cancel pulse duration, $\sim 1.0 \mu s$, is made longer than the FPS camera's horizontal sync interval of 200 ns. The cancel pulse duration represents the response time of this sync separator. Its value compares favorably with response times of $\sim 10 \mu s$ obtained with integration methods of vertical sync separation.

The desired vertical sync interval is obtained by applying the output of G_2 to the vertical sync multivibrator IC-3. The period of IC-3 is set to be greater than or equal to two FPS camera line periods.

The horizontal sync multivibrator IC-1 transforms the composite sync into a constant duration pulse train. During sync stripping, the very narrow (200 ns) input pulses are further narrowed by circuit response times. The reconstituted pulse durations

are therefore made longer than the initial pulse widths. These longer pulses also eliminate a problem encountered by the digital recorders, which use digitized samples of the horizontal sync waveform to display reconstructed images. Narrow sync duration allows too few samples for adequate phase control.

2. Noise Immunity. The susceptibility of the sync stripper circuits to EMP-induced disturbances was determined by deliberately introducing transients into the input composite video waveform. Figure 12 shows the response of the sync stripper without the EMP gate to positive and negative transients of various amplitudes and durations. Note that an erroneous horizontal sync pulse is generated when the induced transient swings negative. These erroneous sync pulses are eliminated by the EMP gate as shown in Fig. 13.

The erroneous horizontal sync pulse is caused by the differentiator circuit. The differentiator response is compared with that of a longer RC input network in Fig. 14.

C. Choosing the Sync Source

The sync source is selected through a front panel switch (see Fig. 15) that operates the select lines on a quadruple 2-to-1 selector, IC-5 of Fig. 11. This switch also removes power from the unused source to minimize power consumption and crosstalk between the two sources.

There are good arguments for using either of the two sync sources to operate the recorders. For redundancy, typical experiments use both. Of course, this requires two sync and reset chassis.

Sync stripper sync has no extreme problems resulting from phase delay (such as those described in Sec. IV.A.2) because both the sync and the video information are subject to the same propagation delays. Unavoidable delay (~ 400 ns) in the sync-stripper circuits produce a small amount of phase shift between the video and the separated sync, but these delays are comparable to those of the phase-corrected resettable sync generator circuits. The phase error thus produced merely displaces the displayed video image to the left or right of the horizontal blanking bar and in no other way affects the data.

*The currently used FPS camera has no equalizing pulses or serrations.

Fig. 12.

Response of the sync-stripper circuits without the EMP gate to positive and negative transients of various amplitudes and durations induced in the FPS camera composite video waveforms. The lower trace is the composite video waveform with induced transient (attenuated by 20 dB so that the entire waveform could be displayed on the oscilloscope); the upper trace is the sync-stripper response.

Fig. 13.

Response of the sync-stripper circuits with the EMP gate to positive and negative transients induced in the FPS camera composite video waveforms. The lower trace is the composite video waveform with induced transient (attenuated by 20 dB so that the entire waveform could be displayed on the oscilloscope); the upper trace is the sync-stripper response.

Problems with skew (such as those described in Sec. IV.A.3) do not exist for sync-stripper sync because both the camera and the recorders operate from the same crystal.

In some applications, the resettable sync generator cannot be used as a sync source. As an example, the "homing" sweep generator being developed for the FPS camera precludes the use of predetermined timing formats. Rather, timing formats will be spontaneously dictated. The sync-stripper circuitry is not disturbed by unpredictable formats, as shown by its immunity to noise transients, and should work well in such an application.

The resettable sync generator is, however, a reliable sync source well protected from the hostile environment of the remote FPS camera and is therefore capable of providing immunity to downhole noise sources.

D. Outputs to Recorders

1. Line Drivers. The outputs of the sync and reset chassis, for those functions described in this section, are designed as 50- Ω line drivers. These outputs include composite sync, horizontal and vertical sync, XY display intensity gate timing, EMP gate

timing, and 40 MHz clock pulses. Except for the last, all outputs (and monitor test points) are channeled through the line-driver circuits shown in Fig. 16. The circuits use SN74128 TTL line drivers. Because of speed requirements, the 40 MHz output is channeled through a circuit that uses SN74S140 Schottky line drivers fed by SN74S132 Schmidt triggers.

2. XY Display Drivers. The XY displays require horizontal and vertical deflection and CRT unblanking. These functions are combined in one circuit module containing either a LASL-designed or a commercial sweep generator.

The unblanking circuit is shown in Fig. 17. IC-3 provides delay and width controls for the XY display intensity gates. Upon receipt of FIDU, the multi-vibrators provide a single-field gate pulse for unblanking the CRTs. The XY displays trigger on TTL-level logic pulses.

The LASL-designed sweep generator shown in Fig. 18 is essentially a constant current integrator that is discharged periodically by the horizontal or vertical sync pulses. The two operational amplifiers (Teledyne Philbrick model 1321) are wired as integrators in an identical manner except for the RC

Fig. 14.

Response of the input differentiator to transients induced in the FPS camera composite video waveforms. For transients of short duration, (a) and (b) show the input composite video waveform with induced transients of both polarities, (c) and (d) show the differentiator out-

(g)

(h)

(i)

(j)

(k)

(l)

Fig. 14. (cont)

put, and (e) and (f) show the fully coupled output. For transients of longer duration, (g) and (h) show the input composite video waveform with induced transients of both polarities, (i) and (j) show the differentiator output, and (k) and (l) show the fully coupled output.

Fig. 18.
LASL sweep generator schematic.

Fig. 19.

Celco model 2SG-7 sweep generator schematic, reprinted with permission of Constantine Engineering Laboratories Co.

Fig. 20.

Block diagram and waveform diagrams depicting the reset-erase generator waveforms and resultant FPS camera waveforms.

Fig. 21.

FPS camera reset-erase generator schematic for events that are synchronized by the TV cameras.

Fig. 22.

FPS camera reset-erase generator block diagram for events that are not synchronized by the TV cameras.

REFERENCES

1. G. J. Yates and B. W. Noel, "A 256-line, 2.8-ms Field Duration TV camera," Los Alamos Scientific Laboratory report LA-6407 (November 1976).
2. K. Schlesinger and R. A. Wagner, "A Mixed Field Type of Vidicon," *IEEE Trans. Electron Devices* **ED-14**, 163-170 (1967).
3. K. Schlesinger and R. A. Wagner, "A Mixed-Field Device for Simultaneous Focus and Deflection," *Proc. Electron Laser Beam Symp., Pennsylvania State University, University Park, Pennsylvania, March 31-April 2, 1965* (Electrical Engineering Department, Electron Physics Laboratory, Pennsylvania State University, University Park, PA 16802, 1965) pp. 471-488.
4. I. T. Saldi and K. Schlesinger, "The FPS Vidicon," *Opt. Spectra* **4**, 53-56 (February 1970).
5. D. B. Hunter, "Supertube," *Opt. Spectra* **9**, 39-41 (November 1975).
6. E. F. Ritz, Jr., "A Theory of Static Deflection in Magnetically Immersed Conical Deflectrons," *IEEE Trans. Electron Devices* **ED-23**, 1325-1332 (1976).
7. Bruce W. Noel and George J. Yates, "FPS-Vidicon Television Cameras for Ultrafast-Scan Data Acquisition," Los Alamos Scientific Laboratory report LA-8236 (May 1980).
8. G. J. Yates, "Fast Scan TV System," Los Alamos Scientific Laboratory, unpublished report, 1972.
9. G. J. Yates, "Digital Nonintegration Method Boosts Response Time of Vertical Sync Separator," *Electronic Design* **19**, 156-158 (1972).