DART II DOCUMENTATION
VOLUME III
RADIAN DART MICROCOMPUTER SYSTEM
HARDWARE DOCUMENTATION
OPERATION SYSTEM DESCRIPTION
23 MAY 1979

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1.0 INTRODUCTION

This Maintenance Manual for the DART II Data Acquisition, Reduction, and Transmission system consists of five sections. Following this brief introductory section, Section 2 describes the purpose and capabilities of the various DART II subsystems and a description of the manner in which they are interconnected. Section 2 also provides a brief description of the DART II mechanical and electrical configuration and the functions of the front panel controls, and lists system specifications. Section 3 describes the manner in which the microprocessor-based Central Processing Unit (CPU) communicates with memory and peripheral devices. Section 4 provides detailed theories of operation for the system components. The final section, the Appendices, provides voluminous reference data. That data includes schematic diagrams, cable lists, adjustment and calibration procedures, device specification sheets, etc.

This volume provides only minimal guidance with respect to a software/firmware operating system. The flexible, programmable nature of the DART II design makes it useful for a wide variety of applications. Operation as a "system" is dependent on the application, which will dictate the circuit board configuration, the number and types of peripheral devices, and the software and firmware requirements. Separate software manuals, describing the operating system, are provided for each application.

2.0 SYSTEM CAPABILITIES AND CONFIGURATION

2.1 GENERAL CONFIGURATION AND CAPABILITIES

Figure 2-1 is a block diagram of the standard DART II Configuration. The system is configured around a 6800 microprocessor which communicates with all other system components by means of a 16-bit address bus, an 8-bit data bus, and a number of special control and monitoring buses. The microprocessor unit (MPU) resides on the Central Processing Unit (CPU) circuit board. The CPU board also contains AC power failure detection and auto-restart circuitry, circuitry for the masking of interrupts from peripheral controllers, circuitry for testing the status of peripheral controllers, circuitry for monitoring the status of the memory back-up batteries, and 512 bytes of pre-programmed Read Only Memory.

The standard system is configured with 32K (K = 1024) bytes of 8-bit, random access read/write solid-state memory on two circuit boards. Memory is expandable, in 16K increments, to 64K. Memory is provided with battery back-up power that provides 24 hours of memory retention in the event of AC line power loss. A memory parity option that provides a one-bit parity generation and checking capability for each memory byte is provided on each memory board.

A time-of-day clock with 0.56" seven-segment display of year (2 digits), month, day, hour, minute, and seconds is provided. The clock is set by front panel controls. Each of the time parameters can be read, under program control, by the CPU. The clock is implemented with low-power CMOS logic and is provided with battery back-up that will provide power for a period in excess of 30 days. The clock accuracy is determined by the accuracy of AC line frequency until a power failure occurs; in that event, accuracy is determined by an internal crystal oscillator.

FIGURE 2-1 BLOCK DIAGRAM OF STANDARD DART II CONFIGURATION

RADIAN

Bulk data and program storage is provided by a flexible disk subsystem. The total formatted storage capacity of a single diskette is 240,000 8-bit bytes. The recording format is IBM 3740 - compatible. The software operating system is normally stored on a portion of the system diskette; the operating program is automatically retrieved and initialized by a non-volatile Read Only Memory loader program after a power outage of sufficient duration to deplete the capacity of the RAM back-up batteries. The disk controller can control up to three additional disk drives, available in an optional disk expansion chassis.

Hardware computing capability is provided by an Arithmetic Processing Unit (APU) which performs computation at much higher speeds than can be realized under software control. The APU allows the CPU to perform other tasks while it is performing computation. The APU can perform 16 or 32-bit fixed point computations and 32-bit floating point computations. The unit can perform addition, subtraction, multiplication, division, exponentiation, logarithms, square roots, trigonometric functions, and inverse trigonometric functions.

A real-time clock circuit provides for software selection of interrupt rates of 1 per second, 10 per second, 60 per second, or a rate determined by an external source.

A rainfall counter, which is battery-backed to provide continued operation during AC power failures, counts contact closures. The input to that circuitry is overvoltage protected.

The I/O controller provides digital input/output capability for 32 channels. That circuit board consists of four independent 8-bit channels, each of which may be configured for

either input or output capability. When wired for input capability, the circuits monitor the status of contact closures or logic levels. When wired for output capability, the circuits provide solid-state switch closures for controlling external devices such as lamps or solenoids. For applications which require only input capability, a Status Input Controller, which is plug-compatible with the I/O Controller, can be installed. The number of channels can be expanded to 64 by the installation of a second I/O Controller.

The asynchronous interface board provides two independent serial interface ports for interfacing with peripheral devices such as teleprinters or asynchronous data modems. Each port can be independently configured for 20 ma. current loop capability or for EIA Specification RS-232-C logic levels by means of switches. Each port is provided with the capability to generate standard modem control signals and to monitor standard modem status signals. The number of stop bits (1 or 2), the ability to generate and check a ninth parity bit, and parity mode (even or odd) are also switch-selectable functions. Standard baud rates, also switch selectable for each port, are 110, 150, 300, 600, 1200, 2400, 4800, and 9600. An additional asynchronous board may be optionally installed to provide a total of four asynchronous ports.

The Analog Multiplexer and the Analog-to-Digital Converter (ADC) provides the capability of monitoring 32 differential input analog data channels. Following the differential input multiplexer is a programmable gain amplifier that allows software selection of full-scale ranges of ± 10 mv, ± 100 mv, ± 1 volt, ± 5 volts, and ± 10 volts, with 100% overrange capability on all but the ± 10 volt range. Channel selection and gain selection switches on the front panel allow the operator to monitor any analog channel on the seven-segment front panel voltage display. That

capability does not interfere with the normal CPU channel and gain selection under software control. The multiplexer has an input impedance greater than 10 megohms and each channel is overvoltage protected. An optional multiplexer expansion chassis allows the number of channels to be expanded to 256.

The Device Controller provides software programmable AC power control for the flexible disk drive and a teleprinter--electromechanical devices whose reliability is increased by not operating them for extended periods when not in use. In conjunction with the external Device Controller Panel, an additional 14 devices may be controlled with isolated relay contact closures. Four of the devices may be relatively high power devices with a current demand of 10 amperes at 115 VAC.

2.2 DART II MECHANICAL AND ELECTRICAL CONFIGURATION

The primary DART II mechanical assemblies are the front panel assembly, the rear panel assembly, the power supply assembly, and the main chassis assembly.

The front panel assembly includes all operating controls and indicating devices.

The rear panel assembly includes connectors for all input and output signals and a cooling fan.

The power supply assembly contains all system power supplies, cooling fans, and a power distribution printed circuit board.

The main chassis assembly contains the flexible disk drive, the system batteries, and a printed circuit card cage attached to a mother board printed circuit.

The primary assemblies are interconnected with a system of cables to provide power and signal distribution throughout the system. Drawing 500C3297-001 is an interconnection cabling diagram. Each cable within the system is provided with a "W" number for identification. The drawing indicates each cable number, the connectors or devices to which it attaches, and (either implicitly or explicitly) its function. A complete assembly drawing, including signature and wire lists, for each cable assembly is provided in Appendix G.

With the exceptions of the power supply distribution board, which is a part of the power supply assembly, and the display devices, which are a part of the front panel assembly, all printed circuit boards are mounted within the card cage attached to the mother board. The boards are accessible by removal of the top panel of the main chassis assembly. Each board has color-coded ejectors which match the color of the card guide into which it is inserted. Table 2.1 is a summary of card cage position assignments for the printed circuit boards.

The system address bus, data bus, control bus, and other connections between the various circuit boards are etched on the mother board. A signature list of all signals on the mother board, including each pin of each connector, is provided in drawing 500D-3269-001 (Appendix B).

Assembly numbers for major DART II assemblies are provided in Table 2.2.

Schematic diagrams are presented in Appendix C.

TABLE 2.1 POSITION ASSIGNMENTS FOR CIRCUIT BOARDS FOR THE
DART II CARD CAGE

POSITION	CARD GUIDE COLOR	CIRCUIT BOARD
1 (Front)	Black	CPU
2	Yellow	Memory (16K)
3	Yellow	Memory (16K)
4	Yellow	Memory (16K)
5	Yellow	Memory or ROM/RAM
6	Aqua	APU/RTC/RNF
7	Brown	Battery Clock
8	Green	Flexible Disk Controller
9	Orange	Asynchronous Interface
10	Blue	Device Controller
11	Red	Status Input or I/O Controller
12	Violet	Magnetic Tape Controller
13	White	Spare
14	White	Spare
15	White	Spare
16	White	Spare
17	Lime Green	Analog to Digital Converter
18 (Rear)	Grey	Analog Multiplexer

NOTE: The bus terminator board must be inserted in either
an unused memory position or one of the spare positions.

TABLE 2.2 PART NUMBERS FOR MAJOR DART II ASSEMBLIES

ITEM	PART NO.
PCBA, CPU	782C0300-001
PCBA, Memory, 16K	782C0301-001
PCBA, APU/RTC/RNF	782C0302-001
PCBA, Asynchronous Interface	782C0303-001
PCBA, P/S Distribution	782C0304-001
PCBA, Flexible Disk Controller	782C0306-001
PCBA, Status Input Controller	782C0307-001
PCBA, Device Controller	782C0308-001
PCBA, Battery Clock	782C0310-001
PCBA, Battery Clock Display	782C0311-001
PCBA, ADC	782C0312-001
PCBA, Analog Multiplexer	782C0313-001
PCBA, ADC Display Logic	782C0314-002
PCBA, ADC Display	782B0315-001
PCBA, Mother Board	782D0317-001
PCBA, Magnetic Tape Controller	782C0318-001
PCBA, I/O Controller	782C0319-001
PCBA, Extender	782C0320-001
PCBA, RAM/ROM	782C0321-001
PCBA, Terminator	782C0324-001
PCBA, Analog I/O Strip	782B0325-001
PCBA, Status I/O Strip	782B0326-001
Flexible Disk Drive	BR8A2A
Power Supply Assembly	500D3293-001
Battery, 12V.	500B3402-001
Battery, 2V	0820-0004
Solid State Relay	SA10014110

2.3 FRONT PANEL CONTROLS

This section provides a brief description of the functions of each front-panel control.

POWER

This control turns power on or off to the entire system, by means of a key-actuated switch.

CAUTION

If the AC power is to be deliberately removed from the system for an extended period the system batteries will be completely discharged. To prevent deep discharge of the batteries during periods of non-use:

- a. First, turn off AC power.
- b. Temporarily disconnect P44 and P45 from the power distribution board.
- c. Reconnect P44 and P45.
- d. Do not reapply AC power until the system is to be used again.

FLOPPY DISK

Actuating this illuminated switch will cause AC power to the flexible disk drive to assume its opposite state. For example, if power is off and the switch is not illuminated, depressing the switch will cause power to be applied to the disk drive. Depressing it again will cause power to be removed from the drive.

CAUTION

If the operating program has, by means of the device controller, applied AC power to the disk drive the switch will be illuminated. In this case, do not manually remove power from the drive. If the program is attempting to write a disk record at the time an operator manually removes disk drive power, the soft-sectored diskette may have its sector format destroyed, rendering the diskette useless until re-formatted!

KEYBOARD PRINTER

This switch controls AC power to the Keyboard Printer (TTY) power receptacle on the rear panel assembly. It functions in a manner identical with that of the Floppy Disk power switch.

PROGRAM LOAD

Depressing this switch will cause the software operating system to be loaded from the flexible disk. See Section 4.2 for a detailed discussion.

CHANNEL SELECT

These thumbwheel switches allow the operator to select any analog channel for a display of its voltage value on the VOLTAGE READOUT display. The switches are encoded in octal. In the normal, non-expanded configuration only values from 00_8 to 37_8 will have meaning. Selection of a channel from the front panel has no effect on the operating program.

GAIN SELECT

This rotary switch allows the operator to set the full-scale display range for the channel selected by the Channel Select switches.

BATTERY CLOCK TIME SET SWITCHES

Set Time - This toggle switch must be up to enable the push buttons to set time. It must be down for the clock to run.

Minute - Depressing this pushbutton results in the minutes incrementing twice a second from 0 to 59.

Hour - Depressing this push button results in the hours incrementing twice a second from 0 to 23.

Day - Depressing this push button results in the days incrementing twice a second from 0 to 28, 30, or 31. The upper limit of the days setting is controlled by the month setting.

Month - Depressing this push button results in the months incrementing twice a second from 1 to 12.

2.4 SPECIFICATIONS

The following specifications apply to the standard DART II Configuration:

ANALOG SECTION

1.	Number of Channels:	32
2.	Input Impedance:	Greater than 10 megohms.
3.	Multiplexing:	Two-wire differential inputs with input overvoltage protection.
4.	Analog-to-Digital Converter:	12-bit, 2's complement format with binary to BCD conversion for front panel display.
5.	Resolution:	One part in 4096 at 100% overrange.
6.	Conversion Time:	2 milliseconds per channel, including switching and settling time.
7.	Voltage Ranges:	Software-selectable full-scale ranges of ± 10 mv, ± 100 mv, ± 1 volt, ± 5 volts and ± 10 volts.
8.	Overranging:	100% of full scale on all but the ± 10 volt range.

DIGITAL SECTION

1.	Controlled Devices	
	Number of devices:	16; two reserved for power control of flexible disk drive and teleprinter; four devices at 115 VAC, 10 Amp. maximum; 10 devices with contact closure.

2. Digital I/O

- a. Number of Bits: 32
- b. Function
Configurable in groups of 8 as input channels for monitoring status of contact closures or logic signals.

Configurable in groups of 8 as output channels for providing solid-state switch closures.

MEMORY

- 1. Type: Random Access, solid-state, static.
- 2. Size: 16K to 64K 8-bit bytes in increments of 16K. Top 512 bytes reserved for ROM.
- 3. Battery Backup Capacity: 24 hours for standard 32K system.
- 4. Memory Parity: Parity bit generation, storage, and checking for each byte available as an option.

CLOCK

- 1. Display: 12 digit
Hour (24):MIN:SEC MO/DAY/YEAR
- 2. Accuracy: Synchronized to 60 Hz power when present; otherwise, controlled by 0.01% crystal oscillator.
- 3. Battery Backup Capacity: 30 days.

BULK MEMORY

1. Type: Standard flexible diskette medium.
2. Format: Soft-sectored; IBM 3740-compatible.
3. Storage Capacity: 240,000 formatted 8-bit bytes.

ASYNCHRONOUS INTERFACES

1. Number of Ports: 2
2. Switch-selectable parameters:
 - Number of stop bits (1 or 2).
 - Current loop (20 ma) or RS-232-C.
 - Baud Rate
 - Parity Generation
 - Even/Odd Parity
3. Modem Status Monitored: CTS, RI, CARDET, DSR
4. Modem Control: RTS, DTR
5. Baud Rates: 110, 150, 300, 600, 1200, 2400, 4800, and 9600

HARDWARE COMPUTATION

1. Method: AM9511 Arithmetic Processing Unit.
2. Type: 16 and 32-bit fixed point operations or 32-bit floating operations.
3. Functions: Addition, subtraction, multiplication, division, square roots, logarithms, exponentiation; trigonometric and inverse trigonometric functions; floating point to fixed point and fixed point to floating point conversions.

ENVIRONMENTAL

1. Temperature: 10°C to 40°C
2. Relative Humidity: 8% to 80%, non-condensing

POWER REQUIREMENTS

1. Voltage: 115V AC $\pm 10\%$
2. Current: 5 amperes maximum

DIMENSIONS

1. Height: 12-1/4 in.
2. Width: 19 in., rack-mounted with slides.
3. Depth: 24 in.

3.0 MPU COMMUNICATION WITH MEMORY AND DEVICES

3.1 MEMORY ADDRESSES

DART II can, under program control of the 6800 micro-processor integrated circuit, address $65,536_{10}$ locations. This memory address space is partitioned into three separate areas, each of which is used for a different purpose. The three areas are used for controlling and monitoring the status of peripheral circuits and devices, for storage and retrieval of data and instructions in random access read/write memory (RAM), and for retrieval of pre-programmed data and instruction from "read only memory" (ROM). Each address location in memory space is an eight-bit location.

Table 3.1 defines, in decimal, octal, and hexadecimal notation, the utilization of memory address space.

3.1.1 Control of Peripheral Devices

The first 128_{10} memory space address locations are reserved for the control and monitoring of circuits external to the CPU card. The only method available to the 6800 MPU for communicating with external devices is by means of the system address and data buses. Thus, the MPU must communicate with external devices by considering them to have addresses in memory space.

The first address area is further partitioned into two sections. The first eight locations are used by the MPU to read the interrupt status of 16 devices, disable the interrupt capability of 16 devices, read the "BUSY" status of 16 devices, read the "DONE" status of 16 devices, generate the master reset pulse for the system, read the status of the RAM battery, read

TABLE 3.1. DART II MEMORY ADDRESS SPACE CONFIGURATION

BLOCK	FUNCTION	DECIMAL ADDRESSES	OCTAL ADDRESSES	HEXADECIMAL ADDRESSES
1st 16K	{ Device Codes	0 + 127	000000-000177	0000-007F
	{ RAM	128 + 16,383	000200-037777	0080-3FFF
2nd 16K	RAM	16,384 + 32,767	040000-077777	4000-7FFF
3rd 16K	RAM	32,768 + 49,151	100000-137777	8000-BFFF
4th 16K	{ RAM	49,152 + 65,023	140000-176777	C000-FDFF
	{ ROM	65,024 + 65,535	177000-177777	FE00-FFFF

read the error condition of the optional RAM parity check, and to communicate with the optional portable front panel. The specific manner in which the first eight locations, called CPU function codes, are used is defined by Table 3.2. Each addressable peripheral device is assigned a specific bit on the data bus for all functions controlled or monitored by the function codes. The bits assigned for specific devices are defined in Table 3.3. The device mnemonics used in Table 3.3 are defined by Table 3.4.

TABLE 3.2. DEFINITION OF CPU FUNCTION CODES

ADDRESS	FUNCTION	
000000	Inputs 8 interrupt status bits or masks 8 interrupts	INTA1
000001	Inputs 8 interrupt status bits or masks 8 interrupts	INTA2
000002	Inputs 8 BUSY status bits	BSYCHK1
000003	Inputs 8 BUSY status bits	BSYCHK2
000004	Inputs 8 DONE status bits	DNCHK1
000005	Inputs 8 DONE status bits	DNCHK2
000006	Reads front panel data switches or sets data lights	FPSTRB
000007	I/O RESET - input battery/parity status	IORST

TABLE 3.3 DATA BUS BIT ASSIGNMENTS FOR CPU FUNCTION CODES

MEMORY ADDRESS	FUNCTION	DATA BUS BIT UTILIZATION							
		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	Read	VLP Interrupt Status	APW Interrupt Status	RTC Interrupt Status	ADC Interrupt Status	P20 Interrupt Status	P21 Interrupt Status	P10 Interrupt Status	P11 Interrupt Status
0	Write	VLP Interrupt Mask	APW Interrupt Mask	RTC Interrupt Mask	ADC Interrupt Mask	P20 Interrupt Mask	P21 Interrupt Mask	P10 Interrupt Mask	P11 Interrupt Mask
1	Read		MCT Interrupt Status			P40 Interrupt Status	P41 Interrupt Status	P30 Interrupt Status	P31 Interrupt Status
1	Write		MCT Interrupt Mask			P40 Interrupt Mask	P41 Interrupt Mask	P30 Interrupt Mask	P31 Interrupt Mask
2	Read	VLP Busy Status	APW Busy Status	RTC Busy Status	ADC Busy Status	P20 Busy Status	P21 Busy Status	P10 Busy Status	P11 Busy Status
3	Read		MCT Busy Status			P40 Busy Status	P41 Busy Status	P30 Busy Status	P31 Busy Status
4	Read	VLP Done Status	APW Done Status	RTC Done Status	ADC Done Status	P20 Done Status	P21 Done Status	P10 Done Status	P11 Done Status
5	Read		MCT Done Status			P40 Done Status	P41 Done Status	P30 Done Status	P31 Done Status
6	Read	Reads Eight Data Bits From Optional Portable Front Panel Switches							
6	Write	Writes Eight Data Bits To Optional Portable Front Panel Lamp Register							
7	Read	Memory Parity Status							
7	Write	No Data Bit Utilization; Generates System Master Reset Pulse							

TABLE 3.4. DEFINITION OF DEVICE MNEMONICS

MNEMONIC	DEVICE
ADC	Analog-to-Digital Converter
APU	Arithmetic Processing Unit
FLP	Flexible Disk Controller
MGT	Magnetic Tape Controller
PXI	Asynchronous Port "X" Input
PXO	Asynchronous Port "X" Output
RTC	Real Time Clock

The remaining 120_{10} address locations in the first memory space addressing partition are used, in conjunction with the system data bus, to communicate with specific peripheral devices. The device addressing structure is such that any one of 15 devices can be uniquely addressed, and any one device can perform eight separate functions. That is accomplished by designating address bits 0, 1, and 2 to define the device function and designating address bits 3, 4, 5, and 6 to define the specific device, as illustrated below:

Table 3.5 summarizes the I/O command structure between the CPU and each standard peripheral controller.

TABLE 3.5. DEFINITION OF DEVICE ADDRESSES AND FUNCTIONS

Device 1X₈ - Battery Clock (ETC)

Status Bit: None

<u>ADDRESS</u>	<u>CPU FUNCTION</u>	<u>COMMAND FUNCTION</u>
10	Read	Seconds
11	Read	Minutes
12	Read	Hours
13	Read	Days
14	Read	Months
15	Read	Year

DATA FORMAT

Data Bit	7	6	5	4	3	2	1	0
Data Bit Weight	80	40	20	10	8	4	2	1

Most Signifi- Least Signifi-
cant Character cant Character

Device 2X₈ - Device Controller (DVC)

Status Bit: None

<u>ADDRESS</u>	<u>CPU FUNCTION</u>	<u>COMMAND FUNCTION</u>
20	Read	Reads status of first 8 ON/OFF points
20	Write	Sets status of first 8 ON/OFF points
21	Read	Reads status of second 8 ON/OFF points
21	Write	Sets status of second 8 ON/OFF points

TABLE 3.5 (Continued)

Device 3X₈ - Status Input Controller (SIC)
 or I/O Controller (IOC)

Status Bit: None

<u>ADDRESS</u>	<u>CPU FUNCTION</u>	<u>COMMAND FUNCTION</u>
30	Read	Reads status of 1st group of 8 bits
31	Read	Reads status of 2nd group of 8 bits
32	Read	Reads status of 3rd group of 8 bits
33	Read	Reads status of 4th group of 8 bits
30	Write*	Sets status of 1st group of 8 bits
31	Write*	Sets status of 2nd group of 8 bits
32	Write*	Sets status of 3rd group of 8 bits
33	Write*	Sets status of 4th group of 8 bits

*Not available with Status Input Controller

Device 4X₈ - Asynchronous Interfaces

Status Bits:

- Bit 0 - Port 1 Input (P1I)
- Bit 1 - Port 1 Output (P1O)
- Bit 2 - Port 2 Input (P2I)
- Bit 3 - Port 2 Output (P2O)

<u>ADDRESS</u>	<u>CPU FUNCTION</u>	<u>COMMAND FUNCTION</u>
40	Read ¹	Reads Input Data from Port 1
40	Write	Writes Output Data to Port 1
41	Write	Clears Output DONE status for Port 1
42	Write	Sets BUSY status for Port 1 Input
43	Read ²	Reads Modem status bits for both Ports

TABLE 3.5 (Continued)

<u>ADDRESS</u>	<u>CPU FUNCTION</u>	<u>COMMAND FUNCTION</u>
44	Read ¹	Reads Input Data from Port 2
44	Write	Writes Output Data to Port 2
45	Write	Clears Output Done Status for Port 2
46	Write	Sets BUSY status for Port 2 Input
47	Read	Reads Station ID Switch Setting
47	Write ³	Sets Modem Control Bits for both ports

¹These commands clear the Input DONE status.

²Data Bit Structure for Reading Modem Status:

<u>DATA BIT</u>	<u>MODEM STATUS</u>
0	CLEAR TO SEND (CTS), Port 1
1	DATA SET READY (DSR), Port 1
2	RING INDICATOR (RI), Port 1
3	CARRIER DETECT (CRDT), Port 1
4	CLEAR TO SEND, Port 2
5	DATA SET READY, Port 2
6	RING INDICATOR, Port 2
7	CARRIER DETECT, Port 2

³Data Bit Structure for Setting Modem Control Functions:

<u>DATA BIT</u>	<u>CONTROL FUNCTION</u>
0	Sets State of REQUEST TO SEND (RTS), Port 1
1	Sets State of DATA TERMINAL READY (DTR), Port 1
2	Sets State of OFF HOOK, Port 1
3	Sets State of R.F. Transmitter Switch, Port 1
4	Sets State of REQUEST TO SEND, Port 2
5	Sets State of DATA TERMINAL READY, Port 2
6	Sets State of OFF HOOK, Port 2
7	Sets State of R.F. Transmitter Switch, Port 2

TABLE 3.5 (Continued)

The baud rate for each asynchronous port may be independently set, by switches on the controller board, to any of the following standard baud rates:

110, 150, 300, 600, 1200, 2400, 4800 and 9600.

Device 5X₈ - Flexible Disk Controller (FLP)

Status Bit: 7

<u>ADDRESS</u>	<u>CPU FUNCTION</u>	<u>COMMAND FUNCTION</u>																						
1. 50 ₈	Write	Selects the register within the FDC, selects programmed and DMA read or write operation.																						
		<table><tr><th><u>DATA</u></th><th><u>FUNCTION SELECTED</u></th></tr><tr><td>0₈</td><td>Programmed write to FDC command register to specify a DMA write operation or a non-DMA operation.</td></tr><tr><td>1₈</td><td>Programmed write to FDC track register</td></tr><tr><td>2₈</td><td>Programmed write to FDC sector register</td></tr><tr><td>3₈</td><td>Programmed write to FDC data register</td></tr><tr><td>4₈</td><td>Programmed read from FDC status register</td></tr><tr><td>5₈</td><td>Programmed read from FDC track register</td></tr><tr><td>6₈</td><td>Programmed read from FDC sector register</td></tr><tr><td>7₈</td><td>Programmed read from FDC data register</td></tr><tr><td>10₈</td><td>Programmed write to FDC command register to specify a DMA read operation or a non-DMA operation.</td></tr><tr><td>3-9</td><td></td></tr></table>	<u>DATA</u>	<u>FUNCTION SELECTED</u>	0 ₈	Programmed write to FDC command register to specify a DMA write operation or a non-DMA operation.	1 ₈	Programmed write to FDC track register	2 ₈	Programmed write to FDC sector register	3 ₈	Programmed write to FDC data register	4 ₈	Programmed read from FDC status register	5 ₈	Programmed read from FDC track register	6 ₈	Programmed read from FDC sector register	7 ₈	Programmed read from FDC data register	10 ₈	Programmed write to FDC command register to specify a DMA read operation or a non-DMA operation.	3-9	
<u>DATA</u>	<u>FUNCTION SELECTED</u>																							
0 ₈	Programmed write to FDC command register to specify a DMA write operation or a non-DMA operation.																							
1 ₈	Programmed write to FDC track register																							
2 ₈	Programmed write to FDC sector register																							
3 ₈	Programmed write to FDC data register																							
4 ₈	Programmed read from FDC status register																							
5 ₈	Programmed read from FDC track register																							
6 ₈	Programmed read from FDC sector register																							
7 ₈	Programmed read from FDC data register																							
10 ₈	Programmed write to FDC command register to specify a DMA read operation or a non-DMA operation.																							
3-9																								

TABLE 3.5 (Continued)

	<u>ADDRESS</u>	<u>CPU FUNCTION</u>	<u>COMMAND FUNCTION</u>
2.	50 ₈	Read	Transfers data from the register specified in 1. above into a temporary holding latch.
3.	51 ₈	Read	Transfers data from the holding latch specified in 2. above into a CPU accumulator.
4.	52 ₈	Write	Writes data into the FDC register specified by 1. above.
5.	53 ₈	Write	Issues a write fault reset strobe to the selected disk drive.
6.	51 ₈	Write	Selects a disk drive.
		<u>DATA</u>	<u>UNIT SELECTED</u>
		1 ₈	Disk unit 0
		2 ₈	Disk unit 1
		4 ₈	Disk unit 2
		10 ₈	Disk unit 3
7.	54 ₈	Write	Outputs MSB of DMA address counter.
8.	54 ₈	Read	Inputs MSB of DMA address counter.
9.	55 ₈	Write	Outputs LSB of DMA address counter.
10.	55 ₈	Read	Inputs LSB of DMA address counter.
11.	56 ₈	Write	Controls the state of the program load light on the front panel.
		<u>DATA</u>	<u>CONDITION</u>
		0 ₈	Off
		1 ₈	On
12.	57 ₈	Write	Clears disk controller DONE status.
13.	57 ₈	Read	Increments the contents of the DMA address counters.

TABLE 3.5 (Continued)

Device 6X₈ - Arithmetic Processing Unit (APU),
Real Time Clock (RTC), and
Rainfall Counter (RNF)

Status Bits:

Bit 5 - Real Time Clock
Bit 6 - Arithmetic Processing Unit

<u>ADDRESS</u>	<u>CPU FUNCTION</u>	<u>COMMAND FUNCTION</u>
60 ₈	Write	Transmits a data byte from the MPU to the APU Stack.
61 ₈	Write	Transmits a command byte from the MPU to the APU Command Register.
62 ₈	Read	Transfers a data byte from the top of the APU Stack to the APU Intermediate Register.
63 ₈	Read	Transfers the contents of the APU Status Register to the APU Intermediate Register; Does not affect BUSY/DONE status.
64 ₈	Read	Transfers the contents of the APU Intermediate Register to an MPU Accumulator and clears the APU DONE Status.
65 ₈	Read	Reads the contents of the Rainfall Counter.
66 ₈	Write	Sets the Real Time Clock Interrupt Rate, when one and only one data bit is true, as follows: Bit 0 - 1 per second Bit 1 - 10 per second Bit 2 - 60 per second Bit 3 - External Source
67 ₈	Write	Clears the Real Time Clock DONE Status.

TABLE 3.5 (Continued)

Device 7X₈ - Analog to Digital Converter (ADC)

Status Bit: 4

<u>ADDRESS</u>	<u>CPU FUNCTION</u>	<u>COMMAND FUNCTION</u>																
70 ₈	Write	Loads the Channel and Gain Selection Register. The Channel is selected by Data Bits 0 (LSB) through 4 (MSB). Gain is selected as follows:																
		<table><tr><th><u>DATA BIT</u></th><th><u>FULL-SCALE RANGE</u></th></tr><tr><td><u>7</u> <u>6</u> <u>5</u></td><td></td></tr><tr><td>0 0 0</td><td>+1 Volt</td></tr><tr><td>0 0 1</td><td>+100 mv.</td></tr><tr><td>0 1 0</td><td>+5 Volts</td></tr><tr><td>0 1 1</td><td>+10 Volts</td></tr><tr><td>1 0 0</td><td>+10 mv</td></tr><tr><td>1 0 1</td><td>Spare</td></tr></table>	<u>DATA BIT</u>	<u>FULL-SCALE RANGE</u>	<u>7</u> <u>6</u> <u>5</u>		0 0 0	+1 Volt	0 0 1	+100 mv.	0 1 0	+5 Volts	0 1 1	+10 Volts	1 0 0	+10 mv	1 0 1	Spare
<u>DATA BIT</u>	<u>FULL-SCALE RANGE</u>																	
<u>7</u> <u>6</u> <u>5</u>																		
0 0 0	+1 Volt																	
0 0 1	+100 mv.																	
0 1 0	+5 Volts																	
0 1 1	+10 Volts																	
1 0 0	+10 mv																	
1 0 1	Spare																	
71 ₈	Write	Loads the Board Selection Register according to the value specified by data bits 0 through 2.																
72 ₈	Write	Causes the ADC to start a conversion using the parameters in its Channel, Gain, and Board Selection registers.																
73 ₈	Write	Clears the ADC DONE Status.																
74 ₈	Read	Reads the least significant byte of the 2's Complement ADC output. Bit 0 is the least significant bit.																
75 ₈	Read	Reads the most significant byte of the 2's Complement ADC output. Bit 0 is the least significant bit.																

TABLE 3.5 (Continued)

 Device 13X₈ - I/O Controller

The operation of this device is identical with that of Device 3X₈.

 Device 14X₈ - Asynchronous Interface (Ports 3 and 4)

The operation of this device is identical with that of Device 4X₈.

 Device 16X₈ - Magnetic Tape Controller

Status Bit: 6

<u>ADDRESS</u>	<u>CPU FUNCTION</u>	<u>COMMAND FUNCTION</u>										
160 ₈	Write	Sets the Command Register to prepare the Controller to perform a function according to which of the following data bits is true: Bit 0: Write a data byte Bit 1: Rewind to BOT Bit 2: Write End of Record Bit 3: Write End of File										
160 ₈	Read	Reads the Status of the Magnetic Tape System: <table><tr><th><u>DATA BIT</u></th><th><u>STATUS</u></th></tr><tr><td>0</td><td>Tape Unit Ready.</td></tr><tr><td>1</td><td>BOT</td></tr><tr><td>2</td><td>EOT</td></tr><tr><td>3</td><td>Rewinding</td></tr></table>	<u>DATA BIT</u>	<u>STATUS</u>	0	Tape Unit Ready.	1	BOT	2	EOT	3	Rewinding
<u>DATA BIT</u>	<u>STATUS</u>											
0	Tape Unit Ready.											
1	BOT											
2	EOT											
3	Rewinding											
161 ₈	Write	Stores a byte of data to be written on tape in the Controller data register.										
162 ₈	Write	Starts the operation defined by the contents of the Command Register.										
163 ₈	Write	Clears the DONE status of the Controller.										

3.1.2 Random Access Memory

The second, and largest, memory addressing partition is reserved for solid state, random access, read/write memory (RAM). That memory area is available to the CPU for storing (writing) and retrieving (reading) 8-bit data bytes under program control. In addition, that memory area is available for the reading and writing of data by the Flexible Disk Controller, a Direct Memory Access (DMA) device.

3.1.3 Read Only Memory

The top 512₁₀ memory address locations are reserved for Read Only Memory (ROM), provided by a pre-programmed ROM device resident on the CPU board. The CPU may read data and instructions from that device, but may not write data to it. The normal function of the ROM is to provide the "loader" program for use by the CPU to load the main system operating program into RAM from the flexible disk when power is applied to the system after a lengthy power outage or when the operator depresses the front-panel "PROGRAM LOAD" switch. The ROM is a single integrated circuit and can be changed by extracting it from a socket on the CPU board.

4.0 THEORIES OF OPERATION

This section contains detailed theories of operation for the various DART II system components. Discussions in this section make frequent reference to the schematic diagram in Appendix C and device data sheets in Appendix D.

In order to avoid confusion, the following definition of terminology with respect to digital logic levels will apply to all discussions. The terms "false," "low," "zero," "logical zero," etc. all refer to the most negative voltage of the two voltage states representing a binary signal. Similarly, the term "true," "high," "one," "logical one," etc. all refer to the most positive voltage of the two voltage states representing a binary signal. It is emphasized that the descriptive terminology is not related to whether the mnemonic assigned to the signal it describes is a "true" or "complement" mnemonic. For example, the term "logical zero" describing the signal END means the same as the same term describing the signal $\overline{\text{END}}$; in both cases, the signal is at its most negative state of voltage.

Finally, the use of the suffix "-" and the use of the overlining bar " $\overline{\quad}$ " in conjunction with a mnemonic both mean the logical complement of the mnemonic and the two symbols may be used interchangeably in either the text or on schematic diagrams. That is, END- and $\overline{\text{END}}$ are equivalent, and represent the logical complement of the signal END.

4.1 POWER SUPPLY ASSEMBLY

The DART II power supply assembly consists of three OEM supplies, the power interconnect board, two fans and related mounting hardware. The batteries and relays which connect to this assembly are also discussed here. The power supply data sheets are included in Appendix D.

Four primary voltages are provided by the power supply assembly: +5 volts, +15 volts, -15 volts, and +24 volts. Secondary voltages for battery back-up are +5 volts and +12 volts.

The +5 volts is provided by a EMA-5/6 CC power supply. The output connections have been strapped for local current sensing. An overvoltage protection circuit has been added to the power supply output. It is set to trigger if the output of the supply exceeds 6.5 volts. When the overvoltage circuit triggers, it will shunt the output of the power supply to ground.

High and low temperature limit switches have been mounted on the 5 volt supply. They are wired in series with the incoming 117 VAC to the DART II. The high temperature limit switch opens at 150°F and the low temperature limit switch opens at 40°F.

The +15 volts and -15 volts are provided by an ETA-12/15B power supply. Two overvoltage circuits have been mounted on this supply, one for the positive output and one for the negative output. They are set to trigger at +17 volts and -17 volts respectively. A connection has been made to a tap on the power transformer secondary to provide 60 Hertz for the real time and battery clocks.

An EMA-18/24B power supply provides the +24 volts. It is strapped for local current sensing.

The function of the power interconnect board (Drawing No. 500C3217-001) is to provide a means of routing the AC and DC voltages to various parts of the DART II chassis. There are also two battery charging circuits located on this board.

The 12 volt battery is charged from the +15 volt supply through diode CR7 and resistor R1. During discharge, the current flows to the clock circuits through diode CR2. The relay circuit causes the battery to be automatically disconnected when the battery is completely discharged. When power is applied, relay RL2 closes allowing the battery to charge. When power is lost, the relay remains closed until the battery voltage decreases to about 2 volts.

The 4 volt battery is charged from the 5 volt supply through shottky diode CR8 and resistor R2. The relay circuit is similar to the 12 volt relay circuit, and disconnects the battery when it is discharged to about 1.5 volts.

Solid state relays RL1 and RL4 connect to the power interconnect board through two octal sockets. These relays are controlled by the Device Controller board and control the AC power for flexible disk drive and the keyboard-printer. They are mounted on the under-side of the DART II chassis on the left side.

4.2 CPU

INTRODUCTION

The CPU board (schematic diagram 500D3201-001) contains the M6800 microprocessor, a read only memory, and associated control and support circuits. These circuits include the system clock, address and data buffers, address decoders, power reset generator and battery status detector.

The M6800

The M6800 microprocessor (U29) provides 16 address output bits for selecting any one of 65,536 memory locations or device interface functions and 8 data bits (inputs or outputs) for transferring data to or from memory or devices. In addition to the address and data bits, several control inputs and outputs are used to control data transfers and to interrupt, restart, or halt the execution of a program. These control signals are described in detail in the M6800 data sheet (Appendix D).

The RESET- input is generated by the power reset circuit, which is described in a later section. The HALT- signal is always true unless the portable front panel is connected, which forces HALT- to be false for halt or single step operations. The IRQ- signal is generated by the BUSY/DONE circuits of all system controllers which have interrupt status, and is transmitted to the CPU by the BIRQ- line. The M6800 responds to a negative transition of IRQ- by jumping to the address specified by locations 177770₈ and 177771₈, which contain the address 200₈ in the loader ROM. In the system operating program, address 200₈ will contain a jump to the interrupt processor routine.

READ ONLY MEMORY

The read only memory (U21) contains 512 bytes of memory, located at addresses 177000₈ to 177777₈. It normally contains the loader program, which loads the system operating software from flexible disk into the read/write random access memory. A complete listing of this program is contained in Appendix E.

When a restart sequence is initiated by a positive transition of the RESET- signal (caused by pressing the program load switch or by restoring AC power), the restart address is read from locations 177776₈ and 177777₈. Execution then begins at the restart address, which is 177000 in the loader program.

The loader program first checks the status of the memory back-up batteries, and proceeds to load the program from disk if the batteries are discharged. The program load switch defeats the battery status circuit, holding it in a "discharged" state, therefore causing a program load regardless of the true state of the batteries. While the program is being loaded, the battery status circuit is also held in discharged state so that a short power failure during the load operation will result in the initiation of another program load. Otherwise, the presence of the normal power-on voltage at the battery status circuit input (during the first program load) could lead to a false test result.

If the loader program finds the battery status to be "charged", the program will execute a jump to location 203, which has been assigned as the "power fail" location. In the system operating program, this location will contain a jump to a power fail routine.

SYSTEM CLOCK

The system clock is derived from a crystal controlled oscillator (Y1 and U8 pins 5, 6, 10, 11, 12 and 13) which operates at 6.7584 MHz. The oscillator output (KCLK) is buffered by U8 (pins 3 and 4) to provide BKCLK- to the system. This signal is generally used by other interface controllers for timing functions unrelated to CPU timing. The oscillator output (KCLK) is divided by eight by U26 and is then split into two phases by U27, generating CK1 and CK2. These signals are then buffered by U28 (containing 4 discrete transistors) and associated components to provide $\phi 1$ and $\phi 2$ for the M6800 (U29).

Also derived from KCLK is K1.6, which is taken from the divide-by-four output of U26 (pin 8). This signal is used by the address decoding section to shorten memory and device enables to 300 ns during write operations.

POWER RESET

The purpose of the power reset circuit is to hold the system in a reset state while +5 volt power is going down (due to AC power failure) and to initialize and restart the system when power is restored. A system reset (BRESET) is generated when the +5 volt power drops below 4.75 volts during power-down, and during power-up BRESET is held true until the +5 volt power reaches 4.8 volts. This circuit also generates RESET- which is used by the M6800. During power-up, RESET- becomes false 12 cycles (of $\phi 2$) after BRESET becomes true. During power-down, RESET- becomes false at the same time BRESET becomes true. Pressing the program load switch on the front panel or switching the reset switch on the optional portable front panel also causes this circuit to produce a system reset.

Operational amplifier U2 is used to compare the +5 volt supply voltage at its inverting input to a reference voltage at its non-inverting input. The reference voltage is adjustable by R34, and should be set to about 4.75 volts. A small amount of positive feedback is provided by R14, which causes the reference voltage to be about .05 volts lower when the +5 volt input is above the reference voltage than when it is below the reference voltage. When the +5 volt supply is below the reference, the output of U2 is high (+13 volts), which turns on transistor Q3, forcing PWRES- false. This causes U17 pin 3 to be true, resetting counter U25, and forces RESET- false. The PWRES- signal is also applied to U16 pin 9, causing BRESET to become true. When the +5 volt supply rises above the reference, the output of U2 goes low (-13 volts), turning off Q3, and forcing PWRES- true, and BRESET false. The reset input of counter U25 then becomes false, and the counter begins counting CK2 clock pulses. The counter will continue to count until a count of 12 is reached (ABCD=0011), which causes the clock input to U25 to be disabled, and RESET- to become true.

Since all CPU data transfers to and from memory are made during $\phi 2$, generating a reset during $\phi 2$ could result in data being written incorrectly. Therefore transistor Q3 is inhibited from being turned on during clock $\phi 2$. The base is held low during $\phi 2$ by U17 pin 6 unless PWRES- is already false at the beginning of $\phi 2$.

The PWRES- signal also goes to a reset switch on the optional portable front panel. It should be noted that this switch is not synchronized to $\phi 2$; therefore this switch is an abortive reset.

BATTERY STATUS TEST CIRCUIT

The proper operation of this circuit is dependent on a specific program sequence which is executed from ROM immediately after power-up. This sequence is described in the section on the read only memory.

The memory back-up voltage, VMEM, charges C6 through R4, so that the power-up battery voltage is stored momentarily after the AC power is restored. The voltage on C6 is compared to a fixed reference voltage (2.8 volts) by operational amplifier U1. If the voltage on C6 is below 2.8 volts, the output of U1 goes high (+13 volts) and turns on transistor Q2, forcing POWLOW- false. The status of the POWLOW- signal is checked by the M6800 by performing a read from address 7. This operation causes CPU7 (U18-3) to be false, and READ (U3-13) to be true, which causes U17-10 to be true, gating the POWLOW- signal onto bit 0 of the data bus (BD0) through diode CR9. If POWLOW- is false when the read is performed, U17-8 forces both RELS and BD0 false. When RELS returns true at the end of the read cycle, U27-5 (RELDS) will be clocked true. This will cause transistor Q1 to turn on, holding C6 at approximately 2.4 volts. This condition will remain until an I/O Reset (write to address 7) is issued by the program, resetting RELDS. Note that RELDS is not set if POWLOW- is true.

When the program load switch is used to initiate a program load, POWLOW- is forced to be false by diode CR10 which connects to the switch through J1-C. This switch closure also causes a short negative going pulse at U3-8, which forces PWRES- false through diode CR6. The resulting M6800 reset has the same effect as a reset caused by a power outage; the program in the loader PROM will be executed, first checking the battery condition. Since POWLOW- has been forced unconditionally false

by the program load switch and diode CR10, the program assumes that the batteries are low and responds by loading the program from the flexible disk.

ADDRESS DECODERS

The device code addresses (0-177₈) are decoded by U12 and one section of U13. The VMA-02 function is gated in at U12-11 to disable decoding during invalid addresses. The signal WRTS- is gated in at U12-6 to shorten write enable times to 300 ns. Read enable times are slightly shorter than 02, or about 550 ns. The output of U12, DEVDEC- is inverted and gated with CK2 by a section of U14, generating DEVSTRB-, which responds to all device addresses. Gate U11 and decoder U10 decode the CPU function codes 0-7.

The ROM addresses are decoded by U24 which generates ROMDEC-, which is inverted and gated with FPROMDIS- to generate ROMEN-. Unless it is disabled by the portable front panel (by FPROMDIS-), ROMEN- is false for addresses 177000 to 177777. The inverse of ROMDEC- is also used by U20 along with address bits A2 through A8 to decode addresses 177774 through 177777. The output of U20 (FPSTDEC-) is used by the portable front panel to disable ROM when the restart addresses are accessed.

The memory selection logic partitions the memory into four, 16K sections which are enabled by MEM1EN-, MEM2EN-, MEM3EN- and MEM4EN-. These signals go respectively to card slots 2, 3, 4 and 5 on the mother board. The memory enable signals are decoded by U4, which is effectively disabled when pin 12 is true or enabled when pin 13 is true. Signal DEVDEC- (U5-9) disables U4 when device codes are addressed, and ROMDEC- (U5-10) disables U4 when ROM is addressed. Decoder U4 is enabled by U6-6 when a read or write is executed by the CPU, the portable front panel or a DMA device. Note that the memory

RADIAN

write enable time for a CPU write is shortened by 300 ns by WRTS- (U5-1).

The DMAEN- input (J2-V) is used by the flexible disk controller to enable memory for data transfers to and from memory during $\phi 1$. Since all CPU transfers are made during $\phi 2$, the transfer operations are independent.

OPTIONAL PORTABLE FRONT PANEL ACCESS

The front panel gains access to the memories via gate input U6-4 (FPMEM-). When using the front panel switches, the ROM section is disabled via U16 (FPROMDIS-). The signal FPHALT- (J1-9) allows the front panel to halt the microprocessor. With the microprocessor halted, the front panel controls the read/write line via the signal FPWRITE- (J1-10).

The front panel starts the microprocessor with signal FPRUN-, (J1-11), which issues a reset term to the microprocessor. However, with the read only memories disabled, the starting address is defined by the setting of the address switches on the portable front panel.

4.3 MEMORY

DART II can accommodate 65,536 8-bit bytes of random access, read/write memory, exclusive of those address locations reserved for device codes (locations 0 through 177₈) and read only memory (address locations 177000₈ through 177777₈). Each memory board provides 16,384 bytes of storage, and the card cage has four slots available for memory. The mother board is configured such that the first (front) memory card responds to the first 16,384 memory address locations, the second card responds to the second 16,384 address locations, etc.

Referring to schematic diagram 500D3205-001, each memory board is segmented into four banks of 4,096 bytes. Each TMS4046-30 memory integrated circuit is configured for addressing 4,096 one-bit locations. Thus, each bank is comprised of eight integrated circuits to provide 4,096 8-bit bytes. Address bits A0 through A11 are provided to all memory integrated circuits in parallel. The particular bank being addressed is determined by U21. First, for any bank to be selected, the signal MEMEN- (U21-13) must be false; this signal, generated by the CPU board, in effect selects a particular memory board for addressing. In normal operation the master reset signal, RES, will be false at U21-12. U21 then decodes address bits twelve and thirteen to determine which of the four banks is to be selected. The signals SEL1-, SEL2-, SEL3-, and SEL4- are supplied to the "chip select" inputs of the four banks of memory devices to effect bank selection. In summary, the signals SELX- and address bits zero through eleven uniquely address each of the 16,384 available memory locations on each board.

The data output (pin 8) and data input (pin 12) terminals for each memory device are connected, providing a bi-directional data bus for the memory board. The direction of data transfer

(i.e., whether data is being written to memory or read from memory) is determined by the logical state of the signal READ, applied to pin 9 of each device. When READ, supplied by the CPU card, is logically true, data may be read from memory; conversely, when READ is logically false, data may be written to memory.

Interface of the memory data lines with the system data bus is accomplished by the bi-directional transfer gates U32 and U44. During READ operation the signal ENDR- is false, transferring the memory output data bits to the system data bus. During WRITE operation ENDR- is true, transferring data from the system data bus to the memory data input ports.

All memory control signals (BRESET, BREAD, MEMEN-, and CPU7-) are generated by the CPU board. Note, however, that memory accesses do not occur only on the MPU $\phi 2$ clock, as would be the case if only the M6800 MPU required access to memory. The memory is shared by the MPU on the CPU board and by the flexible disk controller which can perform direct memory access (DMA) transfers to and from memory. In this case the system address and data buses are controlled by the flexible disk controller. The design of that controller and the CPU board is such that all DMA memory accesses occur during the MPU $\phi 1$ clock, while all MPU accesses occur under program control during the $\phi 2$ clock. Thus, the MPU can operate at full speed while DMA devices, in interleaved fashion, also use memory.

Memory Power

Each memory device has two terminals for power. The first (pin 19) requires +5 volts and is provided by the system 5-volt power supply. This terminal supplies the power-consuming peripheral and driver circuitry within the memory devices, but is not necessary for memory retention when the memory is not

being addressed. The second terminal (pin 20) requires +5 volts during normal operation, but can drop to as low as +2.5 volts without loss of memory data when the devices are not being addressed. The second power source is normally derived from the system 5-volt power supply, but is battery-backed to provide data retention when A.C. line power failures occur. Refer to section 4.1, which provides the theory of operation for the power supply interconnect board, for a description of the manner in which this power source is derived.

Memory Parity Option

The memory board has an option for providing a ninth parity bit for checking data validity. Each of the four memory banks is provided with a ninth memory integrated circuit for storing the parity bit.

When using this option each byte to be written into memory is applied to parity generator/checker U45, which calculates an odd parity check bit, DIP, supplied as the ninth data bit to memory. During read operation, the 8-bit memory byte is again applied to U45. In addition the memory parity bit, DOP, is also applied, by means of U33-11 to U45. If parity checks, U45-6 and U46-2 will be false, and the parity error flip-flop, U46, will not be set. However, if a parity error is detected, the signal at U46-2 will be true and the rising edge of the signal ENDR- will clock U46-5 to a true level.

Once U46 has been set, indicating a parity error, it can only be reset by the master reset signal BRESET which occurs either under program control by the CPU or as a hardware initialization signal when AC power is applied to DART II.

The CPU can determine that a memory parity error has occurred by reading address (device code) 7. That operation causes generation of the signal CPU7- on the CPU board, and when it occurs, the parity error status of U46 is gated to data bus bit 7 by U34-3.

4.4 BUSY/DONE OPERATION

Many DART II interface boards incorporate logic circuitry that implements a BUSY/DONE concept to allow the CPU to determine the status of the peripheral interfaces. Because the circuitry is functionally identical in all interfaces, it has been provided on a single small board which plugs directly into an interface board. The circuitry is shown on schematic diagram 500B3265-001.

In general, the circuitry provides an indication that a device is "BUSY" performing operation or that the commanded operation is "DONE". It provides for status determination by the CPU by means of a polling operation under program control. It also provides for automatically interrupting the CPU when an operation is "DONE". The latter function can be disabled, under program control, by setting an interrupt "MASK" bit within the device. Finally, the circuitry for allowing the CPU, under program control, to determine which device (because all devices have a unique interrupt status bit assignment) initiated an interrupt.

The signal RES- is generally derived from the CPU signal BRESET, which occurs either under program control or when power is applied to the system. That signal has the effect of clearing the BUSY (U2-9), DONE (U2-5) and MASK (U3) flip-flops. The BUSY and DONE flip-flops may also be cleared by the signal CLR-.

When the CPU initiates an operation within an interface the signal STRT- results from the CPU writing to the device code which is to effect the desired operation. STRT- sets the BUSY flip-flop and clears the DONE flip-flop (if it was set). Normally, DNSTR, the steering input of the DONE flip-flop, is connected to BUSY (pin 18). When the peripheral controller completes

the commanded operation it generates the signal DNCLK-, setting DONE. Normally, BSYST, the steering input to the BUSY flip-flop is connected to ground and DONE (pin 15) is connected to BSYCLK- (pin 16). Therefore, when DONE is set, BUSY is cleared.

When DONE is set and the MASK flip-flop (U3) is not set, U4-3 will become a logic zero and the system interrupt bus, BIRQ-, will cause a CPU interrupt when interrupts are enabled within the MPU. The remaining outputs of open collector gates U4 are connected to a system data bus bit uniquely assigned to each peripheral interface. The CPU can determine which device generated an interrupt by reading address location 0 or 1; that operation generates the signal INTA, gating the status of the DONE flip-flop to the data bus by means of U4-6. Similarly, the CPU can at any time determine the status of the BUSY flip-flop by reading address locations 2 or 3, which generates the signal BSYCK, or determine the status of the DONE flip-flop by reading address locations 4 or 5, which generates the signal DNCK.

The CPU can inhibit or enable interrupts from a particular device by setting the MASK flip-flop associated with that device. A CPU write to address locations 0 or 1 generates the MASK flip-flop clock, MSK-. The flip-flop steering input, DAT, is derived from the system data bus bit assigned to the peripheral interface, and will be a logical one if interrupts are to be disabled ("Masked") or a logical zero if interrupts are to be enabled.

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4.5 ASYNCHRONOUS INTERFACE

INTRODUCTION

The asynchronous interface board provides two independent asynchronous serial input/output ports with independently switch-selectable baud rates. Standard baud rates between 110 and 9,600 are available. Each port may be independently configured, by switches, to provide input/output logic levels according to EIA specification RS-232C or to provide current loop input/output capability for interfacing with certain teleprinter devices. Each port is also provided with the capability of monitoring standard modem status signals and generating, under CPU program control, standard modem control signals. Finally, a single eight-bit, switch-selectable identification code, which may be read by the CPU under program control, is provided on the board.

CONTROLLER OPERATION

Circuitry Common to Both Ports

The following discussion makes reference to schematic diagram 500C3212-001 and the device specification sheet for the TR1863 asynchronous receiver/transmitter integrated circuit, included in Appendix D.

The device codes assigned to the asynchronous interface board are either 4X₈ or 14X₈, depending on the positions of switches within the eight-position DIP switch, U35. When device codes 40₈ through 47₈ are to be used, switch sections corresponding to INTA1-, BSYCK1-, DNCK1-, and switch section 1 (at the output of U37-12) should be closed and all other sections of U35 should be open. When device codes 140₈ through 147₈ are to be

used, the switch sections just mentioned should be open and the remaining sections closed.

The CPU may determine the setting of the station identification switch, U21, by reading device code 47₈. That device code is decoded by U23-9 (DC47-), inverted by U12, and supplied to U24-1 together with the signal READ at U24-2. U24-3 is then false during the read operation, gating the switch settings of U21 to the system data bus by means of the tri-state bus driver U22.

Modem status signals (Clear to Send, Data Set Ready, Ring Indicator, and Carrier Detect) for both ports can be read by the CPU as a single eight-bit byte. The status signals are supplied to RS-232 - to - TTL converters U29 and U30, whose outputs are provided to tri-state bus driver U31. A CPU read of device code 43₈ will cause the status signals to be gated to the system data bus by U31.

Modem and other control signals may be transferred to the asynchronous interface by a CPU write to device code 47₈. The signal ENDR-, generated at U6-8, will be false only if either of the signals CLRIDN- or CLRIDN2- are false, a condition that does not occur during a write to device code 47₈. Thus, ENDR- will be true, bi-directional transfer gates U32 and U33 will connect the system data bus to the input of the eight-bit register U18, and data will be clocked into that register during the CPU write to device code 47₈. Three of the four control signals of each of the two 4-bit groups are converted to RS-232C levels by U15 and U16. The remaining bit of each of the 4-bit groups are inverted and supplied to the transistor switches Q1-Q2 and Q3-Q4 to provide solid state switch closures when logical "ones" are transmitted for data bits 3 and 7.

Circuitry Not Common to Both Ports

The remaining circuitry is duplicated for each of the two ports on each board. Therefore, only the operation for one port will be discussed.

Clock Derivation

U20 requires a clock that has a frequency sixteen times as great as the desired baud rate. BKCLK-, supplied by the CPU, has a frequency of 6.7584 MHz. An inverted version of that clock signal is supplied to U1-14 as KCLK. U1 and U7 form an 8-bit binary counter, of which the first seven stages are provided to the baud-rate selection switch, U2. One (and only one) of the first seven positions of U2 must be closed to provide the selected clock frequency, SCLK, to U3-14. U3, U5, and associated combinational logic form either a divide-by-22 or a divide-by-30 counter, depending on the position of the eighth switch in U2. If that switch is closed (it should only be closed when a baud rate of 110 is desired) a divide-by-30 counter is formed; otherwise, a divide-by-22 counter is formed. The resulting TTY1CLK at U5-5, U20-17, and U20-40 has a frequency sixteen times greater than the desired baud rate.

Asynchronous Port Output

The CPU causes the controller to produce a serial output by writing the 8-bit word to be serialized to device code 40_g. The device code is decoded at U23-1, producing the signal DC40- which, after inversion, is provided to U26-2. During the write operation the signal READ- at U26-1 will be true, causing the signal LDTX- to be generated at U26-3. That signal is applied to A2-3, setting BUSY and clearing DONE. During the write operation, data from the system data bus is gated by bi-directional transfer gates U32 and U33 to pins 26 through 33 of U20, where it is clocked into an internal register within U20 by the signal LDTX- at U20-23. At that time U20 automatically begins data

serialization, beginning with the insertion of a start bit, followed by serialized data and either one or two stop bits, depending on the position of switch section 9 of U13. The serial data appears at U20-25, U14-13, and U15-2. U15-3 is biased by R9 and R10 to approximately midway between TTL logic "one" and "zero" threshold levels, with the result that U15-1 switches between RS-232C mark and space levels. If switch section 1 of U13 is closed, the serial data, at RS-232C logic levels, is supplied to J1-16 and, by means of the mother board and an interior cable, to back-panel connector J6. U14 is an open collector inverter which switches the current loop on and off if switch section 2 of U13 is closed.

Note that switch sections 1 and 2 of U13 should not be closed simultaneously.

When U20 has completed transmission of the character, and is prepared to accept a new character, the signal CKODN is generated at U20-24 and provided to U6-12. Provided the signal "clear-to-send" is true at U6-13, the signal DNCLK will be generated at U6-11 and supplied to A2-9, clearing BUSY and setting DONE.

Asynchronous Port Input

Serial input data from a peripheral device is received at J1-15 and converted to TTL logic levels by U27. The serial data, RXD-, is supplied to U20-20. When U20 has received a complete 8-bit character, the signal CKIDN becomes true at U20-19 and A1-9, setting the input DONE status and clearing the input BUSY status. This operation has the effect of notifying the CPU that a character has been received.

The CPU may retrieve the received character from the controller by a read of device code 40_B. That operation results in generation of the signal CLRIDN- at U26-11. That signal is supplied to U20-18, clearing the signal CKIDN at U20-19, and to U20-4, causing the character assembled within U20 to appear at pins 5 through 12 and at pins 3 through 6 of U32 and U33. CLRIDN- also appears at U6-10, causing ENDR- to appear at U6-8 and at U32 and U33, transferring the received character through the bi-directional transfer gates to the system data bus. Simultaneously, CLRIDN- at A1-1 clears the input DONE status in preparation for the receipt of a new character.

Parity Operation

Switch sections 8 and 10 of U13 are normally open to provide the non-parity operation previously described. However, it is possible to transmit and receive serial data with an additional parity check bit inserted between the last (eighth) data bit and the stop bit(s). In order to enable parity operation, switch section 8 of U13 must be closed. If switch section 10 remains open, even parity operation will result; closing switch section 10 causes odd parity operation.

Although the ninth (parity) bit is received and checked by U20, that bit is not available to the CPU under program control. Similarly, when transmitting data, no action under program control of the CPU is required; the parity bit is automatically calculated and inserted by U20.

4.6 DART II FLEXIBLE DISK SUBSYSTEM

Introduction

The Dart II Flexible Disk Subsystem consists of a flexible disk controller circuit board, flexible disk drive and associated cabling. The controller board resides in slot 8 of the main chassis, and connects to the disk drive via a '3M' type connector to the left of the controller slot on the 'mother' board. The disk drive, mounted on the underside of the main chassis, is a CDC 9404 unit. Additional disk drives may be connected to the controller by use of the disk expansion chassis for a total of up to four drives.

The disk subsystem allows the operator to load diagnostics and the Dart Operating System software from diskette, and to store raw data on the diskette.

Flexible Diskette Medium

The diskette is a circular disk of mylar with a magnetic oxide coating enclosed in a sealed jacket. Cutouts are provided on each side of the jacket to allow head contact, drive spindle engaging and index hole detection.

The diskette has 77 tracks (0 thru 76) each having 26 sectors (1 thru 26). An IBM compatible diskette is soft-sectored; i.e., the sector and track identifiers are magnetically pre-recorded on the diskette. Each sector is comprised of a data gap and a data field (Figure 4.6.1). The data gap contains a zero data fill (clock pulses only) followed by a data sync word (FE_H) and a missing clock pattern ($C7_H$) that permits the disk controller to byte synchronize with the serial data stream.

FIGURE 4.6.1 DISKETTE SOFT SECTOR FORMAT

FIGURE 4.6.2 DATA GAP SERIAL DATA STREAM - FE SYNC CHARACTER, C7 CLOCK PATTERN

The sync word also acts as a flag or identifier for the address field (which follows the data gap). The address field contains the track and sector number of the data field that follows the address gap. The address gap contains a zero data fill followed by a different sync word and an identical missing clock pattern ($C7_H$) which identifies the data field. The data field is a fixed length record (128 bytes) followed by two polynomial check characters. Due to this format the controller must precede each operation by an address field search operation to locate the desired sector. As a result, an unformatted or partially erased diskette will not operate properly.

Flexible Disk Drive

The CDC 9404 disk drive is used in an IBM compatible mode of operation. The drive incorporates a belt driven spindle assembly to rotate the diskette (at 360 rpm), a ceramic read/write head, a stepper motor to move the head from track to track, a head load solenoid, an optical index detector, a track-zero indicator switch and an optical write-protect assembly. The disk drive has 20 data I/O and control lines that interface to the disk controller as illustrated in Figure 4.6.3.

The response of a particular disk drive to one of the unit select lines (Unit Select 0,1,2,3 inputs) is determined by the logical state of the unit select switches ($S1-1,2,3,4$) mounted on the disk electronics PCB. When $S1-1$ is closed (on) that disk drive will respond when the Unit Select 0 input is low (logic '0'). The drive will respond to a low Unit Select 1 when $S1-2$ is closed, and so forth. Not more than one unit select switch should be closed at one time. The state of one of the unit ready lines (Unit Rdy 0,1,2,3 output) is determined by the unit ready switches ($S1-5,6,7,8$). When certain conditions are

FIGURE 4.6.3 FLEXIBLE DISK I/O

met and S1-5 is closed (on) the Unit Rdy 0 output will be brought low (logic '0'). The conditions required for a drive to be 'ready' are:

1. The diskette has been inserted into the drive properly.
2. The door is closed.
3. The diskette is at speed.

Read Data/Clk Comp, Track 00, Write Protect, and Write Fault are sourced by open-collector gates (SN7438) and are gated by Unit Select. The Unit Rdy lines are also sourced by open-collector gates but are not gated by Unit Select.

A microswitch mounted near the head-positioning mechanism is actuated when the read/write head has been moved to track 0 (outer-most position). This brings the TRACK 00 output to a low level until the head is moved to some other position.

The WRITE PROTECT line is held low when the optical detector is not interrupted by the diskette jacket. Therefore, a write protect indication will occur when the diskette jacket has been punched in the proper position or is not inserted into the drive.

The WRITE FAULT status line is brought to a low level when one or more of the following conditions has occurred:

1. The disk unit is write enabled without the head loaded.

2. The unit is write enabled without write data being supplied by the disk controller.
3. An incorrect write data rate.

WRITE FAULT will remain low until a low level is placed on the WRITE FAULT RESET input of the selected drive.

The clock and data from the diskette are provided at the READ DATA/CLK COMP line in a bit-serial format with alternating clock and data bits. Each clock and data pulse is approximately 250 ns. in duration with a low level representing a logic '1' data bit or the presence of a clock pulse. The clock and data pulses occur every 4 μ sec with 2 μ sec spacing between each (see Figure 4.6.4).

FIGURE 4.6.4 READ DATA/CLK COMPOSITE

The resulting effective data rate is 250 KHz and the bit rate (clock and data) is 500 KHz.

When a low level is placed on the HEAD LOAD input, and the disk drive door is closed, the head load solenoid will be activated allowing the head pad to press the diskette medium against the read/write head. The head will remain loaded until

this input is returned to a high level or the diskette access door is opened.

The read/write head is stepped in the direction selected by the level on DIRECTION when a 10 μ sec (minimum) 'negative' going pulse is applied to the STEP input. A low level on the DIRECTION input selects step-in (toward the spindle) and a high level selects step-out.

The disk drive write network is enabled when a low level is placed on the WRITE ENABLE input and the clock and data applied to the WRITE DATA input is written on the diskette. The write data must be supplied by the controller in the same format and at the same frequency as the composite read data/clock (Figure 4.6.2).

When writing diskette tracks 44 or greater, the write head current must be reduced by placing a low level on LOW CURRENT. The disk drive requires 115 VAC, 60 Hz, single phase power for the drive motor, +24 volts for the head load solenoid and stepper motor and +5 volts for the logic circuit board.

Flexible Disk Controller (Schematic Diagram 500D3225-001)

The disk controller performs the task of interfacing the flexible disk drive to the DART CPU and memory bus (Figure 4.6.5). The CPU and memory interface consists of eight bi-directional data lines ($\overline{\text{BD0}}$ - $\overline{\text{BD7}}$) used to transfer data to and from the disk controller during programmed and DMA operations, sixteen address lines ($\overline{\text{BA0}}$ - $\overline{\text{BA15}}$) which supply the DMA address and select one of several registers in the controller under program control, two DMA control outputs ($\overline{\text{DMAEN}}$ & $\overline{\text{DMAWRT}}$), two program control inputs ($\overline{\text{DEVSTRE}}$ & $\overline{\text{BREAD}}$), two input timing elements ($\overline{\text{BKCLK}}$ & $\overline{\text{B\#2}}$), four busy-done-interrupt related lines ($\overline{\text{BIRQ}}$, $\overline{\text{INTAI}}$, $\overline{\text{BSYCKI}}$ & $\overline{\text{DNCKI}}$) and a system reset line ($\overline{\text{BRESET}}$).

FIGURE 4.6.5 FLEXIBLE DISK CONTROLLER INTERFACE

The disk interface has 20 status and control lines which connect to one or more (up to four) disk drives in a daisy-chain manner. UNIT XRDY (x=0, 1, 2, 3) allows the controller to check the ready status of any of the disk drives connected on the interface bus. SELX (x = 0,1,2,3) allows the controller to select one of the disk drives. TRK00 (Track 0), WPROT (Write protect), WRT FAULT (Write fault) and IPY (index pulse) inputs allow the controller to check the status of the selected drive. RAWDT is the composite read data/clock serial input to the controller. HLD (head load) permits the controller to load the head of the selected drive. STEP and DIRC (Direction) control the movement of the read/write head. TC43, WG, WRT FAULT RST, and WD control the disk drive write function.

The disk controller PCB contains three programmable latches, a 16 bit DMA address counter, a 4-bit disk controller I.C. register select latch, a 6-bit disk unit select latch and a floppy disk formatter/controller integrated circuit. By hardware enabling certain inverting and non-inverting buffers, the program is able to write to the address counter, register select latch, unit select latch or any four of the registers within the disk controller I.C. Figure 4.6.6 shows the data path taken during such a programmed write operation. Note that all tri-state buffers are disabled during this process.

The contents of the DMA address counter may be read under program control by hardware enabling the tri-state outputs of U11 (to read address bits A8-A15) or U12 (to read address bits A0-A7). This data path is shown in Figure 4.7.7.

Due to the slower access time for the disk controller I.C. (U56), data transferred to and from the controller chip must be buffered by a temporary holding latch (U15). As a result, the transfer must occur in two cycles, first transferring

FIGURE 4.6.6 PROGRAMMED WRITE TO ADDRESS CNTR, REGISTER SELECT LATCH OR UNIT SELECT LATCH

FIGURE 4.6.7 PROGRAMMED READ FROM ADDRESS COUNTERS

data to the holding latch (from either the CPU, memory or disk controller I.C.) and then transferring its contents to the CPU, memory or disk controller I.C.

Figures 4.6.8 and 4.6.9 show the data path taken during a programmed and DMA write operation to a disk controller I.C. register respectively. Note that during a DMA write (Figure 4.6.9) the DMA address counter buffers are enabled to supply the 'from' address for the transfer from the memory cards (the CPU address bus drivers are disabled at this time.)

Figure 4.6.10 shows the first cycle of a programmed or DMA read from the disk controller I.C. During this period data from the I.C. is latched in device U15. Figure 4.6.11 shows the second cycle of a programmed read from the controller where data is transferred from the holding latch (U15) to the CPU upon command. The second cycle of a DMA read is shown in Figure 4.6.12. The DMA address counter buffers are enabled to supply the 'to' address of the data transfer.

Note that programmed data transfers occur during the $\phi 2$ period of the system clock whereas DMA transfers occur during $\phi 1$.

The disk controller also contains the following networks:

1. Disk Unit Ready multiplexer.
2. Data/Clock separator phase-locked loop.
3. Disk controller data timing generator.
4. Disk status and control address decoders.
5. DMA control timing generator.
6. Busy/done network.

FIGURE 4.6.8 PROGRAMMED WRITE TO DISK CONTROLLER REGISTER

FIGURE 4.6.9 DMA WRITE TO DISK CONTROLLER REGISTER

FIGURE 4.6.10 PROGRAMMED DMA READ FROM DISK CONTROLLER REGISTER FIRST CYCLE

FIGURE 4.6.11 PROGRAMMED READ FROM DISK CONTROLLER REGISTER, SECONC CYCLE

FIGURE 4.6.12 DMA READ FROM DISK CONTROLLER REGISTER SECOND CYCLE

The disk unit ready multiplexer (U4, U54) selects one of the four unit ready inputs and outputs its level to the disk controller chip.

The input to the data/clock separator circuit is a pair of D-type flip-flops (U36) which samples the incoming data/clock stream and synchronizes the pulses with the loop oscillator which is running at 4 MHz. The width of the pulses are adjusted to 250 ns. $\pm$ 50 ns by a non-retriggerable one-shot (U23). The pulses are then separated by a gating pulse generated by a window counter (U51) which is driven by the loop oscillator. The separated clock pulses are phase compared (U49) with the loop oscillator divided down by 16 (U37). If a phase error exists between the clock and the divided loop oscillator an error voltage is generated at the output of the integrator (U39). This error voltage changes the loop oscillator frequency in a direction which will tend to reduce the phase error. The voltage-controlled oscillator (U50) uses fixed and trimmer capacitors as timing elements. The trimmer capacitor allows the PLL to be adjusted to an optimum operating range.

The disk controller data timing generator consists of a latch (U7) connected as a shift register, three D-type flops (U17, U18) and miscellaneous gates. This network generates eight sequential overlapping pulses (S1-S8) which produce $\overline{RE}$, $\overline{WE}$ and $\overline{CS}$ (U25, U58) for the disk controller I.C.

The disk status and control address decoders (U26, U27) develop all read/write strobes for the controller from $\overline{DEVSTRE}$, $\overline{BREAD}$ and address bits A0 thru A6.

The DMA control timing generator consists of a series of latches (U24, U46, U47) which provides timing signals for $\overline{DMAEN}$, $\overline{DMAWRT}$, $\overline{DMAPRI}$.

The disk controller PCB has a busy/done network contained on a separate pluggable circuit. It allows the CPU to check the operational status of the disk controller.

The disk controller I.C. (FDC) has four internal registers accessible by the CPU; they are the command/status, track, sector and data registers. Instructions are issued to the command register to cause the FDC to perform operations. At the completion of an operation the status register may be checked for error conditions. The track register will contain the current position of the disk read/write head after a seek or restore command. The sector register specifies the sector number for a diskette read or write operation. During the DMA read/write operation diskette data is transferred through the data register. This register is also used to specify the new track number for a seek operation.

The disk controller is capable of performing four classes of operations under software control; they are a restore, seek, read and write. A restore operation consists of the controller issuing repetitive step-out pulses to the selected disk drive until a track zero indication is received by the controller. This operation is necessary prior to others to coordinate the position of the disk read/write head with the FDC track register. To execute a restore operation the program must perform the following operations:

1. Select the desired disk unit by writing the unit number to location 51_h which generates a 'LDSEL' pulse at the clock input of the unit select latch (U29).
2. Select a write operation to the FDC command register by writing 000_h to location

50₈ which generates a 'LDCMD' pulse at the clock input of the register select latch (U43).

3. Write a restore instruction (002₈) to location 52₈. This generates a 'LDDT' pulse which strobes the instruction into the temporary holding register (U15) and triggers the data timing generator (U19-5) which will then transfer the instruction into the FDC command register.

At the receipt of the instruction the FDC will place the 'DIRECTION' output (U56-16) at a logic '0' and begin issuing 4 μ sec step pulses (U56-15) spaced 10 ms apart until the TRK00 input (U56-34) goes to a logic zero. The FDC then sets the track register to zero.

A seek operation consists of stepping the read/write head in or out to a new position specified by the value held in the FDC data register. The following operations must be performed to execute a seek:

1. Select a write to the FDC data register by writing 003₈ to location 50₈ which generates a 'LDCMD' pulse.
2. Write the new track number to location 52₈ which transfers the number to the holding register and then to the FDC data register.
3. Select a write to the FDC command register by writing 000 to location 50₈ (LDCMD).

4. Write a seek instruction (022₈) to location 52₈ which transfers the instruction to the holding register and then to the FDC command register.

After receiving the seek command the FDC places the DIRECTION output at the appropriate level determined by the old and new track numbers and begins issuing step pulses and incrementing/decrementing the FDC track register until it equals the new track number.

A read operation is accomplished by the FDC loading the head of the selected drive, locating the address field of the desired sector and transferring the data field into memory via DMA (direct memory access). This operation is performed by executing the following sequence:

1. Select a write to the FDC sector register by writing a 002₈ to location 50₈ (LDCMD).
2. Write the sector number to location 52₈ (LDDT) which is transferred to the FDC sector register.
3. Write the least significant FWA (first word address) byte to location 55₈ which generates a 'LDLSB' strobe at the load inputs of the LSB address counters (U30, U31). Write the most significant FWA bytes to location 54₈ which generates a 'LDMSB' strobe at the load inputs of the MSB address counters (U32, U33).

4. Select a write to the FDC command register and a DMA read by writing a 010_8 to location 50_8 (LDCMD).
5. Write a 'READ' instruction (214_8) to location 52_8 which transfers the instruction to the FDC command register.

Upon receipt of the read instruction the FDC places the HEAD LOAD output (U56-28) at a logic '1' level which triggers a 60 ms one-shot (to allow for mechanical settling of the disk head). The FDC checks for this timeout by polling the 'HLT' input (U56-23). When this input returns to a logic '1' level the FDC begins searching the serial data stream for an address field. When one has been located, the FDC compares the sector number with the contents of the sector register. If they are equal the FDC begins assembling data bytes and transferring them to memory by DMA. A DMA request is caused by the FDC setting the DRQ output (U56-38) to a logic '1' which triggers the sequence shown in Figure 4.6.13. If another read or write operation is not initiated after two revolutions of the diskette, the 'HLD' output of the FDC is returned to a logic '0'.

A write operation begins with the FDC loading the head of the selected drive, locating the address field and then transferring data from memory to the FDC where it is serialized, clock pulses inserted and presented to the drive.

The order of events required are identical to those required for a read operation with the exception of steps 4 and 5 which would be changed as follows:

4. Select a write to the FDC command register and a DMA write by writing a 000_8 to location 50_8 (LDCMD).

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FIGURE 4.6.13 DMA READ OPERATION TIMING

5. Write a 'WRITE' instruction (254_h) to location 52_h which transfers the instruction to the FDC command register.

In response to the write instruction the FDC loads the disk head, locates the specified sector and requests a DMA transfer from memory as in the read operation. At the appropriate time the FDC places WG (write gate, U56-30) to a logic '1' level and supplies the serial write data/clock stream (WD, U56-31) to a 250 ns $\pm$ 50 ns one-shot. At the completion of the write operation WG returns to a logic '0' level and WD becomes inactive. Once again the disk read/write head is unloaded if a new operation is not started before two revolutions of the diskette. Figure 4.6.14 illustrates the timing for a DMA disk write operation.

The process of issuing an instruction to the FDC command register causes the disk BUSY flag to be set and the DONE flag to be reset via pin 3 of the busy/done PCB. Issuing a read from location 2_h generates a 'DNCK1' strobe which places the DONE status on data bit 7 ($\overline{BD7}$). Issuing a read from location 4_h generates a 'BSYCK1' strobe which places the BUSY status on data bit 7 ($\overline{BD7}$). A read from location 0_h generates 'INTA1' placing the disk interrupt status on data bit 7 if the interrupt has not been masked.

Upon completion of an operation the INTRQ output (U56-39) of the FDC goes to a logic '1' level setting the DONE flag and clearing the BUSY flag.

During a read operation three types of errors may occur; they are record not found, CRC and lost data. A record not found error indicates that the FDC was not able to locate the sector specified for the operation. A CRC error indicates that the CRC character calculated from the data during the operation did not

FIGURE 4.6.14 DMA WRITE OPERATION TIMING

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RADIAN

equal that read at the end of the data field. A lost data error indicates that the FDC DMA support logic did not transfer the assembled data byte from the controller in time, in which case it was overwritten by the next data byte.

During a write operation four types of errors may occur; they are record not found, CRC, lost data and write fault. Once a write fault indication has been received from a drive, a write to location 53_h must be done. This generates a write fault reset strobe which clears the error in the selected drive.

An interrupt from the controller is cleared by a write to location 57_h.

4.7 ARITHMETIC PROCESSING UNIT, REAL-TIME CLOCK, AND RAINFALL COUNTER

This printed circuit board, hereafter referred to as the APU PCB, contains three independent circuits. First, it contains the interface circuitry for the AM9511 arithmetic processing unit integrated circuit. A full description of the arithmetic processing capabilities for that device is presented with its data sheet in Appendix D. Second, it contains the circuitry for a real-time clock with programmable interrupt rates, three of which are derived from A.C. line frequency, and the fourth of which may be a pulse from an external source. Finally, it contains the circuitry for a rainfall counter (or counter for other sources which provide contact closures); the latter circuit derives its power from the battery operated clock during A.C. power outages, and continues to operate until power is restored.

Reference is made to schematic diagram 500C3209-001 for detailed descriptions of circuit operation.

Real-Time Clock

The real-time clock provides interrupts at one of four time intervals: one interrupt per second, ten interrupts per second, 60 interrupts per second (50 in the case of 50 Hz line frequency), or an external signal.

A 60 Hz signal (50 Hz for 50 Hz line frequency) from the power supply assembly is applied, after limiting by R17, CR5, and CR6, to U30-5. The signal at U30-6 is a 60 Hz square wave. U9 is switch programmable as a divide-by-six (for 60 Hz) or divide-by-five (for 50 Hz) counter. After decoding, the output of U10-3 is a 10 Hz signal. Further division by decade counter U8 provides a 1 Hz signal.

The external pulse from a rear-panel terminal strip and J1-T is limited by R15, CR7, and CR8, applied to U30-11, and, after inversion, to U29-9. Interrupts can be selected to occur at the logic high or logic low levels of the external pulse by closing one (but not both) section of the DIP switch connected to U30-10 and U29-8.

The 60 Hz, 10 Hz, 1 Hz and external pulse signals are applied to selector gate U19. The desired interrupt frequency is selected by enabling one input to U19. This is accomplished by loading register U18 with a CPU write to device code 66₈, causing the four lower order bits of the data bus to be loaded into register U18. The output of U18 is also applied to U19, enabling one of the input frequencies to U19. The output of U19 is applied to the standard BUSY/DONE circuit, A1, at pin 9, causing DONE to become true and a CPU interrupt to occur. The DONE status is cleared by a CPU write to device code 67₈.

The truth table for software selection of the desired interrupt frequency is presented in Table 4.7.1 below.

TABLE 4.7.1 REAL-TIME CLOCK FREQUENCY SELECTION

<u>DATA BIT</u>	<u>FREQUENCY</u>
0	1 per second
1	10 per second
2	60 per second
3	External signal

Rainfall Counter

With the exception of the tri-state data bus driver, U25, power for the rainfall counter circuitry is derived from the +15 volt power supply (J1-20,X) during normal operation and from the battery supply for the battery operated clock (J1-V) during loss of A.C. line power. U25 is used only during CPU count requests, and is powered by the +5 volt supply.

The source of contact closures counted by the circuit is J1-Y, which is connected, through the mother board and a cable, to a rear-panel terminal strip. Transient protection and contact debouncing is provided by R14, varistor RV1, R4, CR1, CR2, R6, and C1.

The non-inverting input to operational amplifier U24 (pin 3) is biased to approximately one-half the supply voltage, +VC, by R13 and R12, with a slight amount of hysteresis provided by R11. When contacts are open, the inverting input of U24 (pin 2) is biased to near +VC, U24-6 is near ground potential, Q1 is in a non-conducting state, and U12-11 is near +5 VC. When contacts are closed, the inverting input to U24 is near ground potential, causing U24 to saturate and its output (pin 6) approaches +VC. Q1 is biased, by R10 and zener diode CR4, into a conducting state, and U12-11 switches to near ground potential.

U12 is a low-power CMOS type D flip-flop connected as a divide-by-two circuit. Its output is connected to a CMOS 7-bit counter, U26. Together, those two devices form an eight-bit counter whose output is connected to the tri-state bus driver, U25.

The contents of the rainfall counter can be determined by a CPU read of device code 65₈. That operation generates the

signal RFSTB- at U5-6 and pins 1 and 19 of U25, causing the contents of the counter to be gated to the data bus during the CPU read cycle.

Arithmetic Processing Unit (APU)

Five CPU commands can be transmitted to the APU. Two of the commands are write functions and three are read functions. Of the five commands, one of the read commands does not arrive at the APU integrated circuit. It is transmitted to an intermediate holding register following one of the other two read commands; this is necessary because data cannot be read from the APU in one CPU read cycle, and data must be transferred to the intermediate register and held for interrogation by the CPU on a subsequent read cycle.

The two CPU write commands are used to write data to the APU data stack (for subsequent arithmetic manipulation) and to write commands to the APU command register (to define the operation to be performed on data previously loaded in the data stack) and cause the APU to execute the command. The two CPU read commands to the APU integrated circuit are used to transfer the APU status to the intermediate register and to transfer data from the APU data stack ("answers" or results of arithmetic operations) to the intermediate register. The other read command causes the contents of the intermediate register to be transferred to the data bus during the CPU read cycle.

The four commands to the APU integrated circuit result in the signals LDBYT-, RDTC-, LDCMD-, and RSTC- being generated by U5 and transmitted to pins 4, 5, 1, and 2 of U22, respectively. U22-11 is the logical NOR of those four signals, with the signature DO-. This signal is applied to U2-3, causing pin 5 of that flip-flop to become true and enabling the 4-bit shift register

U3 to transfer a logical one from stage to stage. Either of the first two signals are applied to the reset input (pin 13) of U11 and cause the signal $\bar{C}/D$ (not command/data) to become true. Similarly either of the second two signals cause the signal $C/\bar{D}$ (command/not data) to become true. The signal $DO-$ also clears the PSZ signal at U2-9, clocks either pin 5 or pin 6 of U11 true, depending on whether the CPU cycle is a read or write cycle, and if the CPU is writing to the APU, clocks the data into register U17.

The signal KCLK, a buffered version of the CPU signal BKCLK-, is a continuous clock with a frequency of 7.6584 MHz. It is divided by four in U21 to provide the signal CLK for the APU chip. KCLK is used to clock the gated shift register, U3, which provides the timing for APU chip control lines.

Figure 4.7.1 is a timing diagram of key APU signals when the CPU writes data to the APU stack. The signal $DO-$ clears the PSZ flip-flop, clears DONE (if set), sets BUSY, clocks U2-5 to a logical one (enabling the shift register U3), clocks data from the CPU into register U17, and clocks U11-6 (WRITEF) to a true state. The signal $DO-$ is generated by the signal LDBYT- which, in turn, is generated by U5 in response to a CPU write to device code 60_8 , the CPU command for writing data to the APU stack. The signal LDBYT- generates the signal ACMD- at U11-13, causing the signal $\bar{C}/D$ to become true. Successive pulses of KCLK then cause a logical "one" to be propagated through the shift register U3, controlling a sequence of events. When U3-2 becomes true, the signal $CS-$ becomes false at U14-18, enabling the APU integrated circuit. When U3-7 becomes true, on the next pulse of KCLK, the signal $WR-$ becomes false at U1-18, setting the PSZ flip-flop and enabling subsequent shift-register stages. At this point, all necessary control signals have been

FIGURE 4.7.1 TIMING DIAGRAM FOR KEY APU SIGNALS WHEN THE CPU WRITES DATA TO THE APU STACK

generated to cause the APU integrated circuit to write data from the CPU data bus to the APU stack. That is, CS- has enabled the device, the false condition of C/D indicates that the internal data register and not the command register is to be selected, the false condition of WR- indicates that a write operation is to take place, and data from the data bus which was clocked into U17 by DO- is enabled to the APU IC by the false condition of READF at U17-1. After two additional pulses of KCLK, U3-14 becomes false, causing WR- to become true and causing U2-5 to become false; the latter condition allows a logical "zero" to be propagated through the shift register by succeeding clock pulses. When U3-14 becomes false, U3-15 becomes true, causing CLKDN- to become false at A2-9. After the next pulse of KCLK, CS- becomes true, disabling the APU integrated circuit. After three successive pulses of KCLK, U3-15 becomes false, causing A2-9 to become true; the latter condition causes DONE to become true, notifying the CPU that the operation has been completed.

Figure 4.7.2 is a timing diagram for key APU signals when the CPU writes a command to the APU integrated circuit command register for execution by the APU. The sequence of events is similar to those which occur when writing to the APU stack, with the following significant difference: The sequence is initiated by a CPU write to device code 61₈, resulting in LDCMD- becoming false at U22-1, and causing the signal C/D to become false for the entire operation. This condition inhibits the setting of the DONE flip-flop by U3-15. Instead, the DONE flip-flop is set by the signal END- which is generated within the APU integrated circuit and supplied to U23-1; END- is generated to indicate that the APU integrated circuit has finished the execution of the command with which its command register was loaded, and that the results of the command execution are available in the APU stack. The command execution time indicated in Figure 4.7.2 is a variable which is dependent on the particular command executed.

FIGURE 4.7.2 TIMING DIAGRAM FOR KEY APU SIGNALS WHEN THE CPU WRITES A COMMAND TO THE APU COMMAND REGISTER

Figure 4.7.3 is a timing diagram for key APU signals when the CPU causes data to be transferred from the APU stack to the intermediate register, U16. The sequence of events is initiated by a CPU read from device Code 62, resulting in the generation of the signal RDTC-, and causing the signal $\overline{C/D}$ to become true. Because a read operation is in progress, the signal READF (U11-5) becomes true and the signal WRITEF becomes false; this condition causes the signal RD- to become false during the sequence of events caused by the shift register operation. A further difference in this operation and previously-described operation is that the PSZ flip-flop is set by the signal PAUSE- from the APU integrated circuit rather than the signal WR-. Until the signal PAUSE- becomes true, propagation of a logical "one" through shift register U3 is suspended because the signal PSZ at U2-9 and U23-4 is false. When PSZ becomes true, the shift register sequence continues, causing data from the top of the APU stack to be clocked into the intermediate register U16 by the rising edge of the signal RD- at U16-11. DONE is set by the positive-to-negative transition of U3-15.

When the CPU reads device code 63₈, the contents of the APU status register is transferred to the intermediate register U16. The sequence of events is identical with those just described for the transfer of the contents of the APU stack to the intermediate register, with one exception. Reading device code 68₈ causes the signal $\overline{C/D}$ to become false. Thus, the DONE flip-flop is not set during this operation. The timing for this operation is such that it will be concluded by the time the CPU, under program control, can retrieve status information from the intermediate register.

The reading of either data or status information held in the intermediate register is accomplished by a CPU read of device code 64₈. That operation results in generation of the

signal INDT- by U5. When the signal INDT- is false at U15-1 and U15-19, the data held by the intermediate register U16 is gated to the data bus for retrieval by the CPU during the read cycle. The signal INDT- is also applied to A2-1, clearing the DONE status at the conclusion of the CPU read cycle.

FIGURE 4.7.3 TIMING DIAGRAM FOR KEY APU SIGNALS WHEN THE CPU CAUSES DATA TO BE READ FROM THE APU STACK AND TRANSFERRED TO THE INTERMEDIATE REGISTER U16

4.8 ANALOG-TO-DIGITAL CONVERTER AND DISPLAY

INTRODUCTION

The function of the analog-to-digital converter (ADC) is to convert analog data from a channel selected by the analog multiplexer to digital form. After conversion, the digital data is supplied either to the CPU if the conversion was the result of a request from that device, or to the front panel display circuitry if the conversion was the result of a request from that circuitry. The front panel display is updated approximately three times per second, and requires approximately two milliseconds per update. At all other times the ADC is available for conversion under program control from the CPU.

Circuit Operation

For purposes of discussion the ADC can be logically divided into four sections: the analog multiplexer interface, the ADC proper, the front panel display logic, and the front panel display.

4.8.1 Analog Multiplexer Interface

The analog multiplexer has input/output connections only to its analog input channels and to the ADC. That is, it has no direct connection to either the CPU or the front panel circuitry. It receives its two main operating parameters from the ADC; those parameters are the analog channel to be selected, and which of five available gains are to be applied to the analog data from the selected channel. The available gains are such that analog data with values of +10 millivolts, +100 millivolts, +1 volt, +5 volts or +10 volts will be converted to a digital value (+1000 decimal) which represents "full-scale" range for both the front panel display and the CPU.

The ADC board (Schematic 500C3249-001) receives multiplexer operating parameters (gain selection and channel selection) from two sources. When performing conversion under program control from the CPU, it receives those parameters from the CPU under program control. When performing a conversion to update the front panel display, it receives those parameters from the front-panel gain selection and channel selection switches.

When operating under CPU control, the channel and gain selection parameters are loaded into an ADC register by a write to device code 70₈. During that operation device code 70₈ is decoded by U20 to generate the signal LDCHS-. That signal clocks the eight bits of the data bus into tri-state register U4. Similarly, board selection parameters are stored in U3 by a CPU write to device code 71₈. In the normal, non-expanded, DART II with a single multiplexer board, the 3 bits of the latter parameter will all be logically zero. As will be later described, when the ADC has performed a conversion in response to a CPU command, the signal UPDATE will be false, enabling the tri-state outputs of U3 and U4 for use by the multiplexer board.

When performing a conversion to update the front-panel display, the front-panel thumbwheel switch settings are provided as inputs to tri-state buffer U2 and the front-panel gain-select switch setting is provided, after decoding by the diode circuitry CR1 through CR4, as an input to tri-state buffer U12. During this mode of operation, the signal UPDATE- is a logical zero, enabling the outputs of tri-state devices U2 and U12 for use by the multiplexer.

4.8.2 Analog-To-Digital Converter

Analog-to-digital conversion take place either upon command from the CPU or upon request from a free-running clock

which periodically generates a pulse to cause an update of the front panel display. In the event a conversion is taking place at the request of one command source at the time a request is made from the other command source, the latter request is "remembered" by the logic circuitry and executed upon completion of the conversion in progress.

Referring to schematic diagram 500C3249-001, the two logical signatures which cause conversion to take place are UPDATE and CPUCS, the former for an update of the front panel display, and the latter upon command from the CPU.

Consider the case where conversion is requested by the CPU. This occurs when the CPU executes a write to device 72₈. This command is decoded by U20 and sections of U19 and U21 to cause the signal STRT- at U20-3 and the standard BUSY/DONE circuit A1-3. (The remainder of this discussion will be facilitated by the timing diagram of figure 4.8.1). This signal causes BUSY (A1-18 and U25-10) to become true. If a front panel update is in progress, the signal UPDATE- is false (U25-9) and the CPU request is held pending completion of the update, at which time U25-9, U25-8 and U18-2 will become true. The next positive transition of the signal CLK, derived from U23-6 (a free-running clock with a period of approximately 2 μ s), at U18-11 will cause the CPU request to be latched at U18-9. Consequently, the signal CPUCONV- will become false at U19-3 and U25-12, U25-11 and U26-1 will become false, and pin 13 of the one-shot U26 will become true for approximately 2 ms. The falling edge of the signal at U26-13 and U26-9 will cause a short (approximately 1 μ s) pulse, STCONV, at pin 5 of one-shot U26.

The signal STCONV is routed to the ADC module, U5, and is a command for the module to perform an analog-to-digital conversion on the analog signal at U5-25. In the standard DART II,

FIGURE 4.8.1 TIMING DIAGRAM FOR KEY ADC SIGNALS IN RESPONSE TO AN ADC CONVERSION REQUEST FROM THE CPU

the sample-hold module U1 is not installed and pins 2 and 12 of the socket for that device are connected. Thus, the analog signal is derived from J1-13, which is connected to the analog multiplexer output.

Upon receipt of the STCONV command the end-of-conversion signal EOC, U5-17, will become false and remain false for the duration of the conversion by the ADC module. Upon completion of the conversion, EOC at U24-12 will become true and upon the next positive transition of CLK U24-9 and U29-2 will become true, generating a short pulse at U29-13. After buffering, this pulse becomes DEOC at U23-8 and U19-4. Because CPUCS is true at U19-5, CLKDN- will become false at U19-6 and A1-9, causing DONE to become true and BUSY to become false at A1-18 and U25-10. Consequently, U25-8 and U18-12 will become false, and upon the next positive transition of CLK, CPUCS will become false.

At this point the conversion requested by the CPU has been completed, and the CPU can determine that the conversion is complete by either of two methods. First, if the interrupt mask bit within the BUSY/DONE circuitry (A1) has not been set by the CPU, the setting of DONE which A1 will cause IRQ- to become false at A1-12 and J2-Y, causing an interrupt request to be sensed by the CPU if interrupts are enabled within the MPU. Alternatively, the CPU can determine, under program control, that the conversion is complete by polling the DONE status of external devices. This is accomplished by reading memory location four. When this occurs, DNCK1- becomes false at J2-U and U10-6 and DNCK becomes true at U10-14 and A1-11. When DONE is true, DNCK causes A1-10 to become false during the read operation by the CPU. A1-10 is connected to data bus bit 4, the bit assigned to the ADC DONE status.

The ADC module, U5, converts analog data to a 12-bit digital value. The module is connected to provide the converted value in 2's complement binary notation. It linearly converts values from -10 volts to +9.9951 volts to binary numbers ranging from -2048 to +2047. The ADC module, in conjunction with selectable gains in the Analog Multiplexer which supplies its analog input, has been assigned a "full-scale" range corresponding to each of five available gains. The full-scale range of $\pm V$ volts will produce a value of ± 1000 in the ADC module after conversion. Thus, for a particular selected full-scale range, the ADC has slightly in excess of 100% overrange capability; the one exception to this overrange capability is the ± 10 volt range, which cannot have 100% overrange because of linearity limitations in the Analog Multiplexer.

After the CPU determines that the conversion is complete, the digital representation of the analog voltage can be retrieved by the CPU under program control. The 12 bits are transferred to the CPU over the system data bus in the form of two 8-bit bytes. One byte (the least significant byte) contains ADC module bits four through eleven, and the other byte (the most significant byte) contains bits zero through three, with the most significant bit (B0-) "sign-extended" to fill in the remaining four bits of the byte. The bytes are transferred by the CPU reading address locations 74₈ and 75₈. Those addresses are decoded by the circuitry of U20, U21, and U19 to generate the signals INA- and INB-, respectively. The signal INA-, on pins 1 and 19 of U6, causes the least significant byte to be transferred to the system data bus during the CPU read operation. Similarly, the signal INB- causes U8 to transfer the most significant byte.

Consider now the case where the ADC conversion takes place to provide an update of the front panel voltage display.

For reference, a timing diagram is provided in Figure 4.8.2. Q1 and its associated circuitry form a free-running unijunction oscillator which generates a pulse approximately two to three times per second. Those pulses initiate update cycles for the front panel display. The pulse from Q1 is shaped by U23 and U28, providing at short duration negative pulse at U28-4, U18-4 and U11-1, setting flip-flop U18 and providing a true signal at U25-2. This constitutes a conversion request to the ADC circuitry, and the request is latched in U18 and until it is serviced.

If a conversion is in progress in response to a CPU request, CPUCONV- will be false, and no further action in the front panel display update cycle takes place until CPUCONV- becomes true, indicating that the ADC circuitry is available for use. At that time U25-3 and U22-12 become true, and on the next positive transition of CLK, the signal UPDATE becomes true at U22-9. When UPDATE becomes true, the falling edge of UPDATE- at U25-13 causes the ADC module to perform a conversion in a manner which is identical to that caused by the falling edge of CPUCONV- at U25-12.

When the conversion is complete, the signals DEOC and UPDATE cause generation of FPCLR- at U11-6 and J1-1 for use by the front panel ADC display logic, and at U22-1 to cause the signal ALZERO- to become true at U22-6 and U17-9. Simultaneously, the signal DEOC- causes the digital output of the ADC module to be loaded into the 12-bit binary counter formed by U14, U15, and U16. Also simultaneously, FPCLR- clocks the value of the most significant (sign) bit of the ADC module into the flip-flop U24, causing the signal PSIGN at U24-6. PSIGN is inverted by U13 and provided for use by the front panel display logic at J1-15. PSIGN is also provided to pins 5 of U14, U15, and U16, causing the counter to be a down-counter if the most significant bit of the ADC module (B0-) indicates that the converted value

FIGURE 4.8.2 TIMING DIAGRAM FOR KEY ADC SIGNALS DURING AN UPDATE OF THE FRONT PANEL VOLTAGE DISPLAY

is a positive number in 2's - complement notation. Conversely, if B0- indicates a negative number (B0- is a logical "one", or true), the counter will be an up-counter.

The 12-bit binary counter formed by U14, U15, and U16 is a part of a binary to binary-coded-decimal (BCD) conversion process. The other part of the process consists of a BCD counter in the front panel ADC display logic, and will be discussed in the description of that circuit. The purpose of the binary counter is to generate a number of sequential pulses equal to the binary number with which it was loaded. The characteristics of 2's-complement binary arithmetic notation are such that, for a positive number, the number of clock pulses required to cause the binary counter to count down to a value of zero are numerically equal to the binary number loaded in the counter at the beginning of the process. Similarly, for a negative number, the number of clock pulses required to cause the binary counter to count up until it overflows is numerically equal to the contents of the counter at the beginning of the process.

After the pulse DEOC- has loaded the counter and PSIGN has provided the up/down steering input, U17-9, U17-10, and U17-13 are all logically true, allowing subsequent pulses, CLK, to appear in inverted form as CTRCLK- at U17-8 and the clock input to the binary counter, U16-14. An inverted version of this signal also appears at U13-4 and J1-14 as FPCLK, for use by the front panel ADC display logic. The binary counter continues to be clocked by CTRCLK- until it reaches the value of zero (counting down for positive numbers) or until it overflows (counting up for a negative number), at which time the proper number of pulses have been supplied to J1-14. The counting process is terminated by the setting of flip-flop U22, causing ALZERO- at U22-6 and U17-9 to become false, thereby suppressing further clock pulses at U17-8. For negative numbers, when counting up, the overflow signal, RC-, is generated at U14-13, and provided as a direct clock

signal to U22-3, setting U22 and terminating the count. For positive numbers, a value of zero within the binary counter is detected by decoding the simultaneously true states of M/M1, M/M2, M/M3, and PSIGN; that decoded state provides a signal at U17-6, U11-2, U11-3, and U28-10. A short pulse is generated at U28-12 and U22-4, setting flip-flop U22, and terminating the count. The rising edge of the signal ALZERO at U25-4 causes U18-5 to become false and upon the next positive transition of CLK at U22-11, the signal UPDATE becomes false, completing the ADC front panel update cycle.

4.8.3 Analog to Digital Converter Display Logic

The A/C Display Logic printed circuit board (Schematic 500C3261-001) plugs directly into the A/D Display printed circuit board on the front panel. It has several functions. First, in conjunction with the 12-bit binary up/down counter on the ADC printed circuit board, it is a binary to BCD converter. Second, it formats the front panel display according to the front panel "Gain Select" switch setting and provides for proper placement of the display decimal point. Finally, it provides for multiplexing the display so that the seven-segment L.E.D. display devices can be driven with a single BCD to 7-segment decoder/driver.

U14, U3, U17, U7, U18, and a single binary section of U9 form a BCD ripple counter with the least significant digit on the left (U14). It will be recalled that FPCLR- is generated by the ADC just prior to its generation of a sequence of FPCLK signals when in the front panel update cycle. The FPCLR- signal is used, after buffering the U1, to generate the signal CLR, which clears the BCD counter chain to zero and clocks the setting of the front panel Gain Select switch into registers U12 and U13. The sequence of FPCLK signals is buffered by U1 to provide the sequence of clock pulses CLK. The entry point of the CLK signals

into the BCD counter chain is determined by combinational logic operating on the gain selection setting held in U12 and U13. Only if the 10 mv full scale gain is selected does the sequence of CLK pulses enter U14. If 100 mv or 5V gains are selected, the CLK pulses enter U3. Otherwise, the CLK pulses enter the BCD counter chain at U17. Once the CLK pulses have entered a decade counter, the output of the counter is gated on down the chain to the next decade counter, with a single exception. U3 functions as a true BCD decade counter in all cases except when the gain selection is 5V. In this case U3 functions as a simple divide-by-two counter, and the divide-by-five section is not used; instead, the output of the divide-by-two section is gated to U17 and following counter stages. This has the effect of transferring five times as many clock pulses to U17 and following stages as would normally be the case, and is necessary because the 5V range is not a decade range, as are all other ranges.

The BCD outputs of the counter stages serve as inputs to tri-state buffers U6, U8, and U10. On the 5V range the QC output of U3, which is normally a logical zero, is manipulated by sections of U4 and U5 before being transferred to the 2A3 input of U6. The basic resolution of the front panel display is $\frac{1}{1000}$ of the full scale range. Therefore, on the 5V range, the least significant digit must have a value of either zero or five. However, because the divide-by-five section of U3 is not used on the 5V range, U3 will have a value of zero or one. Therefore, when U3 has a value of zero, the 2A3 input to U6 is allowed to have a logical zero value. However, when U3 has a value of one (QA is a logical one), the 2A3 input to U6 is forced to a logical one, with the result that the input to U6 has a BCD value of 5. Thus, U6 will always receive from U3 a value of zero or five on the 5V range.

Identically BCD-weighted outputs (DA, DB, DC, and DD, corresponding to BCD weights of 1, 2, 4, and 8) of U6, U8 and U10 are bused together and supplied to the display PCB. The outputs can be bused, provided only one of the tri-state devices is enabled at any given time. This is accomplished by sequentially enabling the devices with the signals LD0- through LD4-. R1, C1, and a section of U1 form a free-running oscillator whose pulses serve as the clock pulses for the divide-by-five counter section of U9. The outputs of that counter are supplied to the BCD-to-decimal decoder U11, causing the signals LD0- through LD4- to be generated sequentially; those signals are also supplied to the front panel display PCB for synchronization of enabling the display digits with the appropriate digit value from this section.

On the 1V or 10V ranges the BCD value of the ADC output is always held in U17, U7, U18, and U9. Therefore, the display digits corresponding to U14 and U3 must be blanked on those ranges. This is accomplished for the display digit corresponding to U3 by decoding the simultaneous occurrence of the signals 1V + 10V and LD1- and generating the signal XLD1- at U4-11. That signal is used to blank the appropriate digit on the 1V or 10V ranges. Similarly, the display digit corresponding to U14 must always be blanked except on the 10 MV scale, when it has values other than zero. That is accomplished by routing the gain-select switch setting corresponding to the 10 MV range to the display PCB, which has circuitry to enable that digit only when the signal S10MV- is false.

The signal FPSGN- is received from the ADC, inverted to form the signal PLUS, and supplied to the display PCB to enable the vertical segment of the +indicator when the ADC determines that a positive analog voltage has been converted.

The signal DPT is generated at U15-6 whenever the gain select switch is in either the 5V or 10V position.

The signal EN1 is generated at U9-12 whenever the converted analog voltage equals or exceeds the full-scale range on the 1V and 10V ranges; it is routed to the display PCB.

4.8.4 Analog to Digital Converter Display

The ADC display (Schematic 500D3257-001) receives BCD data and format signals from the ADC display logic PCB, to which it is attached, and displays the data on seven-segment, front panel, L.E.D. indicators.

There are 6 digits of display information, the left-most of which is reserved for ± 1 indication. The common anode devices are packaged as two digits per package, and are driven in parallel (except for the ± 1 indicator) by seven-segment information from the BCD to seven-segment decoder/driver U6 through seven DIP current-limiting resistors, U5. U6 receives its BCD data, DA, DB, DC, and DD from the ADC display logic PCB. The anodes of the display devices receive current from transistor switches Q2, Q5, Q7, Q8, and Q9, when these switches are enabled by signals LD0-, LD1-, LD2-, LD3-, and LD4-, respectively. The current supply for Q2 is controlled by Q1, which is enabled only when the signal S10MV- is false. The current supply for the remaining switches is controlled by Q6, Q4, and the signal XLD1-. XLD1- is false when LD1- is false and either the 5V or 10V gain ranges are selected. This has the effect of disabling the current supply for Q5, and blanking the digit that it would otherwise intensify.

The signal EN1 has the effect of intensifying the "1" in the ± 1 indicator when it is true.

The signal PLUS has the effect of intensifying the vertical segment of the + indicator when it is true. The horizontal segment of the + indicator is intensified at all times by the current path from its cathode to ground through R6.

The signal DPT is true except when the 5V or 10V ranges are selected. This causes U1-3 to be false and has the effect of intensifying the decimal point just to the right of the +1 indicator. When DPT is false, the decimal point one digit further to the right is intensified.

4.9 ANALOG MULTIPLEXER

Introduction

The function of the analog multiplexer is to select one of 32 differential analog data channels specified by control signals from the ADC board, convert the differential signal to single-ended form, apply one of five available gain factors also specified by control signals from the ADC, and make the selected, conditioned analog data available to the ADC.

Each of the five available gain selections has associated with it independent gain and zero adjustment potentiometers.

Reference is made to schematic diagram 500D3253-001 for the following description of circuit operation.

Circuit Operation

Each input channel is provided with input overvoltage protection by means of a series input resistor and diodes, clamping the input voltage to the solid state multiplexer to a maximum value corresponding to the positive or negative supply voltage. The actual signal multiplexing is accomplished by four, 8-channel, differential multiplexers, U12, U13, U14, and U15. The channel selected for output from each of the multiplexers is determined by the 3-bit binary control signal comprised of A0, A1, and A2. However, the multiplexers are actually switches, and no output occurs unless the enabling signal, ENX, at pin 18 is a logical one. Thus, the outputs of the four multiplexers are bused, and only one of the four is enabled at any one time.

The bused differential outputs of the multiplexers, SIG+ and SIG-, are applied to circuitry comprised of U9, U16, U28, and U29. The purpose of that circuitry is to provide two

single-ended output signals, HLSIG and LLSIG, at different signal levels. HLSIG is a zero-gain version of the differential input signal, but is single-ended. LLSIG is a single-ended version of the differential input signal to which a gain of 10 has been applied.

Indicated on sheet 1 of the schematic diagram are six sections of resistor networks which provide for zero and gain ("SPAN") adjustment for each of the five standard gain selections and one spare selection for special, non-standard applications. The signal HLSIG is used for full-scale gain ranges of $\pm 1V$, $\pm 5V$, and $\pm 10V$. The signal LLSIG is used for full-scale gain ranges of ± 10 mv. and ± 100 mv. Because the principles of operation for all six networks are identical, operation for only a single gain will be described.

Consider the case where the full-scale range is $\pm 1V$. The signal HLSIG is provided to series resistors R39 and R40, to provide the signal 1V. When the $\pm 1V$ range is selected, the signals GNS0, GNS1, and GNS2 will be logical zero, and the solid-state switch U23 will connect the signal 1V to U25-2. Thus, R39 and R40 constitute the input resistance to operational amplifier, U25; in conjunction with feedback resistor R16, the gain of U25 is established, with minor gain adjustment available by means of potentiometer R39. In order to provide for zero adjustment, the summing junction at the signal 1V is provided with means for injecting a small, variable offset voltage. The voltage-divider network R42, R43, and R44 is referenced to precision reference voltages +VR and -VR. +VR and -VR are derived from U26, U27, and reference diode VR1, to provide stable reference voltages of approximately +8 volts and -8 volts. The voltage required for compensating small offsets induced elsewhere is injected at the point 1V through summing resistor R41, and is adjusted by potentiometer R44.

The output of U24 is the conditioned analog voltage supplied to the ADC. In the normal configuration the analog switch U24 is not installed, and pins 9 and 10 are connected with a jumper, connecting the analog output to J1-S and, by means of the mother board, to the ADC board.

Channel selection is provided by the signals CHS0 through CHS4 from the ADC board. Assume for the moment that the signal ENSEL- is a logic zero and that the signal ZBDSEL- is a logic 1. The three least significant bits of the channel selection code (CHS0 through CHS2) become the signals A0 through A2 and are applied in parallel to all four multiplexers. The two most significant bits of the channel selection code (CHS3 and CHS4) are decoded by U10 to produce one of the signals EN1 through EN4 to enable the output of one of the four multiplexers.

Gain selection is provided by the signals GNS0 through GNS2 from the ADC board. With the same assumption that the signal ZBDSEL- is a logic 1, the 3-bit selection code is routed, by sections of U22, to the 8-channel analog multiplexer U23. The code is decoded within that device to select one of the six resistance networks for connection to the inverting input of U25.

The remaining circuitry (viz., that circuitry which generates the signals ENSEL-, ZBDSEL-, and ENOUT-) is provided for applications in which the number of available channels is expanded beyond the 32 provided in the standard DART II configuration. U19 is a three section DIP switch that allows up to eight analog multiplexer boards to be uniquely identified. That switch, in conjunction with the "board select" signals BDS0 through BDS2 from the ADC allows unique selection of one of eight boards (one of 256 channels). In the standard configuration all sections of U19 will be open and the signals BDS0 through BDS2 will be at a logic zero level. In that case pins 3, 4, and 5 of U20 will be at a logic one level, ENSEL- will be a logic zero

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and ZBDSEL- will be a logical one, satisfying the previous assumptions made when describing channel and gain selection.

4.10 BATTERY CLOCK AND DISPLAY

General Description

The battery clock displays time as seconds, minutes, hours, days, months, and year. Time can be read by the computer and is set from the front panel. If AC power fails, the clock can operate on battery back-up power for more than thirty days. For the following general description, the battery clock will be divided into three sections: the time base, the counter section, and the display and output section. For the display section refer to schematic diagram 500C3245-001. Otherwise, refer to schematic diagram 500C3241-001.

Time Base

The time base provides one pulse per second to the counting section in the clock mode, and two pulses per second in the set-time mode. When AC power is available, as in normal operation, the 60 Hz frequency of the AC line provides the time reference. During battery operation a crystal oscillator serves as the reference. Clock counting is inhibited during a computer time read to ensure good data. If a count is missed during a computer read operation, it is made up after the read is completed.

Counter Section

Five pairs of counters count seconds, minutes, hours, days, and months. The number of days are adjusted for each month. Hours follow the 24-hour clock convention.

Time may be set from the front panel when the set-time switch is in the set-time position. Four push button switches labeled months, days, hours, and minutes cause their respective counters to increment twice a second when pushed. The seconds

are not set by a front panel control. They can, however, be closely synchronized to a time reference by simply starting the clock (placing the set time toggle switch in the run position (down)) when the second counts for the two clocks are the same.

The two digits representing year are not a part of the counter section. The year function must be manually set by means of an eight section switch (representing two BCD digits) on the printed circuit board.

Display and Output Section

Clock time is displayed on the front panel, except when the clock is operating on battery back-up power. The computer may request that either the years, the months, the days, the hours, or the minutes be output to its data bus, and may obtain the complete time by a series of requests. Any change of time will be postponed while the computer is reading the time.

Detailed Description

Time Base

The 245 KHz crystal oscillator frequency is divided by 4096, giving a 60 Hz output at U32-1. Sixty cycle AC, brought in from edge connector J1-18 is squared, differentiated, and applied to the reset of U32, synchronizing its output to the AC line frequency (when primary power is lost, the clock runs solely off the crystal). Further division by 60 is provided by U20, U21, and U22, resulting in a one cycle-per-second input to U33-14.

Integrated circuits U33, U13, and U12 function as a differentiator with outputs U12-11 and U12-10. The differentiator produces short pulses occurring at transitions of the one Hertz input, as shown in Figure 4.10.1.

FIGURE 4.10.1 ONE SECOND TIME BASE WAVEFORMS

Output U12-11 will be referred to as PS-A (pulse source A) and output U12-10 as PS-B.

Pulses from PS-A go to gate A which is controlled by FF-A. Pulses from PS-B go to gate B which is controlled by FF-B. The outputs of gates A and B are OR-ed together and taken to FF-U22 through jumper W1. FF-U22 triggers the incrementing of the clock.

Usually, the outputs of gate control flip-flops FF-A and FF-B are high, gate A is enabled and gate B is disabled, and pulses from PS-A are gated through, while those from PS-B are blocked. The one-per-second pulses from PS-A clock FF-U22, causing the clock to increment once a second.

The following describes events initiated by a reading of the clock time by the computer and refers to the timing diagram of Figure 4.10.2.

When a computer time read occurs, CTR clocks FF-A low, disabling gate A and preventing the passage of any pulses from PS-A. FF-A is reset high by pulses from PS-B (which occur midway between pulses from PS-A as shown in Figure 4.10.1).

As shown in Figure 4.10.2, if the CTR occurs during Period I, FF-A will be reset by a pulse from PS-B and gate A will be re-enabled in time to pass the next pulse from PS-A. In this case the clock increments as usual.

If the CTR occurs during Period II, however, FF-A will not be reset in time to pass the next pulse from PS-A, and the clock misses a count.

FIGURE 4.10.2 COUNT INHIBIT-TIMING

This freezes the time for a short period, ensuring that the computer will access stable data.

When the clock misses a count, it is made up one-half second later by gating through a pulse from PS-B. The missed count is detected by FF-B. Every pulse from PS-A clocks FF-B low; the pulses, if gated through, also clock FF-U22, which in turn resets FF-B high. If a pulse from PS-A is not gated through and the clock misses a count, FF-B remains low, enabling gate B. The next pulse from PS-B is then gated through, incrementing the clock and resetting FF-B.

In the set-time mode, a low on SET TM- enables gate B so that pulses from both PS-A and PS-B are gated through to FF-U22.

Signal TM CLK is the buffered output of U22-2. When U22 is clocked by PPSEC, TM CLK goes high, clocking all enabled counters in the counter section. Signal PRE CLK is a delayed version of TM CLK which is used to clear the reset flip-flops. A timing diagram showing the generation of TM CLK/PRE CLK is shown in Figure 4.10.3.

Counter Section

The counter section consists of five stages of counters. Each stage is made up of a units counter, a tens counter, circuitry to detect the maximum count for that stage, a reset flip-flop, and with the exception of the first stage a multiplexer to select the appropriate count-enable input.

All counterclock inputs are tied to the same line, TMCLK, so operation of the entire counting section is synchronous. Counting is controlled by the counter enable inputs. The operation of all stages is similar and will now be described.

FIGURE 4.10.3 TM CLK/PRE CLK

Counting in each stage is accomplished by a pair of synchronous BCD decade counters. Additional circuitry is required to:

- 1) Count in the required modulo, i.e., modulo 60 for seconds and minutes.
- 2) Provide for a carry between stages.
- 3) Disable carry and provide for a manual count-enable in the set-time mode.

Modulo and carry functions operate as follows:

Each stage has a "maximum count" gate, the output of which goes high when that stage and all preceding stages have reached the maximum count. A high output from this gate causes the following events to occur at the next TM CLK pulse:

- 1) The reset flip-flop (U14) is clocked high, activating the preset function of the counters, setting them to their minimum count.
- 2) The succeeding stage increments, having been enabled by the high level output of the maximum count gate.

The reset flip-flops are cleared after each TM CLK pulse by a pulse on the PRE CLK line.

The days stage has a variable maximum count, depending on the month. Integrated circuits U35, U16, U36, and U25 decode the month and day to produce the maximum count output. Except for the second month (February), U36-13 is low and U16-3 reflects

the state of U25-4. A high level at U25-6 (output of maximum count gate) requires that both TD2 and TD1 be high, and that UD1 be high or low, depending on the state of U16-6. If U16-6 is high, then days = 30 will give a maximum count output. If U16-6 is low, then days = 31 will generate the output. The table in Figure 4.10.1 shows the state of U16-6 for each month, and the corresponding count of days which gives a maximum count output. U36-13 is high when the month = 2 and UD8 is high, giving a maximum count output when days = 28 in February.

In the set-time mode, the enable select multiplexers (U3) select the B inputs. Each stage then functions independently and is enabled by a push button on the front panel.

<u>MONTH</u>		<u>U16-6 → MAX. COUNT</u>	
Jan.	01	L	31
Feb.	02	--	--
March	03	L	31
April	04	H	30
May	05	L	31
June	06	H	30
July	07	L	31
Aug.	08	L	31
Sept.	09	H	30
Oct.	10	L	31
Nov.	11	H	30
Dec.	12	L	31

FIGURE 4.10.4 NUMBER OF DAYS IN MONTH

Display and Output Section

Outputs of all counter stages and the year switches are taken to multiplexers U41, U38, U30, and U27, which gate through the outputs of a selected stage. From the multiplexer, outputs of the selected stage then go to the BCD-to-seven segment display drivers and to the bus drivers U7.

The clock display consists of six pairs of seven segment L.E.D. displays corresponding to the five pairs of counters and the year-set switches in the counter section. Decoder U14 decodes the multiplexer select lines and energizes the pair of L.E.D. displays corresponding to the counter stage being output from the multiplexer.

The multiplexer select is generated by counter U14, which by counting up causes the multiplexer to cycle through all counter stages, resulting in a multiplexed display.

During a computer time read, $\overline{\text{STRE}}$ goes low, activating the counter's (U13) load function and passing FPA0, FPA1, and FPA2 on to the multiplexer select inputs. FPA0, FPA1, and FPA2 come from the computer address bus, allowing the computer to select the counter stage to be output. Simultaneously, bus driver U7 on the clock PCB is enabled, transferring the selected counter stage to the computer data bus.

4.11 DEVICE CONTROLLER

INTRODUCTION

The function of the device controller (DVC) is to provide a means of turning various devices on and off either manually or under program control. It has 16 switch inputs, each controlling one of 16 outputs. The momentary closure of an input switch causes the associated output to change states, turning it either on or off. The output status can be either read or altered by the CPU. Each output is a solid state switch closure for driving devices such as lamps and relays. The schematic diagram for the DVC is drawing 500D3233-001.

Two of the inputs and outputs have a preassigned function. The input switches are located on the front panel, and are labeled "Keyboard Printer" and "Floppy Disk". The outputs are used to control relays which control the AC power for a keyboard-printer (through a power receptacle on the back panel) and for the floppy disk drive motor. The input switches connect to J1-15 (TTYS-) and J1-16 (FLPYS-). The outputs are J1-T (TTYON-) and J1-S (FLPYON-).

MANUAL CONTROL

When one of the device switches TTYS- ... SB7- is depressed manually, the signal SWCLK- (U15-11) is generated. The signal generated by a device switch closure is also inverted to generate one of the signals TON...SB7.

The clock pulse CLK- (U6-12, U21-11, U21-3), with a relatively long period (≈25 ms), serves to debounce the input from the device switches. When a device switch is depressed, the rising edge of SCLK- will clock U21-9 high and SWCLK- low.

Thus, SWCLK- is a pulse whose duration is equal to the period of SCLK-.

The two signals generated by a device switch closure (SWCLK- and one of TON...SB7) serve as inputs to the circuit on sheet 2 of the schematic which will turn the device corresponding to the depressed switch on or off.

The Q output of the flip-flops (U24, U12, U26 and U25) indicates the status of the devices being high if the device is on, low if it is off. If a Q output is low when the device switch is depressed, the output of the associated exclusive-OR gate (U19, U23, U9 and U10) will be high. In the manual mode, this input will be selected by one of the multiplexers U (u.c.) U13, U4 and U3) and output of the associated flip-flop which will toggle on the rising edge of its clock input, SWCLK-. The $\bar{Q}$ output of the flip-flop will go low. After being inverted, the $\bar{Q}$ is applied to the base of a transistor, turning it on.

If a Q output is high when the device switch is depressed, the output of the exclusive-OR gate will be low. This will toggle the flip-flop causing $\bar{Q}$ to go high, turning the device off.

Thus, the effect of depressing a device switch is to toggle a flip-flop and change the state of the corresponding device. When any device switch is depressed, SWCLK- will clock data into all the device flip-flops, toggling the one whose switch has been depressed and leaving the rest unchanged.

CPU CONTROL

The CPU can read the status of the devices or turn them on and off by directly addressing the device controller.

When the CPU executes an instruction to read address 20_8 or 21_8 , the signal READA- (U28-1) or READB- (U28-3) will be generated on the device controller board. The signal READA- is generated when address 20_8 is decoded and BREAD is high; READB- is generated from address 21_8 and BREAD. READA- will enable the signals TTYF...SA7F, which reflect the on/off status of eight devices onto the data bus. READB- will place SBOF...SB7F on the data bus.

To change the output status under program control, the CPU executes an instruction to write into address 20_8 or 21_8 , causing signals WRTA- or WRTB- respectively to become false. The corresponding multiplexers (U14 and U13 or U4 and U3) will then select the data bus input (inverted by U5) and output it to the flip-flops. The flip-flops are then clocked by the positive transition of WRTA- or WRTB- at the end of the write operation, storing the data into the flip-flops. Thus, if a given bit on the data bus is false, the corresponding device will be turned on; if it is true, the device will be turned off.

4.12 STATUS INPUT CONTROLLERIntroduction

The function of the Status Input Controller (SIC) is to provide a means for the CPU to determine the status of up to 32 external contact closures or external logic signals. The SIC provides the status of four groups of eight bits; each group of eight bits may be independently read by the CPU. Drawing 500D3229-001 is the schematic diagram for the SIC.

Operation

External signals, by means of a back-panel connector, an interior ribbon cable, and mother board connections are provided as inputs to four eight-bit type D latches, U3, U4, U5, and U6. The status of the external signals is clocked into the latches by the signal SCLK-, a clock signal generated by the free-running unijunction oscillator Q1 and associated passive components. The outputs of the tri-state latches are bused together and provided as inputs to the tri-state octal bus driver U7. The CPU may determine the status of a group of eight bits by reading one of the device codes 30_8 , 31_8 , 32_8 , or 33_8 . Those device codes are decoded by U2 to produce the signals EN1-, EN2-, EN3-, and EN4-, respectively. A particular ENX- signal enables the tri-state outputs of a particular latch. Any of the ENX- signals enable U7 to transfer the contents of the selected latch to the data bus during the CPU read operation.

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4.13 I/O CONTROLLER

Introduction

The I/O Controller (IOC) can perform all the functions of the Status Input Controller. However, it has the additional capability of being configured, in eight-bit groups, as an output device. As an output device it provides solid-state switch closures for driving devices such as lamps or solenoids.

The schematic diagram for the I/O controller is drawing 500D3277-001.

Operation

Each of the four eight-bit sections of the IOC may be independently configured as either an input port or an output port by the addition or deletion of certain components and jumper connections. Sheet 2 of the schematic drawing illustrates the component complement and jumper connections required for configuring a section as either an input or an output section.

The device may be further configured to respond to device codes 30₈ through 34₈ or to device codes 130₈ through 134₈, depending on the position of jumper J2. Device codes 30₈ through 34₈, (or 130₈ through 134₈) in conjunction with the signal BREAD are decoded by U9 to generate the signal RDX- or WRX- for section X, depending on whether the CPU is reading section X configured as an input section or writing to section X configured as an output section.

Input Configuration

Referring to the input configuration for section A on sheet 2 of the schematic diagram, data inputs are provided to the D inputs of octal latch UA4. The clock input to the latch is SCLK-, generated by the free running oscillator comprised of

U10, R11, and C2. Data held in the latch may be read by a CPU read of device code 30₈. That read operation generates the signal RDA-, which enables the tri-state bus driver UA7 to gate the contents of the latch to the system data bus.

Output Configuration

Referring to the output configuration for section A on sheet 2 of the schematic diagram, the data inputs for octal latch UA4 are the inverted bits of the system data bus, provided by U8 at any time device 3X₈ is addressed. The clock for latch UA4 is WRA-, generated during a CPU write to device code 30₈ by U9. The Q outputs of the latch are connected to inverting driver UA1 whose outputs are connected to the same back-panel connector pins that are used in the input configuration. When the input to a section of UA1 is a logical one, that solid-state switch is closed, providing a current path to ground for the device which it is driving; otherwise, the switch is open.

4.14 BUS TERMINATOR

The bus terminator board (schematic diagram 500A3352-001) resides in one of the DART II spare card cage slots. Its purpose is to provide a resistive termination for all system data bus and address bus bits to +5 volts. It provides, for example, pull-up resistors for the open-collector gates on the BUSY/DONE circuits distributed throughout the system.

The circuit consists simply of three DIP resistor networks and filter components for the +5 volt bus.

4.15 NINE TRACK MAGNETIC TAPE INTERFACETheory of Operation

The magnetic tape interface provides an interface between the mag tape unit, which is a nine track write-only unit, and the computer, allowing the computer to write data, issue transport commands, and read tape unit status. Refer to schematic diagram 500D3273-001 for the following discussion.

To issue a command, the computer first loads the command register (U10) by writing one of the following octal codes into address 60_8 .

- 10 - Write End of File
- 04 - Write End of Record
- 02 - Rewind
- 01 - Write Data

If data is to be written, it must first be loaded into the data register (U11 and U4) by writing into address 61_8 .

To initiate the command, the computer addresses location 62_8 , resulting in a pulse being generated on the proper control output to the tape unit.

Addressing location 62_8 takes START- low, clearing DONE, and setting BUSY. If the tape unit is ready and not gapping, flip-flop U21 is set by U14, triggering one shots U17. One one-shot generates a 50 μ sec pulse which is gated to the command output selected by the command register. The other one-shot clears BUSY and sets DONE after a 3 msec delay, at which time an interrupt signals the computer that another command may be given.

The computer may obtain the tape unit status by reading address 60₈. Status is output as follows:

- Bit 0 - Tape Unit Ready.
- Bit 1 - Beginning of Tape
- Bit 2 - End of Tape

The computer may clear the BUSY and DONE flip-flop by addressing location 63₈.