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275°C Thick Film Hybrid Microcircuitry Fabrication Technology

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ABSTRACT

High-temperature electronics is needed for geothermal well-logging tools, jet engine monitors, nuclear reactor instruments, and fossil fuel exploration and production systems. This report describes the step-by-step fabrication technology of thick-film hybrids useful for at least 1000 hours at 275°C. Hybrid technology, qualified to standard military specification, was modified both in materials and fabrication processes to achieve this high-temperature operation. In addition to documenting this Sandia-developed technology, various alternate approaches are described to increase the versatility and applicability of these methods.

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Most commercial materials and products described in this report were purposely tested and used above the maximum temperature recommended by the manufacturer. For this reason, we can make no claim as to which products and materials are best in terms of meeting their advertised specifications. We do not endorse or approve either directly or by implication any apparatus, product, or process, or the use thereof. Instead, this report merely presents those materials and processes found to be acceptable for high-temperature operation in limited tests and measurements taken above the temperature range of commercial guarantee and interest. On the basis of these data, materials and fabrication processes for Sandia's 275°C geothermal microcircuit development are presented for the benefit of future Sandia work and similar work by other organizations.

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INTRODUCTION

This report describes the step-by-step fabrication of hybrid thick film microcircuitry for operation to a minimum of 1,000 hours at 275°C. Conventional hybrid technology was modified in both materials and fabrication processes to achieve this high-temperature capability.

This is the fourth and final report in a sequence describing high-temperature hybrid microcircuitry for 275°C operation. The first three reports in this series describe the investigation and development of passive circuit components,¹ active devices,² and complete circuitry³ for a prototype temperature instrument that was successfully field tested⁴ at 282°C in a geothermal well. For an extensive review of the early perspective taken and decisions made in this high-temperature instrumentation development, refer to the introduction in Reference 1. These reports are all available through the National Technical Information Service (NTIS).

Development since publication of these reports has resulted in a considerable expansion of high-temperature electronics technology. Therefore, a brief description of recent developments will be found in Appendix A of this report, and the directions for future developments are described in Appendix B.

The U.S. Department of Energy's Division of Geothermal Energy (DGE) has sponsored this work as part of the Geothermal Logging Instrumentation Development Program that Sandia is conducting for DGE. High-temperature hybrid circuits are needed to provide bore-hole instruments that can explore and assess geothermal resources.

Need at High Temperature

The original Sandia target of instrumentation capable of operating for 1,000 hours at 275°C is adequate for the geothermal needs to date,⁵ but field and system experience over the past 3 years has

indicated that higher temperatures and longer terms of operation are needed. For example, borehole instruments are needed to monitor down-hole pump performance and reservoir pressure for periods over 1 year ($> 10,000$ hours). Also, temperatures over 350°C have been measured in wells at Cerro Prieto, Mexico; Valles Caldera, New Mexico; and Puna, Hawaii. In addition, oil and gas wells are being drilled in deeper and more thermally hostile geologies. For these reasons, the down-hole instrumentation industry is continually pushing to increase the temperature and time capability of components and circuitry.

A second demand for high-temperature electronics is in jet engine monitors. The Naval Research Laboratory⁶ has initiated joint development efforts with General Electric (Evendale) and Clemson University with the goal of developing a long lifetime 260°C microprocessor and related electronics. The desire to eliminate the complicated, unsafe fuel cooling of current jet engine instrumentation and the incentive to increase the operating temperature of the engine are providing an impetus to this technology development. Through Sandia, the DOE and U.S. Navy are sponsoring the development of a 300°C operational amplifier at Harris Semiconductor, Inc., as one of the efforts in this direction.

The third area of need at high temperatures is in the nuclear reactor industry. For example, a self-contained neutron flux monitor placed in the 300°C sodium coolant loop in a fast breeder reactor is the goal of an Oak Ridge National Laboratory effort.⁷ Although this initial instrument has little need of radiation hardness, many other reactor instruments require both temperature and radiation hardness.

Current Hybrid Technology Development

The well-logging service industry has quickly seized and expanded on high-temperature technology. Supported by this down-hole instrumentation market, at least five hybrid microcircuit manufacturers are now making 200°C products--Seismic Engineering, Dallas, Texas;

Micropac, Garland, Texas; General Electric, Houston, Texas; Teledyne Philbrick, Dedham, Massachusetts; and Micro Networks, Worcester, Massachusetts. Also, several logging companies now make high-temperature microcircuits within their corporation in order to meet their operational requirements of 200° - 225°C range for hot and deep gas and oil wells.

FABRICATION PROCEDURE

In the following step-by-step hybrid fabrication procedures (fabrication sequence is shown in Figures 1 and 2), emphasis is placed on modifications to the well-known standard commercial hybrid materials and processing.⁸ The fabrication begins with standard thick-film techniques using carefully developed and selected high-temperature materials. For example, selection of a thick-film ink for the conductor pattern was based on the compatibility of the ink with the aluminum wire at temperatures up to 300°C ; for the resistors, thick-film ink was chosen for its temperature coefficient of resistance (TCR) from 25 to 300°C and a low resistance drift after aging. The capacitor dielectric ink was carefully selected for a high-insulation resistance up to 300°C ; also, a majority of the capacitors and resistors are screened directly onto the substrates. The completed thick-film networks are then bonded into an open package. Discrete devices such as chip capacitors, resistors, transistors, and diodes are then bonded to the substrate. Finally, all the required wiring interconnections are made and the package is sealed and tested. Each of the following paragraphs describe a key step in the fabrication of a 275°C voltage regulator. This and other circuits are currently being refined and commercially fabricated by Teledyne Philbrick.

Artwork

There are several design points about the artwork for the 275°C voltage regulator that are different from standard military specified hybrids (Figures 3a and 3b). For example, large die-down areas

Figure 1. Hybrid Circuit Voltage Regulator Fabrication Procedure

Figure 2. Thick-Film Printing

Figure 3a: (A) Large die-down areas for redundant transistor placement. (B) Wide-line widths to facilitate rework. (C) Isolated islands for high-temperature testing of transistors before connecting the devices to the circuit. (E) Jumper-wire pads for bypassing resistors to facilitate trimming over a decade resistance range.

Figure 3b: (D) Resistors of large areas to ensure low drift with time and temperature even after laser trimming.

are available for redundant transistor placement (A). In this way inadequate bonding or electrical characteristics of one transistor does not necessitate a second high-temperature die-down step. Also, isolated islands exist for high-temperature testing of a transistor before connecting the device to the resistor network (C). Resistors of large areas are used to ensure low drift with time and temperature even after laser trimming (D). Jumper-wire pads for bypassing resistors are present to facilitate trimming over a decade resistance range (E). In addition to wide line widths (B) and noncompact layout, these prototypes are designed to be fabricated in modular form, thus minimizing the number of components on each substrate in order to facilitate rework and to increase yield. However, such expanded layout is not mandatory for high-temperature performance. In the case of the voltage regulator discussed in this report, four modules were used; as shown in Figure 5, these are VR1 through VR4.

Screens

The screens used for the thick-film printing are the standard 200 and 325 mesh stainless steel. The two different screen meshes are used to vary ink thickness and consequently vary resistor and capacitor values. The emulsion film used is Ulano Red RX-200. The exposures are made with a GE-DXN, XENON, 3400°K, 120 V, 1000 watts light source.

Printer Setup

Standard operating procedures are used with the Presco Model 150 Printer shown in Figure 4.

First Conductor Printing

Standard substrate printing procedures are used to print the first conductor pattern and the bottom plate of the capacitors. To reduce printing time, four circuits (Figure 5) are printed on a 2" x 2", 25 mil thick, 96 percent alumina substrate from the 3M Company.

Figure 4: Presco thick-film printer, Model 150.

Figure 5: To reduce printing time, four circuits are printed on a 2" x 2", 25-mil thick, 96-percent alumina substrate. (A) To separate circuits, substrates are scored with the laser scriber then broken along the laser cut. (B) To facilitate rework and to increase yield, prototypes are fabricated in modular form (VR1-VR4).

Dupont 9910 ink is used--this is a low-frit-content, mixed-bonded gold. After the conductors and capacitor plates are printed, the substrates are placed in a small drying oven using temperature and time specified by the ink manufacturer. The oven used for drying is the Statham Temperature Test Chamber, SD60. After drying, the substrates are then put through the BTU engineering model MQ 81-672 conveyor belt furnace (Figures 6a and 6b). The temperature profile used is an approximate 25-minute rise to an 8- to 10-minute plateau, then an approximate 25-minute cooling cycle. The total time for a complete baking cycle is 1 hour. The 8- to 10-minute plateau temperature is specified by the ink manufacturer as 925°C.

Printing of Crossovers

The crossovers and capacitor dielectric are printed in one step using ESL 4301 K=10, ESL 4515 K=50, or TFS 1005 K=5 dielectric inks. For highly stable capacitors, two layers of ESL 4301 and one layer of ESL 4515 are printed. However, to conserve substrate real estate, the ESL 4515 is used alone if a large temperature coefficient can be tolerated. If substrate room is available, capacitors with a low-temperature coefficient but large area are made with the TFS 1005. Even when using only one type of ink, two layers are printed to reduce the number of pinholes. The first layer is printed, dried, and fired before the second dielectric layer is applied.

Second Conductor Printing

The second conductor pattern that bridges across the dielectric crossovers and serves as the top plate of the capacitors is printed using the DuPont 9910 ink. The same drying and firing procedures are used as with the first conductor.

Figure 6a: Profile control panel of the BTU engineering Model MQ 81-672 conveyor belt furnace.

Figure 6b: Substrates after baking cycle in the furnace.

First Resistor Printing

For the resistors with values of 300-5,000 ohms, Cermalloy 531HT ink is used. After printing, substrates are put in the small drying oven using the manufacturer's recommended settings. They are then put through the belt furnace at the specified temperature profile for the Cermalloy 531HT ink (peak temperature of 850°C).

Second Resistor Printing

Using 541HT ink, the resistors with values of 10K-30K ohms are printed. The same drying and baking procedures are used as with the first resistor printing.

Laser Scribe Substrates

After the final printing and firing, the circuits are ready to be separated. This is done with the Quantronix 113 YAG Laser System scribe (Figure 7). The substrates are scored (Figure 5) with the scribe and then broken along the laser cut.

Clean Substrates

Before the substrates are cemented into the packages, both package and substrate are rinsed with trichloroethylene, then isopropyl alcohol, and finally dried with dry nitrogen.

Cementing Substrates Into Packages

Using DuPont Thick-Film Dielectric Composition 8254, a uniformly thick, slightly translucent coating is applied to the back of the substrate. Using a 1" x 1" ceramic package with AU pads and AU plated Kovar leads, the substrate is carefully positioned in the package to keep substrate pads lined up with package pads. The unit is dried in a 150°C oven for a minimum of 3 hours and then put through the large belt furnace set for a temperature profile of 500°C.

Figure 7: Quantronix 113 VAG Laser System scribe used to score substrates so circuits could be separated.

An alternate method used by Teledyne Philbrick to attach the substrates to the packages makes use of Ablebond nonconductive 71-3 polyimide chip adhesive from Ablestik Laboratories.

Attaching Active Devices

The substrates, now cemented in packages, are ultrasonically cleaned in acetone and isopropyl alcohol before active devices are attached.

The eutectic bonding process is used to attach the active devices to the circuit. As shown in Figure 8, the Unitek Pulsed Heat Die Bonder, Model 8-157-02, is used. The settings used are:

Scrub Time--6.5

Scrub Amplitude--8

Stage Temperature--5.5 (approximately 400°C)

Tip Heat--7

Special care is taken to keep the tip of the bonding tool clean; contamination of die bonding pads can impede aluminum wire bonding to the die. The tool is cleaned by wiping the tip with a cotton swab that is dipped in isopropyl alcohol.

Figure 8: Unitek Pulsed Heat Die Bonder, Model 8-157-02. Used for eutectically attaching active devices to the circuit.

Biasing of Devices

As indicated on the schematic shown in Figure 9, some of the resistors have to be trimmed according to the zero temperature coefficient biasing region (ZTC) needed for proper operation of their associated transistor. Each transistor's ZTC is determined by graphing gate-source voltage versus drain current of the transistor at room

temperature, 150°C , and 275°C . The biasing range where the three characteristics cross is the ZTC region (Figure 10). For this characterization, the packaged substrate is placed on a hot stage attached to a probe station (Figure 11) which is equipped with gold-tipped probes. The temperature is raised to the desired level; the probes are placed on the device pads; and the drain characteristics are graphed on an x-y recorder (Figure 11). When the temperature is changed, the probes have a tendency to shift due to differential thermal expansion. Because of this effect, the probes are lifted during temperature changes to prevent damage to the device. After the ZTC point is determined for all the critical transistors, the circuit is allowed to cool to room temperature before the next fabrication step.

Figure 9: Voltage Regulator Schematic.

Figure 10: Zero temperature coefficient (ZTC) biasing region graph. The biasing range where the three characteristics cross is the ZTC region.

Figure 11: X-Y recorder and probe station equipped with gold-tipped probes.

Laser Trim Resistors

All the resistors are printed approximately 10 percent lower than the circuit values given. After all heating processes, i.e., eutectic die-down and transistor temperature calibration, the resistors are trimmed to within 1 percent of their correct values. The Korad KRT Micro Machining Laser, Model 910193-904 (Figure 12), is used. Aging at 300°C produced no noticeable excess resistance drift (<0.1 percent) that might result from the laser trimming.

Figure 12: Korad KRT Micro Machining Laser, Model 910193-904 used to trim resistors.

Figure 13: The Hughes Constant Voltage Welding Power Supply, Model MCW-550, is used to make electrical connections from substrate to package.

Gold Ribbon Connections

The electrical connection from substrate to package is made using 99.99 Au ribbon, size .003" x .020." The ribbon is parallel gap welded using the Hughes Constant Voltage Welding Power Supply, Model MCW-550 (Figure 13). The parallel gap electrodes are of RWMA-2 (copper chromium) alloy, with a 1/8" square shank and a tip size of .015" x .025." Settings used on the power supply are weld voltage = .70 volts and weld duration = 70 msec. The ribbon is first welded to the package pad and then to the substrate pad. A double layer of thick-film gold on the substrate bonding pads greatly eased attachment problems but is not necessary. On the VR3 package, shown in Figure 5, the 5K ohm resistor (R14, Figure 9) is left disconnected.

Clean Devices

To prepare for wire bonding, devices that have been eutectically bonded to substrates are thoroughly cleaned. The entire substrate is first washed with trichloroethylene, then acetone, and finally with isopropyl alcohol. The wire bonding is done as soon as possible after eutectic die-down and cleaning, certainly within 24 hours, or the bonding yield would drop below 90 percent.

Wire Bonding

For wire bonding active devices to the circuit, the Kulicke and Soffa High-Speed Ultrasonic Tailless Wedge Bonder, Model 484EE, is used (Figure 14). The wire used is the Sigmund Cohn Corporation's #1100 aluminum: 1 percent silicon, type 23890-1-20, size .001", elongation 1.5-3.0 percent, tensile strength 14-16 grams. Settings on the generator are first bond: power 2.5, time 3.0 (the first bond is to the chip), second bond: power 2.5, time 3.0. Of course settings may vary from bonder to bonder; thus a pull-strength test matrix must be determined to choose the bonding parameter window for each machine.

Figure 14: The Kulicke and Soffa High-Speed Ultrasonic Tailless Wedge Bonder, Model 484EE, is used for wire-bonding active devices to the circuit.

Au FILM

Figure 15: Diffusion Barrier Pads. These special diffusion barriers are designed to be used when the aluminum wire bonds are to operate at higher temperatures ($>275^{\circ}\text{C}$) or longer periods of time (>100 hours).

When the wire bonds are to operate at higher temperatures ($>275^{\circ}\text{C}$) or longer periods of time (>100 hours), diffusion barrier pads are used. These special diffusion barriers are designed (Figure 15) using Kovar or nickel disks 1-mil thick and 30-mils in diameter. One μm of gold is deposited on one side and 1 μm of aluminum on the other. Using a wobble bonder, the gold side is thermocompression bonded to the gold thick film. Then the aluminum wire from the transistor is bonded to the aluminum side of the disk. This method of wire bonding achieved higher operational temperatures than aluminum wire to gold thick film. With diffusion barrier pads, 350°C aging produced no bond resistance or adhesion change during 1000 hours.

Attach Temporary Lids

After all circuit connections (excluding VR3s 5K ohm resistor R14, Figure 9) and a careful visual inspection have been made, a temporary lid is placed on the packages. This protects the aluminum wire bonds while leaving the circuit accessible for troubleshooting and rework.

Breadboard Testing of Voltage Regulator

The four packages that make up the voltage regulator are assembled on a breadboard with a simulated load connected to the output of VR4 (see Figure 3 and schematic Figure 9). The simulated load is two 33 μF capacitors and one 610 ohm resistor connected in parallel. A variable potentiometer is used in place of the unconnected 5K ohm resistor (R14, Figure 9) in VR3. Then, with approximately 20 volts applied to the input of VR1, the variable potentiometer is adjusted for an output reading of 15 volts. Varying the input voltage from 16-30 volts, the regulators typically held the output voltage at 15 volts, with 80 dB of voltage isolation.

Attach Permanent Lids

Excluding VR3, the other packages are hermetically sealed using either solder preform packages or welded packages. Immediately prior

to sealing, the circuits go through a vacuum bake at 300°C for a minimum of 1 hour. If a 300°C vacuum oven is not available, a dry nitrogen or air environment is used. From the vacuum oven, circuits go directly to the sealing chamber to prevent any contamination.

A variation of this method is used by Teledyne Philbrick. Although their processing before sealing takes place at 300°C for a minimum of 10 hours, the drying step immediately before lid placement is only 150°C for 1 hour.

Printed Circuit Board Assembly

The next step in fabricating the voltage regulator is to permanently mount VR1, VR2, and VR4 on a printed circuit board. Most commercial printed circuit board materials cannot withstand temperatures above 200°C for extended periods of time. However, DuPont's Pyralin printed circuit board material proved reliable at 275°C for long periods of testing (>1000 hours). To attach packages to the Pyralin PC board, DuPont Formon 8513 88 Au/12 Ge solder paste is used. Solder joints are cleaned with DuPont 8529 Flux Residue remover. The joints are then examined under a microscope for any solder bridges or unacceptable connections.

Oven Test

A VR3 package is temporarily mounted with the other VRs on the printed circuit board with the potentiometer still replacing the 5K ohm resistor. The regulator is again tested using the same testing procedure as before. After determining proper operation, the board is placed in a high-temperature oven (Figure 16). The potentiometer and simulated load are mounted on the outside of the oven. The temperature is raised slowly, and readings of the input voltage, output voltage, and reference voltage (voltage across potentiometer) are recorded at 25°C intervals up to 275°C (Figure 17). After 1 hour of operation at 275°C, the oven is turned off and allowed to return to room temperature.

Active Trim of VR3

After the oven test, the 5K ohm resistor on VR3 is laser trimmed to give an output of 15 volts. This active trimming is done by removing the potentiometer and connecting the 5K ohm resistor to the circuit with gold ribbons. The power supplies and simulated load are connected to the regulator on the laser table. The 5K ohm resistor is trimmed with 20 volts applied to the input until the output is 15 volts. The VR3 package is then removed from the PC board and hermetically sealed. After sealing, the package is permanently soldered to the same board it was actively trimmed on, and a visual inspection of the solder joints is made. The completed system is again checked for correct operation before being committed to a logging instrument.

SUMMARY

The fabrication of a 275°C voltage regulator makes use of hybrid technology that has been qualified to standard military specifications. Modifications to this technology in both materials and fabrication processes are made to achieve this high-temperature operation. While using standard thick-film techniques, one of the key ingredients in achieving this high-temperature operation is with the use of carefully developed and selected materials. Thick-film inks were developed for 25-300°C operation with definite requirements for each one; i.e., ink for the conductor patterns should be compatible with the aluminum wire that is used for the wire bonds, resistor ink was chosen for its TCR and a low-resistance drift after aging, capacitor dielectric ink was selected for a high-insulation resistance. Discrete devices used are carefully selected, tested, and calibrated for proper operation before being committed to a circuit. Another modification to the standard thick-film printing process is in the expanded layout of the artwork (see Figs 3a and 3b); although this is not mandatory, it is used to facilitate rework and to increase yield.

Figure 16: High-Temperature Oven used for testing the voltage regulator to 275°C.

Figure 17: Percentage change of the voltage regulators output for a fixed input. For an input from 16-30 volts, the output was constant at all temperatures.

Appendix A

Update of Developments

A. Passive Components since SAND76-0611¹

The circuit designer now has a diversity of component types which were identified or developed for 300°C use in the last few years. In addition, some thick-film capacitors and resistors have been extended to 500°C operation.

Capacitors

1. Mica sheet capacitors with 1000 V rating at 300°C are now available from KD Components.
2. Custom Electronics has renewed its line of 300°C mica paper storage capacitors.
3. Tests with polyimide impregnation of mica paper capacitors at Sandia reveal low-leakage, high-standoff voltages at 300°C.
4. Thick-film material from Cermalloy (9105HT) provided useful 200 pF capacitors at 500°C. When used in a multilayer form, large 300°C capacitors are possible. Further materials studies are necessary before commercializing a 1 μF ceramic 300°C line.
5. Thin-film capacitors were found satisfactory; Sprague 1000 pF SiO₂ chips were used in 275°C hybrids. The University of Arizona's unique CVD system produced high-temperature Si₃N₄ capacitors.⁹

Resistors

1. Cermalloy readjusted their 500 series (now the 500HT) so that the minimum temperature coefficient occurs at 150°C. Typically, this results in less than a 0.5 percent change in resistance from 25 to 300°C. In addition, Cermalloy developed a 900 HT series which functions to 500°C. There is, however, a 10 percent change in resistance over this temperature range.
2. Purdue University (Prof. R. Vest)¹⁰ is pursuing high-temperature thick films using a unique frit system.
3. Caddock thick-film resistor chips and discretes function well to 300°C.
4. University of Arizona (L. Raymond) has produced a SiW system, thin-film resistor which changes only 2 percent over the 300°C temperature range. This system should be extendable to much higher temperatures and is compatible with monolithic silicon fabrication.

Interconnections

1. Extensive investigation of the aluminum wire to thick-film interface¹¹ was necessary to minimize intermetallic compound formation at the Au-Al interface. Results indicated DuPont 9910 gold and TFS 3028 gold are adequate for circuits operated at 275°C or less. Diffusion barrier pads are used for higher temperatures or longer times.
2. Parallel gap welding has been further studied. Thicker (double printed) thick-films are preferred for welding. Leaded hermetic packages were also found weldable to the thick-film hybrid.

3. AuGe solder in its printable paste form is usable on leadless hermetic packages.¹²

Packages

Teledyne Philbrick has successfully used standard metal hybrid plug-in packages at 275°C. Bakeout before sealing takes place at 300°C for at least 10 hours, although the drying step, immediately before lid placement, is only at 150°C.

Magnetic Components

Research at Texas A&M (Prof. R. K. Pandey)¹³ has uncovered the utility of 2 V Permendur ribbon core material in 500°C transformer design. Windings for 500°C are either anodized aluminum (Permaluster) or ceramic-coated copper (Hi-Temp Transducer). Using these materials and developing fabrication techniques, General Magnetics has produced inductors, transformers, and multipliers which show little performance degradation from 25°C to 500°C.

B. Active Devices Since SAND77-1145²

Diodes

No commercial source of low-leakage, high-temperature Si diodes has been found. Currently the best approach is to use Si JFETs with their source and drain leads connected.

A promising approach to the diode problem uses compound semiconductors gallium arsenide (GaAs) and gallium phosphide (GaP). Prototype diodes using aluminum metallization on GaAs were produced by McDonnell Douglas. At 300°C these diodes are marginally better than silicon, with about 0.1 V at the forward I-V elbow and reverse leakage in the microamp range. Experimental GaP diodes made both at Sandia and at Western Electric have even

better properties. At 350°C the elbow occurred at 0.4 V and reverse leakage up to 20 V was well below 1 μ A. However, development and commercialization of these diodes will take a few years.

Transistors

Considerable development has gone into MOS at Sandia. Long-lived 300°C MOS are now possible, but no commercial source has been identified or developed. See SAND79-1487 for more details.

Dielectrically isolated bipolar duals have been tested at Sandia and found to have low leakage (Intersil 2N4045). Similar devices are used by Oak Ridge National Labs (J. DeLorenzo) in current mirrors for 300°C discrete op amps.

Integrated Circuits

Survey work of commercially available ICs has been performed by Prof. J. Prince at Clemson University.¹⁴ A number of integrated circuits (especially digital) operate fairly well in the 200°C- 300°C range.

Harris Semiconductor has qualified several analog operational amplifier chips for 200°C operation. Harris is also under contract to develop a 300°C quad op amp chip to be commercially available by December 1980.

Sandia's discrete hybrid NAND gate using high-temperature MOS devices demonstrated that dielectrically isolated, monolithic CMOS could function to 350°C.

C. Circuits Since SAND78-1037³

In concert with Teledyne Philbrick, slight modifications to the voltage regulator circuit have resulted in easier production and 80 dB of voltage isolation.

A ring counter-type multiplexer has been designed and fabricated based on the JFET technology. We have placed a contract to make this circuit commercially available.

Various specialty pulse operational amplifiers have been designed by Oak Ridge National Laboratories.

In general, circuit design is waiting on the commercial availability of integrated op amps and gate functions for the next generation of more complex high-temperature circuitry.

Appendix B

Future Hybrid Technology Development

Sandia and Sandia's subcontractors continue to increase high-temperature technology versatility and comparability to the standard-temperature technology. For example, the introduction of high-temperature Integrated Circuits (by Harris Semiconductor) will necessitate a development of new packaging technology including the use of leadless, hermetic chip carriers. The high-temperature sealing and soldering of these carriers to the hybrid will present the first developmental hurdle. Secondly, lifetime tests are being run at Sandia to determine the weakest points of the hybridization and packaging processes. The goal of this effort is a predictable 1,000-hour life at 300°C and 10,000 hours at 200°C. In addition, new solders and application processes are being investigated because the existing gold/germanium system is unsatisfactory in fabrication yield, ductility, and lifetime.

Parallel development efforts in capacitors (thick-film and chip add-on), resistors, and inductors are ongoing. Enhanced resistor stability at 300°C and operation to 500°C have been achieved. Stable thick-film capacitors to 50,000 pF and multilayer ceramic chip capacitors to 0.1 μ F have been prototyped. Chip inductors in the η H range are commercially available from Thinco and are being developed for the μ H range.

In the area of active devices, efforts are underway at Sandia to develop high-temperature, low-leakage diodes using gallium arsenide (GaAs) and gallium phosphide (GaP) semiconductor materials. Laboratory investigation of silicon-based metal oxide semiconductor (MOS) devices has shown that it is feasible to fabricate MOS integrated circuits (ICs) for up to 300°C operation. Plans are being made to start the commercial refinement and fabrication of these MOS ICs.

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