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Shift-Register Coincidence Electronics System
For Thermal Neutron Counters

University of California

LOS ALAMOS SCIENTIFIC LABORATORY

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SHIFT-REGISTER COINCIDENCE ELECTRONICS SYSTEM FOR THERMAL NEUTRON COUNTERS

by

James E. Swansen, Paul R. Collinsworth, and Merlyn S. Krick

ABSTRACT

An improved shift-register, coincidence-counting logic circuit, developed for use with thermal neutron well counters, is described in detail. A distinguishing feature of the circuit is its ability to operate usefully at neutron counting rates of several hundred kHz. A portable electronics package incorporating the new coincidence logic and support circuits is also described.

I. INTRODUCTION

Nuclear material safeguards accountability and control procedures frequently require the nondestructive analysis (NDA) of plutonium-bearing materials, such as fuel rods, cans of plutonium-oxide powder, or pieces of plutonium metal.' A common NDA technique is passive neutron coincidence counting of the material in thermal neutron well counters.' A typical well counter consists of a sample-counting cavity surrounded by ^3He proportional counter neutron detectors embedded in a cadmium-lined polyethylene assembly. The material is assayed by the detection of coincident fission neutrons from the spontaneous fission of the even-mass plutonium isotopes in the presence of a random neutron background originating principally from (a,n) reactions in the material.³

Some advantages of thermal neutron well counters for plutonium assay are (1) high absolute neutron detection efficiency (approximately 10-30%), (2) insensitivity to gamma rays, (3) flexible geometry, and (4) excellent reliability, stability, and noise immunity. The primary disadvantage of these counters is the long (10-100 μs) neutron lifetime (or detector die-away time), which complicates the coincidence counting of thermal neutrons.

Coincidence gates comparable to or longer than the detector die-away time are required for efficient coincidence counting with thermal neutron detectors; these gates are typically 16 to 128 μs long. Early-design coincidence circuits for these detectors had extremely large coincidence deadtimes due to the long gates and therefore were limited to unacceptably low total neutron counting rates (several kHz). The shift-register (SR) coincidence concept of Böhnel⁴ as developed by Stephens, Swansen, and East⁵ resulted in an order-of-magnitude decrease in coincidence deadtime and consequent increase in useful neutron counting rates.

An improved version of this shift-register circuit has been designed as part of a project to provide the inspection and development sections of the International Atomic Energy Agency (IAEA) with a portable thermal neutron coincidence counter for the assay of plutonium samples. This new coincidence-counting system is called the High-Level Neutron Coincidence Counter (HLNCC) and is shown in Fig. 1. An essential requirement of the new system was that the circuitry could process a neutron counting rate of approximately 10^5 neutron/s with excellent reliability and moderate deadtime correction; this counting rate corresponds to a 2 kg sample of PuO_2 (with approximately 20% ^{240}Pu) in the HLNCC. A general description of the HLNCC is given in Ref. 6; a detailed discussion of the system and its applications can be found in Ref. 3.

11. THERMAL NEUTRON COINCIDENCE COUNTING

Neutrons originating from (α, n) reactions in the sample, from external sources, or from different fissions are uncorrelated in time (i.e., random), whereas neutrons emitted by a fissioning nucleus are time correlated. This correlation is exploited by the coincidence circuitry of the counter to distinguish between the coincident fission neutrons and the random background neutrons.

Figure 2a is a conceptual diagram showing the relative probability for detecting a neutron at time t following the detection of another neutron for a fissioning source (or a fissioning-plus-random source). Neutrons from a particular fission are detected at different times due to the detector die-away time' (τ). The probability for detecting another neutron from the same fission decreases approximately exponentially with time, whereas the probability for detecting a random neutron is constant with time (neglecting amplifier recovery time).

Fig. 1

The High-Level Neutron Coincidence Counter (HLNCC), consisting of the neutron detector, preamplifier package, electronics package, and calculator.

To distinguish correlated neutron events from random events (including neutrons from different fissions), two equal time periods are sampled by the coincidence circuit after a neutron has been detected (refer to Fig. 2b). The circuit has a predelay, typically $4\ \mu\text{s}$, after the first neutron has been detected to allow the amplifiers to recover for detecting subsequent neutrons. The first time gate is then opened for typically $32\ \mu\text{s}$ to detect the other neutron (or neutrons) associated with the fission event that gave rise to the first neutron. The neutrons detected during the first gate can be due to either time-correlated spontaneous fission events or random neutron events. As a result, the counts accumulated during this gate are called the real-plus-accidental (R+A) events.

Fig. 2
a) Simplified relative neutron detection probability distribution.
b) Coincidence gate timing diagram.

Following a long delay to ensure that any time correlation is removed, a second time gate is opened for the same duration as the first. The long delay should be at least several times longer than the detector die-away time. The second gate counts only random events and is called the accidental (A) gate. Since the two gates are the same length, the net difference in counts received during the two gates is the net real (R) coincidence count and is related to the spontaneous fission rate in the sample.

III. SHIFT-REGISTER COINCIDENCE COUNTING LOGIC

A simplified block diagram of the new shift-register coincidence counter logic is shown in Fig. 3. The predelay and gate are shift registers operating with a 2 MHz clock; e.g., a 32 μs gate uses 64 shift register stages with 0.5 μs /stage. The predelay SR has a selectable length from 1.0 to 32.5 μs in 0.5 μs steps. The predelay must be at least as long as the recovery time of the

Fig. 3.
Simplified block diagram of the shift-register coincidence logic.

detector and amplifier stages; otherwise, the system deadtime affects the R+A gate more than the A gate and introduces a bias on the net real count R. The gate SR has a selectable length of 8, 16, 32, 64, or 128 μ s.

The standardized logic input pulses are first synchronized with the 2 MHz SR clock and then sent through the predelay SR and gate SR. The number of pulses in the gate at any time is determined by an up-down counter. A pulse entering the gate increments the counter and a pulse leaving the gate decrements the counter. Thus the number of pulses in the gate is just the count in the up-down counter. The contents of the up-down counter are added to the R+A and A accumulators for each input pulse as indicated by the strobe arrows in Fig. 3; the strobe to the R+A accumulator occurs immediately as the pulse leaves the synchronizer, whereas the strobe to the A accumulator is delayed by 1024 μ s. Because a neutron pulse which enters the predelay SR is produced at a later time than those neutron pulses already in the gate SR, the R+A accumulator actually tallies events which precede the neutron pulses which strobe the accumulators; this is functionally equivalent to the conceptual timing diagram in Fig. 2.

The principal advantage of the shift-register coincidence circuitry is that each input pulse generates its own R+A and A gates; it is not necessary for one gate to close before the next can open. This feature greatly reduces the system deadtime and allows useful operation of the circuit to counting rates of several hundred kHz.

The preset timer in conjunction with the stop, start, and reset controls opens an AND gate to allow the collection of data. Each pulse passing through the AND gate is counted in the totals scaler. The data from the SR logic circuit are the measurement time, total counts, real-plus-accidental coincidence counts, and accidental coincidence counts.

Some features which distinguish the new shift-register circuit from the earlier Los Alamos design⁵ are as follows:

- (1) The new circuit has one shift-register gate and two strobes (one prompt and one delayed) rather than two gates and one strobe; this reduces the circuit complexity, but is functionally equivalent to the earlier method.
- (2) The delay between the R+A and A sampling times is 1024 μ s rather than 100 μ s, so there are essentially no real coincidences in the accidental gate with the new circuit.
- (3) A fixed shift-register clock frequency of 2 MHz is used for all coincidence timing functions, so the timing is less critical and is independent of the gate length chosen. In the earlier design the clock frequency varied with the gate length.
- (4) The predelay can be set from 1.0 to 32.5 μ s and is independent of the gate length; this feature is important for optimizing bias (due to pulse pileup) and coincidence counting efficiency.
- (5) The up-down counter has a capacity of 99 rather than 9, so there is no problem with counter overflow at very high counting rates.
- (6) The totals, R+A and A scaler capacities have been increased from 7 to 10 digits to allow long measurements at high counting rates.

IV. THE ELECTRONIC SYSTEM

The portable electronics package supporting the thermal neutron detectors is shown with its associated Hewlett-Packard HP-97 programmable calculator in Fig. 1. Except for the detector preamplifiers, all of the electronic subsystems required for the operation of the counters are contained in the portable

signals can be monitored at six amplifier test points on the front panel of the instrument. (Figure 6 shows the front and rear panels.) The discrimination level can be set by a helipot on the front panel and verified from a test point on the front panel. The six discriminator outputs are ORed to form a single standard logic signal for the SR coincidence logic; this signal is also available on the front and rear panels. A rear-panel switch allows either internal or external signals to be used as inputs to the SR logic; the external signal, if used, is supplied via a rear-panel coaxial connector. The measurement time and gate length are selected by front-panel switches. The predelay, which is infrequently changed, is set by internal switches.

Fig. 5.
Simplified block diagram of the electronics package.

Fig. 6a.
Front panel of electronics package.

Fig. 6b.
Rear panel of electronics package.

The data from the SR logic circuit (measurement time, total counts, real-plus-accidental coincidence counts, and accidental coincidence counts) are displayed simultaneously on the front panel. A microcontroller in the system is used in part to read the data from the display circuitry and transmit the results to an HP-97 calculator and an (RS-232-C)-compatible communications terminal or data link, such as to a computer. The microcontroller also instructs the SR logic circuit when the instrument is in the recycle mode. In the manual or the recycle mode, the instrument can be controlled by the start, stop, and reset pushbuttons.

The instrument derives all dc power-supply voltages from dc-dc converters operating off a single dc supply voltage, which is obtained either from an ac line or a battery. The high voltage is set by a front-panel helipot and can be monitored from a front-panel test point. A separate locking toggle switch is provided to turn the high voltage off and on. Preamplifier power is supplied through a rear panel connector, which also contains the preamplifier signal connections.

V. ELECTRONIC CIRCUITRY

A. General

Three circuit boards in the electronics package contain the amplifier, shift-register, and microcontroller circuitry. These boards were sized to allow possible future production of shift-register coincidence circuits in NIM modules. Because of the high component density required by restrictions on the board dimensions, Multiwire^a was chosen as the fabrication technique for the shift-register and microcontroller boards. Photographs of the front and rear of the shift-register board are shown in Fig. 7. The Multiwire method uses automated point-to-point wiring, where the wires are deposited on an adhesive surface; because the wires may overlap, high circuit density is possible. An additional advantage of Multiwire is the ability to use full ground and power planes, which are concealed in the photographs under the board coatings.

The top view of the electronics package with the top cover removed is shown in Fig. 8. The amplifier-discriminator circuit board seen in the photograph is directly above the shift-register and microcontroller boards. The main power supply is at the rear of the instrument; the dc-dc converters are mounted to the side of the package. This photograph shows the second prototype instrument, packaged for the Los Alamos Scientific Laboratory by E.G.&G., Inc.^b

The power-supply, analog and microcontroller circuitry used in this system is fairly conventional, so only a cursory description of these subsystems is provided below. The shift-register circuitry is described in detail.

^aMultiwire is a registered trademark of the Photocircuits Division of the Kollmorgen Corp., Glen Cove, New York, USA.

^bE.G.&G., Inc., Los Alamos Operations, Los Alamos, New Mexico, USA.

Fig. 7a.
Front view of shift-register board.

Fig. 7b.
Rear view of shift-register board.

Fig. 7c.

Close-up view of a portion of the rear of the shift-register board.

B. Power

The analog and digital circuits require ± 15 Vdc, ± 12 Vdc, and $+ 5$ Vdc power supplies; in addition, the neutron proportional counters require a variable high-voltage supply (0-2000 Vdc). It was found convenient to derive all of these voltages via dc-dc converters operating from a single dc supply (approximately 25 V). This feature allows straightforward operation of the instrument from a battery pack, if desired. Except for the high-voltage supply, commercial converters were used. The variable high-voltage supply was designed around a Del Electronics' PMSB-2.025 converter, as shown in Fig. 9. This circuit allows linear control of the output voltage from 0-2000 Vdc.

^c Del Electronics Corp., Mt. Vernon, New York, USA.

Fig. 8.
Top view of electronics package with top cover removed.

C Preamplifiers

Figure 10 is a view of the preamplifier and distribution box with the top cover removed; Fig. 11 shows a single preamplifier, which is designed for general purpose neutron proportional counter applications. A schematic of this charge-sensitive preamplifier is shown in Fig. 12. The feedback capacity consists of the capacitive tee network C1-C3, which produces a conversion gain of approximately 14 V/pC and a decay constant of approximately 45 μ s with the 47 M Ω feedback resistor. The output is connected to the main electronics package by a 2.5-meter-long cable assembly containing eight shielded, twisted pairs of wire (six for preamplifier signals and two for preamplifier power). For applications where the cable is connected and disconnected frequently, the twisted-pair cable is simpler and more reliable than a coaxial cable assembly.

Fig. 11.
A single charge-sensitive preamplifier.

NOTE:
1. RESISTANCE IN OHMS.

Fig. 12.
Schematic of charge-sensitive preamplifier.

D Amplifiers and Discriminators

Figure 13 is a schematic of one of the six amplifier-discriminator channels. Bipolar pulse shaping with 0.5 μ s time constants was chosen in an effort to provide high noise immunity and gamma-ray insensitivity for a variety of ^3He proportional counter gas mixtures while maintaining high stability, low power consumption, small size, and moderate deadtime.

The first stage provides the first differentiation with components R2-C1, which are pole-zero compensated by R1. Components R3, R4, C2, and C3 perform the integration to produce a quasi-gaussian unipolar pulse at the input to the second stage, which is basically a gain-of-ten amplifier. The third stage provides the second differentiation with R5-C4 and gain control with R6. The gain is adjusted so thermal neutron capture events produce full energy pulses with 6V peak voltage at the output of the third stage. The fourth stage is a

Fig. 13.
Schematic of an amplifier and discriminator channel.

discriminator which typically has a discrimination level of 1.5 V; R7 and R8 provide a few percent hysteresis. The fifth stage is a one-shot multivibrator which generates a 150 ns-wide pulse on a negative-going transition from the discriminator. The outputs of the one shots from all six channels are ORed to form a single digital pulse stream as the input to the shift-register coincidence circuitry.

E. Shift-Register Coincidence Circuit

1. General. Principal considerations in the design of the shift-register coincidence circuit were high reliability, minimal component count, low power consumption, and low deadtime. These considerations led to the circuit shown in Fig. 14, which employs several logic families and is built around MC14517AL and MC14557AL complementary-symmetry metal-oxide semiconductor (CMOS) shift registers. The shift-register clock frequency was selected as 2 MHz to permit

Fig. 14.
Schematic of shift-register coincidence circuit.

the use of very conservative timing relationships; the resultant 0.5 μ s shift-register deadtime is adequate for neutron counting rates in excess of 100 kHz. Three years experience with the circuit has shown excellent reliability with low and high counting rates.

2 Clocking Signals. A number of clocking signals are required for operation of the shift registers, counters, and latches. The primary clock frequency is 4 MHz and is provided by the crystal-controlled Vectron^d CO-238B. The frequency is divided twice by the 74LS107 dual J-K flip-flop; the 74LS08 quad AND gate then generates specialized pulse trains. The MH0026 inverting level shifter produces clocking signals ϕ_1 and ϕ_2 to drive the Am2804 long delay shift registers; these signals swing from +5 to -12 V. Figure 15 shows an idealized timing diagram.

^d Vectron Laboratories, Inc., Norwalk, Connecticut, USA.

Fig. 15.

Idealized timing diagram for the shift-register coincidence circuit. A second input pulse, synchronizer output, and R+A strobe are shown with dotted lines. The predelay out and gate out waveforms are shown changing from logical zero to logical 1 for illustration. The curved interconnecting lines show the logical relationships between the signals.

The MC14517AL gate shift registers are clocked by the level-shifted signal SRCK, which swings from 0 to 12 V. The clock signal $\overline{CK}$, used to synchronize the detector pulses, is the same as SRCK, except that it operates at transistor-transistor-logic (TTL) levels. Four signals ($CK_{1/2}$, $CK_{1/2}+150$, $CK_{1/2}+250$, and $CK_{1/2}+350$) provide suitable timing for the operation of the synchronizer, the up-down counter, and the latches. These consist of 125-ns-wide TTL pulses occurring at a 2 MHz rate and phased relative to SRCK as shown in Fig. 15; the 150, 250, and 350 ns delays are obtained from the ECC TTL DM delay modules.^e

3. Synchronizer. Incoming pulses to the coincidence logic are buffered by a TTL AND gate and shaped into 30-ns-wide inverted pulses by C1, R1, and the TTL NAND gate. The input pulses are first synchronized with the shift-register clock SRCK by the 74LS74 dual edge-triggered flip-flop. The normally set Q output of the first stage, reset by the input signal, enables the second stage. The $\overline{Q}$ output of the second stage is then set by the leading edge of $\overline{CK}$ and is later reset by the leading edge of $CK_{1/2}$. The resulting synchronizer output pulse is approximately 375 ns wide (see Fig. 15). When the synchronizer output signal goes high and sets the Q output of the first stage, the circuit is enabled to accept the next input pulse; however, capacitor C2 delays the transition of the Q output of the first stage sufficiently to preclude double pulsing by the synchronizer when the input pulse overlaps the leading edge of $\overline{CK}$.

4. Predelay. After the synchronizer output is level-shifted and inverted by the MH0026, it becomes the input to the predelay shift register. An MC14557AL, 64-bit, variable-length, CMOS, static shift register is used for the predelay. A six-bit binary code manually selected by the switches shown in Fig. 14 determines the delay. Since the shift-register clock SRCK has a 2 MHz frequency, the maximum delay is 32 μ s. The minimum delay is 1 bit or 0.5 μ s. Input and output data transfer are initiated by the rising edge of SRCK; the output (last bit) occurs after an $\sim$ 150 ns delay, as shown in Fig. 15.

5. Gate. The gate is formed by two MC14517AL, 128-bit, static shift registers. Data are moved by the positive-going edge of the clock SRCK; an $\sim$ 120 ns delay precedes the output signal, as shown in Fig. 15. Delayed outputs of 8, 16, 32, 64, or 128 μ s are inverted and level-shifted to TTL logic levels by the CD4049; the desired gate length is selected by the 74LS151 data selector and manually-switched selector inputs.

^e Engineered Components Co., San Luis, California, USA.

6. Up-down Counter. The two-decade up-down counter is formed by a pair of 74LS192 counters. The count-up input pulse is produced by the CK_2+150 clock, the level-shifted output of the predelay, and the 74LS00 NAND gate. The count-up in the 74LS192 circuits occurs on the trailing edge of the input pulse; see Fig. 15 for the timing relationships. The count-down input is produced by the CK_2+350 clock and the 74LS151 gate length selector. The count-down occurs in the 74LS192 circuits on the trailing edge of the input pulse, as shown in Fig. 15.

7. The R+A Accumulator. The least significant two decades of the R+A accumulator consist of 74LS174 and 74LS175 clocked latches. Each output pulse from the synchronizer causes the contents of the latches to be summed with the contents of the up-down counter in the 82S83 adders. The sum is stored in the latches, and the adder overflow is the input to a pair of HCTR4010 four-decade scalars. The R+A accumulator is thus ten decades long.

The R+A strobe to the latches is produced by the CK_2+250 clock, the synchronizer output and a 74LS08 AND gate. Latching occurs on the leading edge of the strobe, as shown in Fig. 15. Note that during an SRCK clock cycle, the latching strobe precedes the up-down pulses and hence operates on the data from the previous cycle; this introduces an additional 0.5 μ s predelay, so the minimum selectable predelay is 1.0 μ s.

8. The A Accumulator. The A accumulator is identical to the R+A accumulator except that the strobe is generated following a 1024 μ s delay. After the synchronizer output has passed through two Am2804, 1024-bit, dynamic shift registers (operating at 2 MHz with clocks ϕ_1 and ϕ_2), the accidental strobe is formed with the CK_2+250 clock, the delayed synchronizer output, and a 74LS08 AND gate. Relative to the phase of the shift-register clock SRCK, the timing is identical to that for the R+A strobe.

9. Miscellaneous. Since every output pulse from the synchronizer generates an R+A strobe, the R+A strobes are scaled to determine the totals count. Two decades of prescaling by 75L52 TTL counters are followed by a pair of four-decade HCTR4010 counters, so ten decades are available for the totals count. The time, totals, R+A, and A data are displayed continuously by means of a special multiplexing circuit which interleaves the outputs of the prescalers and four-decade scalars; the operation of this circuit will not be detailed here.

F. Microcontroller

The microcontroller section consists primarily of a Motorola^f MC6800 microprocessor with standard support circuits, such as the MC6850 Asynchronous Communications Interface Adapter and MC6821 Peripheral Interface Adapter (PIA); one kilobyte of Intel^g 2708, erasable, programmable, read-only memory (EPROM) and 128 bytes of MC6810 random access memory are used for memory components.

The shift-register coincidence circuitry can operate in manual mode independently of the microcontroller circuitry, which was designed and added after the completion of the first prototype system. The microcontroller was added to the system primarily to interface the display circuitry to readout devices, such as an HP-97 printing calculator, a printing terminal, or a computer. The microcontroller also allows the instrument to operate in a recycle mode and allows future control of the start, stop, reset, and readout functions by an external computer.

G. Interfaces

A custom interface was designed to allow data transfer to an HP-97 calculator, which was selected for use with the portable system because of its printing mechanism, small size, and scientific programming features. The interfaced version of the HP-97 (the HP-97S) was not available at the time of the design and would not have been used because of the extra coupling device required.

After the keyboard matrix of the HP-97 was empirically decoded, interfacing wires were soldered directly to the HP-97 circuit boards and brought to the shift-register electronics package as a ribbon cable. Mechanical switches on the calculator keyboard are emulated by CD4066 MOS switches, which are closed on command by the microcontroller; the proper codes are supplied to the MOS switches via the PIA, as shown in Fig. 16. The code is conservatively held for 60 ms per emulated keystroke; the interface is disabled for an equal time to release the keyboard between electronic keystrokes. During data transfer with the presently used EPROM software, the time, totals, R+A, and A scaler data are stored in calculator registers R₁ through R₄, respectively. Following the data transfer, an "A" command is sent to the calculator to start the data-processing program which begins at label "A" in the HP-97.

^f Motorola Semiconductor Products, Inc., Phoenix, Arizona, USA.

^g Intel Memory Systems, Sunnyvale, California, USA.

NOTES:

1. RESISTORS ARE 100 KΩ.
2. 15 KEYS ARE CONTROLLED FROM THE PIA;
SWITCH NO. 13 IS SPARE.
3. KEY FUNCTIONS ARE SHOWN IN PARENTHESES.

Fig. 16.
Schematic of the calculator interface.

A standard RS-232-C serial communications interface is also included for communication at 300 bits/s with a computer or other compatible device. The data and heading formats are determined by the EPROM program.

VI. PERFORMANCE

An essential performance requirement was the ability of the system to handle totals counting rates of at least 10^5 s^{-1} . A severe test of the system is to place a random neutron source (such as $^{241}\text{Am-Li}$) in the detector with an intensity such that the totals counting rate is approximately 10^5 s^{-1} . Two conditions should then be met: (1) the R+A and A coincidence counting rates should be the same within statistical errors, and (2) the accidental coincidence rate should equal the gate length times the square of the totals rate within statistical errors. The instrument meets both of these requirements within approximately 0.01%.

Another essential requirement was moderate coincidence deadtime at a totals counting rate of approximately 10^5 s^{-1} . This deadtime can be determined by measuring the real coincidence rate of a ^{252}Cf spontaneous fission source, first alone and then with increasing amounts of random neutron background. The results of such a measurement with the HLNOC are shown in Fig. 17, where the normalized, observed real coincidence rate is plotted vs the observed totals rate; 50% deadtime occurs at a totals rate of approximately 300 kHz.

Fig. 17.
Normalized logarithm of observed real coincidence counts per fission of ^{252}Cf vs the observed totals counting rate.

VII . CONCLUDING COMMENTS

Although the shift-register electronics package was designed primarily for use with the High-Level Neutron Coincidence Counter, it can also be used directly with other thermal neutron detectors using ^3He proportional counters. Also, an external input to the buffer and synchronizer of the shift-register logic allows the coincidence circuitry to be used with any TTL-compatible pulse stream.

Complete wiring diagrams and parts lists for the shift-register coincidence counting system are available (without functional description) from the maintenance manual for the second prototype.⁷

Seven coincidence counting systems based on the shift-register logic have been supplied to the International Atomic Energy Agency by the Los Alamos Scientific Laboratory; three of these systems used prototype electronics packages produced by E.G.&G., Inc. and four used essentially identical units manufactured by the IRT Corporation.^h

The electronics system (and associated detector) described in this paper are currently commercially available from the IRT Corporation; other versions are also available from the National Nuclear Corporation,ⁱ which produced the first commercial coincidence module based on the new Los Alamos design.

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^h IRT Corporation, San Diego, California, USA.

ⁱ National Nuclear Corporation, Redwood City, California, USA.

Present address: Los Alamos Scientific Laboratory

REFERENCES

1. G. R. Keepin, Nuclear Materials Management, VII, 3 (1978) 44.
2. N. Ensslin, M. L. Evans, H. O. Menlove, and J. E. Swansen, Nuclear Materials Management, VII, 2 (1978) 43.
3. M. S. Krick and H. O. Menlove, "The High-Level Neutron Coincidence Counter (HLNCC): Users' Manual", Los Alamos Scientific Laboratory report LA-7779-M (1979).
4. K. Böhnel, "Die Plutoniumbestimmung in Kernbrennstoffen mit der Neutronenkoinzidenzmethode," Karlsruhe report KFK2203 (1975); also AWRE translation No. 70 (54/4252) (1978).
5. M. M. Stephens, J. E. Swansen, and L. V. East, "Shift Register Neutron Coincidence Module," Los Alamos Scientific Laboratory report LA-6121-MS (1975).
6. M.S. Krick, M. L. Evans, N. Ensslin, C. Hatcher, H. O. Menlove, J. L. Sapor, J. E. Swansen, M. de Carolis, and A. Ramalho, IAEA-SM-231/50 (1978).
7. D. Altman, "High Level Neutron Coincidence Counter (HLNCC): Maintenance Manual," E.G.&G. report EGG-1183 5091 (1978).