SAND82-0158
Unlimited Release
Printed January 1982

EVALUATION OF UNENCAPSULATED CERAMIC MONOLITHIC
AND MOS THIN-FILM CAPACITORS (25 to 300°C)

W. R. Nance
Sandia National Laboratories
Albuquerque, NM 87185

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ABSTRACT

Several commercial monolithic ceramic and thin-film MOS chip capacitors were evaluated for use in high temperature (300°C) geothermal instrumentation. Characteristics of the commonly used dielectric materials (NPO, X7R, BX) and temperature dependence of the insulation resistance are briefly discussed. Some ceramic capacitors with NPO dielectric materials had insulation resistances above 10 megohms at 300°C and less than 2 percent change in capacitance from 25°C to 300°C, while the X7R and BX dielectric materials exhibited insulation resistances below 10 megohm and changes in capacitance greater than 50 percent. The thin-film capacitors showed good stability at 300°C. However, during aging, bonds and bond pads presented a problem causing intermittently open circuits for some of the devices.

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EVALUATION OF UNENCAPSULATED CERAMIC MONOLITHIC AND MOS THIN-FILM CAPACITORS (@300°C)

I. Introduction

The need for stable and reliable high-temperature components for geothermal logging tools has been of great concern to Sandia. Two such components of interest are the ceramic monolithic and the thin-film chip capacitor in the range of 1000 pF to 1 μ F.

The design specification for capacitors in geothermal instrumentation calls for operating temperatures of 25°C to 300°C with working voltage of > 15 Vdc. The dc insulation resistance must be 10 megohm or greater under these conditions.

Sandia has developed thick-film capacitors for use at 300°C. However, this application has been limited to below 4000 pF due to the physical constraints (i.e. less than 2 inches for the inside diameter of the tool housing) of geothermal instrumentation. The primary concerns for these capacitors for high-temperature hybrid circuits are the physical dimensions and the leakage current at 300°C.

There are some commercial capacitors with satisfactory electrical characteristics at 300°C. In this report a number of commercial ceramic and thin-film capacitors were evaluated by observing the change in capacitance and dissipation factor over a temperature range of 25°C to 300°C at frequencies of 120 Hz, 1 kHz, and 10 kHz. The insulation resistance was observed over the same temperature range with an applied potential of 15 Vdc. The capacitors were also aged at 300°C for 600 hours.

Section II of this report briefly discusses characteristics of the ceramic monolithic capacitors. Information on the thin-film chips is discussed in Section III. The test results for the capacitors are presented in Section IV and the appendix.

II. Ceramic Capacitors

For high-temperature applications, the ceramic monolithic capacitor appears to be promising because of its ability to operate over wide frequency and temperature ranges and for its physical size.¹ Of the four types of dielectric materials commonly used for ceramic capacitors, only the NPO, BX, and X7R were evaluated. There was no attempt made to evaluate capacitors containing Z5U dielectric materials because of the large variation in dielectric constant over its operating temperature range. Table I^{1,2} compares the characteristics of these dielectrics for normal operating conditions.

TABLE I
Dielectric Comparison

	NPO	BX, X7R	Z5U
Dielectric Class	I-A (Low K)	II-A (Mid K)	II-B (High K)
Dielectric Constant	25-100	300-1800	>4000
Dissipation Factor	<0.2%	2.5%	2.5%
Temperature Range	-55° to 125°C	-55° to 125°C	+10° to 85°C
ΔC (Tolerance)	+30 ppm/°C	+15%	+22%, -56%
IR @ 25°C	1000 ΩF	1000 ΩF	1000 ΩF

The most commonly used dielectric in fabricating multilayer ceramic capacitors is barium titanate along with different proprietary modifiers. The theory of ferroelectricity of barium titanate will not be discussed in this report. However, an explanation of the temperature dependence of insulation resistance from the standpoint of electrical conductivity which is expressed by the exponential relation characteristic of semiconductors will be presented.³

The general construction of the multilayer ceramic capacitor as described by Capozzi¹ is shown in Figure 1. Alternating dielectric and conducting layers are stacked upon each other to produce the desired capacitance. The layers are then subjected to a predetermined heat treatment, causing the entire stack to fuse into a

dense monolithic block with alternating conductors exposed at opposite block faces.

Figure 1. Multilayer Capacitor Construction.

Because circuit physical constraints are important in hybrid design, these commercial capacitors are manufactured in dimensions ranging from 50 x 40 x 40 mils to 285 x 298 x 70 mils.

The capacitance is directly proportional to the dielectric constant and area as noted in Equation 1,

$$C = \frac{kAN}{t} \quad (1)$$

where A = The area of overlaps of the electrodes

k = The relative dielectric constant of insulator between electrodes

N = The number of layers

t = The thickness of dielectric

and therefore capacitance is an important factor in the determining the physical size of the capacitor.

The insulation resistance (IR), which is a measurement of the leakage in a dc charged capacitor, may vary due to both intrinsic and extrinsic conditions. For example, fabrication process variations may create additional contaminants which aid in decreasing the insulation resistance (intrinsic), and increasing chip size will also decrease the insulation resistance (extrinsic). Although many factors are involved in the increase of leakage current with increasing temperature, only the intrinsic conduction modes will be discussed. This conductivity in ceramic dielectrics arises from the ionic charge carriers that are mobile due to atomic lattice defects. These ions will move from one atomic interstitial site to another under the influence of an electric field.²

D. D. Glower and R. C. Heckman³ stated that for pure BaTiO₃ ceramic, the predominate mode of conduction is ionic between 100° and 300°C and electronic above 500°C, whereas Drummer and Nordenberg⁴ state that the conduction is predominately electronic with a small amount of superimposed ionic conduction. In either case, conductivity of the dielectric materials should follow the exponential relations characteristic of semiconductors⁵ as given by

$$\sigma = K e^{-\frac{\Delta E}{RT}} \quad (2)$$

where σ = The conductivity

K = A constant (dependent on material)

ΔE = Activation energy

R = Gas constant

T = Temperature in degrees Kelvin

because the carrier density is exponentially temperature dependent.

III. Thin-Film Capacitors

Two types of thin-film capacitors evaluated were high-temperature MIS chip fabricated by the University of Arizona and Sprague's Oxsil MOS-type 15 K chip capacitors. The Sprague capacitors were commercially available while the University of Arizona high-temperature capacitors were fabricated for Sandia's use in the geothermal instrumentation program. The design specifications for the Arizona chip were as follows:⁶ (1) capacitance: 0.01 μF (nominal), (2) dissipation factor: ≤ 1.0 percent, (3) working voltage: 50 WVdc @ 25°C and 20 WVdc @ 350°C, (4) dc resistance: $IR \geq 10$ megohm (20 V @ 350°C). Figure 2 is a cross section of the structure of University of Arizona capacitors.

Figure 2. Cross Section of Thin-film Capacitor. Total Thickness of Thin-film Layer is Approximately 1.5 μm .

IV. Test Procedures

Testing of ceramic and thin-film capacitors was performed according to MIL-STD-202F. The tests performed were capacitance, insulation resistance, and dissipation factor versus temperature. The capacitors were mounted on a 2 x 2 inch alumina substrate with ABLEBOND

71-3 nonconducting epoxy. Gold ribbons were parallel-gap welded from the ceramic capacitors metalized band to the thick-film conductor on the substrate (see Figure 3), while the thin-film capacitors were connected to the thick-film gold conductor by ultrasonically bonded 1 mil aluminum (1 percent Si) wire. Blue M and Delta Design Convection Ovens were used to temperature cycle the capacitors from 25° to 300°C.

The capacitance and dissipation factor were measured at 120 Hz, 1 kHz, and 10 kHz using an HP 4262A LRC meter. The insulation resistance was measured using a KEITHLEY 616 digital electrometer as shown in Figure 4.

(a)

(b)

Figure 3. (a) Ceramic Capacitors Parallel-Gap Welded to the Thick-Film Gold Conductor on an Alumina Substrate.

(b) Thin-Film Capacitors Wire Bonded to the Thick-Film Gold Conductor on an Alumina Substrate.

Figure 4. Equivalent Circuit of a Capacitor with Test Apparatus.
 R_p is the parallel (insulation) Resistance and R_s is
the Equivalent Series Resistance

V. Test Results

Ceramic capacitors from AVX, Centralab, Johanson Dielectric and Vitramon were evaluated. The low-dielectric constant materials (NPO) showed a high degree of stability from 25°C to 300°C as compared to the BX and X7R materials. Temperatures below 200°C created difficulties in measuring the leakage current because of the extremely high-insulation resistance which is characteristic of ceramic capacitors and also the limitations of the test equipment. Figure 5 is a normalized curve of conductivity versus temperature for a capacitor with an NPO dielectric material. This clearly shows that the insulation resistance has a temperature dependence; the aging data presented in the appendix indicates there was also a time dependence, with the insulation resistance changing approximately 10 percent during the first 200 hrs at 300°C and greater than 90 percent in the next 400 hours. Fine tuning of the dielectric composition and fabrication process could improve its high temperature performance.

The change in capacitance for the University of Arizona and Sprague chip capacitors was less than 2 percent during aging (600 hr @ 300°C). Percent change in capacitance, insulation resistance and dissipation factor versus temperature is shown in the appendix. However, during prolonged aging, intermittent open circuits appeared. When viewed through a microscope at 125X, the bond pad appears to be disintegrating (see Figure 6). This could be caused by contaminants or migration of the pad material. Table II is a summary of Sprague and University of Arizona thin-film capacitor's parameters during aging at 300°C for 600 hours.

Figure 5. Normalized Curve of Conductivity vs. Temperature for a Capacitor with a NPO Dielectric Material

(a)

(b)

Figure 6. Photomicrograph of the Degradation (a) University of Arizona and (b) Sprague Thin-Film Capacitor's Al Bond Pad (125X).

TABLE II
Aging at 300°C for 600 hrs.

	<u>University of Arizona</u>	<u>Sprague</u>
Capacitance (nominal)	0.01 μ F	100 pF
Change in Capacitance	$\leq 2\%$	$\leq 2\%$
Dissipation Factor	0 to 0.050 @ 1 kHz	0 to 0.050 @ 1 kHz
Typical Values (DF)	0.010	0.010
Temperature Coefficient	179 ppm/°C @ 300°C	22 ppm/°C @ 300°C
Insulation Resistance	> 2000 megohm	> 3000 megohm

VI. Summary and Conclusion

Because the leakage current and physical size is of primary concern for capacitors in geothermal instrumentation, the ceramic and the MOS thin-film devices look promising. The thin-film capacitors showed better electrical characteristics than the ceramics during above 200 hours at 300°C, although in some cases the deterioration of the wire bonds and bond pads presented electrical problems. The ceramic "NPO" capacitors exhibited excellent capacitance and low-leakage current for approximately 200 hours at 300°C, but leakage current increased steadily during prolonged aging. The X7R and BX capacitors exhibited poor electrical characteristics at high temperatures prior to aging as was expected.

The data taken does not reflect on the performance of these capacitors during normal operating conditions as specified by the manufacturer. The University of Arizona thin-films were the only capacitors evaluated within the manufacturer's specification.

VII. Reference

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WRN:cmg:6228A:12/23/81X

APPENDIX

Figures of percent change in capacitance, insulation resistance, and dissipation factor versus temperature for the ceramic and thin film capacitors evaluated.

Figure 7. Data Taken During Temp. Increase @ 1kHz and 15 WVDC (a) $\Delta C/C$ (%) vs. Temp. (b) IR and DF vs. Temp.

Figure 8. Aging Data @300 °C, 1kHz and 15 WVDC (a) $\frac{\Delta C}{C}$ (%) vs. Temp. (b) IR and DF vs. Temp.

Figure 9. Data Taken During Temp. Increase @ 1kHz and 15 WVDC (a) $\Delta C/C$ (%) vs. Temp. (b) IR and DF vs. Temp.

Figure 10. Aging Data @ 300 °C, 1kHz and 15 WVDC (a) ΔC (%) vs. Temp. (b) IR and DF vs. Temp.

Figure 11. Data Taken During Temp. Increase @ 1kHz and 15 WVDC (a) $\Delta C/C$ (%) vs. Temp. (b) IR and DF vs. Temp.

Figure 12. Aging Data at 300 °C, 1kHz and 15 WVDC (a) $\frac{\Delta C}{C}$ (%) vs. Temp. (b) IR and DF vs. Temp.

Figure 13. Data Taken During Temp. Increase @ 1kHz and 15 WVDC (a) $\frac{\Delta C}{C}$ (%) vs. Temp. (b) IR and DF vs. Temp.

Figure 14. Aging Data @ 300°C, 1kHz and 15 WVDC (a) $\frac{\Delta C}{C}(\%)$ vs. Temp. (b) IR and DF vs. Temp.

Figure 15. Data Taken During Temp. Increase @ 1kHz and 15 WVDC (a) $\frac{\Delta C}{C} (\%)$ vs. Temp.
(b) IR and DF vs. Temp.

Figure 16. Aging Data at 300 °C, 1kHz and 15 WVDC (a) $\frac{\Delta C}{C} (\%)$ vs. Temp. (b) IR and DF vs. Temp.