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TRANSIENT HARDENED POWER FETS

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Abstract

N-channel power FETs offer significant advantages in power conditioning circuits. Similarly to all MOS technologies, power FET devices are vulnerable to ionizing radiation, and are particularly susceptible to burn-out in high dose rate irradiations ($>1\text{E}10$ rads(Si)/sec.), which precludes their use in many military environments. This paper will summarize the physical mechanisms responsible for burn-out, and discuss various fabrication techniques designed to improve the transient hardness of power FETs. Power FET devices were fabricated with several of these techniques, and data will be presented which demonstrates that transient hardness levels in excess of $1\text{E}12$ rads(Si)/sec. are easily achievable.

Introduction

The intent of our research was to develop a radiation hardened power FET device technology that was tolerant to $1\text{E}6$ rads(Si) total dose and would survive a $1\text{E}12$ rads(Si)/sec. transient. The test device for this evaluation was a DMOS device and had the following electrical characteristics: 65 V standoff voltage, 1 A drain current, and less than 1 ohm on resistance, all post irradiation. Although the total dose requirements represent a challenge, techniques for total dose hardening are well known and readily applicable to these devices. In fact, total dose hardened power FETs have previously been reported at this conference, so our activity concentrated on transient

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hardening this technology.¹ Figure 1 illustrates the test circuit for this study, while a Febetron 705 (FWHM = 22 ns) and HERMES II (FWHM = 54 ns) provided the flash x-ray sources.

N-channel power FETs are susceptible to burn-out as a result of an ionizing radiation exposure when they are in an off condition, which immediately suggests a circuit solution to this problem; namely to turn the device on upon initiation of a transient event. This, however, increases the circuit complexity and there are superior solutions. In the off condition, power FET devices failing due to a transient exposure (70 ns pulse width), typically exhibit a peak current with a width on the order of several hundred nanoseconds, followed by a gradually increasing tail (on the order of microseconds) and subsequent electrical short; this is illustrated in Figure 2. This supports the contention that the failure occurs when a high current avalanche breakdown is sustained for a sufficient time to permit thermal runaway. This failure mode can occur for voltage levels well within the normal operating area of the device, and failures² for standoff voltages as low as 0.1 BVds have been observed.

TEST CIRCUIT

Fig. 1

PHOTOCURRENT RESPONSE

Fig. 2

Figure 3 illustrates the cross section for a typical DMOS power FET device. The salient features that pertain to the transient hardness of this structure are the n+/n interface and the parasitic npn bipolar formed by the source (emitter), p- body (base), and drain (collector). Ostensively, the source and body are shorted, which would imply that the emitter and base are also, and thus could not turn on; however, the large lateral currents which are generated in high transient exposures frequently cause a sufficient voltage drop across the parasitic emitter-base junction such that the emitter becomes forward biased. The initial experiments attempted to determine the relative importance of the n+/n interface and the parasitic bipolar in causing the device failure in a transient environment.

The proposed model for the power FET burn-out is based on the behavior of the parasitic bipolar collector region in a high current mode. In a transient radiation environment, large numbers of carriers are generated, leading to an IR drop in the parasitic base region that initiates electron injection from the emitter. As the electron injection increases as a result of higher dose rates, the device begins to exhibit the characteristics of an epitaxial bipolar device in a high injection condition. The depletion region expands at the expense of the lighter doped collector epitaxial layer, until it pins at the n+ junction, and at this point, the electric field increases to a level that will support avalanche breakdown.³ The avalanche current is then available to maintain the emitter forward bias, and if the net gain exceeds unity, then positive feedback exists and a self-sustaining breakdown initiated. This ultimately will lead to device destruction.

Fig. 3

Conceptually, the power FETs could be hardened to transient radiation either by eliminating the parasitic bipolar device (or significantly reducing its gain) or by preventing the initial avalanche breakdown. Bulk CMOS devices traditionally were susceptible to latchup in a transient radiation environment as a result of parasitic bipolar devices, and for some design rules, were hardened to transient exposures by lifetime control, which reduced the parasitic bipolar beta product to less than unity. Similarly, earlier studies have demonstrated that the safe operating area for power MOSFETs can be expanded by lifetime reduction, which reduces both the parasitic bipolar gain and photoinduced stored charge.⁴ This technique unfortunately does not provide total immunity from transient induced failures, except within a restricted operational range. Our experiments attempted to determine the relative importance of the avalanche breakdown and the parasitic bipolar in the failure mechanism and, based on this information, develop a transient hardened power FET.

Discussion

The separation of the effects of the avalanche breakdown and the parasitic bipolar device in the power FET transient failure mechanism was attempted by fabricating a matrix of devices without an n^+ substrate and without an n^+ source diffusion. The devices without a source diffusion naturally were merely pn diodes. The experiment therefore contained four elements:

1. A power FET with a n epi/ n^+ substrate
2. A power FET with a n substrate
3. A pn diode with a n epi/ n^+ substrate
4. A pn diode with a n substrate.

These were exposed to various transient radiation levels over a range of V_{DS} voltages. Figure 4 illustrates a typical exposure result, in this case for an exposure level of $5E10$ rads(Si)/sec, and plots the peak photocurrent observed, which typically

Fig. 4

occured within a microsecond of the transient (20 nsec pulse width) pulse, as a function of V_{ds} voltage. At this level, the control devices all burned out between $5E9$ and $5E10$ rads(Si)/sec and were not plotted; while the diodes, as expected, exhibited no difference in photocurrent response whether an epi/n+ or a n substrate was used. It is clear, however, that the presence of the parasitic bipolar device causes a significant increase in the transient induced photocurrent. In the high dose rate tests, $1E9$ - $1E12$ rads(Si)/sec, there were no failures in either the epi/n+ or n substrate diodes, or in the power FET on the n substrate. Notwithstanding the positive results on the power FET, further experiments were initiated to insure that an optimum solution was obtained.

The experimental process modifications were designed either to reduce the parasitic bipolar gain or to minimize the avalanche breakdown. Devices incorporating these modifications, and combinations of these modifications, were then fabricated and evaluated in a transient environment. Experiments designed to restrict the parasitic bipolar gain in the power FET structure utilized lifetime control (neutron irradiation), enhanced base doping (self alignment with the p+ plug), and Schottky emitters (minimal minority carrier injection), while avalanche breakdown modifications were attempted with graded epi/n+ substrates, or in the extreme case, no n+ substrates.

The experimental results indicated that power FETs with either lifetime control or enhanced base doping could maintain parasitic bipolar gains of approximately three. On conventional epi/n+ substrates, however, this was insufficient to prevent device burnout, although the failure levels in some cases were extended approximately one order of magnitude over the control devices. Unfortunately, all of these variants failed by the $4.4E11$ rads(Si)/sec level. The Schottky diode emitter experiments have not proceeded exactly as planned, and their evaluation continues.

The graded epi experiments were attempted in an effort to maintain a conventional power FET structure that would not exhibit a significant increase in "on" resistance and provide a good back ohmic contact. A variety of epi gradations were applied to the substrate material, ranging over many microns for the transition region, but in all cases, for less than ten microns. Several epitaxial gradation profiles were utilized, including both a conventional monotonic as well as a step. The expectation was that the gradation would spread the region of high field relocation induced by the transient radiation pulse and thus moderate the avalanche breakdown. Based on a one dimension analysis of the doping profiles, a peak field reduction of approximately four was expected. Although this is difficult to experimentally verify; nevertheless, the

graded epitaxial substrate power FETs uniformly failed by transient radiation levels of $1\text{E}11\text{ rads(Si)/sec}$. While this was an improvement over the control samples, which have consistently failed in the mid $1\text{E}10\text{ rads(Si)/sec}$ range with considerable scatter, it still is insufficient for many radiation environments. Further epitaxial gradations will be attempted, but only after our simulation programs more accurately predict the device radiation response and demonstrate the efficiency of the epi gradation approach.

Several device lots from both process facilities have been fabricated with non-epitaxial (bulk) substrates and evaluated in a transient environment, and Figure 5 illustrates a typical photocurrent response from such a device. The non-epi devices all exhibit broad (1-5 microsecond) photocurrent peaks, with little evidence of the prompt pulse; for example, this can be compared with Figure 4 for the response of a conventional epi/n+ substrate. This is a result of the vastly increased photocurrent collection volume, which is restricted in a conventional power FET because of the low lifetime n+ substrate. Although the plotted peak photocurrent appears higher for the non-epi substrate, this is probably a reflection of an inadequate time resolution in the equipment; the spike for the epi/n+ substrate is clearly sharper than the bulk counterpart, which indeed does not even exhibit such a characteristic.

Fig. 5

All power FET devices fabricated on bulk substrates have passed transient radiation tests at the $1\text{E}12$ rads(Si)/sec level. Although other process modifications have improved the transient tolerance of the power FET, the bulk substrate clearly offers the greatest tolerance. It does, however, not come without a cost. Greater care must be taken in forming the back ohmic contact, and the bulk substrate power FET, as presently configured, has a higher on resistance than its epi/n+ counterpart. For a nominal 1 ohm on resistance device, this increase is on the order of 300 milliohms. Further experiments are underway to reduce this resistance, but it is unlikely to ever equal the epi/n+ device value, but the difference may not be important for many system applications.

Summary

The n-channel power FET failure mode in a transient radiation environment has been evaluated and determined to be a result of avalanche breakdown induced by the parasitic bipolar and epi/n+ substrate configuration. Several experimental structures, designed to minimize both the parasitic bipolar gain and transient induced high field relocation, have been fabricated and tested. The conclusions are that significant improvements can be achieved by reducing the parasitic bipolar gain or by grading the epi/n+ junction, but for transient hardness at $1\text{E}12$ rads(Si)/sec levels, the device should be fabricated on bulk substrates.