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Hybrid Microcircuit Via Development

By D. P. Norwood

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Manufacturing processes were developed for making holes in alumina substrates, metallizing substrates on both sides and through the holes (vias), dry film photolithographing 6-μm-thick gold to 127-μm line widths and spacings, determining via quality, and protecting vias during HMC assembly processes. The few problems encountered were solved, and via technology is now established as a reliable and repeatable production technology for hybrid microcircuits. Via resistance on product HMCs usually measures from 4 to 6 mΩ which is well below the 10 mΩ maximum limit.

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SUMMARY

Hybrid microcircuits (HMCs) designed by Sandia Laboratories require metallized vias to interconnect frontside thin-film networks (TFNs) with metallized backside ground planes on 95- by 114-mm-square alumina substrates. Manufacturing processes were developed for making holes in alumina substrates, metallizing substrates on both sides and through vias, dry film photolithographing 6-μm-thick gold to 127-μm line widths and spacings, and determining via quality and acceptance.

Vendor supplied samples of 99.5 percent alumina substrates containing hole patterns made by punching holes in the green (unfired) ceramic with hard tooling were unacceptable because of defects on the hole walls. Therefore, the following alternate methods for fabricating holes in both green and fired ceramic were investigated: ultrasonic drilling and impact milling, punching green (unfired) ceramic using soft tooling, drilling green ceramic with a high speed drill, and laser drilling followed by an air abrasive clean-up.

The critical parameters for hole fabrication are diameter tolerance, location tolerance, via wall surface finish, chipping, cracking, residue beside the hole, lead time, and cost. Both green punching (soft tooling) and green drilling proved to be the best methods except for lead time and location tolerance. Where location tolerances were required to be closer than green fabrication could produce, laser drilling followed by air abrasive clean-up was superior. The shortest lead time was provided by ultrasonic drilling; however, the cost is high and not all defects within the hole were eliminated.

Chromium-gold metallization on the substrate surface and through holes was done in a planetary evaporation system. It was shown that sufficient metallization can be deposited in the hole by metallizing the front of the substrate and then turning it over for backside metallization. This method provides overlapping of metallization inside the ceramic hole and ensures frontside-to-backside conduction. Via metallization quality was found to be dependent on the quantity of gold evaporated and the geometry of the evaporation system. The surface roughness and defects in the ceramic hole also contributed to the resistance of the via intraconnection.

Photolithography techniques were developed that protect both sides of the substrate and the vias from etchants and delineate a thin-film network consistent with critical HMC line width tolerances for radio frequency circuits. For defining the conductor pattern, dry film photoresist was applied to both sides of the

substrate simultaneously. Liquid resist, which had been used for photoprocessing HMC conductors without vias, was not acceptable for HMCs with vias. A minimum dry film resist thickness of 25 μm was found to protect vias and still produce the conductor line widths and spacings required for thin-film networks. Normal liquid resist photoprocessing was used for patterning the resistor circuitry.

Visual and electrical inspection techniques were developed for determining via quality and acceptance. A four-point-probe system was devised which measures frontside-to-backside resistance. This resistance indicates the amount of gold deposited on the via wall and the surface roughness of the via wall.

Thermocompression bonding of gold foil via covers was developed to protect vias during soldering processes.

The techniques developed produce vias which exhibit through-hole resistances of less than 10 mΩ and are acceptable for radio frequency or logic circuit application. Sample parts were fabricated and evaluated on both test substrates and production substrates to prove in the new techniques. The few problems encountered with initiating a new process into production have been solved, and via related technology has been used successfully in production.

DISCUSSION

SCOPE AND PURPOSE

This work was conducted to develop manufacturing processes for thin-film networks (TFNs) containing metallized vias. The project was initiated with a residency at Sandia Laboratories, Albuquerque (SLA) to assist in the development of via technology and was continued at Bendix Kansas City through initial production of radar circuits. The work included development of all technology including hole fabrication, metallization, photolithography, and assembly processing.

PRIOR WORK

A development radar program at SLA required technology to fabricate vias in hybrid microcircuits (HMCs). A cursory evaluation by the hybrid microcircuit technology group at SLA demonstrated the feasibility of via technology. Although TFN and HMC fabrication processes at Bendix had been in production for some time, via technology introduced several new processes not in use at Bendix. The work accomplished in this effort was generally to develop these processes and to establish their compatibility with existing processes which would be used in fabricating HMCs containing vias.

ACTIVITY

Bendix HMC Processes

Hybrid microcircuits manufactured at Bendix are produced on 95- by 114-mm substrates of 99.5 percent aluminum oxide. A layer of tantalum nitride (Ta_2N) is sputtered on the substrates and followed by vacuum evaporated layers of chromium and gold. Typical film thicknesses are 0.05 μm of Ta_2N, 0.025 μm of chromium, and 3 to 7.5 μm of gold. The Ta_2N is used for resistors and Au for conductors. Chromium acts as an adhesive layer between the Ta_2N and Au.

Multi-image photoprocessing techniques are used to process substrates to the thin-film network level. Typically 6 to 12 TFNs are obtained from a large metallized substrate depending on the size of the TFN (25- by 25-mm sizes are common). Two mask levels are required to produce the TFN pattern--the first for the conductor pattern and the second for the resistor pattern. Off-contact printing is used to expose the resist, which for substrates

without vias, is liquid resist which is applied with a roller coater. Exposure is made on a machine capable of a high degree of light collimation over a 100- by 125-mm area.

After the resistors have been photoprocessed, they are thermally stabilized in air at 300°C for 2 hours. Laser scribing is used to separate the large substrate into smaller TFNs. Resistors are trimmed to nominal value using an automated yttrium aluminum garnet (YAG) laser system. Prior to HMC assembly, thin-film networks are prebond etched with ceric ammonium nitrate (CAN) and cleaned. HMCs are assembled with beam lead devices by thermocompression gold-to-gold bonding; capacitors are either Pb-In solder attached or epoxied in place and fine-wire bonded for electrical connection. Ribbon bonding is used to furnish interconnection on the TFN circuitry. Electrical connection and mechanical attachment to the HMC is furnished by thermocompression bonded lead frames.

Via Related Process Changes

Backside metallization of HMCs was required when new circuits were developed at SLA for production at Bendix. Backside metallization is a ground plane for higher frequency circuitry used in HMCs and provides ground interconnections on logic circuitry. The intraconnection between the frontside and backside is a feedthrough--vacuum metallized hole called a via. The presence of the ground plane and the via connections in HMCs meant several changes in HMC process methods at Bendix.

- A method of hole fabrication in alumina substrates had to be developed for HMCs which provided the hole location, diameter tolerances, and electrical characteristics when vacuum metallized.

- Frontside and backside Cr-Au metallization of substrates was required, and the method of deposition had to produce a continuous Cr-Au thin film of sufficient thickness on the via walls to meet the electrical characteristics necessary for HMCs.

- Photoprocessing techniques consistent with TFN line width and spacing tolerances were required to protect vias and backside metallization during etching. A method of aligning the photomask to the via locations at the first level of patterning was required.

- Electrical and visual methods for production inspection of vias had to be developed.

- HMC assembly processes had to be modified as necessary to be compatible with via technology.

The details of the work conducted to develop these capabilities are described in previous reports.[1-5] Each activity is summarized below.

Hole Fabrication in Alumina Substrates

Many hole fabrication methods were investigated to produce holes with acceptable limitations on location, diameter, chipping, cracking, and surface finish.[1,2] The fabrication methods investigated were:

- An improved method of punching green (unfired) ceramic using soft tooling;
- Drilling green ceramic using a numerical control (NC) machine;
- Ultrasonic impact milling;
- Ultrasonic drilling; and
- Laser drilling followed by removal of glassy material using glass bead peening.

The cost of various hole fabrication methods are compared in Table 1 and typical working tolerances are shown in Table 2.

Green hole fabrication processes proved superior in all respects except lead time and location tolerances. The accuracy of hole location in green ceramic is limited by the predictability of the shrinkage factor. Ceramic shrinkage during firing is approximately 17 percent. Where location tolerances were required to be closer than green fabrication could produce, laser drilling followed by air abrasive clean-up was superior. Ultrasonic drilling provides the shortest lead time but is the most expensive.

Tantalum nitride and chromium do not adhere well to surfaces which have been machined; apparently machining removes a surface layer containing silicon, magnesium, and calcium oxides which help adhesion. Refiring the substrates at 1450 ±25°C was shown to restore most of the adhesion between the ceramic and metal. Refiring is required for ultrasonically drilled (or impact milled) holes and for laser drilled holes which have been glass bead peened.

Cr-Au Metallization of Substrates With Vias

Metallizing the walls of the holes in ceramic substrates is required to produce a low resistance electrical path between the frontside and backside of a hybrid microcircuit. To provide the necessary complete via coverage, a planetary substrate holder

Table 1. Cost and Time Comparison of Hole Fabrication Methods

Method	Minimum Lead Time (Weeks)	Direct Cost ($)			
		Drilling 60 Holes in One Substrate	Tooling and Setup	Drilling Cost Per Substrate	
				100 Lot Size	1000 Lot Size
Green Punch (Hard Tooling)	20	2	3000	32	5
Green Punch (Soft Tooling)	16	8	1000	18	9
Green Drill	12	5	200	7	5.20
Ultrasonic Drill	1	50	200	52	50.20
Ultrasonic Impact Drill	1	200	200	202	200.20
Laser Drill With Glass Bead Peening	2	9	200	11	9.20

which revolves during the evaporation process is used.[2-3] Substrates are first metallized on the frontside and through the vias while the planet is revolving; then the substrates are turned over for backside and further via metallization.

The geometry of the planetary system was evaluated to determine the orientation of substrates with respect to the evaporant line of travel which produced the best via coverage and thickness uniformity on the planar surfaces. Figure 1 shows the geometric considerations of the planetary system used at Bendix Kansas City. Best thickness uniformity on the planar surface is obtained when the substrates are mounted on a concave planet. Best via coverage is obtained when the substrates are mounted on a flat planet. Metallization tests were conducted in which the substrates were mounted in different configurations (concave, flat, and mid-point) on each of the three planets on the fixture. In the mid-point configuration, the angle between the substrate and planet is

Table 2. Typical Working Tolerance (True Position) Comparison of Hole Fabrication Methods

Method	Tolerances (mm)			Summation* (Worst Case Pad Size) (mm)
	Diameter	Location	Chip and Crack	
Green Punch (Hard Tooling)	0.076	0.660**		1.625
Green Punch (Soft Tooling)	0.051	0.330**		1.270
Green Drill	0.051	0.330**		1.270
Ultrasonic Drill	0.229	0.127	0.508	1.753
Ultrasonic Impact Milling	0.254	0.127	0.508	1.778
Laser Drill With Glass Bead Peening	0.152	0.127	0.245	1.422

*Summation is the sum of the working hole diameter (0.183 mm), photolithographing alignment tolerance (0.076 mm), and tolerances for diameter, location, and chip and crack. This gives the minimum required gold pad size to produce high yield. The smallest pad size on product is 1.524 mm; therefore, ultrasonic drilling requires 100 percent inspection.

**For green processes, the location tolerance is based on a substrate working area of 76- by 102-mm and is determined by the predictability of shrinkage during firing.

halfway between the concave and flat planet configurations. The effects of gold thickness and via diameter on via resistance for each of the three configurations is shown in Figure 2.

Thickness variation on the planar surfaces was found to be 29.7 percent for substrates on the flat planet, 13 percent for substrates on the mid-point planet, and 6.3 percent for substrates

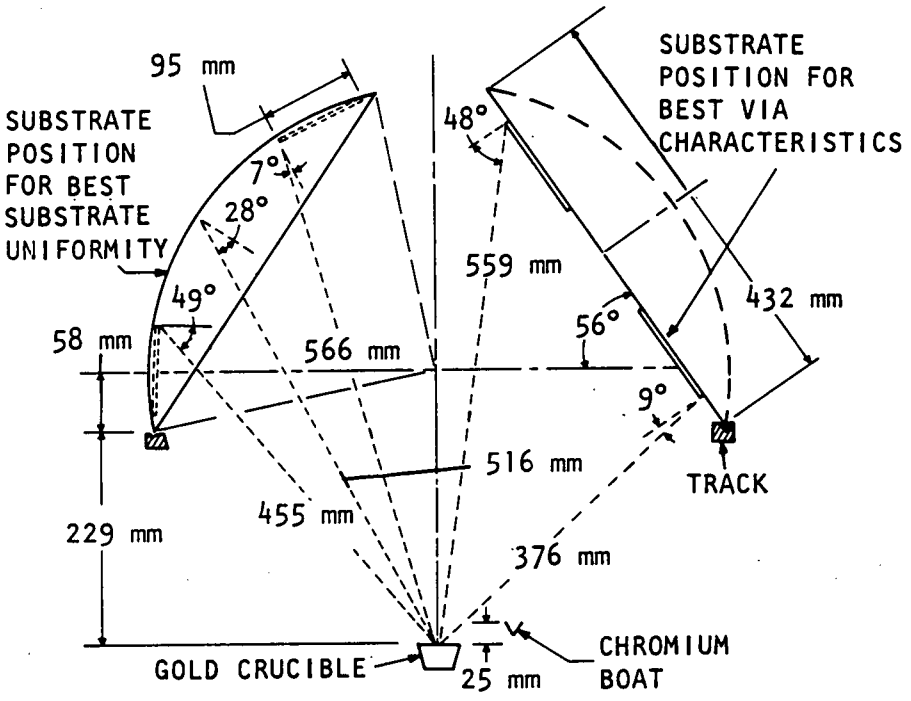

Figure 1. Geometry Considerations for Evaporation Process Using Planetary Fixture

on the concave planet. As a result of these tests, the mid-point planet was chosen for production metallization of substrates with vias.

Photoprocessing of Substrates With Vias

The introduction of metallized vias into ceramic substrates required modification of photopatterning techniques: the vias had to be protected during the etching steps used to delineate the thin-film network pattern.[2,4] Liquid resist proved ineffective in protecting the metallization on the via walls so the technique of "tenting" was adopted for via protection. This process, common in photoprocessing multilayer printed circuit boards, consists of trapping the feedthrough hole between two layers of dry film resist. However, a major difference exists in the tolerances and line widths required for printed circuit boards and those required for thin-film networks. The minimum line widths required for HMCs are 127 μm--a factor of five less than standard printed circuit board circuit paths.

A minimum dry film resist thickness of 25 μm was found to protect vias and still produce the conductor line width and spacings required for thin-film networks. The resistor circuitry is patterned with normal liquid resist photoprocessing.

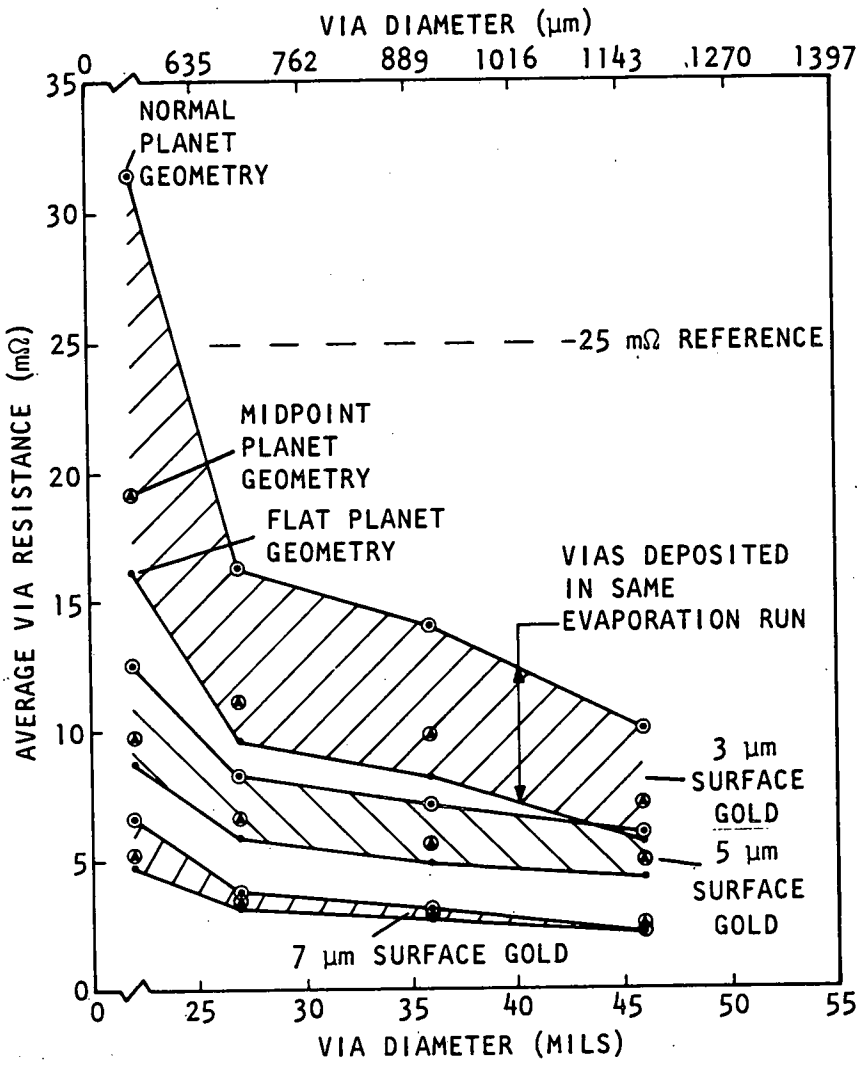

Figure 2. Effects of Via Diameter, Gold Thickness, and Planet Geometry on Via Resistance

The maximum via diameter which could be reliably protected by dry film resist was found to be 1.2 mm. In addition, test results established that resist adhesion to the substrate surface surrounding the via required a minimum distance of 125 μm between the via pad and the via hole; otherwise, via protection could not be ensured during the etching operation.

There are two general categories of dry film resists: solvent base resists and aqueous base resists. The difference is in the type of developer and stripper solutions used in photoprocessing. Aqueous resist was shown to be more desirable for TFN photo-

processing; there are no delay times involved in processing the aqueous resists while solvent resists require a delay of approximately 15 to 20 minutes after lamination and after exposure. Solvent developers are highly active and must be maintained at lower-than-room temperatures to prevent overactive development of the resist pattern; aqueous developers can be used at room temperature or above. In addition, aqueous resist was found to produce conductor patterns closer to mask dimensions because of its sidewall definition after development. Solvent resists were found to undercut during development and to require closer control during processing.

Routine photoprocessing of line widths and spacings of 127 μm to tolerances of ±12.5 μm was shown to be possible using dry film and immersion processing. It was not possible to repeatedly reproduce the conductor tolerances of ±6 μm desired for radio frequency (rf) circuitry in radar HMCs. Spray processing was found to be advantageous in developing and stripping dry film resist because of the film thickness and developing characteristics. It was not possible to produce line widths and spacings less than 75 μm without spraying, and even then results were marginal. However, since HMC product requirements are above 125 μm, this is not a serious limitation.

Since the substrates contain holes, the first level conductor photomask has to be aligned to this hole pattern. The alignment of the photomask to the resist-covered holes in the substrate posed a problem because of the optical system used in the exposure machine. Standard TFN alignment techniques require a clearly visible target on the surface and the dry film resist acted to reduce the visibility of the alignment holes. The problem was resolved by using a backlighting.

Resistor patterns were routinely photoprocessed using techniques developed for TFNs without vias. A potential problem was discovered as a result of increased conductor thickness and the use of the roller coater for applying resist. A combination of the 6-μm-thick conductors and a worn roller resulted in incomplete coverage of resistor material adjacent to the resistor termination pads. In several instances, the resistor path was etched away at the gold terminations. A worn or overused roller was contributing to this condition, and the problem was solved by changing the roller more frequently.

Solid resists were found to be sensitive to higher temperatures after laminating as a result of air trapped within the via. Higher temperatures tended to expand the trapped air, cause a bubble effect in the resist, and sometimes damage the resist coverage. An upper temperature limit of 50°C was imposed on substrates until the dry film resist was removed during the stripping process.

Dry film resist adhesion was found to be a function of substrate surface cleanliness. Substrates photoprocessed with dry film immediately after metallization were found to have good adhesion properties, but substrates delayed in photoprocessing for extended times displayed resist adhesion problems. Further investigation determined that good adhesion properties could be restored by a cleaning operation similar to that used in degreasing.

Component Relief Holes

An unexpected problem occurred in TFN photoprocessing when it was found that metallization deposited in component relief holes could not be adequately etched during photoprocessing. Component relief holes are used in radar TFNs to provide relief for large components which must nest in the substrate and be in intimate contact with the grounding plate attached to the TFN backside. These relief holes are approximately 3 mm in diameter and are either square or round depending on the component shape. The components are rf transistors which require close contact with the metal backplate for grounding purposes.

Since metallizing techniques were designed to ensure complete coverage of via walls, the component relief holes were also coated. Etching during photoprocessing was expected to remove the metallization in these holes which was a requirement for proper rf electrical operating characteristics. Also, since rf transistors were soldered into position, any residual metallization on the component hole wall provided a potential short circuit hazard. Early product requirements would not allow metallization inside the relief holes.

Since the component holes had a surface less smooth than the substrate surface, investigations found that metallization inside these holes would not etch at the same rate as surface metallization. Also, etchant circulation inside the hole was not as good as over the substrate surface which compounded the problem. Generally, studies revealed that the gold could be etched away; however, residual tantalum was found in most component holes after photolithography. An early solution to this problem was to remove the residual tantalum using a swab and selectively etching the component hole with Ta_2N etchant. This approach was found to create resistor problems because some of the etchant would splash onto the resistors resulting in over resistance conditions. A second approach was to physically abrade the component hole with a diamond file. This method was more acceptable, although it created some handling damage to the TFN surface and resulted in enlarging the component hole.

Several methods of removing the residual metallization in component holes were subsequently evaluated for cleaning properties

along with their effects on TFN circuitry. The techniques evaluated were:

- Avoid the problem by sealing or screening the holes during sputtering-evaporation,
- Mechanical removal by abrading, and
- Chemical removal.

The most effective technique for component hole cleaning was glass bead peening using resist protection for the TFN surfaces. Photoresist is used to protect substrates (both sides) which are then stacked approximately five deep for the peening operation. A blank TFN containing component holes is placed over the top and bottom of the stack for more protection. TFN corners and sides are used to align the component holes. This creates a cylinder of component holes through which the glass beads can be sprayed. After peening is conducted, photoresist is then stripped and TFNs are inspected for cleaning effects and damage. Peening was found to result in almost complete removal of the residual metallization.

Although the peening operation was considered a better method for cleaning component holes, two changes in processing preempted its use. Investigations determined that some residual metallization in the component hole was not detrimental to product function if it did not bridge from the top to the bottom of the TFN surface. In addition, metallic buttons were designed that would fit into the component holes during metallization to shield the side walls. This resulted in minimal amounts of residual metallization to remove. These changes have resulted in less rework after photolithography to clean component hole metallization, but have not completely eliminated the problem.

Via Inspection

A four-point-probe measurement technique adopted by Bendix for inspecting plated-through holes in printed circuit boards provided the best method of determining via quality.[2] Increased resistance has been found to be related to plating or printed circuit board hole defects. A significant difference exists between via resistance characteristics and those of plated-through holes in printed circuit boards: printed circuit board hole resistances are measured in microohms, while HMC vias are measured in milliohms. Investigations determined that defective vias could be discovered using the through-hole measurement technique. Defects such as missing metallization, hole surface roughness and discontinuities, and low metallization thicknesses can be detected using a via resistance measurement system.

The measurement system consists of a constant current source and a voltage measurement device. A constant current is applied through the via and the voltage drop across the via is measured. Via resistance is proportional to the voltage drop. Two probes are located on each side of the substrate so the four-point-probe connection can be made. Via resistances can be measured from 1 to 200 mΩ.

A fisheye microscope can be used to make a visual inspection of metallized vias at any processing level. A monocular microscope with a fisheye objective lens is combined with an opaque glass examination platform backlighted by fluorescent bulbs. It operates like a normal microscope except the fisheye lens allows visual penetration down into the via for via wall inspection.

Experience has shown that the via hole surface finish is hard to observe with the fisheye microscope before the substrate is metallized. The ceramic hole surface reflects and diffuses the incident light around the interior of the hole and prevents the shadowing which might be created by voids, pits, or roughness. The fisheye microscope was, therefore, eliminated as a means of detecting flaws in uncoated vias. Immediately after metallization of the hole surface, the defects become apparent because the metallization does not disperse the light. This was a problem in determining hole surface quality or defects after hole fabrication and prior to metallizing. Therefore, ceramic hole inspection techniques were developed to determine hole quality. These techniques were used to check for hole surface conditions and cracking in the ceramic adjacent to the hole. A combination of low-angle light inspection and dye-penetrant testing was used for determining ceramic chipping and cracking; scanning electronic microscope (SEM) photography using backscatter mode made the via wall surface visible for determining roughness. It is possible to use dye-penetrant testing and low angle light for 100 percent inspection; the tests do not adversely affect the ceramic substrate. SEM testing is a destructive test that requires sectioning of the hole; therefore, it is a sampling type of test.

Results of development work showed that a combination of visual and electrical requirements were necessary to ensure via quality. Visual defects could occur on any one via (regardless of lot); therefore, 100 percent inspection was required. The specified production inspection is to sample via resistance on each large substrate (typically four vias), and then visually inspect each via individually. This procedure has been successful in detecting any via related problems.

Via Sealing

Problems were encountered early in development of HMCs containing vias because of the assembly soldering operation.[5] Most HMCs are rf circuits requiring a heat sink or back plate to be soldered to the metallized backside of the HMC to dissipate heat or provide electrical shielding. In addition, several components such as capacitors and inductors are soldered to the frontside TFN circuitry very close to vias. In most instances, one terminal of these applique devices is to be electrically grounded; consequently, the grounded side is located adjacent to or directly on the via. Molten solder flows into the via, and in some instances, will completely fill the via during solder attachment. Backside soldering of the mounting plate for heat sinking results in all vias being partially or totally filled with solder. Frontside circuitry does not require applique components at each via location; therefore, the top side entrance to the via is not always subjected to solder.

Studies conducted on the effects of solder in metallized vias show that degradation of the electrical connection does take place. This degradation results in an increased via resistance which is accelerated with thermal cycling. Tests have shown that a via which is filled with 50-50 PbIn solder will experience an initial decrease in resistance. This decrease results from the addition of more conducting area through the via, but is short lived when the HMCs are subjected to temperature cycling. Solder filled vias will start increasing in resistance at 10 cycles and will continue to increase as long as temperature cycling is maintained; in some instances, open circuiting of the via results. Figure 3 shows the result of 200 temperature cycles on solder filled and non-soldered vias. The temperature cycle was -55 to +125°C. Three thicknesses of metallization (surface gold) were evaluated and via diameters were from 0.64 to 1.27 mm. All soldered vias regardless of metallization thickness showed resistance increases by temperature cycling.

During its life, an HMC will encounter many temperature extremes which could significantly alter the electrical characteristics of a solder filled via. This could, in turn, produce an electrical failure or out-of-tolerance electrical condition on an HMC. Consequently, a method of protecting the via from solder entry was considered necessary to prevent HMC failures and to establish a reliable ground path.

The following methods of preventing solder encroachment into vias were investigated in a combined effort by Bendix and SLA: via plugging by stainless wire, stainless pins, non-metallic plugs, and selective plating. In addition, via sealing with epoxy pre-forms, solder wave discs, and thermocompression (TC) bonded

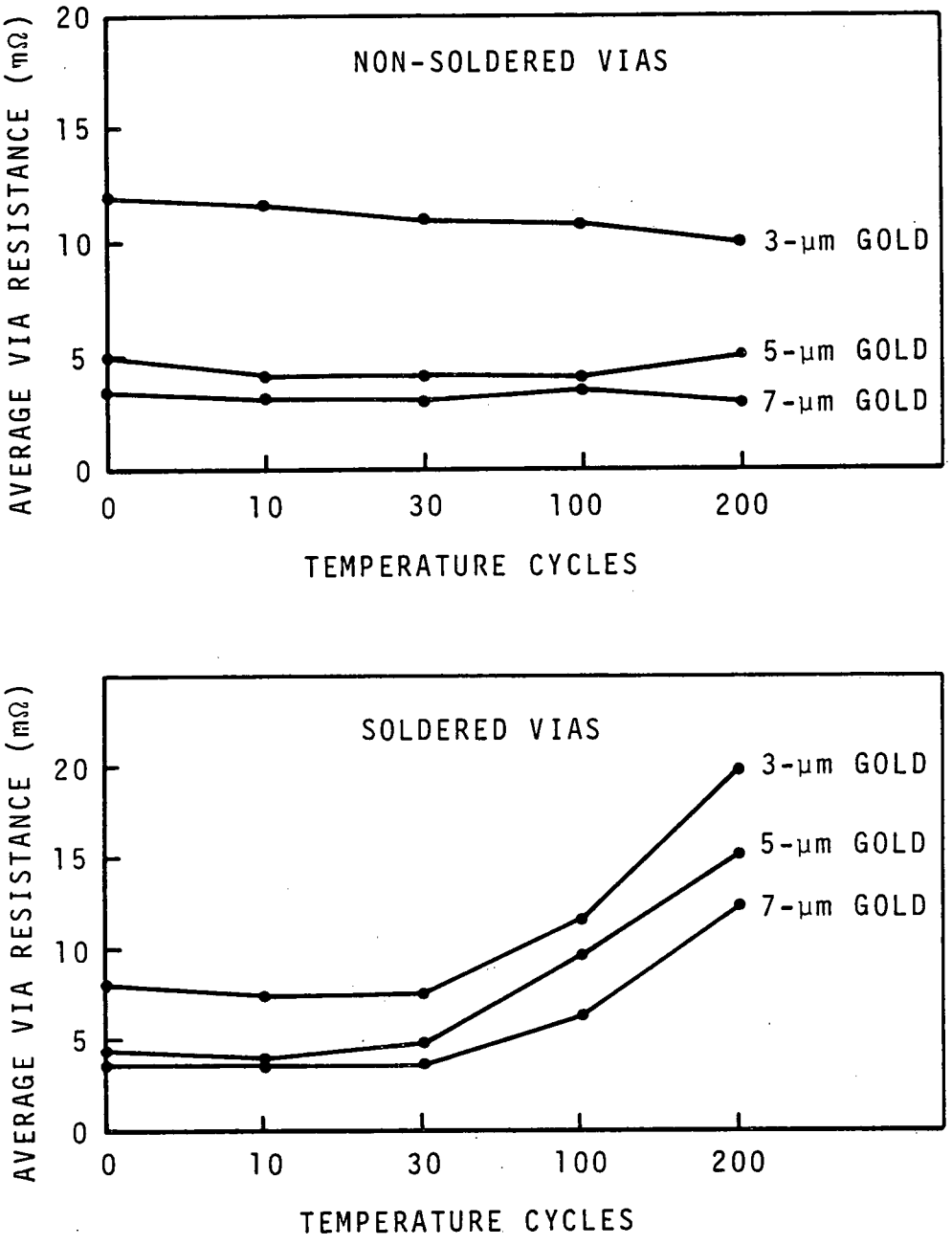

Figure 3. Temperature Cycle Effects on Soldered Vias

gold foil were studied. The most promising method of sealing vias was found to be TC bonding gold foils over the front and backside entrances to the via. This technique consisted of using a thermal compression wobble bonder to bond a 25-μm-thick gold foil to the gold metallization surrounding the via. This method of sealing had advantages in that it could be used on either side

of the HMC and did not introduce a new or different bonding attachment method into production. The same equipment used to TC bond beam lead devices could be used to bond the gold pre-forms over the via. An additional advantage was later discovered when this method of via sealing was introduced into production. Soldering of applique components to a via annular pad had been an awkward operation since the solder would generally flow into the via and the component was precariously located adjacent to the via hole. When foil sealing was introduced, the resultant via location consisted of a flat uniform surface. This eliminated the precarious placement of applique components next to the via.

Tests showed also that the foil sealing method met the environmental testing required by production HMCs with no adverse affects on electrical or mechanical integrity of the via. Details of the environmental and electrical-mechanical testing are included in another publication.[5]

Production Results

Via photolithography techniques were expected to result in a 10 to 15 percent decrease in yield at the thin-film network level. The dry film processing is reliably producing 127-μm conductor definition with no noticeable increase in conductor defects. Product acceptance at the TFN inspection level has been approximately 70 percent which compares favorably to product without vias.

Distributions of via resistance on production TFNs show resistances to be well within the prescribed tolerance. Most vias measure in the range of 4 to 6 mΩ which is well below the 10 mΩ maximum limit (Figure 4). The hole fabrication technique was found to contribute to resistance of the through-hole connection depending on the roughness of the hole surface. Recently, laser drilled holes were introduced into production which resulted in a substantial decrease in via resistance caused by hole surface characteristics. Via resistance, which was averaging approximately 5 mΩ, was found to be approximately 3 mΩ with laser drilled holes. This offered a cost saving in hole fabrication techniques and simultaneously yielded lower resistance vias.

RF characteristics of vias have been found to be well within usable limits for strip line terminations. Work was completed early in the development project to determine the rf characteristics of an as-metallized via. As-metallized vias were found to provide a very good rf connection when compared to a non-metallized via with a 76- by 508-μm ribbon routed through the hole and bonded on either side.

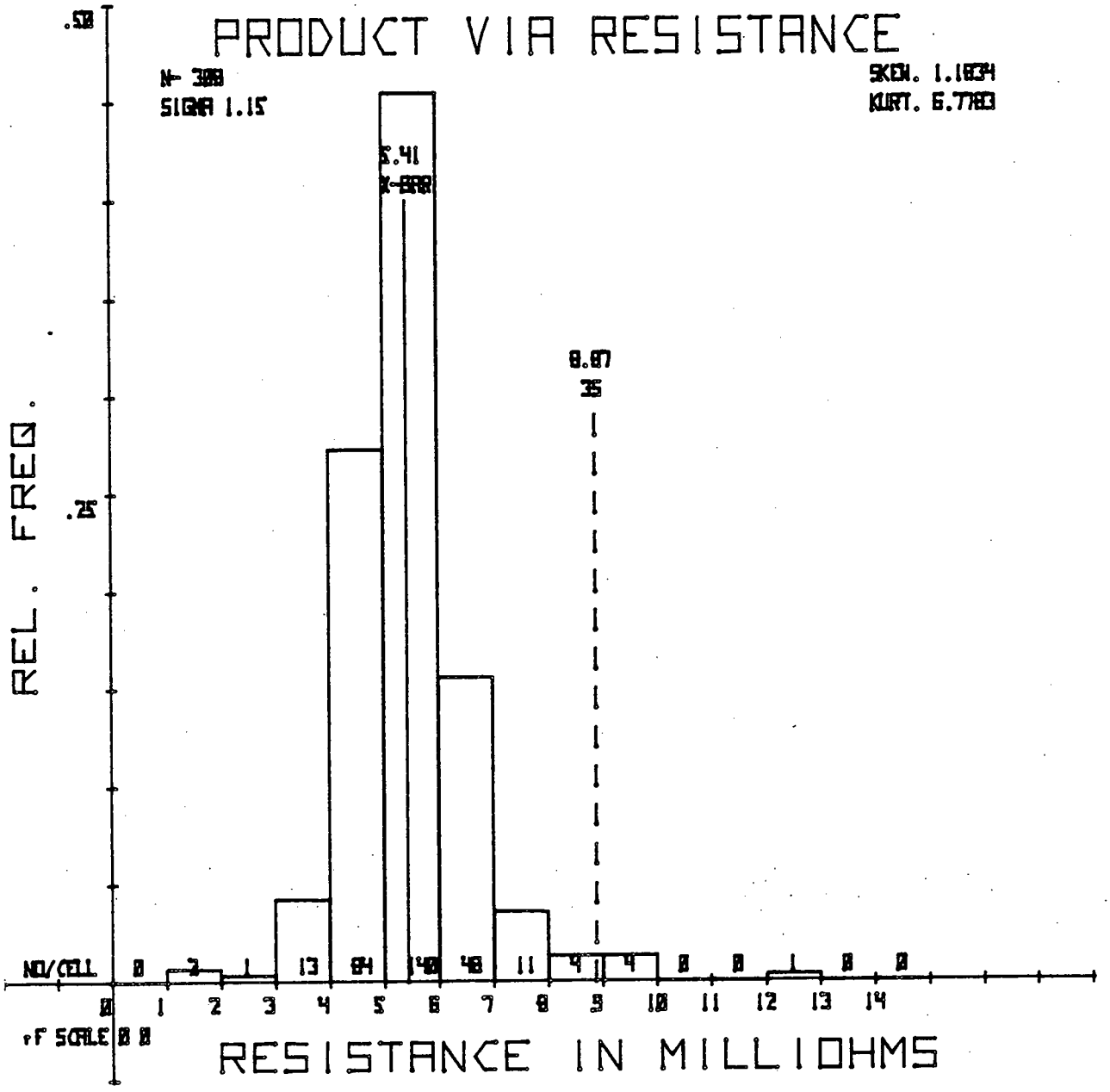

Figure 4. Via Resistance Distribution for 6-μm Gold Production Measurements

ACCOMPLISHMENTS

This project established the processes necessary to manufacture TFNs containing metallized vias. Once these processes were specified and production was ready, additional work was conducted to improve the processes and to solve the remaining

problems. Hole fabrication, photolithography, inspection, and subsequent HMC assembly processes were developed and phased into production. No future work is required unless product or technology requirements change.

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