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THE DIGITAL DATA ACQUISITION CHAIN AND THE COSMIC RAY TRIGGER SYSTEM FOR THE SLD WARM IRON CALORIMETER*†

A. Benvenuti
INFN Sezione di Bologna, I-40126 Bologna, Italy

L. Piemontese
INFN Sezione di Ferrara & Università di Ferrara, I-44100 Ferrara, Italy

A. Calcaterra, R. De Sangro, P. De Simone
Laboratori Nazionali di Frascati dell 'INFN, I-00044 Frascati (Roma), Italy

P.N. Burrows, S.L. Cartwright, S. Gonzales, A. Lath, U. Schneekloth, D.C. Williams, J.M. Yamartino
Massachusetts Institute of Technology, Cambridge, MA 02139 USA

N. Bacchetta, D. Bisello, A. Castro, S. Galvagni, M. Loreti, L. Pescara, J. Wyss
INFN Sezione di Padova & Università di Padova, I-35100 Padova, Italy

B. Alpat, G.M. Bilei, B. Checcucci, R. Dell'Orso, M. Pauluzzi, L. Servoli
INFN Sezione di Perugia & Università di Perugia, I-06100 Perugia, Italy

M. Carpinelli, R. Castaldi, U. Cazzola, C. Vannini, P.G. Verdini
INFN Sezione di Pisa & Università di Pisa, I-56010 San Piero a Grado (Pisa), Italy

R.L. Messner, R.W. Zdarko
Stanford Linear Accelerator Center, Stanford University, Stanford, CA 94309 USA

J.R. Johnson
University of Wisconsin, Madison, WI 53706 USA

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†Talk presented by Piero G. Verdini.

Abstract

The entire data-acquisition chain, from the custom-made front-end electronics to the Fastbus readout and data-reduction module, for the digital readout of the SLD [1] limited streamer tube Warm Iron Calorimeter and Muon Identifier is described. Also described is a Fastbus Cosmic Logic Unit being developed to achieve the capability of reading cosmic ray events, also during the inter-crossing time, for apparatus monitoring and calibration purposes.

Introduction

The SLD Warm Iron Calorimeter and Muon Identifier (WIC) [2] is a structure of 5 cm-thick iron plates interleaved with standard (0.9 mm cell size) plastic limited streamer tubes. To fully exploit the muon identification and tracking potential of the device, a great number ($\approx 10^5$) of tracking channels ("strips," see Fig. 1) must be read; additionally, to achieve maximum hermeticity, the number of outgoing data transfer links must be minimized; last, it is desirable to apply zero-suppression and possibly clustering and mismapping correction algorithms to the data as soon as feasible along the readout chain. This obviously poses heavy restrictions on the cost and the encumbrance of the front-end digital electronics, on the readout mode and on the data reduction and preanalysis capabilities of the data acquisition module.

The custom design D779 CMOS chip—a joint project of SGS [3] and of the Istituto Nazionale per la Fisica Nucleare (INFN)—contains four common threshold discriminators, each followed by a one-shot, plus a 4-bit wide shift register (Fig. 2) having daisy chaining capabilities in a 16-pin dual-in-line micro-die package. The chip has been adopted as a building block for the front-end electronics. The capability of the D779 of giving a Digor—the fast wired-Or combination of the discriminator outputs—easily extended to form triggering information over numbers of D779's, and has also been exploited to construct a cosmic ray trigger for the apparatus.

A dual-D779 hybrid with a fast two-stage, 50 times gain preamplifier [4,5] has been developed jointly with SGS to enable full detection efficiency operation even if the chambers are at an operating point substantially lower than the limited streamer point.

The natural data structure in such a shift-register-based environment is the daisy chain of all the D779's connected to the strips of one plane of the apparatus. To minimize the number of outgoing data (and incoming control) connections, a concentrator board ("splitter board") has also been developed [7] to link daisy chains belonging to the same sub-sub-system and having remote system configuration and diagnostic capabilities. The Splitter Board features a separate DAC threshold setting for the discriminators of each of the ten planes served, independent ADC readout of the threshold values, and combinatory and majority logic which allows a sub-sub-system trigger to form which is then used by the Cosmic Logic Unit (CLU).

The Warm Iron Calorimeter Digital Readout Module (WICDRM) [5,6] was also designed keeping well in mind the daisy chain structure characteristic of the front-end

boards, which minimizes the number of connections with the interior of the detector while retaining the capability to perform two complete readout cycles per Stanford Linear Collider (SLC) pulse, even at the design maximum operating frequency of 180 Hz. A MC68020 microprocessor [8] is used to perform a first stage of data reduction and apparatus monitoring exploiting the intercrossing readout. This choice for the CPU was dictated by its powerful processing and input–output capabilities and full 32-bit architecture; which nicely matches the 32-fold modularity of the front-end electronics and the availability of good software support.

The Front-End Electronics

The SLD Advisory Committee requested that a solution be found for the WIC front-end electronics capable of operating with strip signals much smaller than those characteristic of the limited streamer regime, should detector deterioration advise in favor of a drastic reduction of the electrical field in the chambers. A two-stage preamplifier for the D779, using two very fast 2N918 transistors for a preamplification of approximately 50 times but having the additional requirement of a +12 V power supply, was tested and eventually selected.

Figure 3 summarizes part of the studies made on the threshold curve dependence upon the operating point of the limited streamer tubes in a cosmic ray setup. The lower scale shows the V_{th} applied to the D779's, while the upper scale refers to the threshold voltage renormalized by the preamplification, showing therefore the equivalent pulse height of the strip signals. The complementary plot, showing the high voltage plateau at two different V_{th} settings, is shown in Fig. 4, demonstrating how full efficiency can be attained operating the chambers over a large high voltage range, even in the proportional regime.

The digital front-end electronics of the WIC calorimeter in the SLD detector comprises approximately 90,000 strip readout channels. A block diagram of the readout system is shown in Fig. 5. Eight channels of preamplifiers, discriminators, one-shots and shift-registers are packaged in a single hybrid; four hybrids are packaged in 32-channel boards, and all the boards of each layer of the detector (typically 10 boards/layer) are daisy-chained together. Subsequently groups of approximately 3000 channels are further multiplexed in the splitter boards, and up to eight splitter boards are read by each WICDRM.

Mass production and testing of the boards (one of which is portrayed in Fig. 6) is now completed, and the front-end electronics is being installed on the detector.

The Splitter Board

The front-end boards of the chamber planes belonging to the same sub-sub-system, such as half an octant of the barrel (coffin") or a section of the endcaps, are grouped and powered, controlled and read by a splitter board. Each splitter board can handle up to ten planes. A block diagram is shown in Fig. 7. Through the daisy chains the Splitter Boards provide the front-end boards with regulated power and threshold voltages; upon

the occurrence of a trigger, they provide the load signal, latching the one-shot outputs onto the shift register chain. During the readout they distribute the shift register clock and a test pattern, generated by the Fastbus readout module which transfers to the module the appropriate shift register data from the front-end boards.

To allow for the maximum flexibility in detector operation, each front-end daisy chain has an individual discriminator threshold set by a 12-bit DAC. The DAC outputs in the 0 40 V range undergo a 100 times reduction in a passive network on the boards themselves to improve the signal-to-noise ratio while still transmitting the V_{th} along the daisy chains, together with TTL signals. If one also takes into account the 50 times amplification on the board, one then has an effective V_{th} range of 100 μV to 8 mV, while typical values used are in the neighborhood of 2 mV.

The module also contains combinatory and majority logic circuits capable of forming a trigger signal from the Digor outputs of the individual planes serviced by the Splitter Board. The trigger logic has provisions for excluding and for requiring hits on individual planes, and for setting the minimum number of planes which must be hit for a trigger to be formed. In order to minimize the noise possibly induced by the Digor along the daisy chains, the voltage swing is kept at 500 mV and converted on the splitter board to TTL levels. The total delay between the arrival of a valid Digor combination and the output of a trigger signal is less than 50 nsec.

The timing for the splitter board operations is provided by a Timing and Control Module (TCM) [9], which is synchronized with the 119 MHz LINAC main frequency. Communications with the TCM use two identical sets of four lines, duplicated for reliability. A fiber optic translator board converts the f.o. signals from and to the TCM to differential TTL for up to eight splitter boards, each of which responds to a unique selection address and can therefore receive separate configuration information and operating commands. The splitter boards belonging to the same subgroup receive the shift register master clock and the shift register test pattern from the WICDRM through one fiber optic link whose output, converted to differential TTL, is then distributed. Each splitter board has two individual fiber optic links, one with the WICDRM, carrying the shift register data from the front-end boards, and one to the Cosmic Logic Unit carrying the splitter board trigger signal. A prototype splitter board is currently functioning on the detector, and production of the 42 needed for the WIC is expected to be complete by early autumn this year.

The Digital Readout Module

The design of the Fastbus readout module for the strip information—the WICDRM—was heavily influenced by the following requirements: minimization of the number of modules and connections needed for the whole detector; ability to perform the strip readout at twice the beam crossing rate, not only searching for e^+e^- annihilation data at the crossing itself but also examining cosmic ray events or even random noise in the inter-crossing time to monitor the front-end functionality; and last but not least, maximization of the amount of data processing done within the module itself, thus reducing the load on the other links in the data acquisition chain and the Fastbus traffic.

This brought to the construction of an "intelligent," albeit slave, Fastbus module, based on the powerful Motorola MC68020 microprocessor.

After the front-end one-shot information has been latched upon reception of a load signal into the daisy-chained shift-registers, the readout module proceeds to clock their contents, one long word at a time and at a 4 Mbit/sec rate, into eight parallel input buffers (see the block diagram of Fig. 8) under the full control of the microprocessor. Once the buffers have been filled, a flag signals the processor to latch the data and immediately start a new 32-bit cycle. While waiting for the completion of the shifting operation, the processor can either transfer to RAM the full extent of the data read or start the preliminary elaboration with a zero-suppression which may also include correcting for mismapped cabling of the front-end boards, clustering, data formatting and strip occupation histogramming. Furthermore, extensive testing of the front-end electronics is also possible, and the integrity of the daisy chains can be verified by injecting a preselected pattern at the far end and comparing it with the results of a readout cycle. Communication with the splitter boards goes through an I/O card mounted on the Fastbus auxiliary backplane, which can be customized to convert the particular transmission protocol chosen (optical links in the SLD experiment) to the TTL levels used within the module, thus allowing testing of the chains without requiring the installation of all the components of the system. The production and testing of the six WICDRM modules needed for the whole WIC is well under way and the first batch of two should substitute the prototype (see Fig. 9) which is currently operating on the detector by summer 1989.

The Cosmic Logic Unit

To fully benefit from the dual-readout capability of the WIC strip electronics by collecting cosmic ray events in parallel with the physics data taking, a CLU was designed to collate the splitter board trigger signals and form a versatile cosmic ray trigger. One of the goals was to be able to change the trigger configuration by simply downloading new trigger tables to the unit, possibly under the control of a Fastbus master module when the SLD detector is running in cosmic ray mode and the cosmic ray events undergo the fullest elaboration. Furthermore, logic was added to provide triggering information, in the form of inputs to a Fastbus latch, for the SLD Trigger Supervisor unit when running in physics mode.

The inputs to the CLU are the triggering signals from the 42 splitter boards; since in some cases the logical units forming the detector have been split among more than one splitter board, a first level of signal recombination is done in hardware on the fiber optic to TTL conversion board. A private bus carries the 32 signals thus obtained to the CLU proper. At this point, the barrel accounts for 16 coffin signals, two coffins radially juxtaposed forming an octant, while each endcap is subdivided into six sections, and four signals correspond to the 45-degree chambers. A set of PALs is used to build the pre-triggers, combining the coffins into octants, adding the two middle-plane signals of each endcap, summing the 45-degree signals for each side, and providing a barrel-top and a barrel-bottom sum of the three uppermost (lowermost) octants.

A first level of lookup tables, using two sets of 4Kx4 25-nsec access time RAMs, is

addressed by subgroups of 12 of the pre-triggers and outputs subgroups of four Level 1 triggers. Three of the four RAMs reserved for the cosmic ray trigger are currently used: the first and the second build "tight" and "loose" single and multiple barrel muon triggers; the third combines endcap and barrel-top, barrel-bottom information into similar outputs. At the current stage little thought has been given to the physics trigger outputs, but possibilities studied are a back-to-back muon signal, single penetrating track signals, and back-to-back tracks which only hit the inner coffins but do not exit the detector. One of the reasons for building as much flexibility as possible into the CLU is, of course, to ease the adaptation to the unknown environment of the SLD at the SLC.

Conclusions

The full data acquisition chain for the Muon Tracking System of the SLD is currently being installed and debugged with cosmic ray data. All the components respond well to the expectations, and the threshold plateaus obtained in a test environment (Fig. 4) have been reproduced systematically at the detector octant scale, using the whole readout chain from the front-end boards to the data-acquisition host, thereby demonstrating the functionality of the system. By autumn 1989, the whole WIC detector should be completely instrumented for the strip readout and operational as a muon identifier and tracker, ready for stand-alone cosmic ray data taking.

References

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[5] F. Beconcini *et al.*, Nucl. Instr. and Meth. **A277**, 222 (1989).

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[7] N. Bacchetta *et al.*, submitted to IEEE Trans. Nucl. Sci. (1989).

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[9] S. MacKenzie, "SLD LAC Timing Unit," SLD Internal Note.

Figures

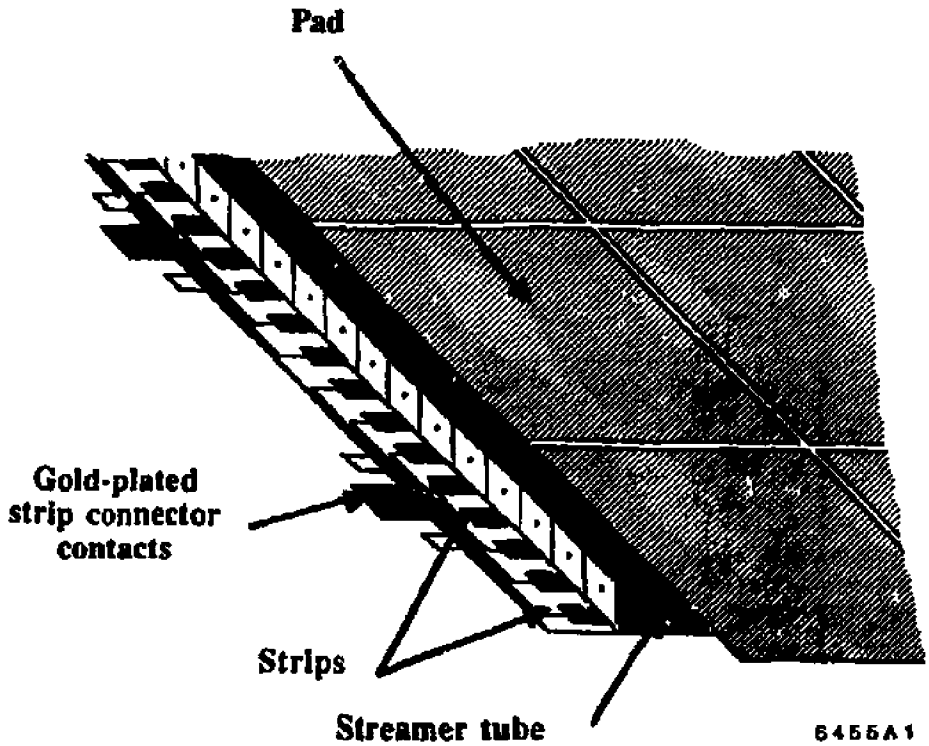
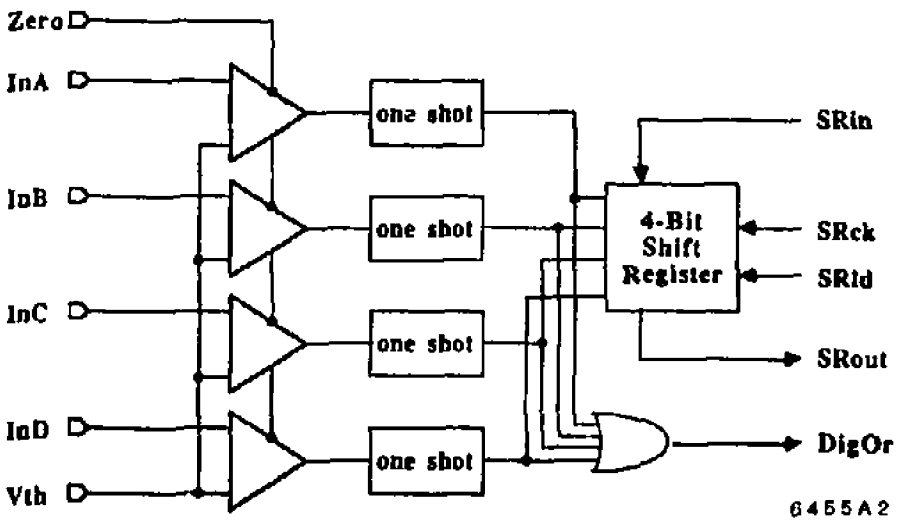

Pad
Gold-plated
strip connector
contacts
Strips
Streamer tube
6455A1

Fig. 1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InA
InB
InC
InD
Vth
one shot
one shot
one shot
one shot
4-Bit
Shift
Register
SRin
SRck
SRld
SRout
DigOr
6455A2

Fig. 2

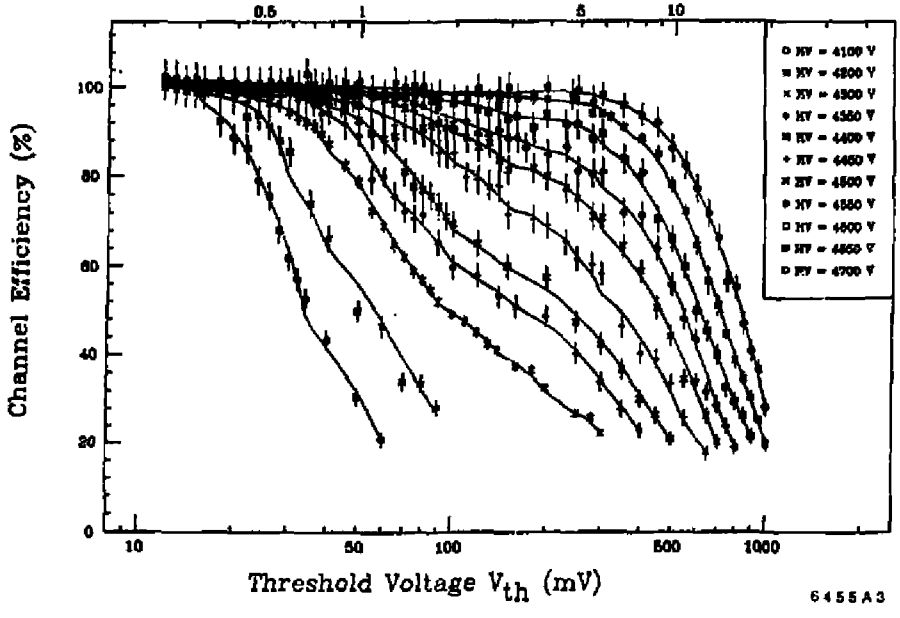
0.5
1
5
10
100
80
60
40
20
0
10
50
100
500
1000
Channel Efficiency (%)
Threshold Voltage V_{th} (mV)
6455A3

Fig 3

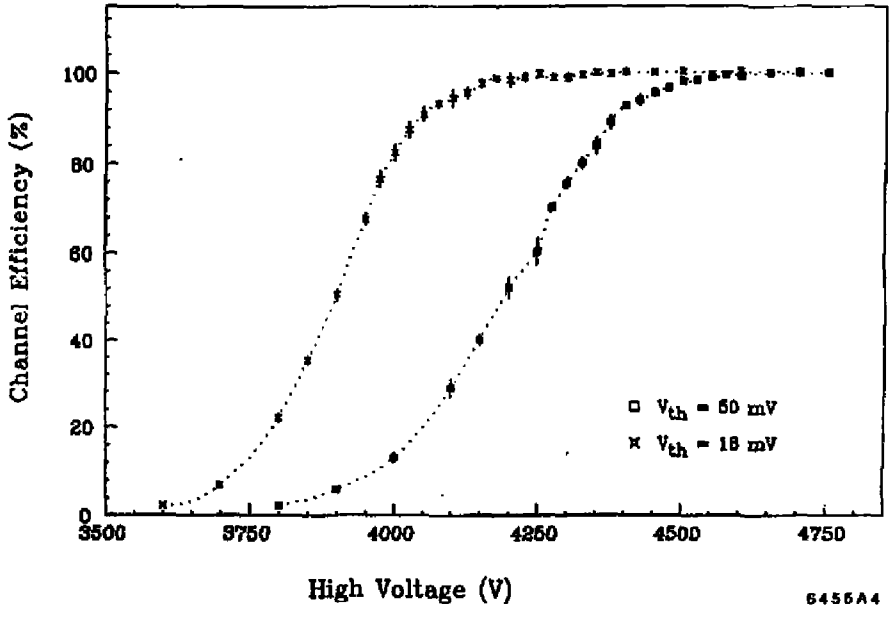
Channel Efficiency (%)
100
80
60
40
20
0
3500
3750
4000
4250
4500
4750
High Voltage (V)
V_{th} = 50 mV
V_{th} = 18 mV
6456A4

Fig. 4

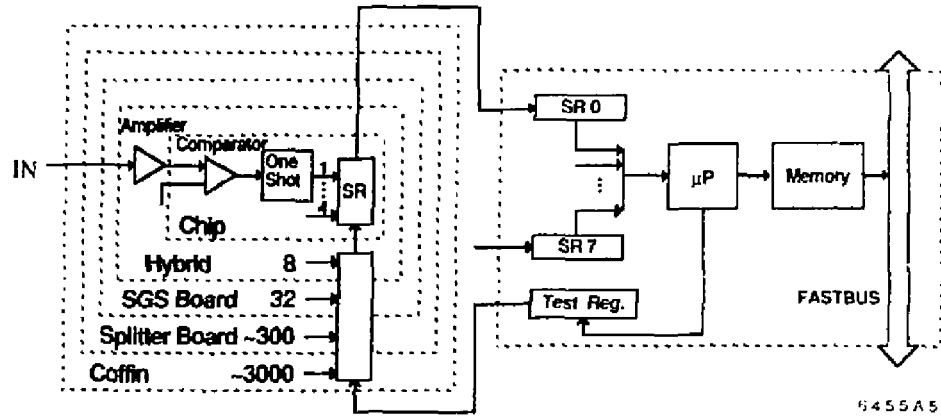
IN
Amplifier
Comparator
One Shot
SR
Chip
Hybrid 8
SGS Board 32
Splitter Board ~300
Coffin ~3000
SR 0
SR 7
Test Reg.
µP
Memory
FASTBUS
6455A5

Fig. 5

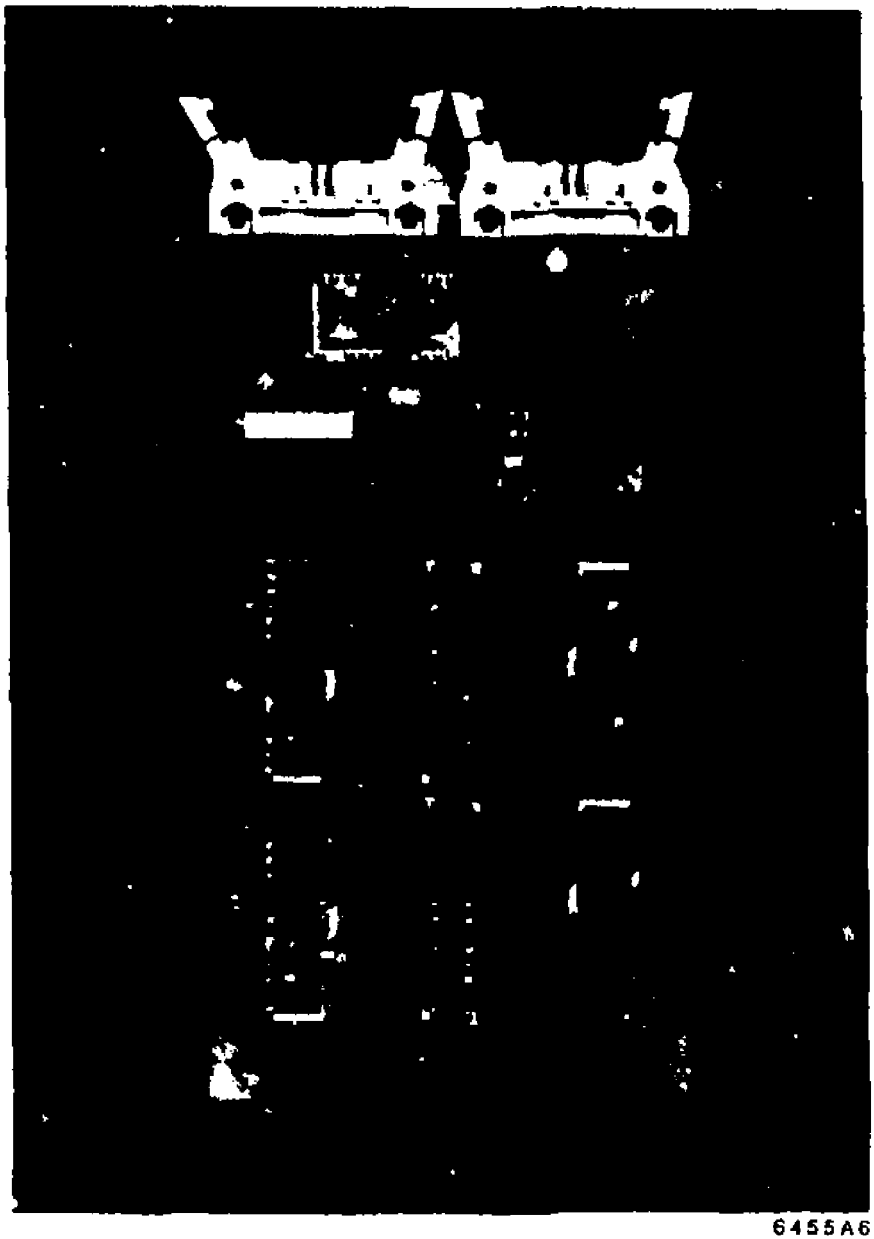

Fig. 6

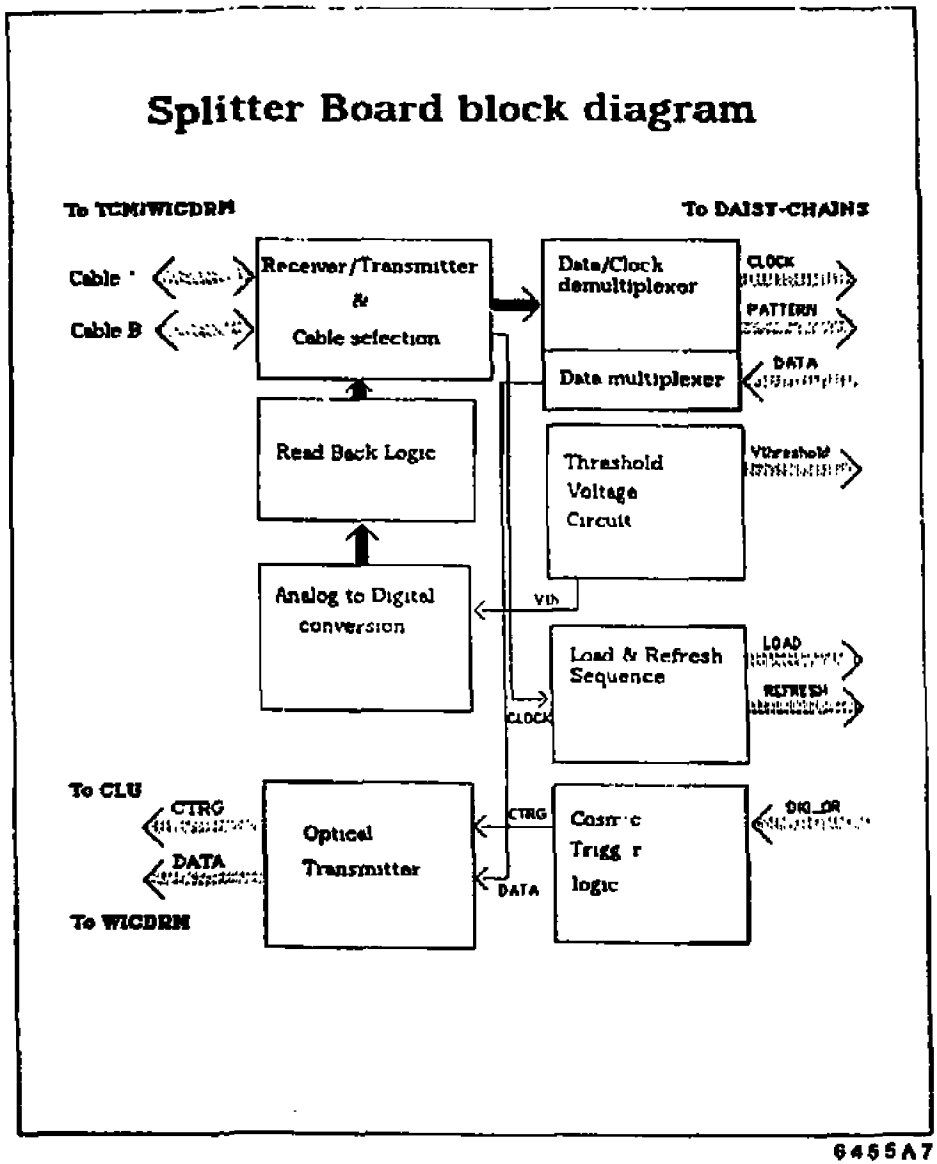
Splitter Board block diagram
To TCM/WICDRM
To DAISY-CHAINS
Cable A
Cable B
Receiver/Transmitter
&
Cable selection
Data/Clock
demultiplexer
CLOCK
PATTERN
Data multiplexer
DATA
Read Back Logic
Threshold
Voltage
Circuit
Analog to Digital
conversion
Vth
Load & Refresh
Sequence
LOAD
CLOCK
To CLU
CTRG
DATA
To WICDRM
Optical
Transmitter
CTRG
DATA
Cosmic
Trigger
logic
6455A7

Fig. 7

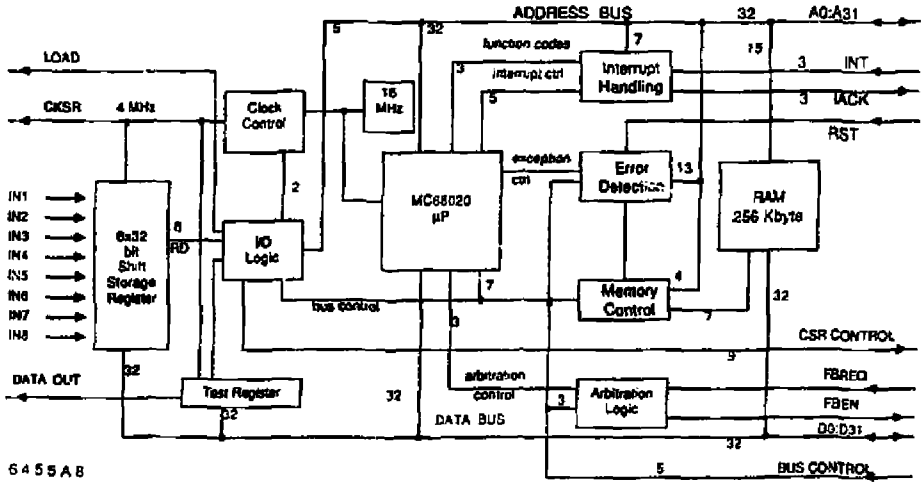
ADDRESS BUS
32
A0:A31
LOAD
CKSR
4 MHz
Clock Control
16 MHz
function codes
interrupt ctrl
Interrupt Handling
INT
IACK
RST
MC68020 µP
exception cntl
Error Detection
RAM 256 Kbyte
IN1
IN2
IN3
IN4
IN5
IN6
IN7
IN8
8x32 bit Shift Storage Register
RD
I/O Logic
bus control
Memory Control
CSR CONTROL
DATA OUT
Test Register
arbitration control
DATA BUS
Arbitration Logic
FBREQ
FBEN
D0:D31
BUS CONTROL
6455AB

Fig. 8

Fig. 9