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INVESTIGATION OF THE IMPURITY TOLERANCE OF SEMICRYSTALLINE
SILICON SOLAR CELLS SILICON IMPACT PROGRAM

Quarterly Technical Progress Report No. 2, January 1—March 31, 1980

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QUARTERLY TECHNICAL PROGRESS REPORT NO. 2

JANUARY 1, 1980 - MARCH 31, 1980

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Sponsored by the Solar Energy Research Institute
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ABSTRACT

Design modifications were made to incorporate thermocouples into the polysilicon casting furnace to allow for the constant monitoring of the temperature profile during the casting process. A source of metallurgical grade (MG) silicon was chosen and the material was prepared by grinding the large pieces into powder using anvils made from semiconductor grade (SG) silicon. The uniformity of the feedstock was ascertained by optical emission spectrograph analysis of three random samples of the feedstock. A total of sixteen casting runs were made this quarter; Union Carbide CMG graphite was found to be the most suitable crucible material. Solar cells were fabricated from the successful castings (five 100% SG, and two containing 1% and 5% MG silicon respectively). The average efficiency from the first SG ingot was 10.4% AM0 (in excess of 12% AM1). In general, solar cells fabricated from the top and bottom of the ingots exhibited better overall characteristics. The addition of MG silicon to the casting caused a large degradation in both light and dark I-V characteristics. The dark current tended to be dominated almost entirely by the space-charge component in these castings. A new method was developed which eliminates temperature scanning in DLTS measurements by incorporating a spectrum analyzer into the system; results are in good agreement with published data. Efforts were directed toward decreasing the

spot size of the scanning photoresponse system from 60 μm to 5 μm . Successful scans were made on a single crystal cell having a large shunt resistance. Electron channelling patterns were obtained for all crystallographic directions in polysilicon material and were assembled into a composite [001]-[011]-[111] standard triangle; further measurement results are presented. Preliminary x-ray topographs were obtained for grains 1 and 2 in solar cell 1-1 using the asymmetrical crystal topography technique; results are discussed.

DESCRIPTION OF PROJECT

This program is designed to provide a scientific basis for understanding the relationship between the key parameters for the formation of cast polycrystalline silicon material, utilizing a mixture of metallurgical and semiconductor grade silicon as feedstock, and the resulting photovoltaic material characteristics. The effects of casting polysilicon over a range of thermal conditions and a range of feedstock impurity levels will be determined by the analysis of both the material itself and the characteristics of solar cells fabricated with the cast polysilicon material.

TABLE OF CONTENTS

Abstract	i
Description of Project	iii
Table of Contents	iv
List of Figures	v
List of Tables	vi
 I. INTRODUCTION	 1
 II. EXPERIMENTAL CASTING	 3
A. Experimental Assembly and Calibration	3
B. Impure Silicon Starting Material	9
C. Experimental Casting	12
 III. EXPERIMENTAL SOLAR CELLS - DATA AND ANALYSIS	 17
A. Solar Cell Fabrication	17
B. Measurement Data and Analysis	18
 IV. THEORETICAL AND EXPERIMENTAL INVESTIGATIONS OF GRAIN AND GRAIN BOUNDARY EFFECTS	 34
A. Deep Level Transient Spectroscopy	34
B. Photoresponse Scanning System	37
C. Electron Channelling	38
D. X-Ray Topography	41
 V. CONCLUSIONS	 47
 References	 51
Appendix A. Solar Cell Process Sequence	53
Appendix B. Lot Data Summary of Solar Cells Fabricated From Ingots 10, 15, 16, 17, 19, 20 and 21	62

LIST OF FIGURES

- Figure 1. Feedthrough System Schematic
- Figure 2. Schematic Diagram of the Inside of the Casting Furnace
- Figure 3. Thermal Profile Inside Casting Furnace
- Figure 4. Wafer Location Within Cast Ingot
- Figure 5. Block Diagram of DLTS System With A Spectrum Analyzer
- Figure 6. Electron Channelling Pattern of Silicon
- Figure 7. Enlargement of the Calculated Electron Channelling Map Shown in Figure 6
- Figure 8. Optical Micrograph of Wafer Containing Sinuous Grain Boundaries
- Figure 9. Electron Channelling Determination of Polysilicon Crystal Surface Normals in a Transverse Section Exhibiting Sinuous Grain Boundaries
- Figure 10. Individual Grain Reflections Obtained by the Asymmetric Crystal Topography (ACT) Method Applied to Grains 1 and 2 in Cell 2-2
- Figure 11. ($35\bar{1}$) X-Ray Reflection Topograph Showing a Portion of Grain 1 in Cell 1-1

LIST OF TABLES

- Table 1. Optical Emission Spectrograph Analysis of Ground Metallurgical Grade Silicon
- Table 2. Summary of Crystal Growth Efforts
- Table 3. Light I-V Summary of Solar Cells Fabricated From Ingots 10, 15, 16, 17, 19, 20 and 21
- Table 4. Dark I-V Summary of Solar Cells Fabricated From Ingots 10, 15, 16, 17, 19, 20 and 21
- Table 5. Further Measurement Data for Solar Cells Fabricated From Ingots 10, 15, 16, 17, 19, 20 and 21

I. INTRODUCTION

This report summarizes the progress achieved during the second quarter of a program designed to provide a basis for understanding the relationship between the growth of cast polysilicon ingots, using a mixture of metallurgical grade and semiconductor grade silicon feedstock, and the resulting photovoltaic material characteristics. Additionally, this program continues the effort begun under "Photovoltaic Mechanisms in Polycrystalline Thin Film Solar Cells" originally sponsored under DOE contract ET-78-D-01-3413 which is a detailed analysis of the mechanisms in polysilicon which limit the photovoltaic conversion efficiency under solar illumination conditions.

Section II summarizes the experimental casting work including the assembly and calibration of the casting station, the preparation and characterization of the impure metallurgical grade silicon feedstock, and the actual casting runs performed during the last quarter. Section III details the characterization of solar cells fabricated from the cast polysilicon ingots including solar cell fabrication, a description of the measurements and analysis performed and the data and analysis. Section IV summarizes the photovoltaic mechanisms effect on theoretical and experimental investigations of grain and grain boundary effects including the progress

achieved on Deep Level Transient Spectroscopy, the photo-response scanning system, electron channelling, and x-ray topography. Section V presents the conclusions and Appendix A is a summary, including statistics, of the data on all solar cells processed to date including the light I-V characteristics, series resistance, shunt resistance, conductance, capacitance, and resistivity.

II. EXPERIMENTAL CASTING

A. Experimental Assembly and Calibration

A Veeco resistance heated Czochralski crystal growing furnace has been modified to allow for the in-situ casting of polycrystalline ingots. The casting technique employed during the course of this investigation is based upon the Bridgeman method of crystal growth. In this method, the crucible is lowered out of the furnace hot zone in such a manner that the solidification front travels normal to the axis of the crucible. This produces a well defined directional solidification within the ingot.

During the first quarter, the design modification consisted of redesigning the heating assembly to allow enough room beneath the heater to drop the crucible completely out of the hot zone. The design modifications were carried out and the new assembly constructed. The furnace has been in operation for three and a half months with only minor modifications to the heat shields and baffles being necessary.

During this quarter further design modifications have been necessary so that thermocouples could be introduced into various locations within the furnace. It is desirable

to have several thermocouples placed at regular intervals along the length of the furnace in order to probe the hot zone and continually monitor temperature changes. As originally designed, the crystal puller did not have any provisions for thermocouple inputs. Thus, it became necessary to design a vacuum tight electrical feedthrough system that could be adapted to this machine.

The crystal growing chamber is constructed in three main segments: a water cooled dome, jacket, and baseplate all of double walled construction. This restricts access into the body of the crystal puller to a small viewport originally intended to mount a constant diameter control mechanism. This put severe design limitations on the physical dimensions of the feedthrough system. The method finally devised is shown in Figure 1. With this arrangement up to ten different thermocouples can be incorporated into the chamber simultaneously. This allows for the constant monitoring of the temperature profile along the entire furnace length during the casting process.

Figure 2 is a schematic representation of the inside of the furnace showing the thermocouple placement as well as the relative locations of the major system components. Three Platinum-6% Rhodium versus Platinum-30% Rhodium

FIGURE 1. SCHEMATIC REPRESENTATION OF THERMOCOUPLE ELECTRICAL FEED-THROUGH ASSEMBLY

Figure 2. Schematic Diagram of the Inside of the Casting Furnace

(type B) thermocouples have been employed to monitor the temperature within the furnace hot zone and provision has been made for attaching a fourth type B thermocouple to the bottom of the crucible. This will allow for a direct probing of the thermal environment seen by the crucible as it is lowered out of the hot zone. The type B thermocouples were chosen since they do not require any temperature compensation at the cold junction and uncompensated copper wire can be used for lead in wire. In order to complete the temperature profile, three Chromel versus Alumel (type K) thermocouples have been employed in the lower region of the furnace owing to their greater sensitivity at lower temperatures. An Esterline-Angus dual channel multipoint chart recorder is being used to simultaneously record all inputs.

In addition to all the thermocouple inputs that are used to characterize the thermal environment of the system, an Ircon temperature sensing system is used in a feedback loop to control the power to the heating elements. This system maintains a constant temperature within the furnace to $\pm 2^{\circ}\text{C}$ at 1400°C .

Figure 3 is a plot of the temperature profile found within the casting furnace. It can be seen that the hot

Figure 3. Thermal Profile Inside Casting Furnace

zone is fairly uniform and that there is a rather steep thermal gradient below the furnace. This sharp thermal break produces an almost planar solidification front throughout the ingot.

B. Impure Silicon Starting Material

Samples of metallurgical grade silicon were ordered and obtained from Ohio-Ferro Alloy Corporation, Hanna Mining Company, and Union Carbide Corporation (Metals Division). These samples were evaluated for suitability as a source of metallurgical grade silicon for the experimental casting runs. The silicon from Ohio-Ferro Alloys Corporation was found to be the most suitable for the task, since out of the samples received it contained the least amount of iron.

Metallurgical grade silicon is very inhomogeneous, owing to the way in which it is manufactured. Thus, to ensure uniformity throughout the course of this investigation it will be necessary to prepare the impure silicon feedstock for the entire program at one time. The method chosen consists of simply pulverizing and mechanically mixing the material. In order to minimize extraneous contamination, the impure silicon chunks, which are about four centimeters in diameter, have been ground against

anvils made from semiconductor grade silicon. The powder has been graded using a one millimeter mesh sieve. Approximately eight kilograms of this material has been produced.

In order to ascertain the uniformity of the impurity distribution and the impurity content of this feedstock, three random samples of approximately 5 grams each were sent to National Spectrographic Laboratories, Inc. for analysis. Table 1 shows results that were obtained from this analysis. These results are in fair agreement with the typical impurity levels found in metallurgical grade silicon which were quoted in the 1st Quarterly Report.¹ It can be seen that the results of the three tests are fairly uniform, thus, it is felt that a uniform feedstock has been prepared.

ELEMENT	SAMPLE 1	SAMPLE 2	SAMPLE 3
B	0.0075	0.0060	0.0065
Al	0.32	0.27	0.30
Sb	<0.01	<0.01	<0.01
Bi	<0.001	<0.001	<0.001
Co	0.003	0.003	0.003
Be	<0.001	<0.001	<0.001
Cr	0.007	0.007	0.007
Cu	0.015	0.015	0.015
Fe	0.38	0.36	0.35
Pb	<0.001	<0.001	<0.001
Mg	0.001	0.001	0.001
Mn	0.008	0.008	0.008
Mo	0.003	0.003	0.003
Ni	0.024	0.025	0.025
Ag	<0.001	<0.001	<0.001
Sn	<0.001	<0.001	<0.001
V	0.041	0.044	0.041
Zn	<0.01	<0.01	<0.01
Zr	0.003	0.003	0.003
Ti	0.039	0.047	0.040
Cd	<0.01	<0.01	<0.01
Ca	0.039	0.050	0.043
C	0.010	0.010	0.011
P	0.003	0.003	0.003
Ta	<0.05	<0.05	<0.05

Table 1. Optical Emission Spectrograph Analysis of Ground Metallurgical Grade Silicon

(All numbers given are in weight percent.)

C. Experimental Casting

As stated above, the casting will take place using in-situ directional solidification based upon the Bridgeman technique of crystal growth. In this technique, silicon will be melted in a resistance furnace, then cooled from the bottom. This will set up a vertical thermal gradient within the ingot. The solidification front will then move from the bottom to the top of the melt as the ingot is lowered from the furnace. The furnace has been designed to accommodate crucibles approximately six inches high and three inches in diameter. Argon is used as the ambient gas in order to protect the graphite heating elements and minimize contamination of the melt.

During the last quarter experimental casting had begun using fused quartz as a crucible material. Even though melt contamination can be held to a minimum using this material, it is totally unsatisfactory in this type of operation. Silicon is able to plastically deform down to about 650°C, and below this point, the stresses induced by the difference between the coefficient of thermal expansion of the quartz and the silicon is sufficient to fracture the silicon ingot.

Ciszek has been successful in employing Union Carbide's CMB graphite as a crucible material using an approach similar to the methods adapted in this study.² CMB graphite is a relatively dense graphite, 1.76 gm/cm^3 , having a maximum grain size of $76 \text{ }\mu\text{m}$. The coefficient of linear thermal expansion of this material closely matches that of silicon in the range of $20\text{-}600^\circ\text{C}$.

Experimentation using CMB graphite as a crucible material began in February. The crucibles were rectangular in cross section, 2×2.5 inches, with a $1/4$ inch wall. The silicon could be melted easily within these containers, with a minimal amount being absorbed into the graphite. After casting, the ingot could be removed from the furnace intact. However, the first several ingots developed cracks during wafering. It is unclear whether these cracks were present in the samples after casting or developed during the wafering operation. In an effort to minimize internal strains, the crucible wall thickness was lowered to an $1/8$ of an inch. This improved the situation and starting with run 16 sheet material has been produced on a fairly regular basis. The experimental castings made to date are summarized in Table 2.

RUN #	DATE	SILICON COMPOSITION	LOWERING RATE (CM/HR)	CRUCIBLE COMPOSITION	GRAIN SIZE (CRYSTALS/CM ²)			REMARKS
					TOP	MID	BOT	
1	12-14-79	100% SG		Quartz				System failure
2	12-18-79	100% SG		Quartz				Crucible failure
3	12-19-79	100% SG	2	Quartz				Ingot shattered upon cooling
4	12-21-79	100% SG	2	Quartz				Ingot shattered upon cooling
5	12-27-79	100% SG		Quartz				System Failure
6	12-29-79	100% SG	1.33	Quartz				Ingot shattered upon cooling
7	01-07-80	100% SG		Quartz				Crucible failure
8	01-09-80	100% SG	1	Quartz				Ingot shattered upon cooling
9	01-22-80	100% SG	2	CMB				Ingot cracked
10	02-02-80	100% SG	2.5	CMB		22		Small cracks in ingot-wafered
11	02-08-80	100% SG	10	CMB				Ingot cracked
12	02-12-80	100% SG		CMB				Crucible failure
13	02-18-80	100% SG	5	Quartz				Ingot shattered upon cooling
14	02-22-80	100% SG		CMB				Crucible failure
15	02-25-80	100% SG	1	CMB				Small cracks in ingot-wafered
16	02-28-80	100% SG	1	CMB				Sheet material produced
17	03-04-80	100% SG	1	CMB	18	27	53	Sheet material produced
18	03-13-80	100% SG		CMB				Crucible failure
19	03-14-80	100% SG	1	CMB	15	15	29	Sheet material produced
20	03-18-80	1% MG	1	CMB	21	32	40	Sheet material produced
21	03-20-80	5% MG	1	CMB	17	24	30	Sheet material produced
22	03-27-80	10% MG	1	CMB				System failure

Table 2. Summary of Crystal Growth Efforts

An average of six wafers are obtained from the top, middle, and bottom of each cast ingot using a Hamco ID saw. Figure 4 is a schematic representation of the ingot indicating the approximate wafer location. About half of these wafers are then processed into solar cells and the remainder are used for other physical studies. The wafers are coded so that their orientation can be readily identified.

Runs 16 through 19 used pure semiconductor grade silicon in order to establish a base line process. The crucible was lowered out of the furnace hot zone at a rate of 1 cm/hr. The crystal grain size varied from 24 mm^2 at the bottom to 59 mm^2 at the top. The smaller grain size at the bottom is probably due to the plethora of nucleating sites that the rough texture of the graphite presents. The last three runs made during this quarter incorporated 1, 5, and 10%, respectively, metallurgical grade silicon. The growth conditions remained the same for these runs.

Figure 4. Wafer Location Within Cast Ingot

III. EXPERIMENTAL SOLAR CELLS - DATA AND ANALYSIS

A. Solar Cell Fabrication

Solar cells (2 cm x 2 cm) have been processed from the cast polysilicon ingots together with single crystal control cells using a standard Solarex process. The standard Solarex process has been reproduced in Appendix A from the JPL sponsored program entitled "Analysis of the Effects of Impurities in Silicon".³ Strict decontamination procedures were incorporated to assure that the various lots do not cross-contaminate each other. This was substantiated by the fact that the single crystal control cells have exhibited average AM0 cell efficiencies of nearly 13% at 25°C. Identification numbers were scribed on the test wafers (polysilicon) prior to processing to distinguish wafers taken from different positions within the ingots. The solar cells are identified by ingot number, Test (T) or Control (C), cell number, and location within the ingot: Top (T), Middle (M), or Bottom (B). An example identification number is shown below:

B. Measurement Data and Analysis

Light I-V Characteristics

The light I-V characteristics of all test and control cells from ingots 10, 15, 16, 17, 19, 20, and 21 are summarized in Table 3. The tabulated values are divided into averages for the control cells and the test cells (top, middle, and bottom of the ingot). The I-V measurements were taken at AM0 conditions at 25°C (standardized using a flight calibrated cell from NASA/Lewis). The blue and red short-circuit currents were measured using Corning Filters #9788 and #2408 respectively. The results of the individual ingots are discussed below:

Ingot #10 (100% SG) - This was the first test lot to be processed and the average AM0 maximum power of the test lot was 56.4 mW (AM0 10.4% efficient) which exceeds 12% AM1 in efficiency. Thus a milestone which required that the baseline casting experiments using 100% SG silicon shall demonstrate greater than 10% AM1 efficiency was exceeded. The best cell in the lot was 60.0 mW (AM0 11.1% efficient) which is nearly 13% AM1. The cells exhibited very good AM0 short-circuit current (140 mA maximum) and good red and blue current response, but they are still significantly below the single crystal values.

	AMO P _{MAX} (mW)	I _{SC} (mA)	V _{OC} (mV)	I _{SC} BLUE (mA)	I _{SC} RED (mA)	F.F.	R _{SHUNT} (Ω) MEDIAN	SILICON COMPOSITION
LOT #10								
CONTROL	69.5	147	612	39.1	79.5	.770	621	
TOP								100% SG
MIDDLE	56.4	138	563	37.9	72.9	.722	824	
BOTTOM								
LOT #15								
CONTROL	66.5	152	585	38.9	82.1	.748	1,950	
TOP	57.4	138	549	34.3	75.4	.762	2,890	100% SG
MIDDLE	56.2	132	558	33.6	71.3	.762	813	
BOTTOM	53.2	132	550	34.7	70.4	.735	2,490	
LOT #16								
CONTROL	68.6	152	592	40.9	81.7	.760	1,660	
TOP								100% SG
MIDDLE	52.0	132	552	38.3	67.3	.710	1,080	
BOTTOM								
LOT #17								
CONTROL	SAME AS LOT #15							
TOP	57.3	137	576	36.8	72.9	.726	206	
MIDDLE	53.2	139	556	39.2	71.9	.692	260	100% SG
BOTTOM	41.3	128	538	37.4	64.8	.600	14	

Table 3. Light I-V Summary of Solar Cells Fabricated From Ingots 10, 15, 16, 17, 19, 20 and 21

	AMO P _{MAX} (mW)	I _{SC} (mA)	V _{OC} (mV)	I _{SC} BLUE (mA)	I _{SC} RED (mA)	F.F.	R _{SHUNT} (Ω) MEDIAN	SILICON COMPOSITION
LOT #19 CONTROL TOP MIDDLE BOTTOM	SAME AS 50.8 48.2	LOT #15 140 127	534 547	35.2 33.6	75.2 66.2	.680 .694	405 415	100% SG
LOT #20 CONTROL TOP MIDDLE BOTTOM	71.8 37.5 42.8 17.2	153 111 124 111	594 535 552 335	41.3 38.7 38.9 38.1	82.1 50.4 59.9 49.8	.790 .626 .615 .457	2,150 503 89 54	1% MG
LOT #21 CONTROL TOP MIDDLE BOTTOM	SAME AS 18.1 15.5 8.9	LOT #15 100 99.7 63.7	409 354 287	37.1 37.4 30.7	42.4 41.8 18.7	.423 .438 .557	21 48 27	5% MG

Table 3. Light I-V Summary of Solar Cells Fabricated from Ingots 10, 15, 16, 17, 19, 20 and 21 (continued)

Ingot #15 (100% SG) - Wafers were processed from the top, middle and bottom of the ingot. Cells from the top of the ingot had very good AM0 I_{SC} (138 mA) while middle and bottom cells had less I_{SC} (132 mA). Blue response was fairly uniform and red response showed degradation from top to bottom.

Ingot #16 (100% SG) - Wafers were processed from the middle of the ingot only. Short-circuit response was the same as the middle cells from ingot #15; however, the red response was lower (67.3 mA).

Ingot #17 (100% SG) - Wafers were processed from the top, middle and bottom of the ingot. Short-circuit current was highest in middle (139 mA) and lowest at the bottom (128 mA), while maximum power decreased from top to bottom of the ingot. Much of the loss in fill factor and maximum power is due to low shunt resistances.

Ingot #19 (100% SG) - Wafers were processed from the middle and bottom of the ingot. Cells from the top had good I_{SC} (140 mA) while the bottom showed a degradation in current (127 mA). Again, there was a loss in fill factor and maximum power due to ohmic shunting.

Ingot #20 (1% MG) - Wafers were processed from the top, middle and bottom of the ingot. There is a large overall decrease in short-circuit current when the MG silicon is added as compared

to the pure SG silicon ingots. The middle cells showed the best I_{SC} (124 mA) while the top and bottom had the same lower average current of 111 mA. The middle cells had the highest maximum power; the top cells were next and the bottom cells were the lowest. The middle and bottom cells exhibited very low shunt resistances.

Ingot #21 (5% MG) - Wafers were processed from the top, middle and bottom of the ingot. The top and middle cells had about equal I_{SC} averages of 100 mA while the bottom had a greatly reduced value of 63.7 mA. Maximum power degraded from top to bottom of the ingot and the overall maximum power of this lot was the lowest processed so far. Finally, all cells exhibited very low shunt resistances.

Dark I-V Characteristics

The dark I-V characteristics of select test and control cells are given in Table 4. One representative cell was chosen from the top, the middle, and the bottom of each processed ingot together with one control cell and a detailed dark I-V analysis was performed. To eliminate the effect of series resistance the dark I-V curves were derived by measuring $I_{SC}-V_{OC}$; shunt resistance was eliminated by subtracting the reverse current from the forward current when plotting the dark I-V. The total dark I-V curve was then generated by combining the $I_{SC}-V_{OC}$ curve with the modified forward

	CELL #	AMO EFFICIENCY (%)	V _{OC} (mV)	V _{MP} (mV)	I _{SCO} (mA)	I _{QNO} (mA)	N _{SC}	V _E (mV)	F.F.	BASE RESISTIVITY AVG (Ω -CM)
LOT #10	CONTROL	12.8	613	522	2.32×10^{-2}	6.10×10^{-9}	3.32	554	.763	.60 - .63
	TOP									
	MIDDLE	11.1	566	470	1.15×10^{-2}	3.37×10^{-8}	2.80	492	.759	1.5 - 2.0
LOT #15	CONTROL	12.8	591	496	3.76×10^{-2}	1.50×10^{-8}	3.56	526	.776	2.1 - 2.2
	TOP	10.6	551	448	2.96×10^{-3}	6.74×10^{-8}	2.28	495	.759	6.1 - 9.3
	MIDDLE	10.3	557	453	5.73×10^{-3}	5.33×10^{-8}	2.50	500	.764	3.4 - 4.2
LOT #16	CONTROL	13.3	593	500	3.07×10^{-2}	1.32×10^{-8}	3.92	502	.790	2.1 - 2.2
	TOP									
	MIDDLE	10.9	562	471	5.14×10^{-3}	5.37×10^{-8}	2.67	472	.773	2.1 - 2.2
LOT #17	CONTROL	SEE LOT #15								
	TOP	10.6	577	478	6.75×10^{-2}	1.85×10^{-8}	3.37	552	.731	1.2 - 1.7
	MIDDLE	10.3	539	429	2.31×10^{-3}	1.29×10^{-7}	2.21	468	.724	1.3 - 1.9
LOT #19	CONTROL	7.6	538	403	3.28×10^{-1}	-	3.44	-	.600	1.3 - 1.8
	TOP									
	MIDDLE									

Table 4. Dark I-V Summary of Solar Cells Fabricated From Ingots 10, 15, 16, 17, 19, 20 and 21

	CELL #	AMO EFFICIENCY (%)	V _{OC} (mV)	V _{MP} (mV)	I _{SCO} (mA)	I _{QNO} (mA)	N _{SC}	V _E (mV)	F.F.	BASE RESISTIVITY AVG (Ω-CM)
LOT #19										
CONTROL	15-C4	SEE LOT #15								
TOP										
MIDDLE	19-TM2	9.0	530	421	6.0×10^{-3}	1.61×10^{-7}	2.35	472	.656	>20
BOTTOM	19-TB3	8.9	547	444	1.26×10^{-1}	4.32×10^{-8}	3.34	546	.694	5.5
LOT #20										
CONTROL	20-C8	13.6	597	496	1.57×10^{-3}	1.32×10^{-8}	2.60	491	.800	2.1
TOP	20-T2T	7.9	559	427	1.25×10^{-1}	2.20×10^{-8}	3.56	552	.685	.6
MIDDLE	20-T7M	9.9	577	478	1.77×10^{-1}	1.08×10^{-8}	4.18	557	.739	.8 - .9
BOTTOM	20-T11B	3.3	344	231	2.16	-	3.36	-	.465	.9 - 1.3
LOT #21										
CONTROL	20-C8	SEE LOT #20								
TOP	21-T2T	3.8	476	289	5.62	-	5.96	-	.409	.2
MIDDLE	21-T11M	2.0	364	221	2.51	-	3.74	-	.422	.2 - .3
BOTTOM	21-T16B	1.1	324	229	2.19	-	2.25	-	.573	.3 - .4

Table 4. Dark I-V Summary of Solar Cells Fabricated From Ingots 10, 15, 16, 17, 19, 20 and 21 (continued)

current curve. The dark current, I_D , was separated into its two components-one originating from recombination in the space-charge region (I_{SCO} , N_{SC})-and the other from recombination in the quasi-neutral regions (I_{QNO}) using a previously described method.^{4,5,6} V_E is the voltage where the contribution from the two regions are equal. Additionally, Table 4 includes the AMO efficiency, V_{OC} , voltage at maximum power (V_{mp}), and the fill factor of the individual cells that were analyzed together with the average base resistivity (four-point probe) of each area within the ingot (top, middle, bottom). The base resistivity values of test cells that exceed about 2 ohm-cm may be inaccurate (i.e. too large) because of the effect of grain boundary barrier height which interferes with a four-point probe measurement. Currently capacitance-voltage measurements are being analyzed to determine the base doping concentration. The results of the individual ingots are discussed below:

Ingot #10 (100% SG) - The space-charge component is relatively low (half the control cell value). However the maximum power point of both the control and test cell (middle) is dominated by the space-charge region ($V_{mp} < V_E$), which lowers the fill factor, but the open circuit voltage is not. The high V_{OC} of the control cell is due to the large low base resistivity (.60-.63 Ω -cm).

Ingot #15 (100% SG) - Cells processed from ingot #15 show a definite trend between the top, middle and bottom: I_{SCO} , I_{QNO} ,

N_{SC} , and V_E all increase from top to bottom of the ingot. The maximum power points of all test and control cells are dominated by the space-charge region. However, cell efficiencies, although they also decrease from top to bottom, are very similar.

Ingot #16 (100% SG) - The space-charge component is relatively low and the maximum power point is almost equal to V_E ($V_{mp} \approx V_E$). The open-circuit voltage is dominated entirely by the quasi-neutral component. The dark characteristics of this cell closely resemble those of a single crystal cell (i.e. V_E occurs well below 400 mV).

Ingot #17 (100% SG) - The cell taken from the top of the ingot has its maximum power point totally dominated by the space-charge region which lowers the fill factor. The open-circuit voltage, however, is dominated by a low quasi-neutral component which yields a relatively good open-circuit voltage (577 mV). The middle cell is also dominated by the space-charge component at the maximum power point. However, that component is more than an order of magnitude lower than the cell taken from the top. The open-circuit voltage is dominated by a large quasi-neutral component which results in a low V_{OC} (539 mV). The bottom cell is totally dominated by the space-charge region resulting in a low fill factor, maximum power, and open-circuit voltage. In general, the dark characteristics degraded from top to bottom of the ingot.

Ingot #19 (100% SG) - The maximum power point of both the middle and bottom cells are dominated by the space-charge region. The open-circuit voltage, however, is lower in the middle cell (530 mV) due to a large quasi-neutral component while the bottom cell has a higher V_{OC} (547 mV) even though V_{OC} is still strongly affected by a larger space-charge component. Bulk resistivity varied considerably between middle ($>20 \Omega\text{-cm}$) and bottom ($\sim 5.5 \Omega\text{-cm}$) (and within each middle wafer) which helps to account for the differences in V_{OC} .

Ingot #20 (1% MG) - The maximum power points of cells taken from top, middle and bottom are all dominated completely by the space-charge component. The middle cell has the best characteristics (highest maximum power and V_{OC}) and the bottom cell has the worst. The bottom cell is totally dominated by the large space-charge component which results in a low V_{OC} (344 mV) and maximum power (17.2 mW).

Ingot #21 (5% MG) - The dark current of cells taken from the top, middle, and bottom are all totally dominated by the space-charge component. The general trend, going from top to bottom, is an increase in the space-charge component and a decrease in N_{SC} . This has the result of decreasing the open-circuit voltage and maximum power of the cells to a large extent.

Overall, cells fabricated from the top and middle sections of the ingots had the best dark characteristics. Cells fabricated from the bottom of ingots tended to be dominated by large space-charge components. Cells fabricated from the middle and top of the ingots showed this same tendency as the percentage of MG silicon increases. At present, the origin of the large space-charge component is unknown and under further investigation. Additionally, the structural characteristics of wafers from the top, middle, and bottom of ingots are being investigated in order to better determine the relationship between the structural and electrical characteristics.

Further Measurements

Table 5 is a summary of further measurements that were made on one typical test and control cell from each processed ingot in order to assure consistent processing and to provide additional information on the photovoltaic characteristics of the processed material. A brief description of the measurement and analysis techniques used to obtain the various parameters and their connection to the physical mechanisms in the solar cells is reproduced below from the JPL program entitled "Analysis of the Effects of Impurities in Silicon".³

Photon Absorption Efficiency - The photon absorption efficiency is the ratio of the total number of absorbed photons to the total number of incident photons in the wavelength band

	CELL #	I _{SC} (mA)	PHOTON ABSORPTION EFFICIENCY %	QUANTUM YIELD		CARRIERS COLLECTED PER ABSORBED PHOTON	R _{SERIES} (Ω) AVG	R _{SHUNT} (Ω) MEDIAN	JUNCTION CAPACITANCE (nF/cm ²) AVG
				λ MAX (MICRONS)	% QY AT λ MAX				
LOT #10									
CONTROL	10-C9	148	92	0.63	86	0.84	0.065	620	49.1
TEST	10-T8M	139	95	0.62	88	0.75	0.061	824	24.8
LOT #15									
CONTROL	15-C4	152	92	0.68	92	0.86	0.082	1,950	26.2
TEST	15-T3M	132	91	0.66	78	0.66	0.053	2,490	24.8
LOT #16									
CONTROL	16-C12	154	93	0.64	96	0.88	0.075	1,660	26.3
TEST	16-T7M	135	91	0.60	87	0.77	0.059	1,080	25.3
LOT #17									
CONTROL	SAME AS LOT #15								
TEST	17-T4T	136	90	0.66	80	0.71	0.12	206	34.1
LOT #19									
CONTROL	SAME AS LOT #15								
TEST	19-T2M	140	92	0.55	80	0.72	0.20	413	29.1
LOT #20									
CONTROL	20-C8	155	94	0.63	95	0.87	0.068	2,150	26.3
TEST	20-T2T	112	91	0.60	77	0.61	0.060	89.4	48.9
LOT #21									
CONTROL	SAME AS LOT #20								
TEST	21-T11M	102	94	0.54	43	0.30	0.072	27.3	81.4

Table 5. Further Measurement Data for Solar Cell Fabricated From Ingots 10, 15, 16, 17, 19, 20 and 21

0.40 - 1.0 μm . This value is used to check the quality of the anti-reflection coating applied to the cell. Consistency of this parameter assures that the optical coupling to the cells is the same.

The intensity of a reflected light beam is measured (versus wavelength) in an integrating sphere spectrophotometer with a Beckman DK-2 monochromator as the light source. The corrected reflectance represents the intensity ratio of the reflected beam to the incoming beam, thus normalizing for variations in the incoming light beam. Utilizing published data, the number of photons per unit area absorbed into the cell is computed for each 1.0 μm band width between 0.4 μm to 1.0 μm . The ratio of the number of photons absorbed to the number of incoming photons, integrated for the six band widths, is the absorption efficiency.

Quantum Yield - The quantum yield is the ratio of the number of carriers collected to the number of incident carriers as a function of wavelength. The quantum yield curve when corrected for surface reflectance (absorption efficiency) provides information on the minority carrier lifetime within the base region.

A light beam is passed through a monochromator and alternately impinges on a defined unit area on the test solar cell and on a calibrated Eppley thermopile. The measured cell current is converted into the number of carriers collected. The current in the calibrated thermopile is used to find the number of incident photons. This ratio represents the cells efficiency of converting photons into carriers and collecting these carriers. Taking these measurements as a function of wavelength results in a curve of quantum efficiency over the bandwidth of solar radiation. The wavelength at which the maximum quantum efficiency occurs and the percent efficiency at this point are listed in Table 3.

Carriers Collected Per Absorbed Photon - This is the ratio of the quantum yield to absorptivity summed over the wavelength band 0.40 - 1.0 μm . This ratio represents a modified quantum yield in that it is a measure of the collection efficiency of the photons that enter the silicon within a particular wavelength band.

Junction Capacitance - The junction capacitance is the capacitance across the depletion region of the pn junction. It is measured in the dark using an AC signal (1 kHz) with no DC voltage across the junction with a General Radio Type 1680 capacitance bridge. The junction capacitance is inversely related to the base resistivity.

Series Resistance, R_{series} - The series resistance is represented as a lumped resistance in series with the pn junction and includes components from contact resistance in both the front and back contacts, the resistance of bulk silicon and the sheet resistance of the diffused region. The series resistance is calculated by choosing points on the illuminated I-V curve at an arbitrary level set 30 mA below the I_{SC} of the AM0, red, and blue curve. The slope of the straight line fit to these points is the series resistance.

Shunt Resistance, R_{shunt} - The shunt resistance is a measure of the cell leakage current consisting of a lumped resistance in parallel with the pn junction. The shunt resistance may be caused by surface leakage along the edge of the cell, by diffusion down dislocations or along grain boundaries or by metallization paths across the junction. The shunt resistance is calculated from the ratio of the voltage to the current measured in reverse and in the dark at 100 mV bias.

Table 5 shows photon absorption efficiency to be pretty consistent between test and control cells and between the various lots. The quantum yield and the number of carriers collected per absorbed photon are good indicators of changes in bulk lifetime. This is particularly prevalent in the two castings containing MG silicon (lot #20, 21). The series resistances are typically low with the exception of lot #19. Shunt resistance, however, is extremely variable with different test lots. The origin of the low shunt resistances in some of the lots cannot be quantified at present. Finally, the junction capacitance is a good indicator of the base resistivity of the silicon.

IV. THEORETICAL AND EXPERIMENTAL INVESTIGATIONS OF GRAIN AND GRAIN BOUNDARY EFFECTS

A. Deep Level Transient Spectroscopy (H.C. Lin, C.D. Wang)

A new method was developed to measure the thermal emission rate of a trap in a semiconductor. The new method eliminates temperature scanning by incorporating a spectrum analyzer into the measurement system. A block diagram of the system is shown in Figure 5. The theory on which the measurements depend is based on the relation between the time constant of a pure exponential wave and the relative amplitudes of its Fourier components. The time constant is given by:

$$(1) \quad \tau_s = \frac{\tau}{2\pi} \sqrt{\frac{10^c - 1}{m^2 - 10^{cn^2}}}$$

$$\text{Where } c = \frac{X_n - X_m}{10},$$

τ is the period of the exponential wave, X_n and X_m are the amplitudes of the n th and m th harmonics in dB respectively.

A block diagram of the system is shown in Figure 5.

The DLTS system was calibrated using a gold-doped p^+n diode prepared by the National Bureau of Standards. The thermal emission rate from the gold-doped diode

Figure 5. Block Diagram of DLTS Systems With A Spectrum Analyzer

$e = e_n + e_p$ can be approximated by e_n because the electron emission rate, e_n , is about an order of magnitude higher than the hole emission rate for the gold acceptor and can be written as follows⁸:

$$(2) \quad e_n = CT^2 \exp[-(E_C - E_T)/kT] = \tau_s^{-1}$$

Thus the separation of the trap level from the edge of the conduction band, $E_C - E_T$, can be determined by measuring the electron emission rates as a function of temperature and using equations (1) and (2). Using this method, the mid-gap level E_T was found to be 0.53 eV below the edge of the conduction band in good agreement with the value of 0.55 eV reported by C. T. Sah.⁸

In order to now perform DLTS measurements on polysilicon material an array of MOS diodes is being fabricated on a polysilicon wafer that was previously investigated.⁷ The array consists of both 1 mm and 2 mm diameter diodes. The diode structure consists of back contact/p-type polysilicon/ $\sim 20 \text{ \AA SiO}_2/\text{Ti}$. At present the diodes are being fabricated.

B. Photoresponse Scanning System

During the last quarter efforts were directed toward scanning with a 5 μm diameter light spot. The system, capable of scanning with a 60 μm light spot, was previously described in an earlier report.⁷ Difficulty was encountered in measuring the short-circuit current generated by the 5 μm spot (10^{-10} ampere range) due to 60 cycle and static pickup at the input of the picoammeter (which is then amplified by the picoammeter). The inside of the light tight box containing the stepping tables was covered with a fine copper screen and then grounded and the design of the picoammeter was also modified slightly to eliminate AC pickup. These steps eliminated the majority of the noise in the signal.

Successful scans have been made of a single crystal solar cell having a shunt resistance greater than 30 k Ω . However, for solar cells with less shunt resistance the picoammeter is unstable and the zero level drifts with time. It is planned to fabricate test cells having planar (non-sawn) junctions in order to obtain favorable shunt resistances to allow accurate scanning with the 5 μm spot.

C. Electron Channelling (R.W. Armstrong, M.E. Taylor, P. Ames)

Electron channelling patterns have been obtained for all crystallographic directions in polysilicon material as shown for the composite $[001]$ - $[011]$ - $[111]$ standard triangle in Figure 6.⁹ The composite standard triangle appears to show excellent resolution of detail in comparison with experimental and calculated results.¹⁰ The current results were obtained from individual grain pieces broken from a longitudinally cut cast polysilicon wafer which was previously analyzed.⁷ The obtainment of fine details in the individual pictures seems to confirm the excellent quality of the cast material.

The composite channelling pattern is to be used in one way as a reference base for determining the orientations of individual grains, often of small size, say 1-2 mm in diameter, observed in longitudinal sections of castings to be separated by sinuous grain boundaries. In addition to determining the orientations of grains separated by the sinuous boundaries, any preference at all for the boundary positions themselves to run in particular directions for any length will also be determined. Preliminary experiments have shown that well-resolved channelling patterns are able to be obtained from the grains on either side of a sinuous boundary.

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P. Ames and M. E. Taylor

Figure 7. Enlargement of the Calculated Electron Channelling Map Shown in Figure 6

Figure 8 is a composite optical micrograph of a polysilicon wafer containing sinuous grain boundaries. Figure 9 shows the relative orientations of the numbered grains in Figure 8 displayed on the calculated map of the electron channelling unit triangle. The orientations were obtained by comparing the individual channelling patterns of each grain with the composite standard triangle. These preliminary results indicate that the range of grain orientations associated with the sinuous grain boundaries lie along the $[111]$ - $[100]$ zone axis and are as far from the $[110]$ direction as possible. This implies that the preferential crystal solidification direction is perpendicular to the $[110]$ direction in this region exhibiting sinuous boundaries.

D. X-Ray Topography (R. W. Armstrong, R. G. Rosemeier)

X-ray reflection topographs have been obtained for grains 1 and 2 in solar cell 1-1 using the asymmetrical crystal topography technique.¹¹ The scanning photoresponse measurements and other electrical characteristics of cell 1-1 were reported earlier.^{7,12} The polycrystal and x-ray geometry for obtaining topographs is shown in Figure 10. For this serial section, grains 1 and 2 are measured to have nearly coincident $[101]_1$ and $[1\bar{1}0]_2$ directions, in agreement with previous results from other serial sections of the same ingot, and the rotation angle about the common $\langle 101 \rangle$ direction fits that described for second order $\{111\}$ twinning.¹¹

Figure 8. Optical Micrograph of a Wafer Containing Sinuous Grain Boundaries (Magnification = 21X)

Figure 9. Electron Channelling Determination of Polysilicon Crystal Surface Normals in a Transverse Section Exhibiting Sinuous Grain Boundaries

Figure 10. Individual Grain Reflections Obtained by the Asymmetric Crystal Topography (ACT) Method Applied to Grains 1 and 2 in Cell 1-1

Preliminary x-ray topographs have been obtained with a zero layer (044) reflection from grain 2 and a ($3\bar{5}\bar{1}$) skew reflection from grain 1.¹³ The reflections were obtained with Cu $K\alpha_1$ radiation. Identification of the reflections has been confirmed by measurement of the relative rotation of the two x-ray images which is able to be checked against the stereographic projection analysis in Figure 10.

Figure 11 illustrates the ($3\bar{5}\bar{1}$) x-ray reflection topograph showing a portion of grain 1 in cell 1-1. The dark regions mean enhanced x-ray reflection intensity (e.g. the metal solar cell contacts absorb x-rays so they appear white). Labelled on the topograph are two ($\bar{1}\bar{1}1$) twins, a single (111) twin and a ($1\bar{1}1$) trace. The dislocation contrast is indicated in the background intensity. The dislocation content is estimated to be below $10^4/\text{cm}^2$ which is very low. The reduced dislocation content is reflected in the relatively good AM1 current density of $30 \text{ mA}/\text{cm}^2$. In the upper right hand corner of Figure 11 is a subgrain boundary and an inclusion (neither of them are optically visible on the cell) which show no deleterious effect in photoresponse.⁶ The x-ray topograph of grain 2 shows the same background dislocation contrast as grain 1. At present, further characterization of this topograph (grain 2) is continuing and the results will be presented in the next report along with direct comparisons of topographs and scanning photo-response measurements.

Figure 11. $(3\bar{5}\bar{1})$ X-Ray Reflection Topograph Showing A Portion of Grain 1 in Cell 1-1

V. CONCLUSIONS

1. A resistance heated Czochralski crystal growing furnace has been redesigned to accommodate the in-situ casting of polysilicon ingots. Design modifications were made to incorporate thermocouples into various locations within the furnace to allow for the constant monitoring of the temperature profile along the entire furnace length during the casting process.

2. Metallurgical grade silicon obtained from several suppliers was evaluated for suitability as impure feedstock for the experimental casting runs and a supplier was chosen. The material was prepared by grinding the large pieces into powder using anvils made from SG silicon. The uniformity of the feedstock was ascertained by optical emission spectrograph analysis of three random samples of the feedstock; results of the analysis are presented.

3. A total of sixteen casting runs were made this quarter. Union Carbide grade CMB graphite was found to be the most suitable crucible material because its coefficient of linear thermal expansion closely matches that of silicon. Grain size of the polysilicon material increased from bottom to top of the ingot.

4. Solar cells were fabricated on wafers taken from the successful experimental cast ingots. A total of seven ingots were processed so far: five ingots were pure SG silicon and the remaining two contained 1% and 5% MG silicon respectively. The average efficiency of cells from the first SG ingot was 10.4% AM0 (in excess of 12% AM1) and a maximum cell efficiency of 11.1% AM0 (which is nearly 13% AM1). Thus a milestone which required that the baseline casting experiments using 100% SG silicon shall demonstrate greater than 10% AM1 was exceeded.

5. Solar cells processed from the SG silicon ingots in general had better I_{SC} from wafers taken from the top and middle of the castings than from the bottom. Additionally, in general, the red I_{SC} response (Corning filter #2408) degraded from top to bottom of the ingot which indicates a general decrease in minority carrier diffusion length from top to bottom of the ingots. The 1% MG silicon ingot had the best I_{SC} from cells in the middle of the ingot; the top and bottom cells had the same response. However, the overall response of all the cells was greatly reduced from the 100% SG ingot levels. The 5% MG silicon ingot exhibited further reduction in the overall I_{SC} and additional degradation from top to bottom of the ingot.

6. Detailed analysis of the dark I-V characteristics of cells taken from the top, middle, and bottom of the cast polysilicon ingots showed that the top and middle cells had the best dark characteristics. Cells fabricated from the bottom of the ingots tended to be dominated by large space-charge components (resulting in degradation in fill factor and V_{OC}). Cells fabricated from the middle and top of the ingots showed this same tendency as the percentage of MG silicon increases. At present the origin of the large space-charge component is unknown and under further investigation.

7. A new method was developed to measure the thermal emission rate of a trap in a semiconductor using Deep Level Transient Spectroscopy. The new method eliminates temperature scanning by incorporating a spectrum analyzer into the measurement system. Measurements of the trap level in an NBS-supplied gold-doped diode show excellent agreement with published results. MOS diodes are presently being fabricated on polysilicon wafers for DLTS measurements.

8. Efforts were directed toward decreasing the spot size on the scanning photoresponse system from 60 μm to 5 μm . System modifications were implemented which enabled several successful scanning measurements to be made with the 5 μm spot on a single crystal cell having a shunt resistance

greater than 30 k Ω . It is planned to fabricate polysilicon test cells having planar (non-sawn) junctions in order to obtain favorable shunt resistances to allow accurate scanning with a 5 μ m spot.

9. Electron channelling patterns were obtained for all crystallographic directions in polysilicon material and were assembled into a composite [001]-[011]-[111] standard triangle. The composite channelling pattern is now used in one way as a reference base for determining the crystallographic orientations of grains, as small as 1 mm in diameter, directly in the SEM. Preliminary measurement results on a polysilicon wafer containing sinuous grain boundaries indicate that the range of grain orientations associated with the sinuous grain boundaries lie along the [111]-[100] zone axis and are as far from the [110] direction as possible.

10. Preliminary x-ray topographs were obtained for grains 1 and 2 in solar cell 1-1 using the asymmetrical crystal topography technique. The topographs show excellent resolution of dislocations (dislocation content estimated to be less than $10^4/\text{cm}^2$), twins, and a subgrain boundary which is not optically visible. More topographs are being taken for further detailed structural analysis and comparison with scanning photoresponse measurements.

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APPENDIX A

SOLAR CELL PROCESS SEQUENCE

Solarex will use a cell fabrication as shown in the flow chart in Figure 1. Each step is described in detail in the following sections, including:

- general process description
- important parameters to be monitored
- quality assurance requirements

Additionally, the decontamination procedures used during the process are discussed.

FIGURE 1
PROCESS SEQUENCE

continued on next page

1. Sodium Hydroxide Etch

The etch is performed in 30% by weight industrial grade NaOH in deionized water. The bath is maintained at greater than 110°C at which temperature it is rapidly boiling. Etch times of 5 to 10 minutes are typically sufficient to remove all saw damage. The etch will continue until all wafers have a thickness between 10 and 12 mils. The temperature, concentration and etch time of each batch will be measured and recorded. After the etch, the thickness of sample wafers will be measured to check for variation across the surface of one wafer and for variations from wafer to wafer. At the completion of the etching step, the resistivity of the wafer will be checked and recorded.

2. Diffusion

The diffusion process will be performed in a standard quartz diffusion tube with the samples mounted in a quartz diffusion boat. The wafers will be arranged parallel to the gas flow, with the control wafers upstream where the chance of contamination by the test wafers is minimized. The diffusion source will be phosphine gas flowing through the tube for 15 minutes. The temperature will be $870^{\circ}\text{C} \pm 5^{\circ}\text{C}$. The tube will be cleaned before each monitor lot. During each lot the gas flow rate and time of diffusion will be monitored.

After diffusion the sheet resistance of several test and monitor cells will be measured and recorded. One monitor or control cell will be measured at 5 locations to investigate the uniformity across the wafer surfaces.

3. Evaporation of Al Back

A layer of Al 5000 to 10,000 Å thick will be evaporated onto the back of the cell after the back etch process. The vacuum chamber pressure, deposition rate and deposition thickness will be monitored and recorded. A maximum pressure of 2.10^{-5} Torr will be allowed. Following the evaporation, the cells will be visually inspected to assure that a continuous film has been deposited on the cell back.

4. P^+ Formation

The P^+ formation will be carried out in a diffusion tube at 750°C with an inert atmosphere for 7 minutes. Once again the tube will be profiled and the temperature and time recorded for each run.

5. Back Evaporation

Solarex's patented Trimet (Ti-Pd-Ag) would be employed for both the front and back contacts of these cells. Resistance heated filaments will be employed for the deposition of the metals. The evaporations are performed by a Kronos Deposition Controller so that all depositions can be identical. The deposition rates are monitored by crystal oscillators and the evaporation plotted graphically. The vacuum pressure will

be recorded by the operator. A maximum pressure of 2.10^{-5} Torr will be allowed. One sample from each lot will be tape tested to assure back contact adhesion. No cell will have its contacts tape tested until after electrical evaluation.

6. Front Pattern Definition by Photolithography

Photolithography will be employed for front pattern definition. All wafers will be processed into 2cm x 2cm cells as shown in Figure 2. The standard photolithography used on these cells will be documented with the following parameters controlled and recorded:

- spin-speed
- bake time
- bake temperature
- exposure time
- mask employed
- develop time

In addition, the light intensity, developer temperature, and rinse temperature are monitored to assure uniformity of front contacts.

7. Front Evaporation

The front evaporation will be performed in exactly the same manner as the back evaporation as described in Section 6. The same parameters will be monitored and data recorded and a tape test performed.

APPLICATION		REVISION			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED

FIGURE 2

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± ± .XXX ±	CONTRACT NO. 954883		SOLAREX CORPORATION 1335 PICCARD DRIVE ROCKVILLE, MD 20850 □ 301 948 0202		
	APPROVALS	DATE	NASA-OAST ULTRATHIN CELL 2CM X 2CM		
	DRAWN D. LEBOWITZ	5-2-78			
	CHECKED J. J. W.	5/2/78			
MATERIAL			SIZE A	CODE IDENT NO. R D	DRAWING NO. 0646
FINISH			DIMENSIONS IN MILS		
DO NOT SCALE DRAWING			SCALE NONE	SHEET	OF

8. Silver Plating

The grid lines will be enforced by silver electroplating. The plating time will be recorded for each lot. During the course of the plating, metal thickness will be checked visually. At the conclusion of the plating, the front pattern conductivity shall be measured electrically.

9. Cut Cells to Size

The cells will be cut to the required 2cm x 2cm size. The lot and cell number will be written on the back of the cell at the time of cutting.

10. Ta₂O₅ AR Coating

The anti-reflective coating will be a quarter wavelength layer of electron-beam evaporated Ta₂O₅. Both the vacuum pressure and the thickness of the deposited film will be monitored and recorded. The consistency of the AR coating will be shown by using the Reflectometer to plot the reflection as a function of wavelength on a sampling basis.

11. Sinter

The cells will be sintered at approximately 450°C for 1 minute. This sintering will assure good contact adhesion and density of the AR coating. Both the time and temperature for each lot will be recorded.

In the event of failure of any of the metallization steps the cells will be reprocessed through all of the metallization steps. A metal stripping etch will be performed and the surfaces cleared in preparation for remetallization. Any reprocessing will be recorded.

Decontamination Procedures

Cross-contamination of one experimental casting group by another will be prevented by proper cleaning and checked by the use of monitor lots. After one casting lot has been run, the diffusion and alloy tubes and boats will be steamed cleaned by gaseous HCl while in place at elevated temperatures. Then they will be cooled, removed from the furnace and etched in HF to remove the outer layer. In addition, all etchant and cleaning baths will be changed with the containers being rinsed in deionized water. Between all steps the wafers or cells will be cleaned in deionized rinsing systems with the conductivity of the water monitored.

After the cleaning process has been accomplished a monitor lot will be run using control silicon. No cast polysilicon wafers will be run until these monitor cells have been completed and the test results show no contamination of the equipment.

APPENDIX B

Data Summary of Cell Lots 10, 15, 16, 17, 19, 20, and 21

Lot No.: E-10 Control

Cell #	I_{sc} (mA)	V_{oc} (mV)	P_m (mW)	I_{mp} (mA)	V_{mp} (mV)	I_{sc} blue (mA)	I_{sc} red (mA)	F.F.
C1	148	614	72.0	137	524	39.4	78.7	.794
C2	147	616	72.9	136	535	39.8	80.2	.804
C3	149	617	73.3	137	534	39.4	80.6	.795
C4	147	617	72.5	135	536	38.4	79.2	.800
C5	148	611	67.3	130	517	39.8	78.7	.743
C6	150	616	73.0	136	536	40.3	80.2	.788
C7	146	609	70.7	139	510	38.4	79.7	.793
C8	147	612	70.8	139	510	38.4	80.6	.785
C9	148	613	69.1	132	522	39.8	78.7	.763
C10	148	613	67.7	134	505	40.3	79.2	.747
C11	147	610	67.0	131	511	39.4	79.2	.748
C12	149	616	72.7	139	522	39.8	79.7	.791
C13	143	594	61.4	125	490	35.5	79.2	.722
C14	146	609	62.3	122	511	38.9	78.7	.700
AVG	147	612	69.5	134	519	39.1	79.5	.770
σ	1.65	5.79	3.74	5.19	12.9	1.19	0.67	.031
C.V.	.0112	.00946	.0538	.0387	.0248	.0304	.00842	.040

LOT NO.: E-10 Control

CELL NUMBER	$R_{\text{series}} (\Omega)$	$R_{\text{shunt}} (\Omega)$	CONDUCTANCE (mS)	CAPACITANCE ($\mu\text{F}/\text{cm}^2$)	RESISTIVITY ($\Omega\text{-cm}$)
C1	.064	620	1.68	.0505	.60 - .63
C2	.023	2,280	.53	.0498	
C3	.057	1,060	.80	.0510	
C4	.072	490	1.92	.0450	
C5	.068	117	8.47	.0500	
C6	.074	8,680	.11	.0508	
C7	.088	2,750	.40	.0507	
C8	.044	2,000	.50	.0500	
C9	.082	430	2.49	.0512	
C10	.070	73	10.7	.0365	
C11	.086	298	3.55	.0502	
C12	.029	1,780	.55	.0507	
C13	.064	198	6.77	.0512	
C14	.086	46	20.0	.0498	
AVG	.065	-----	-----	.0491	
σ	.020	-----	-----	.0038	
C.V.	.31	-----	-----	.077	
MEDIAN	---	620	1.92	-----	

Lot No.: E-10 Test

Cell #	I_{sc} (mA)	V_{oc} (mV)	P_m (mW)	I_{mp} (mA)	V_{mp} (mV)	$I_{sc \text{ blue}}$ (mA)	$I_{sc \text{ red}}$ (mA)	F.F.
T1M	138	568	59.3	128	464	39.4	72.0	.755
T2M	137	549	38.5	88.8	434	38.4	71.5	.511
T3M	138	570	59.8	127	465	38.4	73.4	.759
T4M	139	567	59.7	126	473	37.0	73.9	.758
T5M	BROKEN IN TEST							
T6M	137	555	58.3	123	475	37.4	72.0	.767
T7M	140	566	60.0	128	470	38.4	73.4	.759
T8M	139	565	59.1	125	472	37.0	73.9	.751
AVG	138	563	56.4	121	465	37.9	72.9	.722
σ	1.02	7.27	7.31	13.3	13.1	0.92	0.94	.086
C.V.	.00739	.0129	.130	.110	.0282	.0243	.0129	.119

LOT NO.: E-10 Test

[illegible]

Lot No.: Controls 15, 17, 19

[illegible]

LOT NO.: Controls 15, 17, 19

CELL NUMBER	$R_{\text{series}} (\Omega)$	$R_{\text{shunt}} (\Omega)$	CONDUCTANCE (mS)	CAPACITANCE ($\mu\text{F}/\text{cm}^2$)	RESISTIVITY ($\Omega\text{-cm}$)
C1	----	2,170	0.45	.0263	2.1 - 2.2
C2	.082	4,170	0.38	.0260	
C3	.076	4,310	0.29	.0263	
C4	.088	5,130	0.29	.0263	
C5	.081	1,440	0.68	.0260	
C6	.064	130	7.54	.0260	
C7	.077	2,950	0.16	.0260	
C8	.095	1,950	0.68	.0265	
C9	.093	1,030	0.60	.0265	
C10	----	1,300	0.58	.0265	
AVG	.082	-----	-----	.0262	
σ	.0093	-----	-----	.00020	
C.V.	.11	-----	-----	.00764	
MEDIAN	---	1,950	0.45	-----	

Lot No.: E-15 Test

Cell #	I_{sc} (mA)	V_{oc} (mV)	P_m (mW)	I_{mp} (mA)	V_{mp} (mV)	I_{sc} blue (mA)	I_{sc} red (mA)	F.F.
T1T	138	548	57.7	128	452	36.0	73.9	.764
T2T	137	551	57.2	128	448	32.6	76.8	.759
AVG	138	549	57.4	128	450	34.3	75.4	.762
T3M	132	557	55.9	123	453	33.6	69.6	.764
T4M	133	558	56.4	121	466	33.6	73.0	.760
AVG	132	558	56.2	122	460	33.6	71.3	.762
T5B	133	546	54.0	121	444	34.6	72.5	.741
T6B	132	547	53.6	121	442	35.0	70.1	.746
T7B	131	551	52.0	118	440	34.6	70.1	.722
T8B	132	550	52.1	116	450	35.0	68.6	.720
T9B	131	554	54.1	118	458	34.1	70.6	.744
AVG	132	550	53.2	119	447	34.7	70.4	.735
σ	.748	2.87	.922	1.94	6.52	.332	1.25	.0112
C.V.	.00567	.00522	.0173	.0163	.0146	.00959	.0178	.0153
GRAND STATISTICS								
AVG	133	551	54.8	122	450	34.3	71.7	.747
σ	2.44	4.03	1.99	3.91	7.83	.94	2.44	.0158
C.V.	.0183	.0073	.0363	.0320	.0174	.0274	.0340	.0212

LOT NO.: E-15 Test

CELL NUMBER	R _{series} (Ω)	R _{shunt} (Ω)	CONDUCTANCE (mS)	CAPACITANCE (μ F/cm ²)	RESISTIVITY (Ω -cm)
T1T	.067	2,890	.39	.0205	6.1 - 9.3
T2T	.081	4,900	.18	.0198	
AVG	.074	-----	---	.0202	
σ	-----	-----	---	-----	
C.V.	-----	-----	---	-----	
MEDIAN	-----	2,890	.39	-----	
T3M	.019	18,300	.11	.0253	3.4 - 4.2
T4M	.050	813	1.28	.0245	
AVG	.034	-----	-----	.0249	
σ	-----	-----	-----	-----	
C.V.	-----	-----	-----	-----	
MEDIAN	-----	813	1.28	-----	
T5B	-----	7,270	.20	.0270	3.2 - 4.2
T6B	.066	6,540	.23	.0263	
T7B	.060	361	2.75	.0263	
T8B	.044	2,490	.53	.0273	
T9B	.055	1,020	1.08	.0260	
AVG	.052	-----	-----	.0266	
σ	.011	-----	-----	.00049	
C.V.	.22	-----	-----	.0183	
MEDIAN	---	2,490	.53	-----	

LOT NO.: E-15 Test

[illegible]

Lot No.: E-16 Controls

Cell #	I_{sc} (mA)	V_{oc} (mV)	P_m (mW)	I_{mp} (mA)	V_{mp} (mV)	I_{sc} blue (mA)	I_{sc} red (mA)	F.F.
C1	153	595	71.8	144	499	41.8	81.1	.789
C2	BROKEN							
C3	152	593	70.2	141	499	41.3	81.6	.781
C4	153	592	65.4	133	492	41.3	82.6	.725
C5	153	595	71.7	142	504	40.3	81.6	.788
C6	152	592	69.2	138	500	41.3	81.6	.771
C7	151	588	59.2	120	496	40.3	81.1	.664
C8	152	588	59.2	120	496	40.3	81.1	.664
C9	152	596	72.4	146	495	41.8	81.1	.799
C10	154	594	70.6	140	503	40.3	81.6	.772
C11	154	594	68.5	138	497	41.3	82.6	.749
C12	154	593	72.0	144	500	41.3	82.1	.790
C13	154	594	71.6	145	493	41.3	81.6	.784
C14	153	591	64.1	128	500	41.3	81.6	.709
C15	151	591	68.2	136	402	39.4	82.1	.765
AVG	152	592	68.6	138	498	40.9	81.7	.760
σ	1.22	.237	3.63	7.10	3.86	.710	.44	.0364
C.V.	.00803	.00400	.0529	.0514	.775	.0174	.00538	.0479

LOT NO.: E-16 Controls

CELL NUMBER	$R_{series} (\Omega)$	$R_{shunt} (\Omega)$	CONDUCTANCE (m Ω)	CAPACITANCE ($\mu F/cm^2$)	RESISTIVITY ($\Omega\text{-cm}$)
C1	.032	7,870	.13	.0262	2.1 - 2.2
C3	.073	929	1.01	.0262	
C4	.076	877	1.12	.0260	
C5	.079	961	1.04	.0260	
C6	.040	156	5.81	.0262	
C7	.092	4,450	.27	.0268	
C8	.073	25	38.5	.0252	
C9	.079	1,600	.57	.0262	
C10	.10	1,660	.62	.0268	
C11	.10	2,750	.42	.0270	
C12	.084	14,700	.11	.0263	
C13	.054	9,710	.18	.0265	
C14	.10	2,430	.49	.0262	
C15	.069	144	6.94	.0265	
AVG	.075	----	----	.0263	
σ	.021	----	----	.0004	
C.V.	.28	----	----	.0161	
MEDIAN	----	1,660	.62	-----	

Lot No.: E-16 Test

[illegible]

LOT NO.: E-16 Test

[illegible]

Lot No.: E-17 Test

Cell #	I _{sc} (mA)	V _{oc} (mV)	P _m (mW)	I _{mp} (mA)	V _{mp} (mV)	I _{sc blue} (mA)	I _{sc red} (mA)	F.F.
T1T	132	570	53.0	115	460	35.0	70.6	.705
T2T	137	583	59.6	123	485	36.0	73.9	.747
T3T	135	578	58.4	119	490	35.0	73.0	.745
T4T	136	577	57.5	120	478	36.5	72.0	.731
T5T	142	574	57.8	124	465	38.9	74.9	.711
T6T	142	574	58.0	126	461	39.4	73.4	.714
AVG	137	576	57.3	121	473	36.8	72.9	.726
σ	3.64	4.04	2.07	3.62	11.8	1.75	1.37	.0165
C.V.	.0265	.007	.036	.0299	.025	.0476	.0189	.0227
T7M	138	569	54.2	116	469	39.8	71.0	.692
T8M	137	530	47.7	113	421	38.4	73.0	.655
T9M	138	569	54.6	119	461	38.9	70.6	.696
T10M	143	539	55.6	130	429	39.4	73.9	.724
T11M	137	571	54.3	116	470	39.4	71.0	.694
AVG	139	556	53.2	119	450	39.2	71.9	.692
σ	2.24	17.5	2.83	5.91	20.8	.483	1.31	.022
C.V.	.0162	.0315	.0533	.0497	.0462	.0123	.0182	.032
T12B	BROKEN							
T13B	128	538	41.3	103	403	37.4	64.8	600
GRAND STATISTICS								
AVG	136	562	53.4	118	453	37.8	71.3	.693
σ	4.35	18.2	5.89	7.36	29.7	1.65	3.15	.0460
C.V.	.0319	.0324	.110	.0624	.0656	.0437	.0442	.0664

LOT NO.: E-17 Test

CELL NUMBER	$R_{series} (\Omega)$	$R_{shunt} (\Omega)$	CONDUCTANCE (mS)	CAPACITANCE ($\mu F/cm^2$)	RESISTIVITY ($\Omega-cm$)
T1T	.034	80.0	11.1	.0400	1.2 - 1.7
T2T	.022	216	4.62	.0395	
T4T	.053	806	1.30	.0390	
T5T	.19	206	4.68	.0373	
T6T	.20	167	5.79	.0349	
AVG	.10	---	----	.0381	
σ	.078	---	----	.0019	
C.V.	.79	---	----	.0497	
MEDIAN	---	206	4.68	-----	
T7M	.029	86.3	11.4	.0368	1.3 - 1.9
T8M	.37	260	3.98	.0110	
T9M	.076	152	6.52	.0368	
T10M	.17	703	1.44	.0155	
T11M	.039	297	3.68	.0375	
AVG	.14	---	----	.0275	
σ	.13	---	----	.0117	
C.V.	193	---	----	.427	
MEDIAN	---	260	3.98	----	
T12B	---	849	72.9	.0368	1.3 - 1.8
T13B	.039	14.0	1.54	.0363	
AVG	.039	----	----	.0365	
σ	----	----	----	-----	
C.V.	----	----	----	-----	
MEDIAN	----	14.0	1.54	-----	

E-17 Test

[illegible]

E-19 Test

[illegible]

LOT NO.: E-19 Test

[illegible]

Lot No.: E-20, 21 Controls

[illegible]

Lot No.: E-20 Test

Cell #	I_{sc} (mA)	V_{oc} (mV)	P_m (mW)	I_{mp} (mA)	V_{mp} (mV)	I_{sc} blue (mA)	I_{sc} red (mA)	F.F.
T1T	110	511	31.9	91.7	347	38.9	49.0	.567
T2T	112	559	43.0	101	427	38.4	51.8	.685
AVG	111	535	37.5	96.4	387	38.7	50.4	.626
T3M	124	536	30.1	84.0	359	39.8	58.1	.451
T4M	124	574	52.4	110	475	37.0	59.5	.736
T5M	123	496	23.7	78.7	302	38.4	60.5	.390
T6M	124	561	47.4	102	466	39.4	59.5	.682
T7M	126	577	53.7	112	478	39.4	61.4	.739
T8M	125	571	49.3	105	471	39.4	60.5	.690
AVG	124	552	42.8	98.6	425	38.9	59.9	.615
σ	.943	28.7	11.6	12.7	69.0	.950	1.04	.140
C.V.	.00758	.0519	.270	.129	.162	.0244	.017	.227
T9B	108	281	13.5	77.7	174	37.9	47.0	.447
T10B	108	277	13.6	78.2	173	38.9	46.5	.454
T11B	113	344	18.1	78.2	231	39.4	50.4	.465
T12B	112	346	17.6	81.6	215	38.4	50.9	.452
T13B	116	430	23.4	88.0	265	36.0	54.0	.469
AVG	111	336	17.2	80.7	212	38.1	49.8	.457
σ	3.07	55.7	3.63	3.89	35.1	1.17	2.75	.00826
C.V.	.0276	.166	.211	.0482	.165	.0308	.0553	.0181

Lot No.: E-20 Test

[illegible]

LOT NO.: E-20 Test

CELL NUMBER	$R_{series} (\Omega)$	$R_{shunt} (\Omega)$	CONDUCTANCE (mS)	CAPACITANCE ($\mu F/cm^2$)	RESISTIVITY ($\Omega-cm$)
T1T	.042	503	2.22	.0585	.6
T2T	.045	2,450	.52	.0560	
AVG	.043	-----	-----	.057	
T3M	.19	18.3	53.3	.0445	.8 - .9
T4M	.030	697	1.53	.0478	
T5M	.044	11.2	86.6	.0408	
T6M	.072	89.4	10.8	.0483	
T7M	.026	840	1.47	.0478	
T8M	.034	236	4.09	.0483	
AVG	.066	---	-----	.0463	
σ	.057	---	-----	.00277	
C.V.	.87	---	-----	.0600	
MEDIAN	---	89.4	4.09	-----	
T9B	.050	52.9	31.3	.0488	.9 - 1.3
T10B	.075	53.8	28.7	.0488	
T11B	.062	102	17.8	.0488	
T12B	.047	26.8	34.4	.0488	
T13B	-----	226	7.62	.0480	
AVG	.059	---	-----	.0486	
σ	.011	---	-----	.00032	
C.V.	.19	---	-----	.0065	
MEDIAN	---	53.8	28.7	-----	

LOT NO.: E-20 Test

[illegible]

Lot No.: E-21 Test

Cell #	I_{sc} (mA)	V_{oc} (mV)	P_m (mW)	I_{mp} (mA)	V_{mp} (mV)	$I_{sc \text{ blue}}$ (mA)	$I_{sc \text{ red}}$ (mA)	F.F.
T1T	100	455	19.1	67.6	282	37.4	42.7	.419
T2T	105	476	20.4	70.6	289	39.4	44.2	.409
T3T	105	568	31.9	74.4	425	38.4	44.6	.533
T4T	101	479	20.1	69.1	291	37.0	42.7	.418
T5T	93.6	175	5.91	60.0	98.4	34.6	39.4	.361
T6T	95.5	299	11.4	67.7	169	36.0	40.8	.400
AVG	100	409	18.1	68.2	259	37.1	42.4	.423
σ	4.32	131	8.10	4.34	103	1.56	1.82	.0528
C.V.	.0432	.321	.448	.0636	.398	.0419	.0423	.125
T7M	97.9	359	15.4	70.0	219	36.0	41.2	.437
T8M	95.0	319	12.9	68.2	189	35.5	40.3	.425
T9M	101	365	16.8	71.5	234	37.9	42.2	.455
T10M	102	396	18.5	76.8	241	37.9	43.2	.460
T11M	102	364	15.7	71.0	221	38.9	41.8	.422
T12M	100	318	13.7	71.5	192	38.4	41.8	.429
AVG	99.7	354	15.5	71.5	216	37.4	41.8	.438
σ	2.51	27.5	1.86	2.63	19.5	1.25	.886	.0146
C.V.	.0251	.0775	.120	.0368	.0904	.0333	.0212	.0333
T13B	64.3	277	8.20	48.5	169	32.2	19.2	.460
T14B	63.8	296	8.07	41.3	195	31.7	18.7	.427
T15B	63.8	224	5.44	38.9	140	32.2	18.2	.380
T16B	63.8	324	11.9	51.8	229	30.7	19.2	.573
T17B	62.9	316	11.1	51.3	216	30.7	18.7	.557

Lot No.: E-21 Test

[illegible]

LOT NO.: E-21 Test

CELL NUMBER	$R_{series} (\Omega)$	$R_{shunt} (\Omega)$	CONDUCTANCE (mS)	CAPACITANCE ($\mu F/cm^2$)	RESISTIVITY ($\Omega-cm$)
T1T	.066	21.1	45.3	.0963	.2
T2T	.075	42.6	28.9	.0972	
T3T	.13	95.2	13.0	.0948	
T4T	.072	26.2	42.0	.0948	
T5T	.019	4.47	231	.0575	
T6T	.020	17.9	88.1	.0925	
AVG	.064	----	----	.0888	
σ	.038	----	----	.0141	
C.V.	.59	----	----	.0889	
MEDIAN	---	21.1	42.0	-----	
T7M	.052	47.9	27.4	.0847	.2 - .3
T8M	.033	22.1	51.8	.0937	
T9M	.074	74.3	19.2	.0912	
T10M	.020	108	14.7	.0850	
T11M	.25	78.8	18.8	.0847	
T12M	.056	37.6	36.6	.0847	
AVG	.080	----	----	.0873	
σ	.076	----	----	.00369	
C.V.	.95	----	----	.0423	
MEDIAN	----	47.9	.912	-----	

LOT NO.: E-21 Test

[illegible]