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QMODULE:

CAMAC Modules Recognized by the QAL Compiler

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NOTICE

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FOREWORD

This manual is one of a series describing the components of the Q general-purpose data-acquisition system. This system, developed at the Clinton P. Anderson Meson Physics Facility, is designed to be useful in a variety of experimental situations for managing the acquisition and display of experimental data. It runs on the Digital Equipment Corporation (DEC) PDP-11 family of computers running the RSX-11D operating system and equipped with Microprogrammed Branch Drivers (MBDs) and CAMAC branch highway systems.

The Q system is designed to allow high-speed data acquisition and recording. It is driven primarily by the occurrence of events in the experimental apparatus. It is modular in construction and is easy to use, understand, and modify. Its components are an MBD program for data taking, an RSX handler for data recording and distribution, a control and analysis task (the analyzer task), a histogram entry and retrieval system, histogram plotting and dot plotting packages, and an operator control system. One special piece of hardware is required: a CAMAC module for responding to experimental events.

This manual is closely associated with the manual entitled "QAL and the Analyzer Task," Los Alamos Scientific Laboratory report LA-6884-M (October 1977) and should be read as a supplement to that document.

QMODULE: CAMAC MODULES RECOGNIZED BY THE QAL COMPILER

by

Martin Kellogg, Michael M. Minor, Sally Shlaer,
Nancy Spencer, Richard F. Thomas, Jr., and Henri van der Beken

ABSTRACT

The compiler for the Q Analyzer Language, QAL, recognizes a certain set of CAMAC modules as having known characteristics. The conventions and procedures used to describe these modules are discussed as well as the tools available to the user for extending this set as required.

1.0 HOW TO READ THE MODULE TABLE

Every CAMAC module referred to by name by a QAL operation such as RD16, STROBE, or TLAM in a Q analyzer task must be entered in the module table associated with QAL. Each module is identified by a unique name, normally a two-letter manufacturer's code followed by a four-digit model number, for example, LR2248 (Lecroy Model 2248 octal ADC) or KS3610 (Kinetic Systems Model 3610 hex scaler). The appendix of this manual is a listing of the current module table.

Associated with each named module is a list of the legal functions that can be addressed to it for the purpose of data acquisition. The tables are so constructed as to mask irrelevant differences between functionally equivalent modules. Not all functions recognized by the hardware of a particular CAMAC module need appear in the module table; generally only those useful in data acquisition are entered.

For any given module, the module name is given in a line of the form:

```
MODULE  modnam,amax
or
MODULE  modnam
```

The modnam field specifies the name by which the module is known (KS3610, for example); this is the name referred to by the DEVICE statement of QAL. If the parameter amax is present, this is the highest valid CAMAC subaddress (A) that can be addressed to the module.

Following the MODULE line is a series of OP lines that define the legal operations. Each OP line has the form:

```
OP  fname,fcode,acode
or
OP  fname,fcode
```

The fname field specifies a valid QAL operation (RD16, STROBE, etc.) which is already known to QAL.* Items fcode and acode specify the CAMAC F and A codes that must be supplied to the module to execute the hardware function known as fname. If the acode field is missing from the OP line, it will be supplied from the A subaddress field of any DEVICE statement which refers to the named module.

2.0 HOW TO ADD MODULES TO QAL'S REPERTOIRE

The standard module table is supplied on the Q disks as file [122,7]QMODULE.MAC. Q users may keep a private copy of this file and edit it to add new modules as desired.

First, the pseudo-devices IN: OU: and LS: must be redirected to appropriate disks:

```
RED  DKn:=IN:
RED  DKn:=LS:
RED  DKn:=OU:
```

where:

IN is the disk containing [122,7]OBJ files for the QAL compiler (that is, a Q disk)

*A list of valid QAL device operations can be found in "QAL and the Analyzer Task" Los Alamos Scientific Laboratory report LA-6884-M (October 1977).

OU is the disk for output of new QAL compiler

LS is the disk for output of new QAL load map and QMODULE
list file

Second, after QMODULE.MAC has been edited, it must be reassembled:

```
MAC>OU:[122,7]QMODULE,LS:[122,7]QMODULE/-SP=IN:[122,7]QMODULE
```

Next, rebuild the QAL compiler:

```
MCR>TKB @IN:[122,7]QAL.BLD
```

Finally, the old copy of the compiler must be removed and the new one installed.

```
MCR>REM ...QAL  
MCR>INS OU:[122,202]QAL/INC=1792
```

One word of caution: new QAL compilers are distributed frequently. The update procedure usually deletes all previous versions of [122,7]QMODULE.MAC and [122,202]QAL.TSK from the Q disk. Hence if one elects to modify QMODULE, it is a sensible and necessary precaution to keep the private copy under a private UIC. In addition, variations on QMODULE should be submitted to the Q software support group so that modifications of general interest can be incorporated into the standard system.

ACKNOWLEDGMENTS

We would like to thank Janis Builta, Elvira Martinez, and Lorrie Voorhees for their dedicated effort in preparing this manual.

APPENDIX

QMODULE.MAC

.SETTL EG&G MODULES

```

;
;EG0024 - EG&G TEST MODULE #24
MODULE EG0024
OP      RD24,0          ;READ 24-BIT DATA
OP      RD16,0          ;READ 16-BIT DATA
OP      RC16,2          ;READ AND CLEAR 16-BIT DATA
OP      RC24,2          ;READ AND CLEAR 24-BIT DATA
OP      CL,9,0          ;CLEAR DATA
OP      WR24,16,0       ;WRITE DATA
;
;EG0104 - TIME DIGITIZER TD 104
;
MODULE EG0104,3
OP      RD16,0          ;READ SCALER (A0-3)
OP      RC16,2          ;READ AND CLEAR (A0-3)
OP      TLAM,8,12       ;TEST LAM
OP      CL,9            ;CLEAR SCALER (A0-3)
OP      CLAM,10,12      ;CLEAR LAM
OP      DLAM,24,12      ;DISABLE LAM
OP      STROBE,25       ;TEST CHANNEL (A0-3)
OP      ELAM,26,12     ;ENABLE LAM
OP      TBUSY,27,12    ;TEST BUSY
;
;EG0212 - EG&G C212 COINCIDENCE BUFFER
;
MODULE EG0212
OP      RD16,0,0        ;READ 12 INPUTS
OP      RC16,2,0        ;READ AND CLEAR 12 INPUTS
OP      RD24,0,0        ;READ 24 INPUTS
OP      RC24,2,0        ;READ AND CLEAR 24 INPUTS
OP      CL,9,0
;
;EG0 24 - EG&G QUAD SCALER
;
MODULE EG0424,3
OP      RD16,0          ;READ 16-BIT SCALER (A0-A3)
OP      RC16,2          ;READ AND CLEAR 16-BIT SCALER (A0-A3)
OP      RD24,0          ;READ 24-BIT SCALER (A0-A3)
OP      RC24,2          ;READ AND CLEAR 24-BIT SCALER (A0-A3)
OP      CL,9            ;CLEAR SCALER (A0-A3)
OP      RDOV,12,1       ;READ OVERFLOW
;
;EG0811 - EG&G TD811 TIME DIGITIZER
;
MODULE EG0811,12
OP      RD16,0          ;READ A(0)-A(7)

```

```

OP      RC16,2      ;READ AND CLEAR A(0)-A(7). CLEARS ALL
                  ;REGISTERS LAM AND BUSY ONLY ON A(7).
                  ;A(0)-A(6) ARE ORDINARY READS.

OP      TLAM,8,12   ;TEST LAM
OP      CLAM,10,12  ;CLEAR LAM
OP      CL,11,12    ;CLEAR ALL REGISTERS,
                  ;LAM AND BUSY

OP      DLAM,24,12  ;DISABLE LAM
OP      STROBE,25   ;TEST ALL REGISTERS
OP      ELAM,26,12  ;ENABLE LAM
OP      TBUSY,27,12 ;TEST BUSY

;
      .SETTL JORWAY MODULES
;
;JO0030 - JORWAY MODEL 30 ANALOG TO DIGITAL CONVERTER
;
      MODULE JO0030      ;JORWAY MODEL 30 ADC
OP      RD16,0,0        ;READ DATA
OP      TLAM,8,0        ;TEST LAM, Q=1 IF LAM SET
OP      CONV,28,0       ;INITIATE A CONVERSION CYCLE
OP      DLAM,24,0       ;DISABLE LAM
OP      ELAM,26,0       ;ENABLE LAM

;
;JO0040 - JORWAY MODEL 40 DUAL 24-BIT OUTPUT REGISTER
;
      MODULE JO0040,1
OP      WR24,16         ;WRITE 24-BIT DATA REGISTER
OP      WC24,17         ;WRITE 24-BIT DATA REGISTER (PULSED
                  ;OUTPUT)

;
;JO0041 - JORWAY MODEL 41 OUTPUT REGISTER
;
      MODULE JO0041
OP      WR24,16,0       ;WRITE 12 BITS TO OUTPUT REGISTER
OP      WC24,17,0       ;WRITE 12 BITS (PULSED OUTPUT)
OP      SSET,20,0
OP      SCLR,22,0

;
;JO0060 - JORWAY MODEL 60 DUAL PARALLEL INPUT REGISTER
;
      MODULE JO0060,1
OP      RD16,0          ;READ 16-BIT DATA
OP      RD24,0          ;READ 24-BIT DATA
OP      TLAM,8          ;TEST LAM. Q=1 IF LAM SET
OP      CLAM,10         ;CLEAR LAM
OP      DLAM,24         ;DISABLE LAM
OP      ELAM,26         ;ENABLE LAM
OP      STROBE,28       ;STROBE DATA
OP      WR24,16         ;WRITE CONTROL REGISTER

;
;JO0061 - JORWAY DUAL PARALLEL INPUT REGISTER
;
      MODULE JO0061,1

```



```

OP      RD16,0      ;READ 16-BIT DATA
OP      RD24,0      ;READ 24-BIT DATA
OP      TLAM,8      ;TEST LAM. Q=1 IF LAM SET
OP      CLAM,10     ;CLEAR LAM
OP      ELAM,26     ;ENABLE LAM
OP      DLAM,24     ;DISABLE LAM

```

;JO0063 - JORWAY MODEL 63 - PRIORITY INTERRUPT REGISTER

```

MODULE JO0063
OP      RD16,0,0    ;READ INTERRUPT DATA
OP      RC16,2,0    ;READ AND CLEAR INTERRUPT DATA
OP      TLAM,8,0    ;TEST LAM. Q=1 IF LAM SET
OP      CL,9,0      ;CLEAR INTERRUPT DATA
OP      WR24,16,0   ;WRITE CONTROL DATA
OP      DLAM,24,0   ;DISABLE LAM
OP      ELAM,26,0   ;ENABLE LAM

```

;JO0064 - JORWAY MODEL 64 - DISCRIMINATOR-COINCIDENCE LATCH

```

MODULE JO0064
OP      RD16,0,0    ;READ LATCHES
OP      RC16,2,0    ;READ AND CLEAR LATCHES
OP      CL,9,0      ;CLEAR ALL LATCHES

```

;JO0065 - JORWAY MODEL 65 - 12-BIT NIM INPUT REGISTER

```

MODULE JO0065
OP      RC16,2,0    ;READ AND CLEAR DATA
OP      TLAM,8,0    ;TEST LAM. Q=1 IF LAM SET
OP      CLAM,10,0   ;CLEAR LAM
OP      DLAM,24,0   ;DISABLE LAM
OP      ELAM,26,0   ;ENABLE LAM

```

.SBTTL KINETIC SYSTEMS MODULES

; KS2515 - KINETIC SYSTEMS MODEL 2515 DUAL 10-BIT ADC

```

MODULE KS2515,1    ;KINETIC SYSTEMS 3515 DUAL 10-BIT ADC
OP      RD16,0      ;READ ADC (A0,A1)
OP      RC16,2      ;READ AND INITIATE CONVERSION (A0,A1)
OP      TLAM,8,15   ;TEST LAM, Q=1 IF LAM SET
OP      DLAM,24,15  ;DISABLE LAM
OP      CONV,25     ;INITIATE CONVERSION (A0,A1)
OP      STROBE,25,2 ;INITIATE CONVERSION IN BOTH ADC'S
OP      ELAM,26,15  ;ENABLE LAM
OP      TBUSY,27    ;TEST BUSY, Q=1 IF ADC NOT BUSY

```

; KS3082 - KINETIC SYSTEMS 12 BIT OUTPUT REGISTER

```

MODULE KS3082
OP   RD16,0,0      ;READ DATA
OP   TLAM,8,0      ;TEST LAM
OP   CL,9,0        ;CLEAR REGISTER AND LAM
OP   CLAM,10,0     ;CLEAR LAM
OP   WR24,16,0     ;WRITE REGISTER
OP   DLAM,24,0     ;DISABLE LAM
OP   ELAM,26,0     ;ENABLE LAM

```

```

;
;
; KS3420 - KINETIC SYSTEMS 64 CHANNELS, 24 BIT INPUT GATE
;

```

```

MODULE KS3420,15
OP   R24G1,0       ;READ GROUP 1 F(0)
OP   R24G2,1       ;READ GROUP 2 F(1)
OP   R24G3,2       ;READ GROUP 3 F(2)
OP   R24G4,3       ;READ GROUP 4 F(3)
OP   R16G1,0       ;RD16, GROUP 1 F(0)
OP   R16G2,1       ;RD16, GROUP 2 F(1)
OP   R16G3,2       ;RD16, GROUP 3 F(2)
OP   R16G4,3       ;RD16, GROUP 4 F(3)
OP   TLAM,8,0      ;TEST LAM
OP   CLAM,10,0     ;CLEAR LAM
OP   DLAM,24,0     ;DISABLE LAM
OP   STROBE,25,0   ;PRODUCE "EXECUTE" OUTPUT STROBE
OP   ELAM,26,0     ;ENABLE LAM
OP   TBUSY,27,0    ;PRODUCE "TEST STATUS" OUTPUT STROBE

```

```

;
;
; KS3430 MODIFIED TO INTERFACE 7 NUCLEAR DATA ADC'S
;

```

```

MODULE KS3430,15
OP   RC16,0,0      ;READ 16 BIT DATA REGISTER AND
                  ;INCREMENT
                  ;ADC SELECT REGISTER AT S1.
OP   RD16,1        ;A(0)=READ ADC SELECT REGISTER
                  ;A(15)=READ MODULE ID
OP   TLAM,8,0      ;TEST LAM Q IF SET
OP   CL,9,0        ;CLEAR ADDRESS REGISTER AND LAM
OP   CLAM,10,0     ;CLEAR LAM
OP   WR24,17,0     ;WRITE ADDRESS REGISTER
OP   CL,25,0       ;RESET ADC DATA REGISTER
OP   DLAM,24,13    ;DISABLE LAM
OP   ELAM,26,13    ;ENABLE LAM

```

```

;
;
; KS3520 - KINETIC SYSTEMS MODEL 3520 DUAL 12-BIT ADC
;

```

```

MODULE KS3520,1    ;KINETIC SYSTEMS 3520 DUAL 12-BIT ADC
OP   RD16,0        ;READ ADC
OP   RC16,2        ;READ AND INITIATE CONVERSION
OP   TLAM,8,15     ;TEST LAM, Q=1 IF LAM SET
OP   DLAM,24,15    ;DISABLE LAM

```

```

OP      CONV,25      ;INITIATE CONVERSION
OP      STROBE,25,2  ;INITIATE CONVERSION IN BOTH ADC'S
OP      TBUSY,27     ;TEST BUSY, Q=1 IF ADC NOT BUSY

```

```

;
;
; KS3530 - KINETIC SYSTEMS MODEL 3530-15 CHANNEL RELAY
;          MULTIPLEXER
;

```

```

MODULE KS3530      ;KINETIC SYSTEMS MODEL 3530-15 CHANNEL
                  ;RELAY MULTIPLEXER
OP      RD16,0,0    ;GATE ADDRESS REGISTER ONTO DATAWAY
OP      WR24,16,0   ;WRITE ADDRESS REGISTER FROM DATAWAY
OP      INCR,25,0   ;INCREMENT THE ADDRESS REGISTER

```

```

;
;
; KS3610 - KINETIC SYSTEMS MODEL 3610 HEX 50 MHZ SCALER
;

```

```

MODULE KS3610,5    ;KINETIC SYSTEMS MODEL 3610 HEX 50MHZ
                  ;SCALER
OP      RD16,0      ;READ SCALER (LOW 16-BITS) (A0-A5)
OP      RD24,0      ;READ SCALER (A0-A5)
OP      RDOV,1,12   ;READ 6 OVERFLOW BITS
OP      RC16,2      ;READ SCALER THEN CLEAR SCALER AND
                  ;OVERFLOW BIT
OP      RC24,2      ;READ THEN CLEAR
OP      TLAM,8,0    ;TEST LAM, Q=1 IF LAM SET
OP      CL,9        ;CLEAR SCALER AND OVERFLOW BIT
OP      CLOV,10     ;CLEAR OVERFLOW (LAM SOURCE) BIT
                  ;(A0-A5)
OP      DLAM,24,0   ;DISABLE LAM
OP      ELAM,26,0   ;ENABLE LAM

```

```

;
;
; KS3615 - KINETIC SYSTEMS MODEL 3615 HEX 100MHZ SCALER
;

```

```

MODULE KS3615,5    ;KINETIC SYSTEMS MODEL 3615 HEX 100HMZ
                  ;SCALER
OP      RD16,0      ;READ SCALER (A0-A5) (LOW 16-BITS)
OP      RD24,0      ;READ SCALER (A0-A5)
OP      RDOV,1,12   ;READ 6 OVERFLOW BITS
OP      RC16,2      ;READ THEN CLEAR SCALER AND OVERFLOW
                  ;BIT
OP      RC24,2      ;READ THEN CLEAR
OP      TLAM,8,0    ;TEST LAM, Q=1 IF LAM SET
OP      CL,9        ;CLEAR SCALER AND OVERFLOW BIT
OP      CLOV,10     ;CLEAR OVERFLOW (LAM SOURCE) BIT
                  ;(A0-A5)
OP      DLAM,24,0   ;DISABLE LAM
OP      INCR,25,0   ;INCREMENT SCALER (A0-A5)
OP      ELAM,26,0   ;ENABLE LAM

```

```

;
;
; KS3640 - KINETIC SYSTEMS MODEL 3640 QUAD UP-DOWN PRESET SCALER

```

```

;
MODULE KS3640,3      ;KINETIC SYSTEMS MODEL 3640 QUAD
                    ;UP-DOWN PRESET SCALER
OP      RD16,0       ;READ SCALER (A0-A3)
OP      RD24,0       ;READ SCALER
OP      RDOV,1,12    ;READ 4 OVERFLOW AND 4 UNDERFLOW
                    ;BITS
OP      RC16,2       ;READ THEN CLEAR SCALER AND
                    ;OVERFLOW AND UNDERFLOW
OP      RC24,2       ;READ THEN CLEAR
OP      TLAM,8,15    ;TEST LAM, Q=1 IF LAM SET
OP      CL,9         ;CLEAR SCALER, OVERFLOW BIT, AND
                    ;UNDERFLOW BIT
;
OP      CLAM,10      ;CLEAR BIT J OF LAM SOURCE REGISTER
                    ;J=0-7
OP      WR24,16      ;WRITE SCALER (PRESET)
OP      DLAM,24,0    ;DISABLE LAM
OP      ELAM,26,0    ;ENABLE LAM
;

.SBTTL LECROY MODULES
;
; LR2226 - LECROY RESEACH MODEL 2226A QUAD TDC
MODULE LR2226,3      ;LECROY RESEARCH 2226A QUAD TDC
OP      RD16,0       ;READ REGISTER (TIME)
OP      RC16,2       ;READ AND CLEAR REGISTER
OP      CL,9         ;CLEAR REGISTER
                    ;MODULE IS BUSY FROM VALID START
                    ;"BUSY" IS CLEARED WIH FOURTH REGISTER
                    ;(A3)
;
; LR2228 - LECROY RESEARCH MODEL 2228 OCTAL TDC
;
MODULE LR2228,7      ;LECROY RESEARCH MODEL 2228 OCTAL TDC
OP      RD16,0       ;READ REGISTER (A0-7)
OP      RC16,2       ;READ AND CLEAR REGISTER, CLEARS BUSY
                    ;ON A7 ONLY
OP      TLAM,8       ;TEST LAM, Q=1 IF LAM PRESENT
OP      CL,9         ;CLEAR MODULE (AND LAM)
OP      CLAM,10      ;CLEAR LAM
OP      DLAM,24,12   ;DISABLE LAM
OP      STROBE,25    ;PUT 75 USEC
                    ;SPACING ON ALL INPUTS
OP      ELAM,26      ;ENABLE LAM
                    ;MODULE IS BUSY FROM VALID START
                    ;"BUSY" IS CLEARED WITH A(7)
;
; LR2243 - LECROY RESEARCH MODEL 2243A MULTI-MODE LINEAR ADC
;
MODULE LR2243,0      ;LECROY RESEARCH 2243A MULTI-MODE
                    ;LINEAR ADC
OP      RD16,0,0     ;READ ADC
OP      RC16,2,0     ;READ AND CLEAR
OP      CL,9,0       ;CLEAR

```

```

;
; LR2248 - LECROY RESEARCH MODEL 2248 OCTAL ADC
;
MODULE LR2248,7 ;LECROY RESEARCH 2248 OCTAL ADC
OP RD16,0 ;READ REGISTER (A0-A7)
OP RC16,2 ;READ AND CLEAR (A0-A7)
OP CL,9 ;CLEAR (A0-A7)
;
;
; LR2249 - LECROY RESEARCH MODEL 2249A 12 CHANNEL ADC
;
MODULE LR2249,13 ;LECROY 2249A 12-CHANNEL ADC
OP RD16,0 ;READ REGISTER (A0-A11)
OP RC16,2 ;READ AND CLEAR (A0-A11) CLEARS
;BUSY ON All ONLY
OP TLAM,8 ;TEST LAM, Q=1 IF LAM SET
OP CL,9 ;CLEAR MODULE AND LAM
OP CLAM,10 ;CLEAR LAM
OP DLAM,24 ;DISABLE LAM
OP STROBE,25 ;TEST FUNCTION
OP ELAM,26 ;ENABLE LAM
;
;
; LR2259 - LECROY RESEACH MODEL 2259 12-CHANNEL PEAK ADC
;
MODULE LR2259,13 ;LECROY 2259 12-CHANNEL PEAK ADC
OP RD16,0 ;READ REGISTERS (A0-A11)
OP RC16,2 ;READ REGISTERS AND CLEAR MODULE AND
;LAM, CLEARS ON All ONLY
OP TLAM,8 ;TEST LAM, Q=1 IF LAM SET
OP CL,9 ;CLEAR MODULE AND LAM
OP CLAM,10 ;CLEAR LAM
OP DLAM,24 ;DISABLE LAM
OP ELAM,26 ;ENABLE LAM
;
;
; LR2340 - LECROY RESEARCH MODEL 2340B 16-CHANNEL
;DISCR/COINCIDENCE REGISTER
;
MODULE LR2340,0 ;LECROY RESEARCH 2340B 16-CHANNEL
;DISCR/COINC REG
OP RD16,0,0 ;READ 16-BIT COINCIDENCE REGISTER
OP RC16,2,0 ;READ AND CLEAR REGISTER
OP CL,9,0 ;CLEAR REGISTER
;
;
; LR2341 - LECROY RESEARCH MODEL 2341S 16-CHANNEL COINCIDENCE
;REGISTER
;
MODULE LR2341,0 ;LECROY RESEARCH MODEL 2341S
OP RD16,0,0 ;READ 16-BIT COINCIDENCE REGISTER
OP RC16,2,0 ;READ AND CLEAR
OP CL,9,0 ;CLEAR

```

```

;
;
; LR2550 - LECROY RESEARCH MODEL 2550B QUAD 100 MHZ SCALER
;
MODULE LR2550,3      ;LECROY RESEARCH MODEL 2550B QUAD
                    ;100MHZ SCALER
OP      RD16,0      ;READ 16-BIT SCALER (A0-A3)
OP      RD24,0      ;READ 24-BIT SCALER (A0-A3)
OP      RC16,2      ;READ AND CLEAR 16-BIT SCALER (A0-A3)
OP      RC24,2      ;READ AND CLEAR 24-BIT SCALER (A0-A3)
OP      CL,9        ;CLEAR SCALER (A0-A3)
OP      INCR,25     ;INCREMENT SCALER (A0-A3)
;
;
; LR2551 - LECROY RESEARCH MODEL 2551 12-CHANNEL 100 MHZ SCALER
;
MODULE LR2551,13     ;LECROY RESEARCH MODEL 2551 12-CHANNEL
                    ;100MHZ SCALER
OP      RD16,0      ;READ 16-BIT SCALER (A0-A11)
OP      RD24,0      ;READ 24-BIT SCALER (A0-A11)
OP      RC16,2      ;READ AND CLEAR MODULE AND LAM, CLEARS
                    ;ON A(11) ONLY
OP      RC24,2      ;READ AND CLEAR MODULE AND LAM, CLEARS
                    ;ON A(11) ONLY
OP      TLAM,8      ;TEST LAM, Q=1 IF LAM SET
OP      CL,9        ;CLEAR ALL REGISTERS
OP      DLAM,24     ;DISABLE LAM
OP      ELAM,26     ;ENABLE LAM
;
;
; LR2700 - LECROY RESEARCH MODEL 2700 PCOS CONTROLLER
;
MODULE LR2700,0      ;LECROY 2700 PCOS CONTROLLER
OP      RD16,2      ;READ MEMORY AND ADVANCE TO NEXT WORD
OP      TLAM,8      ;TEST LAM (Q=1 IFF DATA PRESENT)
OP      CL,9        ;CLEAR MEMORY AND SHIFT REGISTERS.
                    ;RESETS LAM AND FRONT PANEL BUSY.
OP      CLAM,10     ;CLEAR LAM
OP      WR24,16     ;SERIALLY CLOCK TEST PATTERN INTO 7700
                    ;SHIFT REGISTERS.
OP      WC24,17     ;GENERATE START CONVERSION. (DOES NOT
                    ;APPEAR TO FOLLOW CAMAC STANDARD--
                    ;WATCH OUT!)
OP      DLAM,24     ;DISABLE LAM
OP      STROBE,25   ;SET DATA COMPLEMENT LATCH
OP      ELAM,26     ;ENABLE LAM
OP      TBUSY,27    ;TEST CONVERT COMPLETE (Q=1 IFF
                    ;COMPLETE)
;
;
;

```

```

.SBTTL NUCLEAR ENTERPRISES MODULES
;

```

; NE9060 - NUCLEAR ENTERPRISES ADC TYPE 9060

```
;
MODULE NE9060      ;ADC TYPE 9060
OP   RD16,0,0      ;READ ADC A(0)
OP   RC16,2,0      ;READ AND CLEAR
OP   TLAM,8,15     ;TEST LAM. Q=1 IF LS AND LE
OP   CLAM,10,0     ;CLEAR LAM AND 8-WORD STORE
OP   WR24,17,0     ;OVERWRITE CONTROL REGISTER
OP   DLAM,24,0     ;DISABLE LAM. INHIBIT CONVERSION
OP   ELAM,26,0     ;ENABLE LAM AND CONVERSION
;
;
;
```

.SBTTL STANDARD ENGINEERING MODULES

; SE0008 - STANDARD ENGINEERING MODEL TD-008 OCTAL TDC

```
;
MODULE SE0008,7    ;STANDARD ENGINEERING MODEL TD-008
                  ;OCTAL TDC
OP   RD16,0        ;READ REGISTER (A0-A7)
OP   RC16,2        ;READ AND CLEAR REGISTER
OP   TLAM,8,0      ;TEST LAM
OP   CL,9,0        ;CLEAR REGISTERS
OP   DLAM,24,0     ;DISABLE LAM
OP   ELAM,26,0     ;ENABLE LAM
;
;
;
```

; SE0100 - STANDARD ENGINEERING MODEL QS100 QUAD SCALER

```
;
MODULE SE0100,3    ;STANDARD ENGINEERING MODEL QS-100
                  ;QUAD SCALER
OP   RD16,0        ;READ SCALER (A0-A3)
OP   RD24,0        ;READ SCALER
OP   RC16,2        ;READ AND CLEAR SCALER
OP   RC24,2        ;READ AND CLEAR SCALER
OP   TLAM,8        ;TEST LAM
OP   CL,9          ;CLEAR SCALER
OP   CLAM,10       ;CLEAR LAM
;
;
;
```

; SE2027

```
;
MODULE SE2027
OP   WR24,16,0
OP   WC24,17,0
;
;
```

.SBTTL SPECIAL MODULES

; MPMUX4 - MP-1 4-IN DATA MUX

```
MODULE MPMUX4,3    ;MP-1 4-IN DATA MUX, DRAWING 63Y-149603
OP   RD16,0        ;READ REGISTER A (A=0,3)
```

```

OP      RC16,2      ;READ REGISTER A THEN CLEAR INPUT
                        ;PERIPHERAL A
OP      CL,9        ;CLEAR INPUT PERIPHERAL A
OP      DLAM,24     ;DISABLE PERIPHERAL UNIT A
OP      ELAM,26     ;ENABLE PERIPHERAL UNIT A
OP      TLAM,27     ;TEST "DATA READY" FROM UNIT A, Q=1 IF
                        ;"DATA READY"
;
;
; MPMWPC - MP-1 MULTIWIRE PROPORTIONAL CHAMBER ENCODER
;
MODULE MPMWPC,7      ;MP-1 MULTI-WIRE PROPORTIONAL CHAMBER
                        ;ENCODER
OP      RDMWPC,0     ;READ GROUP N UNTIL DONE SIGNIFIED BY A
                        ;ZERO DATA WORD. BUFFER = 9 WORDS.
                        ; N=1,8
OP      CL,9,0       ;RESET ALL MWPCS, SET TO ENCODER
                        ;ENCODER MODE
OP      CLAM,10,0    ;CLEAR LAM SOURCE
OP      RDOV,1       ;READ OVER EIGHT, CLEARS LAM SOURCE
OP      RD16,0,0     ;READ AND SHIFT
OP      DLAM,24,0    ;DISABLE LAM
OP      ELAM,26,0    ;ENABLE LAM
OP      TLAM,8       ;TEST LAM
;
;
; PACE 8 INTERFACE
;
MODULE PACE08,15
OP      RC24,0       ;ONLY A(0) FOR FIFO, A(N) FOR CHANNEL
                        ;MODE
OP      TLAM,8,0     ;TEST ENABLED LAMS
OP      WC24,17,13   ;WRITE 24-BIT LAM MASK FOR CHANNEL MODE
OP      CONV,25      ;RUN = A(0), HALT=A(1), FIFO=A(2),
                        ;CHANNEL=A(3), RESET REGISTERS=A(4)
OP      ELAM,26      ;FIFO MODE ONLY:
                        ;A(0) ENABLE FOR >0 WORD
                        ;A(1) ENABLE FOR >1 WORD
                        ;A(2) ENABLE FOR >3 WORDS
;;; OP      TBUSY,27,0 ;TEST HALF GRANT
                        ;Q=0 ACTIVE, Q=1 OTHERWISE
;
;TERMINATE LIST WITH TRIGGER MODULE
1$:
LAST: .WORD 0
      .WORD 1$-LAST
      .ASCII /MPTRIG/
      .WORD 3
; MPTRIG - MP-1 Q TRIGGER MODULE
;
MODULE MPTRIG,3      ;MP-1 Q TRIGGER MODULE
OP      RD16,0,0     ;READ HIGHEST PRIORITY CHANNEL NUMBER
OP      TLAM,8,0     ;TEST LAM, Q=1 IF LAM SET
OP      CLAM,10,0    ;CLEAR LAM

```


OP WR24,16

;WRITE:

;A0, TRIGGER CHANNEL N (N=5-BIT BINARY)

;A1, CLEAR CHANNEL N

;A2, SET CHANNEL MASK N

;A3, CLEAR CHANNEL MASK N

OP DLAM,24,0

;DISABLE LAM

OP ELAM,26,0

;ENABLE LAM

1\$:

.END

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