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**DEVELOPMENT OF COPPER SULFIDE/CADMIUM SULFIDE THIN FILM
SOLAR CELLS**

First Technical Progress Report, July 13—October 12, 1979

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February 14, 1980

Work Performed Under Contract No. EG-77-C-01-4042

Westinghouse R&D Center
Pittsburgh, Pennsylvania

DIST-231
NTIS-25

U.S. Department of Energy

R110

Solar Energy

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Price: Paper Copy \$5.00
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THIN FILM SOLAR CELLS

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First Technical Progress Report
13 July 1979 to 12 October 1979
Contract No. XJ-9-8143-1

February 14, 1980

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1. SUMMARY

Preparation of CdS films by evaporation from a single graphite source, as generally used by the Institute of Energy Conversion (IEC) group at the University of Delaware, has been implemented.

Previously at Westinghouse, four evaporation sources were used to permit uniform coverage of large area substrates. The graphite source used in this period is somewhat smaller than the IEC design to permit accommodation to the heater geometry currently available. Initial efforts with the single source evaporation have been on characterizing the thickness profiles of the deposited films. This is needed to permit selection of conditions for obtaining films of about 30 μm thickness over the central 4 cm x 4 cm area of the substrate.

Barrier processing according to the details of IEC method has been used on four-source CdS films. To date the best cells have only been about 1% efficient. Low short circuit current density values ($\sim 5 \text{ mA/cm}^2$) have been the biggest problem. Annealing in 6% H_2/Ar mixtures at 170°C after electrode grid evaporation generally has resulted in reduced values of J_{sc} .

Plans for the next period include the use of single source films for cell processing and the use of small area diode arrays to map cell performance parameters as a function of position on the substrate.

2. PROGRAM DESCRIPTION

2.1 Objective

The objective of this program is to produce copper sulfide/cadmium sulfide solar cells with conversion efficiency of 9% or greater. Specifically, effort is to be applied to duplicate the basic elements of the cell fabrication sequence used at the Institute of Energy Conversion (IEC) of the University of Delaware.⁽¹⁾ This will demonstrate the transferability of process steps which have resulted in 1 cm^2 cells of 9.15% efficiency.

2.2 Previous Results

In earlier work at Westinghouse, the Clevite wet-processing method was used to produce 4 cm^2 cells with maximum conversion efficiency of about 6.3%.⁽²⁾ The process used by IEC was generally similar, but on careful analysis, was found to differ in some important details. Specifically, in the IEC process, cadmium sulfide powder is thermally evaporated from a single graphite crucible. In the Westinghouse process, four identical quartz sources were used to allow greater thickness uniformity of the CdS deposit over a large area. Scanning Electron Microscope (SEM) studies of the topology of Cu_2S penetration into CdS films prepared by the two methods show characteristic differences. In the four source films, conventional processing (a texturing etch in HCl and barrier formation by immersion in CuCl solution) results in heavy pitting of the CdS film and very deep Cu_2S penetration along grain boundaries. For the single source of IEC, etch pitting is much less and the depth of Cu_2S penetration appears to be much less. The latter is consistent with higher open circuit voltage due to lower total diode opposing current from a smaller effective barrier area than that produced in the four source films.

In addition, the IEC process avoids high temperature air exposure of the cells after barrier formation. Instead, a sequence of annealing periods in a reducing ambient (containing CO or H₂) is used to form the Cu₂S/CdS barrier region. In the Westinghouse approach, a short high temperature (240°C) treatment in an air oven has been used.

Finally, the IEC cells have been made with evaporated gold grid electrodes contacting the Cu₂S layer (applied before the series of optimizing reduction anneal steps). An organic dielectric insulating film is applied to the cell surface prior to gridding to isolate the current collecting bus bar which is evaporated across the grid electrode fingers from the underlying Cu₂S layer. In the Westinghouse cells, a gold plates fine wire mesh was pressed against the cell surface for testing purposes. The nominal area of this contact was somewhat larger than that used by IEC.

2.3 Approach

The differences between IEC and Westinghouse cell fabrication details were judged to have first and second order influences on performance. Matters considered of most importance were the CdS film deposition method and its effect on grain size and the barrier interface topology, barrier formation and heat treatment details, and electrode grid contact preparation. Matters of second order importance were use of small area (1 cm²) cells, the role played by optical reflection of the back contact, consequences of spectral content of illumination, and cell packaging. These considerations were used in defining the content of Task 1 described below.

In considering the prospects for improving cell performance beyond 9%, a major unknown is the role played by the free surface and the grain boundary regions of the polycrystalline material. This includes matters such as the formation of the Cu₂S absorbing layer, the minority carrier transport properties within the layer, surface or grain boundary recombination mechanisms, and the electronic nature of the space charge region in the CdS adjoining the heterojunction.

Empirical and modelling efforts addressing these matters are treated in Task 2, discussed in the next section.

2.4 Program Tasks

Task 1 deals with processing and fabrication of cells of 9% conversion efficiency. Briefly the description of the subtasks includes:

Subtask 1.1. Implement single source CdS evaporation and characterize effects on grain size and barrier topology.

Subtask 1.2. Implement details of IEC barrier formation regarding wet processing and heat treatments.

Subtask 1.3. Implement evaporated gold grid electrode contacts using IEC designs for aperture masks on 1 cm^2 cells.

Subtask 1.4. Assess spectral sensitivity of cells with regard to details of Cu_2S formation, barrier heat treatment and back contact reflectivity.

Subtask 1.5. Prepare, evaluate and package demonstration cells.

Task 2 treats assessment of obtaining greater than 9% conversion efficiency in $\text{Cu}_2\text{S}/\text{CdS}$ cells.

Subtask 2.1. Empirically assess the roles played by grain boundary, crystal surface and processing influences on mechanisms determining photocurrent generation, transport and collection and on diode opposing current.

Subtask 2.2. Model and project performance of cell structures for various free surface and grain boundary conditions influencing optical behavior, photocurrent generation and transport, and diode opposing current.

3. PROGRESS TO DATE

3.1 CdS Film Preparation

One of the principal tasks of this program is the preparation of CdS films and cells using methods giving the highest reported cell efficiencies to date, as reported by the Institute of Energy Conversion (IEC).¹ Thus, work was started to deposit CdS films using a single evaporation source (a graphite source crucible) and the deposition sequence worked out by IEC. Prior to the start of the present contract, Westinghouse technical personnel visited IEC to obtain first-hand the details of the IEC process. Special graphite crucibles and the associated source heaters were ordered from the University of Delaware at that time, for availability early in the contract period. The graphite crucibles have been received, but the source heaters needed to be able to use these crucibles were not received during the first quarter. In lieu thereof, graphite crucibles capable of being used in the source heaters available at Westinghouse were designed, fabricated and evaluated.

Figure 1 shows the crucible design which was evolved and evaluated. The crucible has an integral collimation cone above the orifice. This section of the crucible extends above the surrounding source heater. A separate cylindrical heat shield for this section is needed to prevent excessive heat loss from the extended crucible. The bottom loading feature of this crucible is advantageous in two ways: no space needs to be left between the CdS charge and the quartz wool plug in the orifice — hence, more CdS can be charged and the quartz wool can be used repeatedly since it stays in place between runs.

When the graphite crucible was used in lieu of the quartz crucible in the single evaporation source configuration, the CdS films were too thin and the resulting cells were all short circuited. In an effort to increase the CdS film thickness, the source to substrate

Evaporation Crucible - Material Graphite, DFP-3-2

All Dimensions are in inches

Cylindrical - O. D. $.670 \pm .002$

I. D. $.480 \pm .005$

Orifice - Dia $.125$ to $.130$

Length $.100$ to $.120$

22 1/2° Conical Top Opening to Knife Edge Rim

Fig. 1 - Design of cylindrical graphite evaporation crucible

distance was reduced from 8-1/2" to 6". This was successful in increasing the CdS film thickness, at the center of the 3" x 3" (7.6 cm x 7.6 cm) film area from 23.1 μm to 37.6 μm . However, at the corners of the film, the thickness increased only slightly from 18.8 μm to 21.3 μm . This is considered to be too thin to secure unshort-circuited cells from the standard baseline process. Most of the cells processed from these films were indeed shorted, and the cells fabricated from the thicker center area were low in output.

Because of this experience, an intermediate source-to-substrate distance of 7-1/2" was chosen, and efforts were made to pack more CdS into the graphite crucible. By careful tamping, a total weight of 13.0 grams of CdS could be changed into the graphite crucible, as compared to 11.5 grams without tamping. (The quartz crucibles previously used would hold up to 14 grams.) Under these conditions, the CdS film at the center of the film area was 28.7 μm thick, and at the corners of the area it was 20.3 μm thick. Figure 2 shows the equal thickness contour lines measured for a typical CdS film deposited under these conditions using a substrate temperature of 220°C and a total deposition time of 17 minutes to empty the source.

Even with the efforts described, the cells fabricated from the films were low in output or internally short-circuited. As can be seen from Fig. 2, there is considerable variation in thickness across the area of these films. The previous experience in this laboratory on cells fabricated from films deposited in the multi-source evaporator was that the highest output cells were usually obtained from CdS films having a minimum variation in thickness across the film area — providing the films were over 30 μm in thickness. Conversely, films having the largest thickness gradients (due to uneven evolution from the multiple sources) gave the lowest output cells. In these cases, a specific mechanisms for the lowered cell output could not be ascribed. It is to be noted, that the thickness gradients in those earlier cases were substantially less than the best experience using the single source evaporation.

Fig. 2 — Thickness contours (mils) for a CdS film deposited using single source

One of the advantages of the multiple source evaporation process was that it yielded CdS films with usable areas of 6" x 6". The practice was to subdivide each film into 16 pieces 1-1/2" x 1-1/2" in size, to process an area of about 1-1/4" x 1-1/4" into a cell, and test the central 2 cm x 2 cm portion of each cell using a temporary pressed grid contact. The corners of the 3" x 3" films from the single source evaporator are thin and have to be avoided. Thus, only two cells of the 2 cm x 2 cm active area size could be processed from each such CdS film. In an effort to increase the number of cells that could be realized from each single source deposition film, the size of the cells were reduced to 1 cm x 1 cm active test area. This was done by subdividing each film into nine squares each 2 cm x 2 cm in size, processing the central 1-1/2 cm x 1-1/2 cm portion into cells, and testing the central 1 cm x 1 cm area with a temporary pressed grid contact.

It was found that the 1 cm x 1 cm active area cells gave appreciably lower indicated outputs than the 2 cm x 2 cm active area cells. Table I shows the output data for 7 different cells (all processed from CdS films deposited in the multi-source evaporator) tested using a temporary pressed grid contact — first using 1 cm x 1 cm active area, and then 2 cm x 2 cm active area. It is seen that the larger area cells all had indicated higher values of V_{oc} , J_{sc} , η and fill factor as well as higher shunt resistances. It was reasoned that this artifact of the testing procedure probably arose from a less effective grid contact for the smaller area cells. This occurs since the pressure test rig works with the cell being forced through a window opening in an opaque mask onto the grid using pneumatic pressure on an underlying rubber diaphragm. It was reasoned that the diaphragm and cell would be less compliant over the smaller area. This indeed proved to be the case. When the pneumatic pressure was increased from 100 psi to 150 psi, the indicated output from the 1 cm² area cells rose to nearly the same value as for the 4 cm² area cells. However, when the increased pressure was applied to the 4 cm² area cells, no increase in indicated output was recorded. From this result, it is clear that 100 psi is adequate

TABLE I
CELL TEST - PRESSURE TEST RIG
4 cm² ACTIVE TEST AREA vs. 1 cm² ACTIVE TEST AREA

Cell No.	Date	OCV		J		EFF		F.F.	
		4 cm ²	1 cm ²	4 cm ²	1 cm ²	4 cm ²	1 cm ²	4 cm ²	1 cm ²
655-12	8-29	.459	.459	18.0	18.0	5.6	5.1	68.0	61.0
657-9		.482	.482	18.0	17.4	5.2	4.6	60.0	54.4
654-9		.445	.441	16.4	15.1	4.6	3.9	62.9	57.8
655-10		.453	.453	19.4	18.7	5.8	5.0	65.5	58.9
656-4		.473	.470	17.4	16.3	5.2	4.2	63.5	54.8
657-5		.469	.462	16.8	17.1	4.2	3.5	53.1	44.3
657-13		.458	.454	18.8	16.0	4.4	3.4	51.7	46.8
Average		.463	.460	17.8	16.9	5.0	4.2	60.7	54.0

pressure for the larger area cells. Thus, the 150 psi pressure has been adopted as standard for testing 1 cm x 1 cm cells with the temporary pressed grid contact.

3.2 Barrier Formation and Cell Gridding

Due to the running-in effort required for CdS depositions using the single graphite sources, CdS films from such depositions were not available for barrier formation work during the first quarter. Instead, CdS films produced earlier by simultaneous depositions from four quartz crucibles have been used. This work was pursued primarily to provide experience in the timing and sequencing of the various steps in barrier formation.

Two types of barrier formation treatment were used for comparison. These, referred to as Type W (for the former method used at Westinghouse) and Type D (for the method used by the IEC group at the University of Delaware) are described in Table II.

Table II Post Deposition Etching and Dipping Details		
	Type W Processing	Type D Processing
Etch CdS	2:1 HCl in water 45°C 7 sec	55% HCl 60°C 2 sec
Rinse	None	DI water, 2 beakers
Cu ₂ Cl Dip	15g Cu ₂ Cl 15g NaCl per l of water 6 sec	6g Cu ₂ Cl 2g NaCl per l of water 10 sec
Rinse	DI water, cascade	DI water, 3 beakers + cascade

Four cells were fabricated by the type D process using a CdS film from the same four-source evaporation. Fortin dielectric insulating films were laminated to the Cu₂S surface in an air oven, 1 hr at 160°C.

A gold bus bar stripe had been earlier evaporated on the Fortin. After electrode grid evaporation, the cells were tested, giving the results shown in Table III. Although values of V_{oc} were nearly identical for the cells, short circuit current values were low and variable, as were the values of fill factor. Two of the cells 599-5-B and 599-5-D were subsequently annealed in an ambient of flowing 6% H_2/Ar . In both cases, short circuit current values declined significantly as a result of annealing, as shown by the data in Table IV.

Table III Characteristics of Four 1 cm^2 Cells Made by Type D Processing, Followed by Fortin Lamination at 160°C in Air and by Gold Grid Evaporation				
Cell No.	V_{oc} (V)	J_{sc} (mA/cm ²)	Fill Factor	η (%)
599-5-A	0.400	1.4	0.33	0.2
599-5-B	0.405	4.0	0.53	0.9
599-5-C	0.400	4.7	0.39	0.7
599-5-D	0.405	5.3	0.29	0.6

Table IV Changes in Photovoltaic Characteristics of Two Typical Cells, Processed as Described in Table III, as a Function of Total Anneal Time at 170°C in Flowing 6% H_2/Ar					
Cell No.	Total Anneal Time (hr)	V_{oc} (v)	J_{sc} (mA/cm ²)	f.f.	η (%)
599-5-B	0	0.405	4.0	0.53	0.9
	7.25	0.430	1.55	0.45	0.3
	17.5	0.425	1.56	0.45	0.3
	33.0	0.488	0.25	0.47	0.05
599-5-D	0	0.405	5.3	0.29	0.6
	17	0.440	2.2	0.46	0.4
	33	0.395	0.39	0.72	0.1

Another four cells using the same CdS substrate deposition were fabricated using the type W process of Table II. They were similarly provided with a Fortin dielectric film (laminated with H₂ for 1 hr @ 160°C) containing a gold bus bar. After the gold grid electrode evaporation, the cell performance results shown in Table V were obtained. Short circuit current and open circuit voltage values were somewhat higher than for cells of Type D processing, although fill factor values were generally poorer. As in the case of Type D cells, annealing at 170°C in 6% H₂/Ar resulted in poorer cell performance as shown in Table VI.

Table V Characteristics of Four 1 cm ² Cells Made by Type W Processing, Followed by Fortin Lamination for 1 hr at 160°C in H ₂ and Gold Grid Evaporation				
Cell No.	V _{oc} (v)	J _{sc} (mA/cm ²)	Fill Factor	η (%)
599-7-A	0.428	10.0	0.35	1.5
599-7-B	0.425	9.5	0.35	1.4
599-7-C	0.428	7.6	0.34	1.2
599-7-D	0.430	9.8	0.34	1.5

Table VI Changes in Photovoltaic Behavior of a Typical Cell (599-7-A) Prepared by Type W Processing as a Function of Total Anneal Time at 170°C in Flowing 6% H ₂ /Ar				
Total Anneal Time (hr)	V _{oc} (v)	J _{sc} (mA/cm ²)	f.f.	η (%)
0	0.428	10.0	.35	1.5
3.5	0.435	6.1	.43	1.2
11.0	0.445	6.0	.39	1.1
18.0	0.440	6.4	.46	1.3
23.0	0.435	5.1	.44	1.0

At this stage, we are not able to judge the significance of the difference between Type D and Type W processing for CdS films prepared by the four source evaporation method. A fifth cell from the same CdS substrate, prepared by the type W process, was given a 2 min, 250°C air heat treatment and tested with a temporary pressed grid electrode. This cell had a much higher fill factor (0.61), comparable value of J_{sc} (9.3 mA/cm²) and slightly lower open circuit voltage than the cells of Table V. This suggests that the four-source CdS films prepared earlier at Westinghouse cannot be optimized by Type D processing and hydrogen annealing of the type developed by IEC. During the next quarter, results of using CdS films prepared by single source evaporation will be explored.

4. PLANS FOR THE NEXT QUARTER

Work will continue on use of the single graphite evaporation source to prepare CdS films. Barrier processing and heat treatment will be done using single source CdS films. Formation of small area test diodes in linear and x-y arrays will be explored as a means of mapping position dependence of photovoltaic parameters.

5. REFERENCES

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