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**AUTOMATED ARRAY ASSEMBLY TASK
DEVELOPMENT OF LOW-COST POLYSILICON SOLAR CELLS**

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By
Kimberly L. Allison
Gregory T. Jones
Sang S. Rhee
Sanjeev R. Chitre

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Sensor Technology, Inc.
Chatsworth, California

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PREFACE

The information presented in this report on the Production Process and Equipment Development Area (formerly Automated Array Assembly Task) represents work performed from July 1979 through December 1979 by Sensor Technology, Inc., in Chatsworth, California. This program is directed by Sang S. Rhee. Principal contributors include Kimberly L. Allison, Gregory T. Jones and Sanjeev Chitre.

The JPL Technical Program Manager is Dale Burger.

ABSTRACT

Three types of polysilicon materials were experimentally evaluated with Sensor Technology's standard production processing sequence, during this reporting period. These materials include Wacker, Crystal Systems, and Exotic Materials polysilicon wafers. The average crystal grain size in the three polysilicon materials was obtained by statistically averaging the longest and shortest dimensions of each crystal grain in a set of random grain size measurements.

An equation was derived to compute the fractional power loss associated with insufficient gridline coverage of polysilicon crystal grains. Two numerical examples are provided to illustrate the use of the fractional power loss equation in determining the suitability of the gridline spacing in a particular polysilicon grid pattern design.

Other processes were explored for the purpose of improving the polysilicon solar cell efficiencies. Several metallization techniques were examined for suitability with a spray-on-dopant junction formation process sequence. A metallization problem was incurred in this program with cause and solution yet to be determined.

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INTRODUCTION

The production of low-cost, large area, high efficiency polysilicon solar cells is the overall goal of this program. The major tasks which comprise this project include: (1) development of a low-cost polysilicon solar cell process sequence which achieves ten percent (10%) efficient large area polysilicon solar cells in batch quantities, (2) development of a front surface grid pattern optimized with respect to crystal grain size, (3) investigation of a polysilicon wafer surface macrostructure or texturizing process suitable for large scale production, (4) study of junction formation techniques, (5) investigation of anti-reflective coatings suitable for polysilicon solar cells, and (6) exploration of other processes, as necessary, to obtain high efficiency or low-cost polysilicon solar cells.

Work was performed this quarter in the following areas: (1) experimental evaluation of the three types of polysilicon materials using Sensor Technology's standard single crystal production processing sequence, (2) determination of the average crystal grain sizes in three types of polysilicon material, (3) derivation of an equation to compute the fractional power loss associated with insufficient

gridline coverage of crystal grains, and (4) numerical examples illustrating the use of the fractional power loss equation in determining the suitability of the gridline spacing in a particular polysilicon grid pattern design, and (5) exploration of several metallization techniques for suitability with a spray-on dopant junction formation process sequence.

TECHNICAL DISCUSSION

A. Brief Description of Polysilicon Material

Three types of large area polysilicon wafers were investigated this quarter. The polysilicon material vendors include: Wacker Chemical Corporation from Santa Clara, California, Crystal Systems, Inc., from Salem, Massachusetts and Exotic Materials, Inc., from Costa Mesa, California.

The Wacker polysilicon wafers are 3.94 in x 3.94 in (10 cm x 10 cm) square and 18 mil (.457 mm) thick. A picture of a typical solar cell made from Wacker material is shown in Figure 1. The polysilicon wafer material has a coarse grain structure with varying crystal grain sizes. The average crystal grain size for this sample lot was found to be 0.16 inches. See section D1 and E2 for more details.

Two types of Crystal System material grown with the Heat Exchanger Method were procured. The first type is 100% single crystal silicon (non polysilicon) a part of the same ingot as the polysilicon second type. The second type is 44% single crystal silicon and 56% polysilicon. These wafers are characterized by a single crystal circular region, surrounded by predominantly large crystal grains. Small crystal grains lie at the boundary between the single crystal region and the large grain polysilicon region. Pictures

of the solar cells made from the two types of Crystal System material are shown in Figures 2 and 3. The wafers are 3.44 in x 3.94 in (10cm x 10cm) square and 20 mil (.508 mm) thick. A discussion of the crystal grain size measurements are given in section D 2.

The Exotic Materials wafers are 4.0 inches (10.16 cm) round and 25 mil (.635 mm) thick. A picture of a typical solar cell made from the fast pull (Czochralski) polysilicon is shown in Figure 4. The polysilicon wafer material is similar in general appearance to the Wacker material and also has a coarse grain structure with varying crystal grain size. The average crystal grain size for this sample lot was found to be 0.16 inches. See section D3 for more details.

B. Baseline Processing Sequence

The three types of polysilicon material were processed according to the baseline processing sequence in Figure 5. This process sequence is used in the production of our single crystal 4 inch diameter solar cells. In the experiments discussed in this report the options indicated in the flow diagram were not utilized. The sole exception was the surface macro-structure process (two stage standard NaOH texturizing process). The solar cells had the silicon glass removed but no anti-reflective coating applied.

FIGURE 1: Polysilicon solar cell made from Wacker material and electrical performance curve.

FIGURE 2: Polysilicon solar cell made from Crystal System's HEM material and electrical performance curve. Degree of single crystallinity is 100%.

FIGURE 3 : Polysilicon solar cell made from Crystal System's HEM material and electrical performance curve. Degree of single crystallinity is 44%.

Figure 4: Polysilicon solar cell is made from Exotic Material's material and electrical performance curve.

FIGURE 5: Block diagram of the baseline processing sequence for polysilicon solar cells.

C. Electrical Performance Characteristics

The electrical performance characteristics for typical Wacker, Crystal Systems and Exotic Materials solar cells, which were made from the baseline process sequence discussed above, are represented in Figure 1, 2 and 3, and 4 respectively. The Wacker material and the two types of Crystal System material were processed in the same batch for comparison. The Exotic Materials cells were processed in separate batches using the same baseline process sequence. The short circuit currents for the Wacker material and single crystal Crystal System material are nearly the same (2.45 amps) while the open circuit voltage of .520 volts and .550 volts respectively, differ significantly. It appears from the data that the open circuit voltages for the three types of polysilicon material vary from .515 volts to .530 volts, which is significantly less than the open circuit voltage for single crystal material.

The average efficiencies (η) and fill factors (FF) of the three large area polysilicon materials obtained with the baseline fabrication sequence (no A.R. coating) are listed below:

- (1) Wacker: $\eta = 8.5\%$, $FF = .659$
- (2) Crystal System: $\eta = 8.9\%$, $FF = .632$
(100% single crystallinity)
 $\eta = 5.1\%$, $FF = .556$
(44% single crystallinity)
- (3) Exotic Materials: $\eta = 7.2\%$, $FF = .670$

The data indicates that the Wacker polysilicon solar cells perform significantly better than the other two types of polysilicon solar cells. Crystal Systems single crystal solar cells which were made with their HEM process, performed slightly better than the Wacker cells processed in the same batch.

D. Crystal Grain Size Measurements

A study was conducted to determine the average crystal grain size in Wacker, Crystal Sytems, and Exotic Materials polysilicon wafers. A discussion of the measurement technique and results for the three polysilicon materials follows.

The average crystal grain size, d_g , in a sample lot of 4" x 4" Wacker polysilicon wafers was computed on the basis of a statistical analysis of crystal grain size measurements. A total of 200 individual grains was measured from a random sampling of grains in four polysilicon wafers. A complete measurement consisted of visually measuring both the longest and shortest grain dimensions. After the completion of two hundred

such measurements, the average crystal grain size, d_g , was computed from the statistically averaged values of the longest and shortest grain dimensions (d_l , and d_s , respectively), i.e:

$$d_l = 0.212 \text{ inch}$$

$$d_s = 0.105 \text{ inch}$$

$$d_g = \frac{1}{2} (d_l + d_s) = 0.16 \text{ inch}$$

The average crystal grain size for the Wacker polysilicon material examined in this study was found to be 0.16 inches.

The size distribution of crystal grains in a typical Crystal Systems wafer which is partly polysilicon was investigated. This wafer is characterized by a 100% single crystal circular region, surrounded by predominantly large crystal grains. Small crystal grains lie at the boundary between the single crystal region and the large grain polysilicon region. A total of 50 random small crystal grain size measurements was obtained from a typical Crystal Systems wafer, by visually measuring both the longest and shortest grain dimensions. The statistically averaged value of the longest and shortest grain dimensions are listed below:

$$d_l = 0.095 \text{ inch}$$

$$d_s = 0.057 \text{ inch}$$

$$d_g = 0.076 \text{ inch}$$

The average small crystal grain size for the Crystal Systems wafer examined in this study was 0.076 inches. The percentage of active area contained by the small crystal grain region is approximately 5%.

The average crystal grain size, d_g , in a typical Exotic Materials polysilicon wafer was computed on the basis of a statistical analysis of fifty randomly selected crystal grains. The statistically averaged longest and shortest grain dimensions (d_l and d_s , respectively) were utilized to compute the average crystal grain size, i.e.:

$$d_l = 0.210 \text{ inch}$$

$$d_s = 0.108 \text{ inch}$$

$$d_g = \frac{1}{2} (d_l + d_s) = 0.16 \text{ inch}$$

The average crystal grain size for the Exotic Materials wafer examined in this study was 0.16". This value is identical to the average crystal grain size obtained for Wacker material.

E. Fractional Power Loss Due to Insufficient Gridline Coverage of Polysilicon Crystal Grains

A study was conducted to identify the necessary criteria which must be satisfied to optimize the gridline spacing for polysilicon solar cells. An important criterion identified earlier (see the first quarterly report), is

that the spacing between successive gridlines must be less than the average crystal grain size, in order to avoid power losses due to insufficient gridline coverage of the polysilicon crystal grains. A generalized equation for computing the fractional power loss is derived below followed by a numerical example and a discussion of results.

1. Generalized Equation for Computing the Fractional Power Loss

The derivation of a generalized equation for computing the fractional power loss due to insufficient gridline coverage of polysilicon crystal grains resides in four assumptions which are listed below:

- (1) All crystal grains within a given grain size distribution are randomly distributed throughout the polysilicon wafer.
- (2) All crystal grains are square.
- (3) All crystal grains are aligned so that two sides of each grain are parallel to a gridline.
- (4) All crystal grains not contacted by a gridline have zero power output.

Consider a succession of parallel gridlines in a polysilicon sample, each with a width of t_0 and a spacing between center lines of s . Attention will now be focused on a set of two parallel gridlines and a one dimensional coordinate system used for reference to indicate the random location, x , of the "i"th crystal grain of size g_i , as shown in Figure 6. On the basis of assumption (1) the midpoint of a crystal grain of size g_i is equally likely to be located at any point between $x = 0$ and $x = s$ in Figure 6. The probability that the i th crystal grain will contact a gridline can now be determined.

There are three regions in Figure 6 in which the midpoint of the i th crystal grain can be located. If the midpoint of the i th crystal grain is located anywhere along the x-axis in Region I or III the i th crystal grain will touch a gridline. If the midpoint of the ith crystal grain is at any location along the x-axis in Region II the ith crystal grain will not touch a gridline. Thus, the three regions locating the midpoint of the ith crystal grain are represented as follows:

$$\text{Region I} \quad 0 \leq x \leq (g_i + t_0) / 2$$

$$\text{Region II} \quad (g_i + t_0)/2 < x < s - (g_i + t_0)/2$$

$$\text{Region III} \quad s - (g_i + t_0) / 2 \leq x \leq s$$

Figure 6. A depiction of the three regions between two parallel grid lines where the midpoint of the i th crystal grain may be located within a distance of $x = 0$ to $x = s$.

From the above discussion, it is clear that the fractional length of s for which the i th crystal grain may contact a gridline is just the summation of the x distances in region I and III divided by s which is $(g_i + t_o)/s$. This fractional length represents the probability that the i th square crystal grain of size g_i will hit a gridline within a distance S between the center lines of two parallel gridlines.

The probability that the i th square crystal grain of size g_i will not hit a gridline is given by $1 - (g_i + t_o)/s$.

It follows that for an arbitrary crystal grain of size g_i , where $g_i + t_o \geq s$, this grain will touch a gridline with 100% probability. On the other hand, for an arbitrary crystal grain of size g_i , where $g_i + t_o < s$, there is a probability that this grain will not hit a gridline.

The probability of the i th crystal grain not hitting a gridline implies the existence of a power loss or the basis of assumption (4), which assumes zero power output from a crystal grain not contacted by a gridline. Since the power output of a given crystal grain of area g_i^2 is directly proportional to its area, the fractional power loss, g , in a distribution of grain sizes due to crystal grains of size $g_i < s - t_o$ not hitting gridlines is given by:

$$q = \left(1 - \frac{g_i + t_o}{s} \right) \frac{g_i^2 n_i}{A}$$

where:

g_i^2 = area of i th crystal grain

$\left(1 - \frac{g_i + t_o}{s} \right)$ = probability of
 i th crystal grain not hitting a
 gridline.

n_i = number of grains with area g_i^2
 in a given grain size
 distribution

A = the total area encompassed
 by all grains in a given grain
 size distribution

If there are a total of "K" different grain sizes in a particular crystal grain size distribution, for which $g_i < s - t_o$, $i = 1$ to K , the fractional power loss, Q , in this crystal grain size distribution, due to all grains of size g_i ($i = 1$ to K) is given by:

$$Q = \frac{1}{A} \sum_{i=1}^K \left(1 - \frac{g_i + t_o}{s} \right) g_i^2 n_i \quad \text{Eq. (1)}$$

This result may be used to compute the fractional power loss in a polysilicon solar cell due to insufficient gridline coverage of those crystal grains for which $g_i < s - t_o$. If the fractional power loss Q , is significant, this is an indication that the gridline spacing, s , is not optimized. Two numerical examples illustrating

the application of this equation to a gridline spacing sensitivity analysis of a polysilicon grid-pattern design are presented in the next section.

2. Fractional Power Loss Calculations for Two Gridline Spacings in Wacker Polysilicon Solar Cells

a) Determination of Crystal Grain Size Distribution

The crystal grain size distribution in a given polysilicon material must be determined prior to calculating the fractional power loss for a given grid-pattern design. In this study four sample Wacker polysilicon wafers were chosen. Two hundred crystal grains were measured (g_i), grouped (ith group) and counted (n_i). The total area of the sample (A) was determined. The average crystal grain size was computed. These data are given in Table 1. The average crystal grain size for the Wacker polysilicon material was found to be 0.16 inches. It was assumed for convenience that the crystal grain size distribution obtained from these measurements is characteristic of the grain size distribution in the Wacker polysilicon wafer material.

b) Gridline Spacing for Minimal Fractional Power Loss

The gridline spacing, s , and width, t_0 , for the solar cells made from Wacker polysilicon material

Table 1. Data for determining crystal grain size distribution in Wacker polysilicon wafer material.

Group $i = 1 \text{ to } K$	Grain Size g_i (inches)	Number n_i	Area $g_i^2 n_i$ (in ²)	Total Grain Size $g_i n_i$ (inches)
1	.07	1	.0049	.07
2	.08	8	.0512	.64
3	.09	6	.0486	.54
4	.10	10	.1000	1.00
5	.11	11	.1331	1.21
6	.12	14	.2016	1.68
7	.13	16	.2704	2.08
8	.14	16	.3136	2.24
9	.15	31	.6975	4.65
10	.16	7	.1792	1.12
11	.17	12	.3468	2.04
12	.18	11	.3564	1.98
13	.19	5	.1805	.95
14	.20	8	.320	1.60
15	.21	17	.7497	3.57
16	.22	3	.1452	.66
17	.23	3	.1587	.69
18	.24	3	.1728	.72
19	.25	10	.6250	2.50
20	.26	3	.2028	.78
21	.27	4	.2916	1.08
22	.28	1	.0784	.28
TOTAL NUMBER		200	--	32.08
Sample Area			5.63	
Average Grain Size				0.16

are 0.125 inches and 0.010 inches respectively as shown in Figure 7. The only crystal grain sizes which have a probability of not hitting a gridline in this case are for those grains where $g_i < s - t_0$ or $g_i < 0.115$ inches. Within the two hundred random crystal grain size measurements, there was a total of 36 crystal grains which fell into this category. These 36 crystal grains were divided into five groups (i.e. $K = 5$) ranging in size from 0.07 inches to 0.11 inches. The contribution of each group to the fractional power loss, Q , (in the 200 crystal grains) is tabulated in Table 2.

The fractional power loss, Q , was found to be 0.77%. For this case, the power loss associated with insufficient gridline coverage of polysilicon crystal grains is minimal. This result shows that a 0.125 inch gridline spacing is close to the optimum value for Wacker polysilicon material.

c) Gridline Spacing for Significant Fractional Power Loss

The fractional power loss Q is a significant factor to consider for gridline spacing optimization. For example, consider a gridline pattern with spacing s

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FIGURE 7: Gridline Pattern For Wacker Polysilicon Solar Cells.

Table 2. Summary of the contributions of all crystal grains to the fractional power loss Q for $g_i < s - t_o = 0.115$ inches in Wacker polysilicon material.

ith Group	g_i	n_i	$\frac{g_i + t_o}{s}$	$1 - \frac{g_i + t_o}{s}$	$\left(1 - \frac{g_i + t_o}{s}\right) g_i^2 n_i$
1	.07	1	.64	.36	.0018
2	.08	8	.72	.28	.0143
3	.09	6	.80	.20	.0097
4	.10	10	.88	.12	.0120
5	.11	11	.96	.04	.0053
TOTAL					.0431 in ²

$$Q = \frac{1}{A} \sum_{i=1}^5 \left(1 - \left(\frac{g_i + t_o}{s} \right) \right) g_i^2 n_i = \frac{.043}{5.63} = 0.77\%$$

$A = 5.63 \text{ in}^2$ (Area of 200 sampled crystal grains)

$s = 0.125 \text{ in}$

$t_o = 0.010 \text{ in}$

$(g_i)_{\text{max}} = 0.11 \text{ in}$

$(g_i)_{\text{min}} = 0.07 \text{ in}$

$K = 5$

and width t_0 equal to 0.17 inches and 0.010 inches respectively for the Wacker polysilicon material above. The only grain sizes which provide nonzero contributions to the fractional power loss Q , are those for which $g_i < s - t_0$ or $g_i < 0.16$ inches. Of the two hundred random crystal grain size measurements, 113 crystal grains fell into this category. These 113 crystal grains were divided into nine groups (i.e., $K = 9$) ranging in size from 0.07 inches to 0.15 inches. The contribution of each group to Q is tabulated in Table 3. The final value of Q for this case is 5.30%, which indicates that for $s = 0.17$ inches, a significant power loss may occur due to insufficient gridline coverage of the crystal grains.

F. Other Processes

1. Spray-on Dopant Junction Formation

A processing sequence was identified last quarter which yielded 10% efficient 4" x 4" Wacker polysilicon solar cells in batch quantity. This process sequence utilized texturizing, gettering, n^+ spray-on dopant junction formation, nickel plating and SiO AR coating.

Table 2. Summary of the contributions of all crystal grains to the fractional power loss Q for $g_i < s - t_o = 0.160$ inches in Wacker polysilicon material.

ith Group	g_i	n_i	$\frac{g_i + t_o}{s}$	$1 - \frac{g_i + t_o}{s}$	$\left(1 - \left(\frac{g_i + t_o}{s}\right)\right) g_i^2 n_i$
1	.07	1	.47	.53	.003
2	.08	8	.53	.47	.024
3	.09	6	.59	.41	.020
4	.10	10	.65	.35	.035
5	.11	11	.71	.29	.039
6	.12	14	.76	.24	.048
7	.13	16	.82	.18	.049
8	.14	16	.88	.12	.038
9	.15	31	.94	.06	.042
				TOTAL	.298 in ²

$$Q = \frac{1}{A} \sum_{i=1}^9 \left(1 - \left(\frac{g_i + t_o}{s} \right) \right) g_i^2 n_i = \frac{.298}{5.63} = 5.30\%$$

$A = 5.63 \text{ in}^2$ (Area of 200 sampled crystal grains)

$s = 0.17 \text{ in}$

$t_o = 0.010 \text{ in}$

$(g_i)_{\text{max}} = 0.15 \text{ in}$

$(g_i)_{\text{min}} = 0.07 \text{ in}$

$K = 9$

Efforts were directed this quarter toward achieving similar spray-on dopant solar cell process results for Crystal Systems and Exotic Materials polysilicon. Good results were not achieved due to a serious metallization problem encountered over the course of this study.

It was apparent that some surface contamination, metallization technique, errors, etc., were responsible for the poor metallization. Avenues were explored to try to resolve this problem.

2. Metallization Study

Initial spray-on dopant experiments with Crystal System polysilicon material clearly indicated a serious metallization problem. The gold/nickel metallization did not adhere to the polysilicon surface, readily peeling off. Similar experiments were performed with single crystal wafers that confirmed the problem.

The initial approach to the metallization problem dealt with silicon surface contamination. After the spray-on dopant driven step, the phosphor glass and any excess dopant material are usually removed in an HF solution. The first experiments etched the phosphor glass longer in the HF solution and followed this procedure with surface scrubbing with a nylon tipped brush

to remove any excess dopant material. No metallization adherence improvement was observed. The second experiments cleaned the polysilicon surfaces with sulphuric acid and hydrogen peroxide solutions. The nickel plating still did not hold. A thick layer of gold and nickel was plated to improve adhesion. The presence of the gold did not improve the plating results. Sintering the gold did not improve the results. The metallization readily peeled off the polysilicon surfaces.

A second approach to the metallization problem dealt with the use of plated nickel without gold. The first experiments plated nickel without gold followed by resist removal in an ultrasonic bath. Except for some spots along the main gridlines the nickel came off the silicon surface along with the resist material. The second experiments sintered the nickel at 450°C for 10 minutes prior to the resist removal. The nickel adhered to the polysilicon surface, however, the resist material also adhered to the silicon surface and could not be removed easily.

A third metallization scheme utilized a print-on nickel paste. The nickel paste, Conductrox 5517, was procured from Thick Film Systems, Inc., Santa Barbara, California. The nickel was sintered in 50°C steps from 400°C to 700°C for 25 seconds and 60 seconds in an air atmosphere. It was also sintered at 400°C and at 600°C from zero to fifteen minutes in an air

atmosphere. The nickel did not adhere in any of the experiments. These results indicated that the nickel had a high temperature melting frit (the temperatures tried were too low). One experiment was tried at 850°C. The nickel adhered to the silicon surface, but also penetrated the p-n junction. The air fired nickel formed an oxide which was hard to solder. The sintering temperature, time, and oxide problems need to be resolved. It is recommended that more work be done with this metallization scheme and also that experiments be performed to electro-deposit copper onto the nickel to replace the solder.

The fourth and last metallization scheme studied this quarter dealt with print-on silver paste. The silver paste, Conductrox 3347 was procured from Thick Film Systems Inc., Santa Barbara, California. It was printed onto four inch diameter spray-on doped Exotic Materials polysilicon wafers and sintered for 45 seconds at 700°C. The silver migrated into the crystal grain boundaries and increased the shunting effects. Silver adhesion was fairly good. At the same sintering temperature, but for a shorter time (25 sec), the silver did not adhere to the polysilicon surface. More experiments with printed silver at higher temperatures and shorter times are needed. The silver frit should melt faster without as much migration. Additional investigation on the sintering

of metals in polysilicon material to determine segregation characteristics is recommended.

CONCLUSIONS AND RECOMMENDATIONS

The work performed on the development of low cost polysilicon solar cells during this quarter has led to a number of conclusions and recommendations. The electrical performance data (I-V curves) indicate that the Wacker polysilicon solar cells perform significantly better than the Crystal Systems and Exotic Materials polysilicon solar cells which were evaluated with Sensor Technology's standard (single crystal) solar cell production process sequence. The Crystal Systems single crystal solar cells, which were made with their HEM process, performed slightly better than the Wacker polysilicon solar cells processed in the same batch.

A theoretical analysis of the fractional power loss showed that a 0.125 gridline spacing is close to the optimum value for Wacker polysilicon coarse grain material. The fractional power loss was computed to be 0.77% for the Wacker polysilicon solar cells with 0.16 inch average crystal grain size and with a gridline spacing of 0.125 inches and width of 0.010 inches. The calculations also showed that fractional power loss is a significant factor to consider for gridline spacing optimization.

Experimental results with spray-on doped polysilicon solar cells did not compare with the good results achieved last quarter which was due to a serious metallization problem. It was apparent that some surface contamination, metallization technique, errors, etc., were responsible for the poor metallization. Plated gold/nickel, plated nickel, printed nickel and printed silver metallization schemes were all found to be unsatisfactory at this time. The cause of the metallization problem was not resolved this quarter.

It is recommended that more work be done on the printed nickel metallization scheme and that experiments be performed to electro-deposit copper onto the nickel. Additional investigation on the sintering of metals in polysilicon material to determine segregation characteristics is recommended.

PROGRESS SUMMARY AND PROGRAM PLAN

The progress summary and program plan for the Development of Low-Cost Polysilicon Solar Cells is given in the milestone chart in Table 4. The program was extended three months. Work will continue on the metallization scheme as funds allow. More polysilicon solar cells are planned for production with POCl_3 diffusion and electroless gold/nickel plating. A complete overhaul of the spray-on dopant equipment to eliminate any system contaminants will be scheduled. Experiments with spray-on dopants and AR coatings will be performed.

Table 4. Milestone Chart for Development of Low-Cost Polysilicon Solar Cells

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