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SLIFER Decipher

Dale R. Breeding, Gordon S. Worthen, John J. Loukota,
Don Fogel, John P. Watterberg

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SLIFER DECIPHER

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ABSTRACT

This manual describes the design, operation, and performance characteristics of the SLIFER Decipher used by Sandia Laboratories to record the SLIFER data from underground nuclear tests.

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SLIFER DECIPHER

1. Introduction

The SLIFER Decipher (SD) is a digital instrument that records a time-varying frequency signal in the range from 700 kHz to 1500 kHz with an amplitude greater than 200 mV. This signal is referenced to an input fiducial marker. The primary purpose of this instrument is to reduce data recorded on magnetic tape from the SLIFER system.*

The SD records 512 samples after the fiducial signal, with a sample interval of 50 μ s (for a total recording time of 25.55 ms). The measurement essentially uses a 20-cycle period-averaging counter technique.

Figure 1-1 shows a front view of the SD, and Figure 1-2 shows the corresponding rear view. Figures 1-3 and 1-4 are top and bottom views, respectively, of the SD with the covers removed. Figure 1-5 shows a simplified block diagram of the SD.

*Bass, et al, SLIFER Measurement for Explosive Yield, SAND76-0007, Sandia Laboratories, Albuquerque, NM, April 1976.

Figure 1-1. SLIFER Decipher -- Front View

Figure 1-2. SLIFER Decipher -- Rear View

Figure 1-3. SLIFER Decipher -- Top View

Figure 1-4. SLIFER Decipher -- Bottom View

Figure 1-5. Block Diagram of the SLIFER Decipher

2. Physical Description

2.1 Overall Dimensions

Overall dimensions for the SLIFER Decipher are as listed below:

Front Panel:

Height	5.25 in. (13.3 cm)
Width	19 in. (48.3 cm)

Chassis:

Height	5.25 in. (13.3 cm)
Width	17.25 in. (43.8 cm)
Depth	12.625 in. (32.1 cm)

Weight:

15 lb (6.8 kg)

2.2 Front Panel Controls, Connectors, and Readouts

Figure 1-1 shows a front view of the SD, displaying the control switches, connector jacks, and digital readouts. A brief description of each of these features follows:

POWER Switch -- This switch applies 28 V to the TEST-SHOT switch and to the remote closures.

POWER Indicator -- This indicator lights whenever the unit is ON, whether for test purposes or for remote recording.

TEST-SHOT Switch -- In the TEST position, this switch allows power to be applied to all of the circuits, independent of remote closures. This position is used for readout of recorded data and for bench work (recording and reading).

In the SHOT position, the only way in which power can be applied to internal circuits is for the POWER ON remote closure to be engaged. This position is used only for remote recording of data.

PRINT/READ-RECORD Switch -- In the PRINT/READ position, the prerecorded data can be printed or else read visually. In the RECORD position, the unit accepts and records data.

SHOT ENABLE Indicator -- This (green) light indicates that the unit is ready to accept remote closures. For this indication, the following conditions must be met:

- a. The battery switch for memory power (internal to the chassis) must be in the ON position.
- b. The POWER switch must be ON.
- c. The TEST-SHOT switch must be in the SHOT position.
- d. The PRINT/READ-RECORD switch must be in the RECORD position.
- e. 28-V power must be supplied to the unit.

FIDU Connector -- This connector (in parallel with the connector on the rear panel) is used for a fiducial or start pulse to initiate the storing of the next 512 data periods.

SIGNAL Connector -- This connector (in parallel with the connector on the rear panel) is used to bring in the signal that is to be recorded.

ADDRESS Readout -- This display reads the address of data in the memory.

PERIOD Readout -- This display reads the period of the frequency of the source signal.

DATA ENABLE Switch -- This switch is used to enable the unit (i.e., to begin storing data in the RECORD mode).

MANUAL TRIGGER Switch -- This switch simulates a fiducial input or start trigger.

The three switches labeled RESET, MANUAL STEP, and AUTO STOP-AUTO PRINT READ are used in conjunction with the PRINT/READ-RECORD switch to read or print the recorded data.

RESET Switch -- When this switch is engaged, the address counter is reset to 000.

AUTO STOP-AUTO PRINT READ Switch -- With this switch in the AUTO STOP position, the address counter advances only by means of the MANUAL STEP switch, advancing one count each time the switch is engaged. With this switch in the AUTO PRINT READ position, the address counter advances automatically, approximately 2.5 counts per second or 10 counts per second, depending upon the position of the PRINT SPEED switch (S9) on the rear of the chassis. These switch positions also drive the digital printer at the corresponding speeds.

2.3 Rear Panel Controls and Connectors

Figure 1-2 shows a rear view of the SD, displaying the control switches and connector jacks. A brief description of each of these features follows:

PRINT SPEED Switch -- This switch controls the speed of the data output, either FAST (10 prints per second) or SLOW (2.5 prints per second).

DATA OUT Connector -- The data output connector (J5) pin connections are as shown in Table 2-I.

FIDU IN Connector -- This connector (in parallel with the connector on the front panel) is used for a fiducial or start pulse which is utilized to initiate the storing of the next 512 data periods.

SIGNAL IN Connector -- This connector (in parallel with the connector on the front panel) is used to bring in the signal that is to be recorded.

REMOTE CLOSURES Connector -- A closure between the pins shown in Table 2-II performs the functions shown.

DC PWR IN Connector -- This connector is used to couple the SD with the DC power needed for operation (+ on pin B, - on pin A).

2.4 Internal Controls

Battery -- The memory battery must be fully charged in order to maintain data in the memory.

Battery Switch -- This switch determines the supply of voltage to the memory. In the ON position, power is from the internal battery. In the OFF position, power is from the 5-V DC-DC converter that also supplies all of the other 5-V power.

TABLE 2-I
Printer Connections

SD (Connector Type LJT06-19-32P)	Function		HP 5055A (Connector Type Amphenol 57-30500)
A	Col. 1	1	1
B		2	2
C	LSB	4	26
D		8	27
E	Col. 2	1	3
F		2	4
G		4	28
H	Data	8	29
J	Col. 3	1	5
K		2	6
L		4	30
M		8	31
N	Col. 4	1	7
P++		2	8
R*	MSB	4	32
S+		8	33
g	+ inhibit		22
j	+ print		23
h	+ 5 volt		25
R*	Ground		50
T	Col. 7	1	13
U		2	14
V	LSB	4	38
W		8	39
X	Memory Col. 8	1	15
Y		2	16
Z		4	40
a		8	41
b	Col. 9	1	17
c		2	18
d		4	42
e	Address	8	43
f	Col. 10	1	19
P++		2	20
R*	MSB	4	44
S+		8	45

|| Jumper in connector
* Jumper in connector
+ Jumper in connector

TABLE 2-II

Remote Closures
(Connector Type LJT00-13-98S)

	<u>Function</u>
F	
G	ENABLE
H	
K	POWER ON

3. Operating Instructions

3.1 Remote Recording

To Operate in this mode, proceed as follows:

- a. Connect a 28-V source to the recorder.
- b. Switch POWER to ON.
- c. Switch TEST-SHOT to SHOT.
- d. Switch PRINT/READ-RECORD to RECORD.
- e. Switch AUTO STOP-AUTO PRINT READ to AUTO STOP.
- f. The memory battery switch (internal) must also be ON.

With the switches in these settings and with 28 V applied, the SHOT ENABLE (green) light should be on. If the light is not on, determine the problem; do not use the recorder.

3.2 Remote Recording Simulation Using Test Box

To operate in this mode, proceed as follows:

- a. Connect the test box remote closure cable to the REMOTE CLOSURES jack (J2) of the SD. Connect the TRIGGER from the test box to the FIDU IN jack (J3) of the SD. Connect SIGNAL OUT from the test box to the SIGNAL IN jack (J4) of the SD.
- b. Turn the test box power ON.
- c. Press the POWER ON remote closure on the test box. SD power should come on (as indicated by readouts lighting up, etc).
- d. Press the ENABLE remote closure on the test box. The SD should start recording the period of the signal from the test box.
- e. Press the TRIGGER push-button switch on the test box. This simulates a fiducial pulse and also changes the frequency, causing the SD to record data and power down.

The RESET switch on the test box must be pressed to repeat steps c. through e. for another simulation.

3.3 Data Readout

To operate in this mode, proceed as follows:

- a. Switch TEST-SHOT to TEST.
- b. Switch PRINT/READ-RECORD to PRINT/READ.
- c. In order to print the data, connect a Hewlett Packard Model No. 5055A digital recorder to the DATA OUT connector (J5) and place the PRINT SPEED switch (S9) on the rear of the chassis in the FAST position. Turn the SD power ON. Press the RESET switch to verify that the address reads 000. Turn the HP digital printer power ON and place the HP OPERATE/STANDBY switch in the OPERATE position.
- d. To read data out, press RESET and then place the AUTO STOP-AUTO PRINT READ switch in the AUTO PRINT READ position. After the entire memory has been printed, place the OPERATE/STANDBY switch on the HP printer in the STANDBY position and the AUTO STOP-AUTO PRINT READ switch in the AUTO STOP position.

3.4 Test Operation

To operate the unit on a bench, connect a 28-V power source to the recorder. To record, place the TEST-SHOT switch in the TEST position and the PRINT/READ-RECORD switch in the RECORD position.

Press the DATA ENABLE switch. The SD should now be recording the input signal. The SD will stop recording either upon receiving a fiducial input or upon pressing the MANUAL TRIGGER. Power will remain on. Data may be read out as described in Section 3.3.

4. Performance Characteristics

Input Power: 28±4 V DC, 600 mA

Input Signals:

Power On: Relay closure

Power Off: Relay closure

Enable: Relay closure

Signal: 700-1500 kHz, 0.2-10 V peak-peak, 50-Ω input impedance

Fiducial: Pulse, >200 ns wide, 5 V

Sample Rate: 50 μs

Storage: 1024 samples total (512 after fiducial, 512 before fiducial)

Resolution: ±1 ns on the period of the input signal

Time Reference: Data stored at address 000 represent fiducial input time.

Time Correction: For the time to the center of the sample window (20-cycle gate), add 13.5 x (period reading), or approximately 15 μs; accurate to ±1 μs

Printer Output:

Rate: 2.5 or 10 prints per second

Logic: 1-2-4-0 BCD, positive logic, TTL levels

Output Drive: 10 TTL loads

Operational Environmental Limits:

Temperature: 0 to +70°C

Humidity: 93% noncondensing

Shock: 30 g, 50-ms half-sine, 3-axis, both directions

Pressures: 10,000 feet altitude

Nonoperational Environmental Limits:

Storage: -65 to +150°C

Shock: 30 g, 50-ms half-sine, 3-axis, both directions

Pressures: 50,000 feet altitude

5. Circuit Description

5.1 Fiducial Input Circuit

The fiducial input circuit consists of J3, J6, and the pulse generator A1U6A.

The fiducial pulse inputs the circuit through either J3 (on the front panel) or J6 (on the back panel). This positive-going pulse (0 to +5 V) triggers the pulse generator A1U6A. The outputs of this pulse generator (Q and $\overline{Q}$) will be discussed subsequently in Section 5.6.

5.2 Signal Input Circuit

The signal input circuit consists of J4, J7, the amplifier A1U3, and the pulse-shaping network A1U14A.

The SLIFER oscillator output arrives at either J4 (on the front panel) or J7 (on the back panel). This signal (from 700 kHz to 1500 kHz) is AC-coupled to the amplifier A1U3 through capacitor Cf. The amplifier input is biased by the voltage divider circuit consisting of R19, R20, R21, and R22 so that the amplifier is held in an off state until a signal greater than approximately 10 mV appears at pin 4.

The positive output of the amplifier is pulled to +5 V through resistor R18.

A1U14A takes the pulses from A1U3, reshapes them to square pulses, and outputs the squared pulses to the 20-count gate circuit.

5.3 20-Cycle Gate Generating Circuit

The 20-cycle gate is generated by the circuit consisting of integrated circuits A1U4; A1U5A and B; A1U14B, C, and D; A1U15A and B; and A1U13C.

The signal input pulse train from A1U14A (see Figure 5-1) starts the counter A1U4A, assuming the clock input (pin 1) is low. The counter output, Q3, is a divide-by-8 output and, along with the input pulse train, enables the gate A1U5B. The output of A1U5B is inverted by A1U15B and sets the 20-cycle gate flip-flop (A1U14B and A1U14C) high.

Figure 5-1. Timing Diagram 20-Count Gate Generator Circuit

A1U4A output Q4 and A1U4B output Q1, along with the input pulse train, enable gate A1U5A. The output of A1U5A is inverted by A1U15A and resets the 20-cycle gate flip-flop (A1U14B and A1U14C).

The clock input (A1U4A pin 1) is controlled by A1U4A output Q4 and A1U4B output Q1. When both are high, A1U14D goes low and A1U13C goes high, thereby stopping the counter. A reset pulse returns Q1 and Q4 to low, once again enabling A1U4A to begin counting another 20-cycle gate.

5.4 Period Counter

The period counter circuit consists of integrated circuits A1U13A, A1U20C and D, A1U12, A1U11, and A1U21.

A1U13A is a gate that allows the 50-MHz oscillator pulses to pass through during the time the 20-cycle gate is high (see Figure 5-2).

A1U20C resets the period counter when the 20-cycle gate generator circuit is reset or when a $\overline{WE}$ pulse and a 20-cycle gate appear simultaneously.

A1U11, A1U12, and A1U21 are counters that count the 50-MHz pulses and give a BCD output. This BCD output is the period of the incoming frequency (in nanoseconds) and is written into memory by a $\overline{WE}$ command (see Figure 5-2).

Figure 5-2. Timing Diagram Period Counter/ $\overline{\text{CS}}$ / $\overline{\text{WE}}$

5.5 Internally Generated Timing

Internal timing has the 50-MHz oscillator as the heart of the system. The 50-MHz oscillator is divided down to 20 kHz at the QD output of A1U27 by the divide-by-2500 circuit consisting of A1U24, A1U25, A1U26, and A1U27.

The positive-going edge of the QD pulse triggers the pulse generator A1U37B, which generates the $\overline{\text{WE}}$ command. The $\overline{\text{WE}}$ command writes the output of the period counter to memory on the trailing edge of the pulse (Figure 5-2).

The negative-going edge of the QD pulse triggers the pulse generator A1U9B, which generates the $\overline{\text{CS}}$ command. The $\overline{\text{CS}}$ command loads an address into memory on the falling edge of the pulse (Figure 5-2).

5.6 Externally Initiated Timing

The externally initiated timing starts with commands remotely generated while in a SHOT mode or manually generated by front panel switch settings while in a TEST mode.

5.6.1 SHOT Mode -- A POWER ON closure between pins H and K of J2 latches relay K1, turning on the 5-V power supply PS1. An ENABLE closure between pins F and G of J2 latches relay K2, enabling the unit as follows.

When K2 is energized, pin 10 of the relay goes low, setting the flip-flop (A1U7C and D) high at pin 10 and low at pin 11. When the pulse at pin 10 goes high, it enables the gate A1U50A. When the pulse at pin 11 goes low, it triggers A1U0B, whose output pulse sets the flip-flop (A1U17A and B) pin 3 high, enabling the $\overline{\text{WE}}$ gate A2U15C, and also sets the flip-flop (A1U20A and B)

pin 3 low and pin 4 high.

When A1U20A pin 3 goes low, it disables gate A1U17D and ensures that pin 11 of A1U17D goes high, which enables the reset generator A1U37A and the stop record counter gate A1U17C. When A1U20B pin 4 goes high, it holds the reset generator A1U37A in a ready state and also sets the MSB of the address selector high, so that only the upper 512 addresses of memory are selected to accept data.

A trigger pulse out of the fiducial pulse generator A1U6A is initiated either by a manual trigger (S4) which sets the flip-flop (A1U7A and B) pin 4 low or by a fiducial pulse input. The pulse sent out by A1U6A pin 7 is inverted by A1U55E and resets the 20-cycle gate generator through A1U15A. A pulse sent out by A1U6A pin 6 sets the flip-flop (A1U50B and C) pin 4 high and also sets the flip-flop (A1U20A and B) pin 3 high and pin 4 low.

When pin 4 of A1U50B goes high, it enables the POWER OFF gate A1U50D. When pin 3 of A1U20A goes high, it enables the stop-record gate A1U17D. When pin 4 of A1U20A goes low, it triggers the reset generator A1U37A and also sets the MSB of the address selector low, so that only the lower 512 addresses of memory are selected to accept data.

The reset generator (A1U37A), when triggered, resets the divide-by-2500 counter circuit, resets the 20-cycle gate counters, triggers the pulse generator A1U9A (whose outputs also reset the 20-cycle gate counters and reset the period counters through gate A1U20C), sends out a $\overline{CS}$ pulse, and resets the record address counter A1U19.

The record address counter A1U19 counts at a 20-kHz rate until Q10 of the counter goes high (after 512 counts). This turns on the power-off transistor Q1 which in turn resets the relays, turning off the unit.

3.6.2 TEST Mode -- In the test mode, remote closures are not necessary to operate the SD. Placing S3 in the TEST mode turns on the 5-V power supply PS1. The SD is then enabled by depressing front panel switch S5. The enable sequence of events is almost the same as in the SHOT mode; however, the power does not shut off as in the SHOT mode.

5.7 Memory

The memory consists of thirteen 1024x1-bit random access memory (RAM) integrated circuits. Each memory chip has 10 address inputs, a data input, a data output, a $\overline{CS}$ input, and a $\overline{WE}$ input.

The addresses are generated in the RECORD mode by A1U19 as it counts the 20-kHz pulses from the QD output of A1U27. A1U19 counts up to 512 and then starts again. In the PRINT mode, the addresses are generated by A1U39. The buffers (A1U28, A1U29, and A1U30) select which address to present to the memory chips, depending on which mode the SD is in.

The addresses are loaded into memory on the negative edge of the $\overline{CS}$ pulse. The $\overline{CS}$ pulse is generated by A1U9B in the RECORD mode (Section 5.5) and by A1U48A in the PRINT mode (Section 5.8).

The data present at the data input are loaded into the selected address on the trailing edge of the $\overline{WE}$ pulse. The $\overline{WE}$ pulse is generated by A1U37B in the RECORD mode (Section 5.5) and is disabled in the PRINT mode.

The memory integrated circuits will retain their memory after SD shutoff as long as the battery (BT1) power is present.

The data stored in the memory integrated circuits are sent to the readout drivers for visual display at the front panel or for printout from J5 on the back panel.

5.8 Print Mode

In the PRINT mode, the sequence of events is dictated primarily by the 20-kHz pulses from the QD output of A1U27.

When the PRINT/READ-RECORD switch (S2) on the front panel is placed in the PRINT/READ position, the 20-kHz pulses start the counters A1U38 and A1U51A, provided that the gate A1U5C has been enabled by the front panel switch S6 being in the AUTO PRINT position. These counters take the 20-kHz pulses and count them down to 9.76 pulses per second at the Q12 output of A1U38 and 2.44 pulses per second at the Q output of A1U51A.

The print rate is selected by the setting of back panel switch S9. These pulses (2.44 per second or 9.76 per second) clock the address counter A1U39, trigger the $\overline{CS}$ generator A1U48A, trigger the print command generator A1U44, and clock the readout address counters A1U41 and A1U42. After 1024 of these pulses, A1U39 resets the system through A1U48B.

The print command may be given manually using the front panel switch S7, provided that the front panel switch S6 is in the AUTO STOP position. Depressing S7 sets flip-flop A1U52C pin 10 low, which triggers A1U46B. The pulse out of A1U46B activates the print system in the same way as do the 9.76-per-second or the 2.44-per-second pulses.

The reset command may also be sent manually by depressing the front panel switch S8. This triggers the reset generator A1U48B in the same way as does the 1024-count pulse from A1U39.

APPENDIX A
Parts List and Drawings

DWG CLASSIFICATION LEVEL
UNCLASSIFIED

NOTES: PROCUREMENT INFORMATION

1. DRAWING OR PART NUMBERS LISTED PARENTHETICALLY AS REFERENCE IN THE DESCRIPTION COLUMN ARE FOR INTERNAL STOCK AND PROCUREMENT PURPOSES AT SANDIA.
2. PROCURE ITEMS LISTED BY COMMERCIAL PART NUMBER IN THE 'DESIGN AGENCY NO'. COLUMN AS MANUFACTURED BY THE SOURCE LISTED OR AS DEFINED ON THE REFERENCED SANDIA DRAWING WHEN LISTED, OR A COMMERCIAL EQUIVALENT WHEN A SANDIA DRAWING IS NOT LISTED.
3. PLASTIC SHEET, ITEM 1, MAY BE PURCHASED FROM REGAL PLASTICS, ALBUQUERQUE; STANDARD COLOR 2423 (TRANSPARENT).
4. TO BE SUPPLIED BY SANDIA LABORATORIES ORG. 1123.

ASSEMBLY INFORMATION

7. FOR SPECIFIC PROCESSING, MANUFACTURING ASSEMBLY REQUIREMENTS NOT OTHERWISE COVERED ON THE DRAWING, SEE 173126.
8. USE THE SUFFIX SPECIFIED OR ANY HIGHER OF 7-DIGIT STANDARD(S), SG OR 400000 SERIES SPECIFICATION(S).
9. FOR EXPLANATION OF DIMENSIONS, TOLERANCES AND SYMBOLIZATION, SEE 9900011.
10. COMPONENTS NOT IDENTIFIED BY ITEM NUMBERS ON THE ASSEMBLY ARE LOCATED IN THE LIST OF MATERIAL BY REFERENCE DESIGNATIONS.
11. USE THIS DIMENSION FOR PRINT INSPECTION MEASUREMENT ONLY. DO NOT USE PRINTS MORE THAN .100 INCH OUT-OF-SCALE FOR DRILLING TEMPLATES.
12. ORIENT COMPONENTS IN POSITIONS SHOWN.
13. ASSEMBLY HARDWARE IS SUPPLIED WITH PART(S).

DWG CLASSIFICATION LEVEL										SIZE	CODE IDENT NO.	DWG NUMBER	
UNCLASSIFIED										A	14213	T42342	
ISSUE										SCALE	SHEET 2 OF 13		

DWG CLASSIFICATION LEVEL

UNCLASSIFIED

ASSEMBLY INFORMATION CONTINUED

- 14. DO NOT MARK DESIGNATIONS APPEARING IN BRACKETS AND DIMENSIONS APPEARING WITHIN OUT-LINE OF VIEWS ON THE UNIT.
- 15. WELD AND INSPECT PER 9912117.
- 16. ENGRAVE .125 ± .030 INCH CONDENSED CHARACTERS, GROOVE WIDTH .020 TO .030 INCHES, GROOVE DEPTH .020 INCH MIN., WHITE FILLER, ITEM 58. LOCATE APPROXIMATELY AS SHOWN.
- 17. ENGRAVE LINES AND .190 ± .030 INCH CHARACTERS, GROOVE WIDTH .020 TO .030 INCHES, GROOVE DEPTH .020 INCH MIN., WHITE FILLER, ITEM 58. LOCATE APPROXIMATELY AS SHOWN.
- 18. ENGRAVE .100 ± .020 INCH CONDENSED CHARACTERS, GROOVE WIDTH .015 TO .020 INCHES, GROOVE DEPTH .020 INCH MIN., WHITE FILLER, ITEM 58. LOCATE APPROXIMATELY AS SHOWN.
- 19. MARK (WITH COVER COAT) REFERENCE DESIGNATIONS, FUNCTIONS, PART NUMBER AND SERIAL NUMBER; .120 INCH CHARACTERS, CONTRASTING COLOR. LOCATE APPROXIMATELY AS SHOWN.
- 20. REFERENCE DESIGNATIONS APPEARING WITHIN A DOTTED RECTANGLE ARE TO BE MARKED ON OPPOSITE SIDE.

DWG CLASSIFICATION LEVEL

UNCLASSIFIED

SIZE

A

CODE IDENT NO.

14213

DWG NUMBER

T42342

ISSUE

B

SCALE

SHEET

3

OF

13

DWG CLASSIFICATION LEVEL

UNCLASSIFIED

WIRING INFORMATION

25. ALL SOLDERLESS WRAPPED ELECTRICAL CONNECTIONS SHALL BE PER SANDIA FURNISHED SPECIFICATION.
26. ALL WIRE SHALL BE ITEM 63, UNLESS OTHERWISE SPECIFIED.
27. UNLESS OTHERWISE SPECIFIED, ALL WIRE WRAP HOOK-UP WIRE SHALL BE SIZE 30; ITEM 62.
28. ALL SHIELDED WIRE SHALL BE ITEM 68, UNLESS OTHER WISE SPECIFIED.
29. ALL WIRES TERMINATING AT COMPONENTS HAVING SCREW TYPE TERMINALS SHALL BE EQUIPPED WITH PREINSULATED LUG TERMINALS. TERMINAL SIZE TO BE DETERMINED BY THE SCREW TERMINAL AND THE WIRE SIZE.
30. CLAMP WIRE HARNESSSES AS SHOWN. CLAMP SIZES ARE TO BE DETERMINED AT ASSEMBLY BY THE SUPPLIER.
31. LACE ALL WIRES INTO A HARNESS USING TAPE, ITEM 65, UNLESS OTHERWISE SPECIFIED.
32. LOCATE COMPONENTS APPROXIMATELY IN LINE BETWEEN THEIR TERMINATION POINTS.
33. DASH-DOT LINE SHOWN ON AY-T42342 INDICATES PATH OF WIRES TO BE FOLLOWED WHEN UNIT IS WIRED.

DWG CLASSIFICATION LEVEL

UNCLASSIFIED

SIZE

A

CODE IDENT NO.

14213

DWG NUMBER

T42342

ISSUE

B

SCALE

SHEET

4

OF

13

QUANTITY REQUIRED				DESIGN AGENCY NO.	DESCRIPTION	NOTE	SHEET ZONE	ITEM
			NA	AYT42342-000	ASSEMBLY, SLIFER DECIPHER			
			NA	CKT42342-000	SCHEMATIC, SLIFER DECIPHER			
			NA	CMT40173-000	CIRCUIT MASTER READOUT BOARD			
			NA	173126	GENERAL SPECIFICATIONS FOR ACCEPTANCE EQUIPMENT	7		
			NA	990001	DIMENSIONS, TOLERANCE AND SYMBOLIZATION	8,9		
			NA	SS323207-000	SOLDERLESS WRAPPED ELECTRICAL CONNECTIONS	25		
			1		PLASTIC SHEET, LUCITE, RUBY RED, .125 THICK	3	1/B6	1
			1		ALUMINUM SHEET, 2024-T4 .06 THICK		2/A6	2
			1		ALUMINUM PLATE, 6061-T6, 3/16 THICK			3
			2	ARS	ALUMINUM BAR, 6061-T6, 3/8 SQUARE		2/F5	4
			2		ALUMINUM BAR, 6061-T6, 3/8 SQUARE		2/F5	5
			2		ALUMINUM FLAT, 6061-T6, 3/8 X 5/8		2/F5	6
			1		PLASTIC SHEET, PHENOLIC, 1/16 THICK		3/C7	7
			1		POWER SUPPLY & RELAY BOARD		3/A4	8
			1		BATTERY BOARD		3/A7	9
			1		READOUT BOARD		2/A3	10
			1		SUB-CHASSIS FRAME (ASSEMBLY OF ITEMS 4, 5 & 6)		2/D6	11
								12
			1	DL-T40173-000	P.C. READOUT BOARD	4		13
			1	170926-00	PLATE, IDENTIFICATION			14
								15
								16
								17
								18
			12	616-CG1	PLUG ADAPTER, AUGAT			19
								20
			1	VIP170512-43-PX	DRAWER, ELECTRICAL EQUIPMENT, ZERO MFG. CO.			21
			9	6012-1-A-BA	GUARD, SWITCH, BLACK VEMALINE PRODUCTS CO. (872836)			22
			16	X1558B	TERMINAL STUD, DOUBLE TURRET, CAMBRIDGE THERMIONIC (817349)			23
			3	2371	SPACER, SLEEVE 4-40 X 3/8 LG. HERMAN SMITH INC. (607136)			24
								25
								26
								27
								28
			4	1P16-3T12-2	PLUG ASSEMBLY, 12 INCH LONG, CONN EACH END, AUGAT			29
			4	1P16-3T24-1	PLUG ASSEMBLY, 24 INCH LONG, CONN ONE END, AUGAT			30
			2	516-AG10D	DIP SOCKET, 16 CONTACT, AUGAT			31

ISSUE					DWG CLASSIFICATION LEVEL					MFG AGENCY NUMBER				
B					UNCLASSIFIED					14213				
					SIZE					DWG NUMBER				
					A					T42342				
					SHEET					5 OF 13				

NA=DOCUMENTS AR=AS REQD ARS=AS REQD PER ASSEMBLY EM=EXPENSE MATL PM=PROCESS MATL				DWG CLASSIFICATION LEVEL UNCLASSIFIED				
QUANTITY REQUIRED				DESIGN AGENCY NO.	DESCRIPTION	NOTE	SHEET ZONE	ITEM
								32
								33
			4		SCREW PAN HD. 2-56 UNC X 3/8 LG.			34
			19		SCREW PAN HD. 4-40 UNC X 1/4 LG.			35
			3		SCREW FLAT HD. 4-40 UNC X 1/4 LG.			36
								37
			4		SCREW PAN HD. 8-32 UNC X 3/8 LG.			38
								39
								40
								41
			4		NUT HEX 2-56. SELF-LOCKING			42
								43
								44
								45
								46
								47
			4		WASHER FLAT #2 NOM. I.D.			48
								49
								50
			ARS		HARDWARE, MOUNTING, PER 173126			51
								52
			ARS	85884-3	TERMINAL, CLIP AMP SPECIAL INDUSTRIES (633245)			53
								54
								55
								56
								57
			ARS		FILLER, ENGRAVERS ENAMEL, HIGH GLOSS WHT			58
					NEW HERMES ENGRAVING MACHINE CO.			
			ARS		SOLVENT, ENGRAVERS ENAMEL CLEANER			60
					NEW HERMES ENGRAVING MACHINE CO.			
			ARS		WIRE INSULATED, SIZE 30 WHITE			62
			ARS	MIL-W-16878	WIRE INSULATED, SIZE 22 WHITE			63
			ARS	MIL-I-7444	INSULATION, SLEEVING, VINYL			64
			ARS	MIL-T-713	LACING TAPE, NYLON, WAXED, TYPE P. CLASS 2			65
			ARS	QQ-S-571	SOLDER, SN 60, FORM W, TYPE R OR RMA, COND. P2			66
			ARS		WELDING MATERIALS			67
			ARS	RG-196A/V	CABLE, COAXIAL (631518)			68

DWG CLASSIFICATION LEVEL UNCLASSIFIED					MFG AGENCY NUMBER 14213	
SIZE A					DWG NUMBER T42342	
SHEET 6 OF 13						

ISSUE	B																		
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NA=DOCUMENTS AR=AS REQD ARD=AS REQD PER ASSEMBLY EM=EXPENSE MATL PM=PROCESS MATL				DWG CLASSIFICATION LEVEL UNCLASSIFIED				
QUANTITY REQUIRED				DESIGN AGENCY NO.	DESCRIPTION	NOTE	SHEET ZONE	ITEM
		1	8136-FG1		IC SOCKET PANEL, 60 PATTERNS, 16 LEADS, ALGAT		3/G2	A1
		1	8136-FG1-30		IC SOCKET PANEL, 30 PATTERNS, 16 LEADS, ALGAT		2/G2	A2
		1	CMP-01CY		INTEGRATED CIRCUIT, COMPARATOR PRECISION MONOLITHICS, INC.			A1U3
		1	MC14520CL		INTEGRATED CIRCUIT, DUAL BINARY UP COUNTER MOTOROLA			A1U4
		1	SN74LS11J		INTEGRATED CIRCUIT, TRIPLE 3-INPUT POSITIVE AND GATE, TEXAS INSTRUMENTS			A1U5
		6	MC14528CL		INTEGRATED CIRCUIT, DUAL RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR, MOTOROLA			A1U6 A1U9 A1U37 A1U44 A1U46 A1U48
		6	MC14011CL		INTEGRATED CIRCUIT, QUAD 2-INPUT NAND GATE MOTOROLA			A1U7 A1U17 A1U20 A1U52 A2U15 A1U50
		1	MC14025CL		INTEGRATED CIRCUIT, TRIPLE 3-INPUT NOR GATE MOTOROLA			A1U8
		1			DISCREET COMPONENT BOARD (ITEM 19, R19, R20, R21, R22)			A1U1
		1			(C1, R17, R18)			A1U2
		1			(C6, C9, C10, R9)			A1U10
		1			(C3, C4, R3, R6)			A1U16
		1			DISCREET COMPONENT BOARD (ITEM 19, C7, C8, R8)			A1U36
DWG CLASSIFICATION LEVEL UNCLASSIFIED						MFG AGENCY NUMBER 14213		
SIZE A						DWG NUMBER T42342		
SHEET 7 OF 13								

ISSUE

B

NA=DOCUMENTS AR=AS REQD AR=AS REQD PER ASSEMBLY EM=EXPENSE MATL PM=PROCESS MATL				DWG CLASSIFICATION LEVEL UNCLASSIFIED				
QUANTITY REQUIRED				DESIGN AGENCY NO.	DESCRIPTION	NOTE	SHEET ZONE	ITEM
			1		DISCREET COMPONENT BOARD (ITEM 19, C16, C17, R15, R16)			A1U45
			1		↑ C11, C12, R11, R12			A1U47
			1		↑ C13, C15, R13, R14			A1U49
			1		↑ R23, Q1, C18, R25			A1U40
			1		DISCREET COMPONENT BOARD (ITEM 19, C5, R7, R26)			A1U54
			1		DISCREET COMPONENT BOARD (ITEM 19, R27, R28, R29)			A1U53
			1		DISCREET COMPONENT BOARD (ITEM 19, C19, C20, C21, C22)			A1U57
			4	SN74LS196J	INTEGRATED CIRCUIT, 50 MHZ PRESETTABLE DECADE COUNTER, TEXAS INSTRUMENTS			A1U11
								A1U25
								A1U26
								A1U27
			2	SN74196J	INTEGRATED CIRCUIT, 50 MHZ PRESETTABLE DECADE COUNTER, TEXAS INSTRUMENTS			A1U12
								A1U24
			1	SN74500J	INTEGRATED CIRCUIT, QUAD 2-INPUT NAND GATE, TEXAS INSTRUMENTS			A1U13
			1	SN74LS00J	INTEGRATED CIRCUIT, QUAD 2-INPUT POSITIVE NAND GATE, TEXAS INSTRUMENTS			A1U14
			1	SN7428J	INTEGRATED CIRCUIT, QUAD 2-INPUT POSITIVE NOR BUFFER, TEXAS INSTRUMENTS			A1U15
			3	MC14049CL	INTEGRATED CIRCUIT, HEX BUFFER, INVERTING, MOTOROLA			A1U18
								A1U22
								A1U55
DWG CLASSIFICATION LEVEL UNCLASSIFIED						MFG AGENCY NUMBER 14213		
SIZE A						DWG NUMBER T42342		
SHEET 8 OF 13								

NA=DOCUMENTS AR=AS REQD AR=AS REQD PER ASSEMBLY EM=EXPENSE MATL PM=PROCESS MATL				DWG CLASSIFICATION LEVEL UNCLASSIFIED				
QUANTITY REQUIRED				DESIGN AGENCY NO.	DESCRIPTION	NOTE	SHEET ZONE	ITEM
			13	IM6508	INTEGRATED CIRCUIT, 1024 BIT READ ACCESS MEMORY, INTERSIL, INC.			A2U1 THRU A2U13
			1	TR-134R	BATTERY, MERCURY, 5.4V, 1AH, MALLORY (600821)			BT1
			2	150D226X0035R2	CAP., FIXED, ELECT., 22UF ± 20 %, 35 WVDC, (603627) SPRAGUE ELEC. CO.			C1, C2
			1	CK05BX102K	CAP., FIXED, CERAMIC, .001UF ± 10%, 200 WVDC (633189)			C3
			3	CK05BX221K	CAP., FIXED, CERAMIC, 220PF ± 10%, 200 WVDC (633185)			C4 C16, 17
			1	150D106X0035R2	CAP., FIXED, ELECT., 10UF ± 20%, 35 WVDC, (603625) SPRAGUE ELEC. CO.			C5
			2	CK05BX151K	CAP., FIXED, CERAMIC, 150PF ± 10%, 200 WVDC (633184)			C7, C9
			1	CK05BX331K	330PF (633186)			C8
			1	CK05BX471K	470PF (633187)			C10
			2	CK05BX101K	CAP., FIXED CERAMIC 100PF ± 10%, 200 WVDC (633183)			C11, 15
			3	150D225X0035B2	CAP., FIXED, ELECT., 2.2UF ± 20%, 35 WVDC (603622) SPRAGUE ELEC. CO.			C12, 13 C18
			4	CK06BX103K	CAP., FIXED, CERAMIC, .01UF ± 10%, 200 WVDC (633234)			C19, C20 C21, C22
			1	VK30BX104M	CAP., FIXED, CERAMIC, .1 UF ± 20%, 200 WVDC (603782)			C23
					DWG CLASSIFICATION LEVEL UNCLASSIFIED		MFG AGENCY NUMBER 14213	
					SIZE A		DWG NUMBER T42342	
ISSUE C					SHEET 10 OF 13			

QUANTITY REQUIRED				DESIGN AGENCY NO.	DWG CLASSIFICATION LEVEL UNCLASSIFIED	NOTE	SHEET ZONE	ITEM
					DESCRIPTION			
		1	IN965B		SEMICONDUCTOR DEVICE, DIODE, 15V ZENER (871548)			CR1
		1	IN914		SEMICONDUCTOR DEVICE, DIODE, SWITCHING (839085)			CR2
		1	5082-4860		DIODE, LIGHT EMITTING, RED, HEWLETT-PACKARD			DS1
		1	CF3-GT-1762		LAMP, INCANDESCENT, GREEN, 28V, ELDEMA CORP (613345)			DS2
		8	5082-7340		INDICATOR, DIGITAL, HEXADECIMAL, HEWLETT-PACKARD			DS3A THRU DS4D
		1	AN3102A-16-11P		CONN, RECP, ELEC. (609029) & (609132)			J1
		1	LJT00-13-98S		BENDIX, SA1438-10 (358315)			J2
		4	UG-290A/U		RF (818367)			J3, J4 J6, J7
		1	LJT00-19-32S		CONN, RECP, ELEC, BENDIX, SA1438-3 (358188)			J5
		2	SL110		RELAY, ARMATURE, LATCHING, POTTER-BRUMFIELD (837664)			K1, K2
		1	1005-128		POWER SUPPLY, 5V, 1 AMP, TECHNETICS, INC.			PS1
		1	2N2222A		TRANSISTOR, LOW POWER, SILICON, NPN (633801)			Q1

NA=DOCUMENTS AR=AS REQD ARS=AS REQD PER ASSEMBLY EM=EXPENSE MATL PM=PROCESS MATL					DWG CLASSIFICATION LEVEL UNCLASSIFIED	MFG AGENCY NUMBER 14213
ISSUE B					SIZE A	DWG NUMBER T42342
					SHEET 11 OF 13	

QUANTITY REQUIRED				DESIGN AGENCY NO.	DESCRIPTION	NOTE	SHEET ZONE	ITEM
		2	RLR20C104GR	RESISTOR, FIXED, FILM, 100K, $\pm 2\%$, 1/2W (440007-388)				R1 R24
		7	RLR05C104GM	100K, $\pm 2\%$, 1/8W (440005-388)				R3, R4 R12, 13 R19, 20 R25
		1	RLR05C152GM	1.5K $\pm 2\%$, 1/8W (440005-300)				R23
		1	RLR05C472GM	4.7K, $\pm 2\%$, 1/8W (440005-324)				R5
		5	RLR05C103GM	10K, $\pm 2\%$, 1/8W (440005-340)				R6, R8 R16, 21 R22
		1	RLR05C303GM	30K, $\pm 2\%$, 1/8W (440005-362)				R7
		1	RLR05C113GM	11K, $\pm 2\%$, 1/8W (440005-342)				R9
		2	RLR05C102GM	1K, $\pm 2\%$, 1/8W (440005-292)				R10, 18
		4	RLR05C513GM	51K, $\pm 2\%$, 1/8W (440005-374)				R14, 15 R11, 30
		1	RLR07C182GR	RESISTOR, FIXED, FILM 1.8K $\pm 2\%$, 1/4W (440018-304)				R17
		1	RLR05C512GM	RESISTOR, FIXED, FILM 5.1K $\pm 2\%$, 1/8W (440005-326)				R26
		3	RLR05C2236M	RESISTOR, FIXED, FILM, 22K $\pm 2\%$, 1/8W (440005-356)				R27 R28 R29

NA=DOCUMENTS AR=AS REQD ARS=AS REQD PER ASSEMBLY EM=EXPENSE MATL PM=PROCESS MATL				DWG CLASSIFICATION LEVEL UNCLASSIFIED		MFG AGENCY NUMBER 14213	
ISSUE C				SIZE A		DWG NUMBER T42342	
				SHEET 12 OF 13			

QUANTITY REQUIRED				DESIGN AGENCY NO.		DWG CLASSIFICATION LEVEL UNCLASSIFIED				
						DESCRIPTION	NOTE	SHEET ZONE	ITEM	
			2	8837K4		SWITCH, TOGGLE, 2 PDT, ON-NONE-ON, MS25307-232 (856349) CUTLER-HAMMER			S1, S9	
			2	8838K4		SWITCH, TOGGLE, 4 PDT, ON-NONE-ON (858444) CUTLER-HAMMER			S2, S3	
			4	2PB299-T2		SWITCH, PUSH BUTTON, HONEYWELL, MICROSWITCH DIV (870609)			S4, S5 S7, S8	
			1	8837K4		SWITCH, TOGGLE, 2 PDT, ON-NONE-ON, MS25307-232 (856349) CUTLER-HAMMER			S6	
			1	8869K4		SWITCH, TOGGLE, MINIATURE, 2 PDT, ON-NONE-ON (874457) MS90311-231, CUTLER-HAMMER			S10	
			1	134		HOLDER, BATTERY, KEYSTONE ELECTRONICS			XBT1	
			1	7538		LAMPHOLDER, INDICATOR LIGHT, DIALIGHT CORP. (600269)			XDS2	
			2	532-AGIOD		SOCKET, DIP, AUGAT, INC.			XDS3	
									XDS4	
			2	VB10/IDV3		SOCKET, RELAY, VIKING INDUSTRIES (871386)			XK1 XK2	
			2	2006		TERMINAL BOARD, JUNCTION TYPE, 6 TERMINALS (625774) CINCH MFG. CO.			TB1 TB2	
			1	52		TERMINAL BOARD, MINIATURE, 2 TERMINALS (625808) CINCH MFG. CO.			TB3	

NA=DOCUMENTS AR=AS REQD AR=AS REQD PER ASSEMBLY EM=EXPENSE MATL PM=PROCESS MATL						DWG CLASSIFICATION LEVEL UNCLASSIFIED		MFG AGENCY NUMBER 14213	
ISSUE B						SIZE A		DWG NUMBER T42342	
						SHEET 13 OF 13

1. RED - CIRCUITRY NEAR SIDE
2. BLUE - CIRCUITRY FAR SIDE
3. BROWN - CIRCUITRY BOTH SIDES
4. TERMINAL SIZES ARE (COLOR CODE SIZES REQ'D IN TABLE AND ON LAYOUT).

TERMINAL SIZE	HOLE DIA	HOLE DIA	HOLE DIA
.040	⊕	⊕	⊕
.050	⊕	⊕	⊕
.062	⊕.027/.033	⊕	⊕
.075	⊕	⊕	⊕
.086	⊕	⊕	⊕
.100	⊕	⊕	⊕
.125	⊕	⊕	⊕
.150	⊕	⊕	⊕
.175	⊕.096/.102	⊕	⊕

5. ALL LINE WIDTHS ARE .002, .005, .010, .015, .020, .025, .040, .050, .100, .125, .150 (CIRCLE SIZE).
6. MINIMUM CLEARANCE BETWEEN CIRCUITS AND CIRCUITRY AND EDGE OF THE BOARD IS .010, .015, .020, .025, .030, .040, .050, OTHER (CIRCLE SIZE).
7. LOCATE IDENTIFICATION INFORMATION AS SHOWN.
8. SUPPLIER WILL BE FURNISHED DUPLICATE REPRODUCTION OF MASTER DRAWING CM-T40173 FOR PLATE MAKING PURPOSE.
9. MATERIAL: PLASTIC SHEET, LAMINATED, 2 OZ. COPPER CLAD BOTH SIDES, GLASS BASE, EPOXY RESIN, FLAME RETARDANT, .062 THK (FL-GF OR GH-062-C-2/2, MIL-P-13949)(531 236)
10. FABRICATE PRINTED-WIRING ASSEMBLY PER 9928006 TYPE 2.
11. SEE T42342 AND AY-T42342 FOR COMPONENT VALUES AND ASSEMBLY INFORMATION.

AGENCY APPROVALS			SHEET	TITLE		
ORG	DATE	APPROVALS	ISSUE	A	LAYOUT READOUT BOARD DECIFER	
			SHEET INDEX			
			PART CLASSIFICATION			
			UNCLASSIFIED			
			DWG CLASSIFICATION LEVEL			
			UNCLASSIFIED			
SIZE	CODE IDENT. NO.	DWG NUMBER				
D	14213	DL-T40173				
SCALE	4/1	SHEET	1	OF	1

ITEM 11
SCALE 1/1
SUB-CHASSIS FRAME
MAY BE A BOLTED ASSEMBLY OR WELDING AS SHOWN
ALL 4-ØD HOLES MAY BE LOCATED AT ANY WITH AT 22 AND ITEMS 8 AND 9

ITEM 1
SCALE 1/1
ABOUT HAVE TO BE MATCH
PAGES AND DENTED EXCEPT
AS SHOWN FROM ITEM 2

ALL MODIFY AS SHOWN
JKT & CABLE CONNECTORS (ITEMS 29 & 30)
ARE SHOWN FOR REFERENCE ONLY

ITEM 9
SCALE 1/1
BATTERY BOARD

ITEM 8
SCALE 1/1
POWER SUPPLY & DISPLAY BOARD

NAME	C						
DMS CLASSIFICATION LEVEL							
UNCLASSIFIED							
DATE CLASSIFIED BY				DATE REVIEWED			
E 12213				AY-142342			
AUTHORITY				REASON			

APPENDIX B
Data Sheets

CMP-01CY

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage, V + to V-	36V	Output Sink Current (Continuous	
Output to Ground	-5V to +32V	Operation)	75 mA
Output to Negative Supply Voltage	50V	Operating Temperature Range	0 to 70°C
Ground to Negative Supply Voltage	30V	Storage Temperature Range	-65 to 150°C
Positive Supply Voltage to Ground	30V	Lead Temperature (Soldering, 60 s)	300°C
Positive Supply Voltage to Offset Null	0 to 2V	Output Short Circuit Duration --	
Power Dissipation (See Note)	500 mW	to ground	Indefinite
Differential Input Voltage	±11V	to V+	1 min
Input Voltage ($V_S = \pm 15V$)	±15V		

Note: Maximum package power dissipation vs. ambient temperature

Maximum Ambient	Derate Above Maximum
Temperature for Rating	Ambient Temperature
100°C	10.0 mW/°C

Pin Connections (Top View)

CO238-A1

Features:	Consumes space of only one 14-pin DIP 0.35 in. high
Frequency:	3 MHz thru 100 MHz
Output:	Drives 10 TTL loads (above 50 MHz drive capability decreases: at 100 MHz drives 2 Schottky TTL loads). Logic "0": 0.4V max, sink 16 ma. Logic "1": 2.4V min, source 2 ma. Symmetry: 50/50±15% (improved symmetry available on some models).
Input Voltage:	5 VDC ±5%
Input Current:	1b-80 ma, Current drain depends upon frequency - it is typically 15-20 ma in 4-20 MHz range.
Tuning Option Available:	No
Accuracy (Maximum error at 25°C):	±0.005%
Stability Standard (See below for options):	0°C to +70°C: ±0.0025%. +20°C to +30°C: ±0.0005%
Stability Options Available:	1; 2 (to 70 MHz); 3 (above 6 MHz); 5 (above 4 MHz); 6; and 8
Definition of Stability Options:	1 = -55°C to +85°C: ±0.005%. 2 = -55°C to +125°C: ±0.005%. 3 = 0°C to +50°C: ±0.0003%. 5 = 0°C to +50°C: ±0.0005%. 6 = 0°C to +50°C: ±0.001%. 8 = 0°C to +70°C: ±0.01% (includes initial accuracy)
Size/Weight:	0.5 x 0.8 x 0.35 in., 1/8 oz. (12.7 x 20.3 x 8.9 mm, 3 g).
Mounting:

0.011 NOTE: Pins 4 and 8 may be externally tied together.

DS3630N

General Description

The DS3630 is a high-current buffer intended for use with CMOS circuits interfacing with peripherals requiring high drive currents. The DS3630 features low quiescent power consumption (typically 50 μ W) as well as high-speed driving of capacitive loads such as large MOS memories. The design of the DS3630 is such that V_{cc} current spikes commonly found in standard CMOS circuits cannot occur, thereby reducing the total transient and average power when operating at high frequencies.

Features

- High-speed capacitive driver
- Wide supply voltage range
- Input/output TTL compatibility
- Input/output CMOS compatibility
- No internal transient V_{cc} current spikes
- 50 μ W typical standby power
- Fan out of 10 standard TTL loads

Connection Diagram

IM6508

Features

- Low Power Operation
- Excellent Speed Operation
- TTL or CMOS Compatible On Inputs and Outputs
- 4V-11V V_{CC} Operation
- Static Operation
- On-Chip Address Register

General Description

The IM6508's are high-speed, low-power, silicon gate CMOS 1024-bit static RAM's organized 1024 words by 1 bit. In all states, these RAM's exhibit the microwatt power requirements typical of CMOS. Inputs and three-state output are TTL compatible. The basic part operates at 4 to 7 volts with a 5V, 25°C access time of 350 ns and supply current of 100 μ A. Faster access times and lower supply currents are offered in a DASH-1 version. Higher operating voltages are offered in an "A" version. Data retention is guaranteed to 3 volts on all parts.

Write Enable and Chip Select functions are active in the low state. These functions are specified for easy interface to common I/O data busses. On-chip address registers (clocked by the falling edge of CS_1) can often improve system performance and reduce package count.

These devices are ideally suited for memory systems requiring low operating power, high performance or non-volatility (battery backup).

Pin 1 is designated either by a dot or a notch.

MC14001CL

Quad 2-Input "NOR" Gate

The MC14001 quad 2-Input NOR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 10 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 16 Vdc
- Single Supply Operation - Positive or Negative
- High Fanout >50
- Input Impedance = 10^{13} ohms typical
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4001A

Maximum Ratings (Voltages referenced to V_{SS} , Pin 7)

<u>Rating</u>	<u>Symbol</u>	<u>Value</u>	<u>Unit</u>
DC Supply Voltage	V_{DD}	+16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Logic Diagram
(Positive Logic)

$$3 = \overline{1+2}$$

$$V_{DD} = \text{Pin 14}$$

$$V_{SS} = \text{Pin 7}$$

MC14011CL

Quad 2-Input "NAND" Gate

The MC14011 quad 2-input NAND gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 10 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 16 Vdc
- Single Supply Operation - Positive or Negative
- High Fanout - >50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Symmetrical Output Resistance - 750 ohms typical

Maximum Ratings (Voltages referenced to V_{SS} , Pin 7)

<u>Rating</u>	<u>Symbol</u>	<u>Value</u>	<u>Unit</u>
DC Supply Voltage	V_{DD}	+16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Logic Diagram
Positive Logic

$$3 = \overline{1 \cdot 2}$$

V_{DD} = Pin 14

V_{SS} = Pin 7

MC14013CL

Dual Type D Flip-Flop

The MC14013 dual type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data (D), Direct Set (S), Direct Reset (R), and Clock (C) inputs and complementary outputs (Q and $\bar{Q}$). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Static Operation
- Quiescent Power Dissipation = 25 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 16 Vdc
- Single Supply Operation
- Toggle Rate = 10 MHz
- Logic Edge-Clocked Flip-Flop Design - Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse.
- Pin-for-Pin Replacement for CD4013A

Maximum Ratings (Voltages referenced to V_{SS} , Pin 7)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Truth Table

Clock†	Inputs			Outputs	
	Data	Reset	Set	Q	$\bar{Q}$
0	0	0	0	1
1	0	0	1	0
X	0	0	Q	$\bar{Q}$
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	.	.

X = Don't Care

† = Level Change

. = Invalid Condition

Block Diagram

MC14025CL

Triple 3-Input "NOR" Gate

The MC14025 triple 3-input NOR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 10 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 16 Vdc
- Single Supply Operation - Positive or Negative
- High Fanout - >50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Symmetrical Output Resistance - 750 ohms typical
- Pin-for-Pin Replacement for CD4025A

Maximum Ratings (Voltages referenced to V_{SS} , Pin 7)

<u>Rating</u>	<u>Symbol</u>	<u>Value</u>	<u>Unit</u>
DC Supply Voltage	V_{DD}	+16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Logic Diagram (Positive Logic)

MC14040CL

12-Bit Binary Counter

The MC14040 12-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave-shaping circuit and 12 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-driving circuits.

- Fully Static Operation
- Quiescent Power Dissipation = 50 nW/package typical at $V_{DD} = 5.0$ V
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 16 Vdc
- Low Input Capacitance = 5.0 pF typical
- All 12 Buffered Outputs Available
- Common Reset Line
- 13 MHz Typical Counting Rate at $V_{DD} = 15$ V
- Pin-for-Pin Replacement for CD4040A

Maximum Ratings (Voltages referenced to V_{SS} , Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Truth Table

Clock	Reset	Output State
0	No Change
0	Advance to next state
X	1	All Outputs are low

X = Don't Care

Logic Diagram

MC14049CL

Hex Buffers

The MC14049 hex inverter/buffers are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic-level conversion using only one supply voltage, V_{CC} . The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage for logic-level conversions. Two TTL/DTL loads can be driven when the devices are used as CMOS-to-TTL/DTL converters ($V_{CC} = 5.0\text{ V}$, $V_{OL} \leq 0.4\text{ V}$, $I_{OL} \geq 3.2\text{ mA}$). Note that pin 16 is not connected internally on these devices; consequently connections to this terminal will not affect circuit operation.

- Direct Drive of two TTL/DTL Loads
- High Source and Sink Currents
- High-to-Low or Low-to-High Level Converter
- Quiescent Power Dissipation = 5 nW/package typical
- Single-Supply, Pin-for-Pin Replacements for Type MC14009

Maximum Ratings (Voltages referenced to V_{SS} , Pin 8)

<u>Rating</u>	<u>Symbol</u>	<u>Value</u>	<u>Unit</u>
DC Supply Voltage	V_{CC}	+16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	+18 to -0.5	Vdc
DC Current per Input Pin	I_{in}	10	mAdc
DC Current per Output Pin	I_{out}	45	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Logic Diagram

NC = Pin 16
 V_{SS} = Pin 8
 V_{CC} = Pin 1

MC14518CL

Dual Up Counters

The MC14518 dual BCD counters are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518 will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Quiescent Power Dissipation = 1.0 μ W/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 16 Vdc
- Low Input Capacitance = 5.0 pF typical
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-Clocked Design - Incremented on Positive Transition of Clock or Negative Transition on Enable
- 6.0 MHz Counting Rate

Maximum Ratings (Voltages referenced to V_{SS} , Pin 8)

Truth Table

Rating	Symbol	Value	Unit	Clock	Enable	Reset	Action
DC Supply Voltage	V_{DD}	+16 to -0.5	Vdc		1	0	Increment Counter
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc	0		0	Increment Counter
DC Current Drain per Pin	I	10	mAdc	X		0	No Change
Operating Temperature Range	T_A	-40 to +85	$^{\circ}$ C		0	0	No Change
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}$ C	X	X	1	No Change

X = Don't Care

MC14519CL

4-Bit AND/OR Selector or Quad 2-Channel Data Selector or Quad Exclusive "NOR" Gate

The MC14519 is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

This device exemplifies the design versatility of MCMOS logic structure. This part provides three functions in one package: a 4-Bit AND/OR Selector, a Quad 2-Channel Data Selector, or a Quad Exclusive NOR Gate.

- Quiescent Power Dissipation = 100 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 16 Vdc
- Single Supply Operation - Positive or Negative
- High Fanout >50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Plug-In Replacement for CD4019 in Most Applications

Truth Table

Control Inputs		Output
A	B	Z_n
0	0	0
0	1	Y_n
1	0	X_n
1	1	$X_n \odot Y_n$

Note: $X_n \odot Y_n$ means X_n (Exclusive NOR) Y_n

MC14520CL

Dual Up Counters

The MC14520 dual binary counters are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Quiescent Power Dissipation = 1.0 μ W/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 16 Vdc
- Low Input Capacitance = 5.0 pF typical
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-Clocked Design - Incremented on Positive Transition of Clock or Negative Transition on Enable
- 6.0 MHz Counting Rate

Maximum Ratings (Voltages referenced to V_{SS} , Pin 8)

Truth Table

Rating	Symbol	Value	Unit	Clock	Enable	Reset	Action
DC Supply Voltage	V_{DD}	+16 to -0.5	Vdc	$\nearrow$	1	0	Increment Counter
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc	$\searrow$	X	0	Increment Counter
DC Current Drain per Pin	I	10	mA	X	$\nearrow$	0	No Change
Operating Temperature Range	T_A	-40 to +85	$^{\circ}$ C	$\nearrow$	0	0	No Change
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}$ C	1	$\searrow$	0	No Change
				X	X	1	Q0 thru Q3 = 0

X = Don't Care

MC14528CL

Dual Monostable Multivibrator

The MC14528 provides the function of a dual, retriggerable, resettable, monostable multivibrator. This device may be triggered from either edge of an input pulse, and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, C_X and R_X .

- Separate Reset Available
- Low Quiescent Power Dissipation - 25 nW at 5.0 Vdc
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse

Maximum Ratings (Voltages referenced to V_{SS} , Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+16 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Block Diagram

SN74LS00J

Quad 2-Input NAND Gate

Guaranteed Operating Ranges

Supply Voltage			Temperature
Min	Typ	Max	
4.75V	5.0V	5.25V	0 to 75°C

SN74LS11J

Triple 3-Input AND Gate

Guaranteed Operating Ranges

Supply Voltage

<u>Min</u>	<u>Typ</u>	<u>Max</u>	<u>Temperature</u>
4.75V	5.0V	5.25V	0 to 75°C

SN74S00J

Quadruple 2-Input NAND Gates

Typical Propagation Time . . . 3 ns at $C_L = 15$ pF

Typical Power Dissipation. . . 19 mW per Gate at 50% Duty Cycle

Recommended Operating Conditions

	<u>Min</u>	<u>Nom</u>	<u>Max</u>	<u>Unit</u>
Supply Voltage, V_{CC}	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20
	Low logic level			10
Operating free-air temperature, T_A	0		70	°C

positive logic: $Y = \overline{AB}$

SN7428J

Quadruple 2-Input Positive-NOR Buffers

positive logic:

$$Y = \overline{A+B}$$

SN74196J
SN74LS196J

- Performs BCD, Bi-Quinary, or Binary Counting
- Fully Programmable
- Fully Independent Clear Input
- Input Clamping Diodes Simplify System Design
- Output Q_A Maintains Full Fan-out Capability In Addition to Driving Clock-2 Input

Types	Guaranteed		Typical Power Dissipation
	Count Frequency	Clock 1 Clock 2	
196	3-50 MHz	0-25 MHz	240 mW
LS196	0-30 MHz	0-15 MHz	60 mW

Description

These high-speed monolithic counters consist of four, dc-coupled, master-slave flip-flops which are internally interconnected to provide a divide-by-two and a divide-by-five counter. These counters are fully programmable (that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs). The outputs will change to agree with the data inputs independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which, when taken low, sets all outputs low regardless of the states of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low but will remain unchanged when the count/load is high and the clock inputs are inactive.

All inputs are diode-clamped to minimize transmission-line effects and simplify system design. These circuits are compatible with most TTL and DTL logic families. Typical power dissipation is 60 milliwatts. Circuits are characterized for operation from 0 to 70°C.

314A-512
316A-223

Series 314 and 316 cermet resistor networks are packaged in 14 and 16 pin dual inline combinations, respectively. Series 314A consists of 13 resistors; Series 316A consists of 15 resistors, all resistors of identical value and with one common connection. Available in a broad range of resistance values, all are substantially smaller than networks made of individual resistors. Series 314A and 316A may be used as pull-up resistors for unused TTL gates, parallel high-speed circuitry, wired OR configurations, pull-down applications or TTL-MOS interfacing.

Network Specifications		Series 314A, 316A Part Number Explanation	
Net- work	Power Dissipation Rating (Up to 70°C)	Series Designation	Resistance Value
314A	125 mW/resistor 1.6 W/package	314A 316A	First two digits are significant figures and the third indicates the number of zeros fol- lowing the first two digits. Examples: 101 = 100 ohms 102 = 1000 ohms 122 = 1200 ohms
316A	125 mW/resistor 1.8 W/package

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