A Progress Report Entitled: New Technology for Linear Colliders

Grant No. DE-FG02-91ER40613

RF-91-1147(6788)

SEP 3 0 1991

Prepared by

Peter M. McIntyre
Physics Department
Texas A&M University
College Station, TX 77843

Submitted through

Texas A & M Research Foundation
Box 3578
College Station, TX 77843

August 1991

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

MASTER

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

ctp
8/11/91

NEW TECHNOLOGY FOR LINAC COLLIDERS

1991 PROGRESS REPORT AND RENEWAL PROPOSAL

The purpose of this contract is to develop and evaluate new technology for future e^+e^- linac colliders.^[1] TeV linac colliders will require major improvements in the performance of microwave power tubes:^[2] >100 mW/m peak power, ~20 GHz frequency, and high efficiency. For the past three years we have been developing gigatron^[3], a new design concept for microwave power tubes. The gigatron design concept is described in detail in Appendix A and illustrated in Figure 1. It incorporates three key innovations: a gated field-emitter cathode which produces a fully modulated electron beam directly into the vacuum;^[4] a ribbon beam geometry which eliminates space charge and phase dispersion, and a traveling wave coupler which provides optimum output coupling even over a wide ribbon beam. Section I presents an overview of the gigatron project from its inception through the proposed three-year renewal. Section II describes the features of field emitter cathodes for microwave applications. During the past two years our research has focussed on the fabrication and testing of gated field-emitter cathodes, and the development of a cathode assembly suitable for use in gigatron.

During the past year we have built prototypes of two cathode designs: a stripline edge-emitter array and a porous silicon dioxide cathode. A highlight of our results is the development and testing of the porous SiO_2 cathode^[5]. It delivers exceptional performance as a modulated electron source in general and for gigatron in particular. Its high emitter density ($\sim 10^{10}/\text{cm}^2$) and low work function accommodate higher tube gain, simpler cathode coupling, and higher peak power than any other technology. The protection of the active emitting surface by ~2 μm of porous SiO_2 should provide for rugged operation in a tube environment.

Section III describes the recent accomplishments of our program:

- o fabrication of stripline edge-emitter cathodes;
- o fabrication of porous SiO_2 cathodes;
- o operation of cathodes with 24 A/cm^2 emission from 9.3 V modulation - a new performance record for field-emission microdevices.
- o study of the role of surface and pore charging in field-emission from porous SiO_2 .

Section IV describes the incorporation of a field emitter cathode into a resonant input coupler for gigatron.

Section V summarizes our research program proposed for the coming three years. The major milestones are

- o microwave modulation of porous SiO_2 cathodes (1992);
- o operation of the cathode/resonant coupler in a round-beam power tube (1993)
- o operation of a 10 cm-long, 1 MW prototype gigatron to evaluate all key features of the ribbon beam and traveling wave coupler (1994).

Following these developments, we will be ready to build and test a 100 MW gigatron in 1995.

The discovery of copious field-emission from porous SiO_2 is a fundamentally new development in electronic phenomena. It is a result of reducing the scale length of the pore structure until it is comparable to the quantum mechanical wavelength of the emitted electrons. This remarkable new material has a number of unique optical and electronic properties (Appendix E) in addition to its performance as a field-emitter.

In a related (separately funded) spinoff of this research, we have developed the knife-edge chamber,^[6] an ultra-precise track chamber for use in Supercollider experiments. This development is described in Appendix B. We have used our cathode fabrication procedures to fabricate an active

cathode and grid-anode plane for a microscopic multi "wire" proportional chamber. It uniquely offers the performance in spatial resolution, live time, and radiation hardness needed for tracking in SSC detectors.

(Appendices A+B removed - reprint, & preprint)

Figure 1. Isometric view of ribbon electron beam and traveling wave coupler.

SEP 8 1991

POROUS SILICON AND SOME OF ITS PROPERTIES

Porous silicon was found in the 1950s by Uhler and Turner^[1] while studying the electropolishing of silicon wafers in dilute hydrofluoric (HF) acid solutions. Since then, this porous material has been widely studied by many investigators. This appendix describes the formation of porous silicon in concentrated HF and some properties of porous silicon from heavily doped silicon wafers.

A. Chemical Process

Formation of porous silicon layers on a silicon wafer is carried out by anodic oxidation in hydrofluoric acid as shown in Fig. C-1. The silicon wafer is connected to the positive terminal of a power supply so that it serves as the anode. A noble metal such as platinum is connected to the negative terminal, and serves as the cathode. The chemical reactions have been studied by a number of researchers [1-5]. In concentrated HF solution,

Fig.C-1 A diagram of anodic oxidation of silicon.

the disproportion reaction leading to the anodic dissolution of silicon occurs at the surface of a substrate. That is

where h represents a hole in silicon, and e represents an electron; $n < 2$ is a number which relates to conduction band and valence band efficiencies. Silicon difluoride, SiF_2 , is an unstable substance. It reacts with hydrofluoric acid forming silicic acid (H_2SiF_6) and hydrogen gas (H_2):

In the anodic oxidation, the presence of holes is essential. In P-type silicon, where the majority carriers are holes, the reaction can be carried out easily. However, in N-type silicon where majority carriers are electrons, holes must be otherwise introduced in order to carry out the anodic oxidation [1,3,4,6]. One way to do this is to illuminate the surface. Light with wavelength $\lambda < 1.2 \mu\text{m}$ can produce electron-hole pairs in a silicon substrate. High intensity illumination produces a large number of holes uniformly at the surface of the wafer. As the porous silicon layer grows, the efficiency of illumination drops because of the limited depth of penetration. Another way to generate holes is to supply sufficient voltage to the electrodes to cause avalanche breakdown in the space charge region. Since the N-type silicon is the anode, and the HF solution contacts the platinum cathode, the electrolyte-semiconductor system behaves much like an inverse-biased Schottky diode with the electrolyte serving the role of the "metal"[7]. The breakdown occurs when the cell voltage is raised to a critical value at which holes diffusing from the N-type silicon are accelerated in the space charge region to gain sufficient kinetic energy to produce hole multiplication. This occurs first at defects scattered through the single crystal and causes non-uniform etching.

B. Model of Formation

During the anodic dissolution, a porous layer is formed on the surface of the silicon wafer. A model of dissolution was suggested by Memming and Schwandt, and later modified by Unagami. The Memming-Schwandt model follows^[4]. In concentrated HF solutions, the divalent dissolution of silicon can be interpreted in the following steps.

1. The surface of silicon is covered with fluorine ions.
2. When an electric field is applied across the interface, holes move towards the surface.
3. Some of the holes are trapped at the surface, and they weaken the silicon-silicon bonds.
4. Thermal energy swings away the Si-F groups exposing the holes.
5. Fluorine ions occupy the holes and release their charges.

In the dissolution, Step 3 through Step 5 is repeated, and SiF_2 is removed from the reacting site. As a result, every dissolved silicon atom absorbs two holes which subsequently are occupied by two fluorine ions leaving two protons in the solution. These steps are shown in Fig. C-2 (a-e).

Unagami's study indicated some more details of the formation of the porous silicon film^[2].

1. An insoluble surface porous film exists at the surface of porous silicon layer. The film is formed by the deposition of elementary silicon at the early step of anodization.
2. There is no disproportionation reaction in the porous silicon layer below the surface. The anodic reactions only take place at the base of the pores.
3. The porous silicon layer is formed by the local dissolution which is initiated by the surface layer and is promoted by the hindrance layer composed of silicic acid.

Fig.C-2 The dissolution of a silicon atom in a concentrated HF solution.

Local etching or local dissolution is the cause of forming porous structure. The etching must be self-sufficient; otherwise, the reaction would proceed laterally across the wafer (electropolishing). Beside the hindrance layers of silicic acid, several other factors also contribute to the local etching: defect complexes, ionized impurities^[8], bubble branching^[9].

C. Density and Thickness

Current density plays an important role in the anodic reaction. While porous silicon is forming, its thickness and density are functions of current density. In the sense of microstructure, current density is one of the factors that control the pore size which will be mentioned later. Faraday's Law of electrolysis states that the quantity of dissolved silicon M is directly proportional to its equivalent weight w , to the current I , and to the time t .

$$M = wIt. \quad (C5)$$

$$M = A_1 \cdot X$$

$$I = A_0 \cdot j$$

where j = current density (A/cm^2), $\bar{A}_1$ = average porous area (cm^2), X = average thickness (μm) of porous silicon film, A_0 = the reacting area (cm^2). The density ρ_p of the porous layer can be related to that of solid silicon $\rho_s = 2.33 \text{ gm/cm}^3$ as

$$\frac{\rho_p}{\rho_s} = \frac{A_1}{A_0} = \frac{wjt}{X} \quad (C6)$$

Many researchers have studied the thickness and the density of porous silicon [2,5,6,10]. They collected experimental data under a wide range of process parameters (current, time, HF concentration) and devised models or

formulas for calculation. Unno et al. suggested an empirical model to calculate the thickness and the density of porous silicon^[11] as a function of time t:

$$X = k j^m t, \quad (C7)$$

$$\rho = \rho_s - (B/A_0 k) j^{1-m} - (C/A_0 k) t^n \quad (C8)$$

where X = thickness in cm. B, C, k, m, n are constants with values given in Table C-1.

TABLE C-1
Parameters of Equations C7 and C8.

HF Concentration	50 wt%	40 wt%	30 wt%
B	35	38	39
C	0.11	0.15	0.22
k	0.87	0.80	0.65
m	0.98	0.96	0.92
n	0.53	0.48	0.42

The equations were derived to fit experimental data in the following ranges: X - up to 25 μm , ρ - from 0.8 to 1.1 gm/cm^3 , J - up to 0.2 A/cm^2 , and t - up to 600 sec.

D. Pore Sizes and Microstructure

Porous silicon has the same crystalline structure as that of the parent wafer. [2,6,12] Quantitative analyses led to large values for specific surface area and sharp pore size distribution. Mean pore radii were found in the range 10-300 Å depending on the conditions: N-type or P-type material, doping level, current density, concentration of HF solution, reaction time. Table C-2 summarizes the measured pore diameter under several process conditions.

Generally, lower density corresponds to larger pore size, higher dopant concentration and larger current density relate to larger pore size. Although the range of pore size varies greatly from 10 to 300 Å, for each particular process conditions the distribution of pore diameters is

Table 4. Pore Sizes in Porous Silicon Films.

Author, Date and Reference	PSF Forming Conditions	Pore Diameter
Unagami et al. 1978 [2]	$T_{PSF} = 15 \sim 60\mu m, J = 30 \sim 100mA/cm^2$ P type (111) oriented	10 ~ 300 Å
G. Bomchi et al. 1983 [12]	$T_{PSF} = 80\mu m, J = 10 \sim 240mA/cm^2$ P ⁺ 0.01Ωcm, (111) oriented	20 ~ 100Å
Beale et al. 1984 [14]	$J = 30mA/cm^2, \rho = 49\%$ of ρ_{Si} P ⁺ 0.01Ωcm	150Å
Herino et al. 1985 [13]	$J = 80mA/cm^2, T_{PSF} = 20\mu m$ and $80\mu m$ P ⁺ 0.01Ωcm, (100) oriented	50 ~ 90Å
Beale et al. 1985 [12]	$J = 100mA/cm^2, T_{PSF} = 2 \sim 8\mu m$ P ⁺ 0.01Ωcm, (100) oriented	35Å
Yue 1988 [15]	$J = 80mA/cm^2, T_{PSF} = 40 \sim 100\mu m$ P type 0.007Ωcm, (111) oriented	18Å

rather sharp. Herino et al. analysed a 20 μm thick sample and an 80 μm thick one^[13]. The result showed that in both samples, the radii of pores were 25 to 45 $\text{\AA}$ with a mean value of 38 $\text{\AA}$.

Microstructure of porous silicon has been studied by several researchers^[12,13,14]. Photographs on cross-section TEM images of porous silicon film on heavily doped silicon were taken by Beale et al. (Fig. C-3). The structure pattern showed the films consisted of many long voids running perpendicular to the silicon surface, and with many small buds on the sides of the pores. Their study showed that the microstructure of the film was depth independent. Once the sidewall of a pore had formed, it was remarkably inert to further anodic attack. The interface of the substrate was planar with local unevenness on a scale comparable with the size of the pores. The study also showed the strong correlation between mass density and pore sizes of porous silicon.

Fig. C-3 Microstructure of porous silicon on heavily doped substrate [14].

E. Resistivity and Chemical Activity

Resistivity of porous silicon has been studied by a number of researchers^[2,12,14]. Beale et al. measured this in many different ways which included two and four terminal measurements of porous films formed on both N-type and P-type silicon with films both on and off their substrates, and employed various techniques for contact formation such as aluminum evaporation with and without sintering at 400°C, silver-loaded epoxy resin, and physical contact with a tungsten probe. In all the measurements they made, the resistivity of porous silicon was found to be greater than 10^5 ohm-cm. They also found the resistivity was dependent of illumination and the ambient temperature. The resistivity of a porous silicon film is observed to gradually increase in the atmosphere at room temperature due to slow oxidation.

Porous silicon film has very active chemical properties because it has a huge specific surface area and a weak bonding of silicon at the residual single-crystal silicon surface. The average value of specific area in porous silicon was reported to be $200 \text{ m}^2/\text{cm}^3$ ^[12] which is 200,000 times greater than that of a bulk silicon wafer. The surface energy of a sample of 1 cm^2 with a $10 \text{ }\mu\text{m}$ thick porous was 0.2 J ^[13] which is 2,000 times greater than that of bulk silicon. Therefore, porous silicon film can react with water, alcohol, and even toluene at room temperature, releasing hydrogen gas. While reactions of normal silicon with dilute sodium hydroxide and with concentrated nitric acid are not observable, porous silicon film can dissolve in dilute NaOH solution quickly, and it reacts with concentrated HNO_3 with explosive violence. The oxidation of porous silicon film is also much faster than that of bulk silicon. One study showed that 300°C was sufficient to oxidize the entire porous silicon film in dry oxygen^[6]. It was observed that at 1000°C, a $5 \text{ }\mu\text{m}$ thick porous

silicon film was entirely oxidized in less than 2 minutes in wet oxidation^[10]. Once it is oxidized, the film becomes very stable both in chemical activity and physical structure. It also becomes a good insulator. Because of these properties, oxidized porous silicon has been used as an insulator in integrated circuit technology.

REFERENCES (APPENDIX C)

1. A. Uhlir, Jr., "Electrolytic shaping of germanium and silicon," Bell System Technical Journal, vol. 35, pp. 333-347, 1956.
2. T. Unagami, "Formation mechanism of porous silicon layer by anodization in HF solution," Journal of the Electrochemical Society, vol. 127, pp. 476-483, 1980.
3. D.R. Turner, "Electrolytic etching of semiconductors," in The Surface Chemistry of Metals and Semiconductors. Harry C. Gatos, ED. New York: John Wiley & Sons, Inc., 1960, Part III, chap. 3, pp. 285-310.
H. Gerischer, "On the role of electrons and holes in surface reaction on semiconductors," Surface Science, vol. 13, pp. 265-278, 1969.
4. R. Memming and G. Schwandt, "Anodic dissolution of silicon in hydrofluoric acid solutions," Surface Science, vol. 4, pp. 109-124, 1966.
5. Y. Arita, "Formation and oxidation of porous silicon by anodic reaction," Journal of Crystal Growth, vol. 45, pp. 383-392, 1978.
6. Y. Arita and Y. Sunohara, "Formation and properties of porous silicon film," Journal of the Electrochemical Society, vol. 124, pp. 285-295, 1977.
7. S.K. Ghandhi, VLSI Fabrication Principles. New York: John Wiley & Sons, 1983.
8. R. Tenne, V. Marcu, and N. Yellin, "Evidence for nonuniform flow of charge carriers through semiconductor junctions," Applied Physics Letters, vol. 45, pp. 1219-1221, 1984.
9. H.A. Tenhunen, "Formation of anodic porous film on silicon for silicon-on-insulator VLSI structures," Dissertation, Department of Electrical Engineering, Cornell University, 1986.

10. Y. Watanabe, Y. Arita, T. Yokoyama, and Y. Igarashi, "Formation and properties of porous silicon and its application," Journal of the Electrochemical Society, vol. 122, pp. 1351-1355, 1975.
11. H. Unno, K. Imai, and S. Muramoto, "Dissolution reaction effect on porous-silicon density," Journal of the Electrochemical Society, vol. 134, pp. 645-648, 1987.
12. G. Bomchil, R. Herino, K. Barla, and J.C. Pfister, "Pore size distribution in porous silicon studied by adsorption isotherms," Journal of the Electrochemical Society, vol. 130, pp. 1611-1614, 1983.

M.I.J. Beale, N.G. Chew, M.J. Uren, A.G. Cullis, and J.D. Benjamin, "Microstructure and formation mechanism of porous silicon," Applied Physics Letters, vol. 46, pp. 86-88, 1985.
13. R. Herino, A. Perio, K. Barla and G. Bomchil, "Microstructure of porous silicon and its evolution with temperature," Materials Letters, vol. 2, No. 6A&B, pp. 519-523, 1984.
14. M.I.J. Beale, J.D. Benjamin, M.J. Uren, N.G. Chew, and A.G. Cullis, "An experimental and theoretical study of the formation and microstructure of porous silicon," Journal of Crystal Growth, vol. 73, pp. 622-636, 1985.

K. Barla, J.J. Yon, R. Herino, and G. Bomchil, "Oxide formation from porous silicon layers on p-substrates," in Insulating Films on Semiconductors. J.J. Mimonne and J. Buxo, ED. New York: Elsevier Science Publishers B.V., 1986, chap. 2, pp. 53-56.
15. W.K. Yue, "Electron Field Emission in Porous Silicon," Dissertation, Department of Electrical Engineering, Texas A&M University, 1991.

APPENDIX D

CURIOSA WITH POROUS SiO_2 CATHODES

In exploring the field-emission properties of porous SiO_2 cathodes, a considerable range of pore size and porous layer thickness was studied. One region of process parameters produced excellent cathodes for gigatron and other e -beam applications; those results are presented in Section II. Two other parameter regions were identified which do not perform well as cathodes, but do exhibit remarkable properties which may be of considerable interest for other applications. They are produced when the current density is reduced (reduced pore diameter, low pore density), and when the reaction time is reduced to make a very thin porous layer.

The wall effect. For samples with narrow pore width and low pore density, thick dielectric walls separated adjacent pores. During field emission, electrons charged the walls and built up a space charge (Fig. D-1). With this built-up charge, the current grew slowly as voltage increased. However, when the applied field reached a critical value which overcame the maximum space charge, current rapidly increased, exhibiting negative resistance. Several causes may contribute to this phenomenon. One cause may be that the high applied field creates a tunnel in the space charge region or thins this region so that electrons can tunnel through. A second cause may be that under sufficiently high external field the electrons obtain enough energy to generate secondary electrons when they strike the wall. The wall charge and the negative resistance effects are shown for Sample #313 in Fig. D-2. In some instances the negative resistance caused high-frequency oscillation, probably at a resonant frequency of charging and discharging in the pores.

(a)

(b)

(c)

(d)

Fig.D-2 Photographs of the I-V curves with negative resistance.

Fig. D-1 A diagram of the wall charges.

The memory effect. For samples with wide pore widths and shallow porous layers, the deposition of the metal film is very close to the silicon substrate. A phenomenon of nonvolatile memory was observed. At high voltage the metal (anode) and the substrate (cathode) shorted. In this case, the anode current was externally limited to avoid permanent damage of the diode by excessive power dissipation. The diode remained a short circuit at low current and after the modulation was removed. If a higher current was applied on the shorted diode at low voltage, the anode and cathode returned to an open circuit. The diode remained open at low voltage and after the modulation was removed. These I-V relations were repeated many times. An example is shown for Sample #169 in Fig. D-3. Fig D-3a shows an "off" state. The device remains off until the applied voltage reaches 37 volts when it suddenly turns on. Fig. D-3b is an "on" state until the current reaches 9 mA when the device suddenly turns off.

(a) The memory logic OFF state.

(b) The memory logic ON state.

Fig.D-3 Photographs of the I-V curves with the memory effect.

We do not adequately understand this phenomenon. It is clearly a consequence of reducing the anode-cathode gap to a breakdown limit. We have observed reversibility over several hundred on/off cycles, suggesting that the device might possibly be useful as a sub-micron bistable memory element, switchable at CMOS voltage levels. We plan to further study the memory effect during the coming year in an effort to understand its physical origin and its durability.

Figure 1-1. Electron gun for FEA cathode tests.

END

**DATE
FILMED**

10/2/191