A CHARGED PARTICLE DETECTOR SYSTEM FOR HIGH RATE EXPERIMENTS

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This paper describes a charged particle detector system under development at BNL for use at the Multi-particle Spectrometer (MPS) and eventually at ISABELLE. The object is to take full advantage of the position accuracy, resolving time and instantaneous rate capabilities of narrow anode spacing drift-proportional chambers.

The system will have position resolution $\sigma \approx 100\mu$, time resolution ≈ 8 ns, detector sensitive time ≈ 50 ns, and consecutive particle resolving power of 40 ns per wire. We plan to implement this system in a large system of 30,000 wires at the MPS and greater than 100,000 wires in ISABELLE experiments.

Central to the development of this detector system is the production of two custom integrated circuits. First I will describe the detectors.

Drift Proportional Chambers

The basic detector is a narrow anode spaced drift chamber with field wires, Fig. 1. The drift time

Fig. 1 Drift Proportional Wire Chamber

between field and anode wires 2 mm apart is about 40 ns with argon-isobutane. Thus it is important to quantize the time measurement in 4 ns intervals which with the diffusion time spreading will give a position measurement standard deviation of 100μ . This type of drift chamber is capable of fully efficient operation in magnetic fields above 10 Kgauss.

The MPS drift chambers will be modules containing a super x-measuring chamber with 4 mm anode spacing which will have 5 mm cathode strips at $\approx 30^\circ$ to the anode. These cathode strips give two stereo views of the avalanche which is at the anode and thus in time with the anode signal. With either a three-fold gate array or a simple microprocessor algorithm this gives three dimensional points of each hit which are at the same time within a few nanoseconds. The active area of this chamber will be 1 meter high by 1.5 meters wide. The projected error in Y of these three projected measurements is $2 \times .5$ cm or 1 cm which should be adequate for track finding but is not accurate enough to measure the track angle. So included in this module will be a Y measuring drift chamber also with 4 mm anode spacing. In addition, to resolve the right-left ambiguity, an additional x-chamber and a y-chamber without cathode readout located adjacent to their partner but staggered by 1/2 wire spacing will be employed.

Electronics System

The electronics is divided into two subsystems. An amplifier-shaper-discriminator followed by a digital delay-time encoder register.

Fig. 2 is a block diagram of a hybrid version under development for us by Amperex. It uses standard

Fig. 2 8-Channel Hybrid Amplifier-Shaper-Discriminator

IC chips equivalent to packaged IC's we've been using for years. Thus the performance of this subsystem is known and is shown in Table I. Eight channels are

TABLE I

Amplifier - Discriminator Specifications 8 Channels per Hybrid

Amplifier

Gain $X100 \pm 20$
Bandwidth - 3 db at greater than 80 MHz
Small signal risetime less than 6 ns
Delay match in package ± 2 ns
Input noise at 100 Ω less than 40 μ v rms

Differentiating Network

1K resistor tolerance $1K \pm 10\%$
15 pF capacitor tolerance 15 ± 5 pF

Discriminator

Time slewing less than 3 ns for 20 to 100 mv overdrive
Delay less than 15 ns at 20 mv overdrive
Delay match in package within 3 ns for 20 mv overdrive
Offset match in package - all units within 3 mv
Output - Standard ECL with 100 Ω to -2 volts

Package: Metal top cover tied to ground pin on 40 pin DIP

Diodes 1N3062 or equivalent
100 Ω resistors are $\pm 20\%$ and must withstand the discharge of a 100 pF capacitor from 5Kv

packaged in one 40-pin DIP shown in Fig. 3. This configuration allows a printed circuit board along the frame edge of the drift proportional chamber described above that can mount adjacent hybrids at 1.6 inch intervals in the plane of the frame. This eliminates connectors between the anode wires and the amplifier-discriminator electronics. The hybrids will be mounted on sockets to facilitate replacement of defective circuits. These hybrids cost \$6.50 per channel

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in 5000 channel quantities.

8 CHANNEL AMPLIFIER-DISCRIMINATOR HYBRID

Fig. 3

Simultaneously with the development and production of these hybrids is an engineering study of a custom IC capable of even greater sensitivity and operating at a lower power level. Packaged two to a standard 14-pin DIP, preliminary estimates indicate this circuit would be less expensive for systems containing more than 30,000 wires.

The digital delay-time encoder register subsystem is the key to achieving the inherent capabilities of narrow anode spacing drift proportional chambers. Fig. 4 is a block diagram of this subsystem. Standardized

Fig. 4

Digital Delay Time Encoder Register

pulses of 10 to 15 ns width enter a 226-bit long serial shift register that is clocked at 250 MHz. Following this long shift register is some routing logic and a 32-bit shift register. One microsecond after an event of interest has passed through the drift-proportional chamber the 250 MHz clock is stopped leaving the time history of that event stopped in the 32-bit shift register segments. At this time control logic is used to connect the 32-bit pieces in series. Then the 250 MHz clock is turned back on and the desired event comes out serially at 128 ns per wire. In this way a one meter wide chamber can be read out in 32 μ s. Since data handling capabilities of large spectrometers are limited to a few hundred events per second the shift registers of ten or more such chambers will be connected in series.

It is obvious that this custom IC requires state-of-the-art technology. Two approaches are under study. One is to design 2 or 4 way multiplexed shift registers using processes currently in production. For example a 4-phase version operating at 63 MHz still gives 4 ns resolution but can readily be made with V-MOS, D-MOS

or N-channel SOS design rules. A two-phase system illustrated in Fig. 5 presses the current MOS techno-

Fig. 5 Two-Phase Digital Delay-Register

logy a bit but the simplified clock control systems will probably justify the effort to engineer this system. Fig. 6 is a proposed pinout that would allow direct coupling on the same printed circuit that has the amplifier-discriminator hybrids. This arrangement would eliminate the need for a connector pair for each chamber wire and drastically reduce the system cabling cost. Table II is a preliminary set of specifications for this IC.

TABLE II

Digital Delay - Register IC

Inputs:

Inputs (I), Serial In (SI) and Control (Ct)
Single ended ECL
Capacitive loading less than 5 pF
Current sink or source less than .1 ma

Clock (Cl)

Differential ECL
Capacitive loading less than 5 pF
Current sink or source less than .1 ma

Outputs (SO)

Differential ECL to drive 100 Ω at -2 volts

Shift Registers - Dynamic

Maximum clock rate at least 125 MHz
Minimum clock rate without losing data 10 KHz
Input setup time less than 4 ns before leading edge of clock
Propagation delay through AND-OR gates - fast enough that 16 bit shift register maintains synchronization to at least 125 MHz
Temperature range 0 - 50°C
Vcc 1, 2 - whatever is required $\pm$ 5%
Package - 22 pin plastic DIP

DIGITAL DELAY-TIME ENCODER IC

Fig. 6

Recent developments in silicon gate SOS raise the prospect of 300 MHz shift registers operating at low logic levels and very low power. An active effort is under way to apply this technology. It should be noted that once a custom IC of this type is in production the cost would be \$2-\$4 per channel.

In conclusion, I have described a detector-electronic system under development at BNL which utilizes the inherent capabilities of narrow anode spacing drift proportional chambers to resolve position to 100 μ , time to better than 10 ns, and suffer dead time losses limited only by the physics of the drift proportional chamber. This type of detector will be essential for many experiments at high event rates such as those planned for ISABELLE.

Footnote

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