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Laboratory Test System

By G. L. Asher

MASTER

Published March 1980

Final Report

Prepared for the United States Department of Energy
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**Kansas City
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By G. L. Asher

Published March 1980

Final Report
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LABORATORY TEST SYSTEM

BDX-613-2368, Final Report, Published March 1980

Prepared by G. L. Asher

A laboratory test system was developed to perform automated electrical testing on electronic components. Test and analysis capabilities were made versatile to permit easy adaption to various product designs. This flexibility provides test methods for prototype hardware and for evaluating new product designs.

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SUMMARY

This project was initiated to develop a laboratory test capability for evaluating new and existing digital product designs. In recent years, Bendix Kansas City has become more active in supplying early development hardware to the design laboratories for evaluation. Because of the more complex electronic designs being used in new components, more highly automated test systems are needed to evaluate development hardware.

To meet this requirement, a universal test system was developed to provide both basic test capabilities and flexibility to adapt easily to specific product applications. This laboratory evaluation system will reduce the need to develop complex dedicated test systems for each new product design, while still providing the benefits of an automated system.

A special purpose interface chassis was designed and fabricated to permit a standardized interface between the test system and the product application. Connector assignments by system functions provide convenience and function isolation. Standard cables were used to reduce the need for special purpose hardware.

Electrical testing of a developmental electronics assembly demonstrated the adaptability of this system for a typical product application. Both the interface hardware and the software were developed for this application.

DISCUSSION

SCOPE AND PURPOSE

Work had previously been done to acquire most of the basic instruments and equipment needed for a laboratory tester. The purpose of this project was to structure the system's hardware and software architecture to provide a universal test system for product testing and design evaluation.

ACTIVITY

System Hardware

The goal for the test system hardware architecture was to provide capability for fully automated testing and to retain versatility for adaptation to many product applications. This required the structure to be flexible enough to accommodate future expansions, as new requirements are identified.

The test system (Figure 1) is structured with the DEC PDP-11/34 minicomputer as the system controller. All instruments are fully programmable, which permits control of their operation by means of software. Direct access to the instruments also has been provided. This feature allows for individual non-automated operation at the user's option and provides the flexibility needed in a laboratory environment to build simple test setups quickly.

The PDP-11/34 is provided with peripheral equipment (Figure 2) for convenient interaction with the test system. Magnetic disks and paper tape equipment provide permanent program and data storage. Two CRT terminals and a DECWRITER II printer are available for the operator to communicate instructions to the test system. System response may be displayed on these terminals or may be sent to a peripheral line printer for hard copy output.

The instrument's interface with the PDP-11/34 minicomputer is made through the Bendix-developed expanded input/output port chassis which contains 40 addressable 16-bit, three-state registers.

Programmable power and signal sources (Figure 3) have been provided for use as driving functions. These include two Sorenson (60 V, 30 A) and four Fluke (65 V, 1 A) programmable power supplies and six Burr-Brown voltage sources. Six 12-bit digital-to-analog converter channels with a ± 10 V output range are also provided. The HP8015A is a dual output, 50-MHz pulse generator with programmable output amplitude and pulse shaping capability.

Figure 1. Test System Block Diagram

Figure 2. Test System Peripheral Equipment

Figure 3. Test System Mainframe Chassis

A Dana 4700 digital multimeter has been incorporated to provide dc voltage, ac voltage, and resistance measurement capability. This permits direct measurements of dc and ac voltages up to 1000 V and provides 1 μ V resolution on the lower scale. Four wire resistance measurements from 1 m Ω to 100 M Ω can be made. Analog-to-digital converters were included to provide higher speed dc voltage measurements. The test system contains 32 channels with 12-bit resolution for a ± 10 V input range.

Digital data can be communicated between the product application and the test system through input/output ports. Three each 16-bit input and output ports are provided at the interface chassis front panel.

A total of 80 relays have been incorporated in the test system which may be used for switching signals and load control. The relays are mounted in the interface chassis, and their coils are actuated by computer-controlled relay driver circuits.

The interface chassis (Figure 4) was designed to provide a standardized interface panel between the test system and the specific product applications. Tester hardware functions are accessible from this chassis through front panel connectors. Selected functions also have been brought out through plug-in jacks which permit simple patch cord test setups to be made easily.

System Software

The task in developing the software was to write a software routine for each programmable instrument that would allow complete control of the instrument from application programs. This software had to be developed in parallel with the system hardware development and still meet the time objectives of this project.

The RT-11 was chosen as the initial operating system for the test system. This system appeared to provide the means to evaluate the laboratory test system's potential usefulness, and it could be implemented within the scope of this project. The RT-11 is a small, easy-to-use, single-user system that supports all DEC peripheral devices. In addition, it allows direct manipulation of the input/output registers where the communication between the program and the instruments take place. This system allowed the most straightforward handler programming and debugging. It also provided a good basis on which to develop an initial application program. In addition, several RT-11 handlers already existed because of prior development work.

The RT-11 operating system provided numerous utility routines which greatly expedited the software development effort. These

Figure 4. Test Setup

routines include the text editor, the FORTRAN compiler, the MACRO assembler, the linker, the subroutine library facility, the file manipulating routines, and a debugging aid.

Each instrument handler was written in MACRO-11 assembly language to provide maximum execution speed and optimum bit manipulation capabilities. Each routine conforms to the PDP-11 FORTRAN calling convention, that is, they are callable by FORTRAN statements.

FORTRAN was chosen for the primary application language over both BASIC-11 and MACRO-11. FORTRAN lies approximately midway, speed-wise, between BASIC and MACRO. It is roughly 10 times faster than BASIC and 10 times slower than MACRO. FORTRAN provides the software power of a high level language and has a faster execution speed than BASIC. Furthermore, FORTRAN is a much easier language to learn than MACRO assembly language and is one in which the potential users are more likely to have had some experience. While BASIC may have obvious benefits for some applications, it is believed that FORTRAN is the better choice for the medium and large test routines that are likely to be used for general development testing applications. The vast majority of the application programs probably will be written in FORTRAN, using subroutines called from the system and user libraries. If the execution speed of FORTRAN becomes too slow to meet test requirements, special purpose assembly language routines can be written which may resolve the timing problems. These routines will execute at assembly language speed and are callable from a main line FORTRAN program using the standard subroutine CALL procedure. FORTRAN coding is generally very readable, and with the liberal use of comment statements, the software can be documented conveniently within the applications program coding. This can save considerable time in making program modifications to accommodate new sets of test conditions.

Test Implementation

The electronics assembly selected to demonstrate and to evaluate the adaptability of the test system for testing developed hardware contains both linear circuits, which provide regulated outputs to other system components, and digital circuits, which detect and decode complex digital bit patterns. One of the objectives of this effort was to demonstrate that a development test program could be implemented on the test system to support development testing until production test equipment becomes available.

Developing the subassembly test capability on the system involved:

- Establishing a test approach for each set of test conditions required,

- Developing the necessary dedicated interface hardware, and
- Developing the application software needed to perform the test.

Generally, a complete product test system would have a block diagram similar to that shown in Figure 5. The hardware implementation of the block diagram for the test assemblies is presented in Figure 4. This figure shows the tester's interface chassis, the dedicated application hardware, and the product being tested.

The software for testing the assemblies was modularized at the test levels identified in the development specification. Each test was written as a FORTRAN subroutine, which can be executed individually or used in conjunction with other subroutines and thereby developing larger test sequences. Figure 6 shows a simplified flow diagram for the test sequence. A description of the implementation of one of the regulator tests, including some of the software listings, is included in the Appendix.

Development test requirements for the assemblies were successfully implemented using the test system. Prior to this capability, development testing had been performed using a manually-operated test setup. Implementing the testing on this equipment provided a totally automated system. This reduced the unit testing time and provided better control of applied test signals for identifying unit-to-unit variations. Since most of the parameters are software controlled, this system has the flexibility to respond to new test requirements and to perform worst-case circuit analysis as the design evolves during the development phase of an electronic assembly.

ACCOMPLISHMENTS

A laboratory test system has been developed to provide test capability and design analysis for supporting early development hardware. This system allows the operator to automate testing, which provides more reliable test results and reduces the testing time. The software is modularized into handler routines, which control instruments and manipulate data. This provides a flexible, but simple, user-oriented system for constructing test programs.

A product application was selected to demonstrate the system's use and to evaluate the system's flexibility. The test requirements were implemented for printed wiring assembly and final assembly testing of the development hardware. Dedicated interface hardware was assembled to provide the interface between the interface chassis and the product under test. The applications software was written which performed the required tests. This

Figure 5. Generalized Applications Block Diagram

Figure 6. Test Sequence Flow Diagram

proved to be a more flexible and efficient approach in providing test capability for the development hardware.

FUTURE WORK

The laboratory test system will provide a versatile laboratory tool to support development testing and design evaluations on complex digital electronic assemblies. The present system provides the basic capability to perform automated testing of electronic components.

As more complex component designs evolve, additional analysis capability will have to be incorporated into the test system. The system has been designed to accommodate future capability expansions with minimal effort. Future expansion will be directed by the type of analysis required on new component designs.

As the need arises to support more users, the present single-user operating system (RT-11) will become inadequate to handle the expected workload. For this reason, it is proposed that a multi-user system be incorporated which will allow software development and product testing to proceed simultaneously on a time sharing basis. The RSX-11M operating system is a multi-user system with good potential for this application.

Appendix

REGULATOR CIRCUIT TEST

Introduction

The following describes the implementation of one of the tests performed on the regulator circuit in an electronic assembly. The intent of this description is to give an example which will show a typical approach and which will demonstrate some of the capabilities of the test system.

Figure A-1 shows a simplified block diagram of the circuit function being tested and the dedicated interface hardware developed to implement the test. Two input signals (J-INPUT and K-INPUT), shown in Figure A-2, are applied to the unit under test. These signals result in the expected L and M OUTPUT responses shown in Figure A-3. The test requires verification of the following measurements and conditions.

- Measure the voltage at L-OUTPUT when the load switches are in the following states:
 - S1-open, S2-open;
 - S1-closed, S2-open; and
 - S1-open, S2-closed.
- Measure the voltage at M-OUTPUT with K-INPUT both high and low.
- Measure the times (T_1 through T_4) of the L-OUTPUT signal defined in Figure A-3.
- Measure the propagation delays (T_5 and T_6) on the M-OUTPUT signal defined in Figure A-3.
- Monitor the voltage at L-OUTPUT to ensure that operation of the load switches (S1 and S2) do not cause transients which exceed acceptance limits.
- The above conditions are to be tested at three different levels on the J-INPUT and K-INPUT voltage amplitude.

Test Solution

One objective in approaching a test solution was to minimize the dedicated hardware needed by using the test system hardware and software capabilities. All the pulse width and pulse sequencing on the J-INPUT and K-INPUT pulses are controlled by the two

Figure A-1. Test Number 2, Block Diagram

Figure A-2. Input Pulse Sequence

TIMING DIAGRAM NOT DRAWN TO SCALE

Figure A-3. Test Number 2, Timing Diagram

programmable clocks (PCLOCK) in the PDP-11/34 minicomputer. Since these clocks are under software control, timing changes may be made by software changes only. The L and M OUTPUT voltages are measured using the analog-to-digital (A/D) converter channels appropriately scaled with resistive attenuator networks.

The external load switches (S1 and S2) are provided by the test system's relays located in the interface chassis and operated under software control. Timing of these switches is controlled from the tester's programmable clocks.

The propagation times (T_5 and T_6) were measured using a hardware counter located in the dedicated hardware interface adapter. Gating and enable of the counter is under software control through a bit set on OUTPUT PORT number 1. This allows the same counter circuit to be used to measure the four propagation times. The counter value is read into the computer and converted to time by a software calculation.

The L OUTPUT risetime measurements were made using one of the tester's programmable clocks. Figure A-4 shows a diagram of the implementation for this measurement. The PCLOCK is initially set for 10 ms with a selected resolution of 10 μ s. This clock is started counting down by the program software. The output levels of interest are detected with hardware level detectors, which generate interrupts to the computer. The computer services the interrupts by reading the current value of the PCLOCK and storing its value. The L OUTPUT times (T_1 through T_4) are then computed from these stored readings as indicated in Figure A-4.

A hardware monitor was used to verify that the L OUTPUT remained within the specified voltage range. Level detectors set to trigger at the lower and upper limits are used to set a status latch if an out-of-limits conditions is detected. The state of this latch is checked by software at the end of the pulse sequence to give a pass/fail indication in the test results.

Hardware

Figure A-1 is a block diagram showing the dedicated hardware which was designed to implement this test. Design of this hardware was made considerably simpler since all the timing controls were implemented in the software.

A discrete transistor switch design was used to apply the voltage from the programmable power supplies to the J- and K-INPUT. The state of these switches is changed under software control to generate the required pulse sequences.

The voltage level on the input and output signals needed to make timing measurements are detected using hardware voltage comparators. The output of these detectors are used to drive interrupt

DEFINING EQUATIONS:

$$T_1 = (CNT\ 2 - CNT\ 3) \times 10\ \mu s$$

$$T_2 = (CNT\ 2 - CNT\ 4) \times 10\ \mu s$$

$$T_3 = (CNT\ 2 - CNT\ 5) \times 10\ \mu s$$

$$T_4 = (CNT\ 1 - CNT\ 5) \times 10\ \mu s$$

Figure A-4. L Output Timing Diagram

lines for making the L OUTPUT timing measurements and to gate the propagation counter circuit.

A dedicated hardware counter circuit was designed to make the propagation time measurements (T_5 and T_6). This circuit was used in order to get the resolution needed for measuring times in the 1 to 10 μ s range. The counter operates from a 5 MHz clock. The gating of the counter is provided by logic circuitry which allows the counter to run during the T_5 and T_6 times. Reset and enable of the counter is under software control from the PDP-11/34. The count value is read into the PDP-11/34 through INPUT PORT number 1. This count value is converted to time by software calculations.

Software

Applications program for performing this test is written as a FORTRAN subroutine to be called from a main program. A simplified flow diagram of this subroutine is shown in Figure A-5. The subroutine itself consists mainly of FORTRAN calls to the system library. Figure A-6 is a complete listing of subroutine REG2. Liberal use of comment statements and line comments have been used to make the coding more readable.

REG2 also contains two special purpose assembly language routines, DR11K2.MAC and TRAIN.MAC, which are callable from the FORTRAN subroutines. These routines are written in MACRO-11 assembly language coding in order to speed up the execution of this portion of the software. The same operations could be performed using the generalized calls available in the system library; however, in this case the slower execution time cannot be tolerated. Figure A-7 shows a listing of DR11K2.MAC that was used to set up and service the interrupts occurring during the L OUTPUT time measurements. The assembly language routine, TRAIN.MAC, generates the K-INPUT pulse train shown in Figure A-2 and measures the propagation times T_5 and T_6 . Listing for this routine is given in Figure A-8.

Figure A-9 shows a hard copy printout of a test run on the regulator circuit. The output format is specified using FORTRAN WRITE statements, which allow the descriptors as well as measured parameters to be printed.

Figure A-5. Test Number 2, Flow Diagram

```

1      SUBROUTINE REG2
2 C
3 C      SUBROUTINE      REGULATOR TEST 2
4 C
5 C
6 C
7 C
8 C
9      INTEGER*2 TT,ARRAY(4),ITIME(5),ULL,OHL
10     REAL LOU(3),ML,MH,VL(3),PTIM(4),VML,VMH,T(4)
11     DATA ARRAY/4*0/
12     COMMON /RSTIME/ ITIME
13 C
14     TT=5
15     LP=6
16 C
17 C      INITIALIZE HARDWARE
18 C
19     CALL ZERO
20     WRITE(TT,900)
21 900   FORMAT(///,T50,'TEST 2',/,T40,'VOLTAGE REGULATION',/)
22 C
23 C      PRESET HARDWARE
24 C
25     N=0
26 10    N=N+1                !INC WHEN INPUTS CHANGE
27     CALL FLUKE (4,5.0)
28     CALL RELAY(49)        !APPLY 5V TO LOAD BOX
29     IF(N.NE.1) GOTO 20    !N=1; INPUTS=MAX VALUES
30     CALL FLUKE(1,32.5)    !K PULSE SOURCE
31     CALL SOREN(1,32.5)    !J PULSE SOURCE
32     GOTO 40
33 20    IF(N.NE.2) GOTO 30    !N=2; INPUTS= MIN VALUES
34     CALL FLUKE(1,21.5)    !K PULSE SOURCE
35     CALL SOREN(1,22.3)    !J PULSE SOURCE'
36     GOTO 40
37 30    IF(N.NE.3) GOTO 110   !N=3; INPUTS= NOM VALUES
38     CALL FLUKE(1,28.0)    !K PULSE SOURCE
39     CALL SOREN(1,28.0)    !J PULSE SOURCE
40 40    CONTINUE
41 C
42 C      INITIALIZE RELAYS
43 C
44     CALL RELAY(44,62,63)   !SHORT SOURCE RES
45     CALL RELAY(10,64)      !CONNECT L,M LOADS
46     CALL RELAY(46,61)      !APPLY PWR TO J,K DRVS

```

Figure A-6. Subroutine REG2 Program Listing

```

47 C
48 C      DELAY 3 SECONDS FOR SETTLING OF RELAYS AND SOURCES
49 C
50      CALL DELAY(3.0)
51      CALL LCDSBL
52 C
53 C      THIS SECTION CONTROLS OPERATION FROM START OF J INPUT
54 C      PULSE TO END OF K INPUT HEADER PULSE
55 C      ITIME - ARRAY WITH COUNT VALUE OF P-CLOCK 2 AT
56 C      HARDWARE INTERRUPTS
57 C
58 C
59 C      ENABLE IN-1 INTERRUPT LINES 0-4, SET UP DR11-K FOR INTERRUPTS
60 C
61      CALL INENBL("37)
62      CALL SETK2
63      CALL PCSET(1,0,1,10)          !SET TO 1MS
64      CALL PCSET(2,0,0,1000)       !SET TO 10MS
65 C
66 C      RAISE J-INPUT LINE <BIT0 OF OUT1>
67 C      WAIT FOR 1 MS
68 C
69      CALL OUT1("1)
70      CALL PCSTR(1)
71      CALL PCWAIT(1)
72 C
73 C
74 C      START CLOCK 2 FOR 10MS -- RAISE K-INPUT LINE
75 C
76      CALL PCSTR(2)
77      CALL OUT1("3)
78 C
79 C      WAIT FOR 10MS -- SERVICE ALL RISETIME INTERRUPTS
80 C      READ M OUTPUT WITH ADAC CHANNEL 2
81 C
82      CALL PCWAIT(2)
83      CALL ADACR(2,IRAW)           !READ M OUTPUT LEVEL
84 C
85 C      -- LOWER K-INPUT -- DISABLE ALL IN-1 INTERRUPTS
86 C
87      CALL OUT1("1)
88      CALL INDSBL("177777)
89 C
90 C      THIS SECTION CONTROLS OPERATION FOR 35MS AFTER HEADER PULSE
91 C
92      CALL PCSET(2,0,1,350)        !SET TO 35MS
93      CALL PCSTR(2)
94      CALL OUT1("11)               !RESET WINDOW DETECTOR LATCHES

```

Figure A-6 Continued. Subroutine REG2 Program Listing.

```

95      CALL OUT1(*1)                !ENABLE WINDOW DETECTOR
96 C
97 C      MH=ATTENUATED VOLTAGE READING OF M OUTPUT WITH K-INPUT HIGH
98 C      ML=ATTENUATED VOLTAGE READING OF M OUTPUT WITH K-INPUT LOW
99 C
100     CALL ADACC(2,IRAW,MH)          !CONVERT ADAC TO VOLTS
101     CALL ADAC(1,LOUT(1),1)        !READ L OUTPUT LEVEL, 2V RANGE
102 C
103 C      LOUT(1)=ATTENUATED VOLTAGE READING ON L OUTPUT
104 C      WITH S1-OPEN; S2-OPEN
105 C
106     CALL ADAC(2,ML,1)              !READ M OUTPUT LEVEL, 2V RANGE
107     CALL PCWAIT(2)                 !TIME=HEADER PUL + 35MS
108 C
109 C      THIS SECTION CONTROLS OPERATION DURING K INPUT PULSE TRAIN
110 C      "ARRAY" STORES VALUE OF M OUTPUT PROPAGATION DELAY COUNTER
111 C      PROPAGATION DELAY COUNTER RESOLUTION IS .2 MICROSECONDS
112 C
113     CALL TRAIN(ARRAY)
114 C
115 C      THIS SECTION COMPLETES TEST AFTER PULSE TRAIN
116 C
117     CALL PCSET(1,0,1,20)           !SET TO 2MS
118     CALL PCSTRT(1)
119     CALL ADAC(1,LOUT(2),1)         !READ L OUTPUT LEVEL, 2V RANGE
120 C
121 C      LOUT(2)=ATTENUATED VOLTAGE READING ON L OUTPUT
122 C      WITH S1-CLOSED; S2-OPEN
123 C
124     CALL PCSET(2,0,1,400)          !SET TO 40MS
125     CALL PCWAIT(1)                 !TIME TO OPEN LOAD SW S1
126     CALL PCSTRT(2)
127     CALL RELAY(-47)                !OPEN S1 LOAD SW
128     CALL PCSET(1,0,1,300)          !SET TO 30MS
129     CALL PCWAIT(2)                 !TIME TO CLOSE LOAD SW S2
130     CALL PCSTRT(1)
131     CALL RELAY(48)                 !CLOSE S2 LOAD SW
132     CALL PCSET(2,0,1,300)          !SET TO 30MS
133 C
134 C      LOUT(3)= L OUTPUT LEVEL WITH S1-OPEN, S2-CLOSED
135 C      ADAC SAMPLES 30MS AFTER S2 CLOSES
136 C
137     CALL PCWAIT(1)                 !10MS DELAY
138     CALL PCSTRT(2)
139     CALL ADAC(1,LOUT(3),1)         !READ L OUTPUT LEVEL, 2V RANGE
140     CALL PCSET(1,0,1,200)          !SET TO 20MS
141     CALL PCWAIT(2)                 !TIME TO OPEN LOAD SW S2
142     CALL PCSTRT(1)

```

Figure A-6 Continued. Subroutine REG2 Program Listing

```

143      CALL RELAY(-48)                !OPEN S2 LOAD SW
144      CALL PCSET(2,0,1,490)         !SET TO 49MS
145      CALL PCWAIT(1)                 !20MS DELAY
146 C
147 C      READ STATUS OF INPUT 1 PORT AND STORE RESULT IN INP1
148 C          BIT5 CONTAINS ULL DETECTOR STATUS
149 C          BIT6 CONTAINS OHL DETECTOR STATUS
150 C          BIT=LOW -- NO ERROR DETECTED
151 C          BIT=HIGH -- L OUTPUT DETECTED OUTSIDE ACCEPTANCE RANGE
152 C
153      CALL IN1(INP1)                 !READ STATUS REG
154      CALL PCSTRT(2)
155      CALL PCWAIT(2)                 !TIME TO END TEST
156      CALL OUT1                      !TERMINATE INPUT PULSES
157      CALL ZERO                      !RESET HARDWARE
158 C
159 C      THIS IS END OF PULSE SEQUENCE -
160 C
161 C      PERFORM CALCULATIONS
162 C
163 C
164 C
165 C      VOLTAGE CONVERSIONS AND CALCULATIONS
166 C
167 C      VL(I)= SCALED ADAC VOLTAGE READINGS OF L OUTPUT SIGNAL
168 C      VMH= SCALED ADAC VOLTAGE READING OF M OUTPUT WITH K-INPUT HIGH
169 C      VML= SCALED ADAC VOLTAGE READING OF M OUTPUT WITH K-INPUT LOW
170 C
171      DO 50 I=1,3
172 50      VL(I)=LOUT(I)*10.           !CONVERT ATTENUATED ADAC VOLTAGE
173      VMH=MH*10.                   !CONVERT ATTENUATED ADAC VOLTAGE
174      VML=ML*10.                   !CONVERT ATTENUATED ADAC VOLTAGE
175 C
176 C
177 C      PERFORM TIME CONVERSIONS AND CALCULATIONS
178 C
179 C      PTIM= M OUTPUT PROPAGATION TIMES IN MICROSECONDS
180 C
181 C      T(I)= ARRAY CONTAINING THE CALCULATED RISETIME READINGS OF
182 C          THE L OUTPUT PULSE
183 C          READINGS CONVERTED TO TIME BY MULTIPLYING P-CLOCK 2 COUNT
184 C          VALUE BY CLOCK PERIOD OF 10 MICROSECONDS
185 C
186      DO 51 I=1,4
187 51      PTIM(I)=ARRAY(I)*.2         !CONVERT COUNT TO TIME
188      T(1)=(ITIME(2)-ITIME(3))*10.
189      T(2)=(ITIME(2)-ITIME(4))*10.
190      T(3)=(ITIME(2)-ITIME(5))*10.
191      T(4)=(ITIME(1)-ITIME(5))*10.

```

Figure A-6 Continued. Subroutine REG2 Program Listing


```

192      T(1)=T(1)*.85
193      T(2)=T(2)*.88
194      T(3)=T(3)*.90
195      T(4)=T(4)*.90
196 C
197 C      THESE CALCULATIONS CHECK STATUS OF THE L OUTPUT
198 C      WINDOW DETECTOR BY LOOKING AT BITS AND BIT6 OF INPUT 1
199 C
200 C      ULL=VALUE OF INP1 WITH ALL BITS MASKED TO ZERO EXCEPT BITS
201 C
202 C      OHL=VALUE OF INP1 WITH ALL BITS MASKED TO ZERO EXCEPT BIT6
203 C
204      ULL=INP1.AND."40
205      OHL=INP1.AND."100
206 C
207 C
208 C      PRINT RESULTS
209 C
210      IF(N.NE.1) GOTO 70
211 C
212      WRITE(LP,905)
213 905    FORMAT(/,T20,'J AND K INPUT PULSES AT MAXIMUM AMPLITUDES',/)
214      GOTO 80
215 70    IF(N.NE.2) GOTO 71
216 C
217      WRITE(LP,906)
218 906    FORMAT(/,T20,'J AND K INPUT PULSES AT MINIMUM AMPLITUDE',/)
219      GOTO 80
220 C
221 71    WRITE(LP,907)
222 907    FORMAT(/,T29,'J AND K INPUT PULSES AT NOMINAL AMPLITUDE',/)
223 C
224 80    WRITE(LP,908)
225 908    FORMAT(T35,'L OUTPUT VOLTAGE MEASUREMENTS:',/)
226      WRITE(LP,909) VL(1)
227 909    FORMAT(T40,'L OUTPUT AMPLITUDE (S1-OPEN; S2-OPEN)='
228      + ,F10.3,2X,'VOLTS',/)
229      WRITE(LP,910) VL(2)
230 910    FORMAT(T40,'L OUTPUT AMPLITUDE (S1-CLOSED; S2-OPEN)='
231      + ,F10.3,2X,'VOLTS',/)
232      WRITE(LP,911) VL(3)
233 911    FORMAT(T40,'L OUTPUT AMPLITUDE (S1-OPEN; S2-CLOSED)='
234      + ,F10.3,2X,'VOLTS',/)
235 C
236      WRITE(LP,912)
237 912    FORMAT(/,T35,'M OUTPUT VOLTAGE MEASUREMENTS:',/)
238      WRITE(LP,913) VMH
239 913    FORMAT(T40,'M OUTPUT AMPLITUDE (K PULSE HIGH)='

```

Figure A-6 Continued. Subroutine REG2 Program Listing

```

240      + F10.3,2X,'VOLTS',/)
241      WRITE(LP,914) VML
242  914   FORMAT(T40,'M OUTPUT AMLITUDE (K PULSE LOW)=',
243      + F10.3,2X,'VOLTS',/)
244 C
245      WRITE(LP,915)
246  915   FORMAT(/,T35,'L OUTPUT RISETIME MEASUREMENTS:',/)
247      WRITE(LP,916) (I,T(I),I=1,4)
248  916   FORMAT(T40,'T',I1,2X,'TIME=',F10.0,2X,'MICROSEC',/)
249 C
250      WRITE(LP,921)
251  921   FORMAT(/,T35,'L OUTPUT WINDOW DETECTOR STATUS:',/)
252      WRITE(TT,922) ULL,OHL
253  922   FORMAT(T40,'ULL STATUS=',O8,/,T40,'OHL STATUS=',O8,/)
254      IF(ULL.EQ.0) GOTO 105
255      WRITE(LP,923)
256  923   FORMAT(T45,'L OUTPUT DETECTED BELOW 17.65 VOLTS',/)
257  105   IF(OHL.EQ.0) GOTO 106
258      WRITE(LP,924)
259  924   FORMAT(T45,'L OUTPUT DETECTED ABOVE 20.0 VOLTS',/)
260  106   IF((ULL.OR.OHL).NE.0) GOTO 108
261      WRITE(LP,925)
262  925   FORMAT(T45,'L OUTPUT VOLTAGE REMAINED WITHIN ACCEPTANCE LIMITS',/)
263  108   CONTINUE
264 C
265 C      THIS COMPLETES TEST AT ONE SPECIFIED SET OF INPUT
266 C      CONDITIONS - LOOP BACK TO 10 TO REPEAT SEQUENCE FOR
267 C      NEW SET OF INPUT VALUES
268 C
269      GOTO 10
270  110   CONTINUE
271      WRITE(5,5555) N
272  5555   FORMAT(I5)
273      RETURN
274      END

```

Figure A-6 Continued. Subroutine REG2 Program Listing

FILE: DK :DR11K2.MAC

```
1      .TITLE  DR11K2
2      .IDENT  /V1.0/
3 ;
4 ;++
5 ;
6 ; FILE NAME:  DR11K2.MAC
7 ;
8 ; VERSION:   1.0
9 ;
10 ; FUNCTION:
11 ;
12 ;     THIS ROUTINE SETS UP THE VECTOR AND SERVICES INTERRUPTS
13 ;     THROUGH DR11-K #2 FOR THE . TEST #.
14 ;
15 ; CALL DEFINITION:
16 ;
17 ;     INTEGER*2  ITIME(5)
18 ;     COMMON    /RSTIME/,ITIME
19 ;     CALL DR11K
20 ;
21 ;
22 ; AUTHOR:   D.R. MOUNTJOY      13-NOV-78
23 ;
24 ;+-
25 ;
26 ;
27      .GLOBL  SETK2,K2DSBL
28      .MCALL  .REGDEF,..V2..
29      ..V2..
30      .REGDEF
31
32 ;-----
33 ;
34 ;-- SYMBOL DEFINITION
35 ;
36
37 K2VEC   = 330
38 K2CSR   = 167410
39 NPSW    = 340
40 K2INR   = K2CSR+2
41 PCLOCK2 = 164004      ;READ REGISTER OF PCLOCK 2
42 ENABLE  = 100
43
44 ;
45 ;-----
46 ;
```

Figure A-7. DR11K2.MAC Program Listing

```

47 ;-- COMMON STORAGE
48 ;
49      .CSECT  RSTIME
50 STORE: .BLKW  5
51      .CSECT
52
53 ;
54 ;-----
55 ;
56 ;-- SETUP ENTRY POINT
57 ;
58 ;      CALL BEFORE ALLOWING INTERRUPTS TO SET UP INTERRUPT VECTORS
59 ;
60 SETK2:
61      MOV      #K2ISR,@#K2VEC ;SET UP INTERRUPT VECTORS
62      MOV      #NPSW,@#K2VEC+2
63      MOV      #177777,@#K2INR ;CLEAR INPUT REGISTER
64      MOV      #STORE,PNTR      ;SET UP POINTER TO STORAGE LOCATION
65      MOV      #ENABLE,@#K2CSR ;ENABLE FOR INTERRUPTS
66      RTS      PC
67
68 ;
69 ;-----
70 ;
71 ;-- INTERRUPT SERVICE ENTRY POINT
72 ;
73
74 K2ISR:
75      MOV      @#PCLOK2,@PNTR ;MOVE TIME TO STORE
76      INC      PNTR
77      INC      PNTR
78      MOV      @#K2INR,TEMP      ;INPUT BITS INTERRUPTING
79      BIC      TEMP,@#167550      ;CLEAR INTERRUPT ENABLE REGISTER
80      MOV      TEMP,@#K2INR      ;CLEAR DR11-K INPUT REG
81 ;
82      MOV      #ENABLE,@#K2CSR
83      RTI                      ;RETURN FROM THIS INTERRUPT
84
85 ;
86 ;-----
87 ;
88 ;-- DISABLE DR11-K'S INTERRUPT
89 ;
90
91 K2DSBL: CLR      @#K2CSR
92      RTS      PC
93
94 ;

```

Figure A-7 Continued. DR11K2.MAC Program Listing

```

95 :-----
96 ;
97
98 PNTR: .WORD 0          ; INCREMENT TO STORE
99 TEMP: .WORD 0
100
101      .END

```

Figure A-7 Continued. DR11K2.MAC Program Listing

FILE: DK :TRAIN.MAC

```
1      .TITLE  TRAIN
2
3 ; PULSE TRAIN TEST
4 ;
5 ; CALLED IN TEST  AS:
6 ;
7 ;          INTEGER*2 ARRAY(4)
8 ;          ...
9 ;          ...
10 ;          CALL TRAIN( ARRAY )
11 ;
12 ; THIS ROUTINE PRODUCES 7 SERIES OF 4 PULSES EACH. THE RISE AND FALL
13 ; TIMES OF THE FIRST PULSE IS MEASURED.  FINALLY, 2 ADDITIONAL
14 ; PULSES ARE GENERATED, AND RISE AND FALL TIMES ARE MEASURED
15 ; ON THE LAST ONE.  THESE 4 RISE AND FALL TIMES ARE RETURNED
16 ; TO THE CALLING PROGRAM AS 4 1-WORD INTEGERS IN AN ARRAY.
17 ;
18 ; RELAY 47 IS SET ON THE 5TH LOOP THRU THE PULSE SERIES.
19 ;
20 ; ASSEMBLY COMMAND STRING
21 ;
22 ;      $TRAIN<MAC,TRAIN
23 ;
24 ; BY D.R. MOUNTJOY
25 ; 10/25/78
26 ;
27 ;
28 .PAGE
29 ;
30 ;-----
31 ;
32 ;
33
34      .GLOBL  TRAIN,LCD$BL,RELAY
35      .MCALL  .REGDEF,..V2..,CALLS
36      ..V2..
37      .REGDEF
38
39
40 CLOCK1  = 172540
41 CLOCK2  = 164000
42 CL1BUF  = CLOCK1+2
43 CL2BUF  = CLOCK2+2
44
```

Figure A-8. TRAIN.MAC Program Listing

```

45 PULSE      = 2                ;TO START PULSE TRAIN ( 2ND BIT OF OUT1 ).
46 OUT1       = 167610
47 IN1        = 167536
48
49
50 ;
51 ;-----
52 ;
53 ;-- MACRO DEFINITIONS
54 ;
55
56 .MACRO RESET                ;TO RESET COUNTERS
57     BIS     #10,@#OUT1
58     BIC     #10,@#OUT1
59 .ENDM RESET
60
61 .MACRO CWAIT UNIT,?A ;TO WAIT FOR CLOCK X COMPLETION
62 A:     BIT     #200,@#UNIT
63     BEQ     A
64 .ENDM CWAIT
65
66 .MACRO DELAY NUMBER
67     .REPT   <NUMBER>
68     NOP
69     .ENDR
70 .ENDM DELAY
71
72 ;
73 ;
74 .PAGE
75 ;
76 ;-----
77 ;
78 ;-- TRAIN ENTRY POINT
79 ;
80 ;     ALL CLOCKS SET TO: DOWN, 100 KHZ, SINGLE INTERRUPT
81 ;
82 .ENABL LSB
83
84 TRAIN:
85     CLR     @#CLOCK1        ;CLEAR CLOCK CSR'S
86     CLR     @#CLOCK2
87     RESET                    ;RESET COUNTER
88     MOV     2(R5),R0         ;ADDRESS OF PARAMETER LIST -> R0
89     BIC     #PULSE,@#OUT1   ;CLEAR PULSE BIT
90     MOV     #7,COUNTR        ;SET UP COUNTER
91     CALLS   LCDSBL           ;TURN OFF LINE CLOCK TEMPORARILY
92

```

Figure A-8 Continued. TRAIN.MAC Program Listing

```

93 LOOP:
94     MOV     #100.,@#CL1BUF    ; = 1 MSEC
95     MOV     #1,@#CLOCK1      ; START CLOCK 1
96
97     CMP     #7,COUNTR        ;1ST TIME THROUGH ?
98     BNE     1$               ;BRANCH IF NO
99
100    RESET                    ;RESET COUNTER
101    BIS     #PULSE,@#OUT1     ;RAISE PULSE 1
102    DELAY   3                 ;SMALL DELAY
103    MOV     @#IN1,R1          ;INPUT COUNT
104    ASH     #-8.,R1           ;SHIFT RIGHT 8 TIMES
105    MOV     R1,(R0)+          ;STORE IN PARAMETER LIST
106    BR      2$
107
108 1$:   BIS     #PULSE,@#OUT1
109 2$:   MOV     #80.,@#CL2BUF
110     CWAIT   CLOCK1
111     MOV     #1,@#CLOCK2
112     CMP     #7,COUNTR
113     BNE     C
114     RESET
115     BIC     #PULSE,@#OUT1
116     DELAY   3
117     MOV     @#IN1,R1
118     ASH     #-8.,R1
119     MOV     R1,(R0)+
120     BR      D
121
122 C:   BIC     #PULSE,@#OUT1
123 D:   MOV     #60.,@#CL1BUF
124     CWAIT   CLOCK2
125
126     MOV     #1,@#CLOCK1
127     BIS     #PULSE,@#OUT1    ;RAISE PULSE 2
128     MOV     #120.,@#CL2BUF
129     CWAIT   CLOCK1
130
131     MOV     #1,@#CLOCK2
132     BIC     #PULSE,@#OUT1
133     MOV     #100.,@#CL1BUF
134     CWAIT   CLOCK2
135
136     .ENABL   LSB
137
138     MOV     #1,@#CLOCK1
139     BIS     #PULSE,@#OUT1    ;RAISE PULSE 3
140     MOV     #80.,@#CL2BUF

```

Figure A-8 Continued. TRAIN.MAC Program Listing


```

141      CWAIT   CLOCK1
142
143      MOV      #1,@#CLOCK2
144      BIC      #PULSE,@#OUT1
145      MOV      #100.,@#CL1BUF
146      CWAIT   CLOCK2
147
148      MOV      #1,@#CLOCK1
149
150      BIS      #PULSE,@#OUT1      ;RAISE PULSE 4
151      MOV      #80.,@#CL2BUF
152      CWAIT   CLOCK1
153      MOV      #1,@#CLOCK2
154
155      BIC      #PULSE,@#OUT1
156
157      CMP      #3,COUNTR          ;5TH TIME THRU ?
158      BNE      M                  ;BR IF NOT
159      SAVE
160      CALLS    RELAY <R47>        ; OR SET RELAY R47
161      UNSAVE
162 M:
163      CWAIT   CLOCK2
164
165      DEC      COUNTR
166      BLE      Z
167      JMP      LOOP
168
169 Z:
170
171 ; LAST 2 PULSES
172 ;
173      .ENABL   LSB
174      MOV      #100.,@#CL1BUF      ;1 MS
175      MOV      #1,@#CLOCK1        ;START C 1
176      BIS      #PULSE,@#OUT1      ;RAISE PULSE
177      MOV      #80.,@#CL2BUF
178      CWAIT   CLOCK1
179
180      MOV      #1,@#CLOCK2        ;START C2
181      BIC      #PULSE,@#OUT1      ;LOWER PULSE
182      RESET    ;RESET COUNTER
183      MOV      #60.,@#CL1BUF
184      CWAIT   CLOCK2
185
186      MOV      #1,@#CLOCK1
187      BIS      #PULSE,@#OUT1      ;RAISE PULSE
188      DELAY    3

```

Figure A-8 Continued. TRAIN.MAC Program Listing

```

189      MOV     @#IN1,R1      ;INPUT COUNTER VALUE
190      ASH     #-8.,R1
191      MOV     R1,(R0)+
192      RESET
193      CWAIT   CLOCK1
194
195      BIC     #PULSE,@#OUT1  ;LOWR BIT
196      DELAY   3
197      MOV     @#IN1,R1
198      ASH     #-8.,R1
199      MOV     R1,(R0)
200      RESET
201
202      RTS     PC
203
204 COUNTR: .WORD    0
205 R47:    .WORD    47.
206
207
208      .END

```

Figure A-8 Continued. TRAIN.MAC Program Listing

***** TEST 3 *****

VOLTAGE REGULATION

J AND K INPUT PULSES AT MAXIMUM AMPLITUDES

L OUTPUT VOLTAGE MEASUREMENTS:

L OUTPUT AMPLITUDE (S1-OPEN; S2-OPEN)= 18.251 VOLTS

L OUTPUT AMPLITUDE (S1-CLOSED; S2-OPEN)= 18.241 VOLTS

L OUTPUT AMPLITUDE (S1-OPEN; S2-CLOSED)= 18.163 VOLTS

M OUTPUT VOLTAGE MEASUREMENTS:

M OUTPUT AMPLITUDE (K PULSE HIGH)= 15.095 VOLTS

M OUTPUT AMPLITUDE (K PULSE LOW)= 0.156 VOLTS

L OUTPUT RISETIME MEASUREMENTS:

T1 TIME= 270. MICROSEC

T2 TIME= 690. MICROSEC

T3 TIME= 2580. MICROSEC

T4 TIME= 4100. MICROSEC

M OUTPUT PROPAGATION TIMES:

FIRST PULSE

T5 TIME = 0.2 MICROSEC

T6 TIME= 0.8 MICROSEC

LAST PULSE

T5 TIME = 0.0 MICROSEC

T6 TIME= 0.8 MICROSEC

L OUTPUT WINDOW DETECTOR STATUS:

L OUTPUT VOLTAGE REMAINED WITHIN ACCEPTANCE LIMITS

Figure A-9. Test Readings Printout

BDX-613-2368

LABORATORY TEST SYSTEM, G. L. Asher, Final,
March 1980.

A laboratory test system was developed to perform automated electrical testing on electronic components. Test and analysis capabilities were made versatile to permit easy adaption to various product designs. This flexibility provides test methods for prototype hardware and for evaluating new product designs.

ELECTRICAL: Test System

LABORATORY TEST SYSTEM, G. L. Asher, Final,
BDX-613-2368, March 1980.

A laboratory test system was developed to perform automated electrical testing on electronic components. Test and analysis capabilities were made versatile to permit easy adaption to various product designs. This flexibility provides test methods for prototype hardware and for evaluating new product designs.

LABORATORY TEST SYSTEM, G. L. Asher, Final,
BDX-613-2368, March 1980.

A laboratory test system was developed to perform automated electrical testing on electronic components. Test and analysis capabilities were made versatile to permit easy adaption to various product designs. This flexibility provides test methods for prototype hardware and for evaluating new product designs.