BDX-613-1038

HIGH-TEMPERATURE REVERSE BIAS AND POWER BURN-IN AT TRANSISTOR JUNCTION TEMPERATURES FROM 150 to 300°C

PDO 6984770 and EP 46557
Topical Report

J. P. Gracey, Project Leader

Internal Distribution November 1974

Prepared for the United States Energy Research and Development Administration Under Contract Number AT(29 1) 613 USERDA

Bendix Kansas City Division

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Available From the National Technical Information Service, U. S. Department of Commerce, 5285 Port Royal Road, Springfield, Virginia 22161.

Price: Microfiche $2.25
Paper Copy $5.45

BDX-613-1038
Distribution Category UC-38

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Prepared by J. P. Gracey, D/144, under PDO 6984770 and EP 46557

Transistor preconditioning processes of high-temperature reverse bias and power burn-in were investigated at junction temperatures from 150 to 300°C to find the optimum junction temperature, test times, and test sequence for determining failures of the 2N2222A, beam lead, and SA1825 transistors. Positive ionic contamination of the silicon dioxide was the predominant failure mode. The optimum time on HTRB for removing early failures is given for various junction temperatures. The failure rate for burn-in was inversely proportional to the time on burn-in, and independent of the junction temperature when specific electrical conditions were applied. Twenty-four hours on burn-in at the maximum power-dissipation rating of the device is recommended. There is no preferred order for the HTRB and burn-in tests. Further work is required to demonstrate the advantages of using high-reliability transistors.

THE BENDIX CORPORATION
KANSAS CITY DIVISION
P.O. BOX 1159
KANSAS CITY, MISSOURI 64141

A prime contractor for the United States Energy Research and Development Administration
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CONTENTS

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ILLUSTRATIONS

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TABLES

SUMMARY

This project is an investigation of the transistor preconditioning processes of high-temperature reverse bias (HTRB) and power burn-in at junction temperatures ranging from 150 to 300°C to find the optimum junction temperature, test times, and test sequence for identifying potential early failures. The 2N2222A transistor was selected as the principal transistor for study because of its versatility and widespread use.

Extensive experiments were performed on the 2N2222A to establish its failure rates on HTRB and power burn-in at different junction temperatures. Failure modes were determined, and the optimum preconditioning time for each junction temperature was estimated. For HTRB, the optimum time for removing early failures was found for various junction temperatures, and the activation energy of 1.1 eV was confirmed for the surface-degradation failure mode. For power burn-in, the failure rate was found to be independent of the junction temperature when specific electrical conditions producing high power dissipation were applied to the transistor. The failure rate was proportional to the reciprocal of the time on burn-in. An experiment to determine whether HTRB and power burn-in should be performed in a particular sequence showed that there is no preferred order for the tests.

In addition to studies of the 2N2222A transistor, seven types of beam lead transistors were studied to determine any potential failure modes present in devices built with the new technology and to find out whether, as they do with conventional transistors, HRTB and power burn-in can effectively accelerate such failure mechanisms. The beam lead transistor experiments showed that, despite the presence of silicon nitride passivation, beam lead devices are susceptible to the surface-degradation failure mode. This discovery indicates that PNP beam lead transistors are especially vulnerable to failure because of the location of the collector contact on the active side of the chip. Beam lead transistor failure rates for HTRB were comparable to those of the 2N2222A transistor. Care must be exercised in the selection of full-power ratings for burn-in so as not to overstress the device.

HTRB and power burn-in were performed also on a group of SA1825 transistors. The SA1825 is a high-reliability version of the 2N2222A transistor. The experiments were designed to establish whether such high-reliability devices offer any advantages over similar screened commercial transistors. Two failure modes were present in this group of SA1825 transistors which caused an unusually large number of early failures and which eventually caused the lot to be scrapped, except for a limited number of transistors which were used in noncritical applications. Thus no general conclusions could be reached concerning the advantages

of high-reliability devices. Additional studies are being performed on other such devices and further results will be presented in the final report for this project.

DISCUSSION

SCOPE AND PURPOSE

This project was initiated in January, 1971, to investigate the transistor preconditioning processes of high-temperature reverse bias (HTRB) and power burn-in at junction temperatures from 150 to 300°C. (This range is much greater than the range from 150 to 175°C which is normally used for high-reliability transistors.) Both processes were studied to determine a failure-rate-versus-time curve for different junction temperatures to find the optimum junction temperature, test times, and test sequence for use with the 2N2222A transistor.

The 2N2222A transistor was selected for study because of its widespread use throughout industry and, in particular, because of the present and planned use of its high-reliability version in many systems at both Bendix and Sandia. In addition, knowledge gained from the study of this versatile transistor was expected to be applicable to other types of transistors.

In addition to the investigation of the 2N2222A, seven types of beam lead transistors were studied to determine failure modes of devices built with the new technology and to discover whether HTRB and power burn-in can effectively accelerate the failure mechanisms of beam lead transistors as they do with conventional transistors.

HTRB and power burn-in were also performed on a group of SA1825 transistors to determine whether such high-reliability devices offer any advantage over similar screened commercial transistors.

The work performed for this project was initially funded by Sandia Laboratories as EP 46557. This was later followed by funding under PDO 6984770.

ACTIVITY

Procedure

For the high-temperature preconditioning experiments, a group of 4000 2N2222A transistors was procured from Texas Instruments. Three thousand of these were manufactured in Dallas, Texas and bore a date code of 009; the other 1000 units were manufactured in Singapore and bore a date code of 7024A. None of the transistors had undergone any type of preconditioning after manufacture. All were serialized, with the Dallas group numbered 1 through 3000 and the Singapore group numbered 3001 through 4000.

All units were tested for hermetic seal. The Veeco method was used for fine leak to a maximum limit of 10^{-8} cm^3/s, and Mil-Std-883[1] was used for gross leak.

The electrical tests outlined in Appendix A were performed on each unit. Thirty-four tests were performed using a Fairchild 600D automatic transistor tester. Data were recorded on punched cards according to device serial number. Because, as noted in Appendix A, several of the tests were for various reasons redundant, 29 meaningful tests were performed. A three-digit code was punched on each data card to identify the data. For initial testing, the test code was A01. Other codes were used for subsequent testing, as indicated in Appendix B.

After initial testing, a large group of devices was subjected to the following "treatment" sequence:

- Baked at 200°C for 24 hours with no applied voltage;
- Cycled five times through the temperature range from -65 to +200°C; and
- Tested again for the electrical tests specified in Appendix A. (Test Code A04 was used to identify these data.)

At the conclusion of the treatment sequence, subgroups having the following distribution were selected for the individual experiments to be performed.

- Seventy-five percent of each subgroup consisted of Dallas transistors (Lot 009). Half of the units had been treated as previously described, and half had not.
- Twenty-five percent of each subgroup consisted of Singapore transistors (Lot 7024A). Half of the units had been treated, and half had not.

The distribution of parts was selected in this manner so that it would be representative of the original makeup of the group, and so that the effects of baking and temperature-cycling could be measured.

The 2N2222A experiments were divided into the following five basic sets.

- Step-Stress HTRB

  This experiment was designed to select the electrical condition (V_{CB}) which would be used in the stress-in-time HTRB experiments, and to make a rough determination of the temperature at which permanent degradation of the transistors occurred within a short time.

- Stress-In-Time HTRB

  After the optimum V_{CB} had been determined from the step-stress test, the HTRB test was conducted for long periods of time at given temperatures to establish the failure-rate-versus-time curve.

- Step-Stress Burn-In

  This test was designed to select the optimum electrical conditions for burn-in in a manner similar to that for the step-stress HTRB. In this case, the power-level input to the device was determined.

- Stress-In-Time Burn-In

  As with the stress-in-time HTRB, once the optimum electrical condition was determined, failure-rate-versus-time curves were established for various temperatures.

- Sequence of HTRB and Burn-In

  An experiment was conducted to determine whether HTRB or burn-in should be performed first.

HTRB of 2N2222A Transistor

Step-Stress Tests to Determine Optimum Electrical Conditions

The step-stress test consisted of holding constant both the electrical condition (V_{CB}) and the time interval of the stress (16 hours on HTRB at each temperature) while varying the temperature of a selected group of transistors. The purpose of this test was to determine roughly at what temperature permanent device degradation occurred in a short time. The information obtained then served as a starting point for the more extensive data taken during the HTRB stress-in-time experiments where the optimum HTRB conditions were determined. Also, by comparing the results of step-stress tests for several groups of transistors at different electrical conditions, an evaluation of the optimum electrical condition for the stress-in-time experiments was made.

Three groups of twenty-four 2N2222A transistors were selected for step-stress testing. Each group was given the same step-stress in temperature, but different V_{CB} voltages (40, 55, and 70 volts) were used. Figure 1 shows the temperature stress values used in the tests. After the completion of each 16-hour interval, the series of electrical tests shown in Appendix A was performed on each transistor at room temperature and the data were recorded on punched cards.

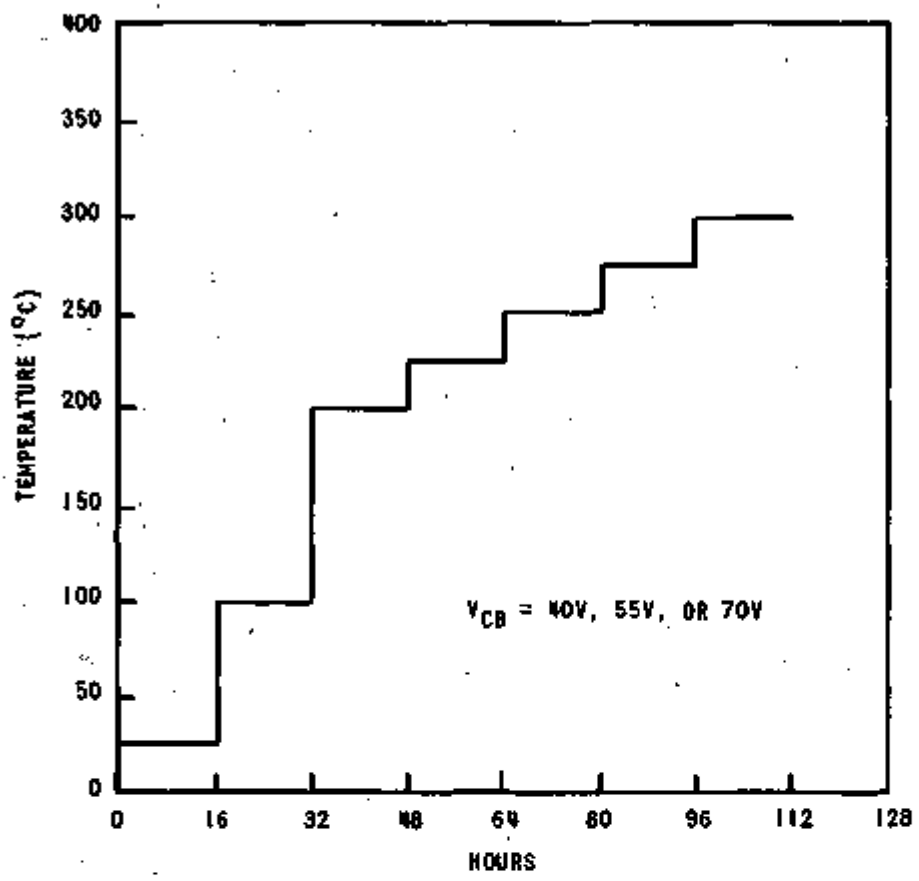


Figure 1. Step-Stress HTRB

When the step-stress HTRB data were first taken, a complete analysis was virtually impossible since each run consisted of more than 7000 individual data points and the analysis had to be made by hand. A computer program was later designed to perform the analysis (Appendix C). The computer analysis agrees in general with the original work done manually except for the one notable exception (V_{CE} Sat test) described below.

The original procedure was to plot all data for all tests on a few units selected at random from each of the three step-stress groups to determine which tests were the better indicators of failure. An example of this method is shown in Figure 2. These tests were then evaluated for the entire group. The procedure was followed for both step-stress HTRB and burn-in, and it produced the following results.

- As indicated in Figure 2, the most sensitive parameter for the detection of failure was the lowest-current h_{FE} test,

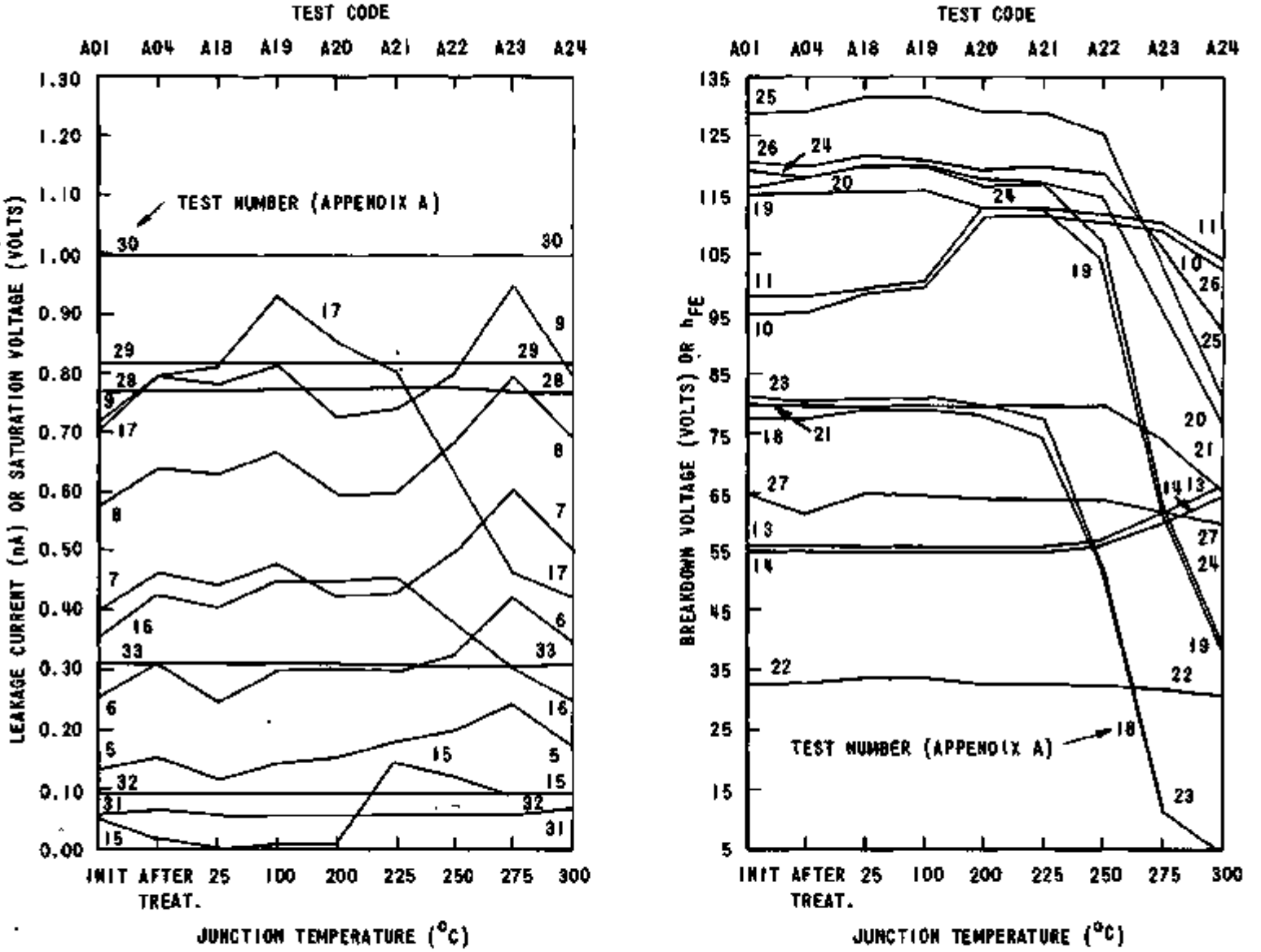


Figure 2. Plot of All Tested Parameters for Unit 14 of V_{CB} = 55-V Step-Stress HTRB Group (Test 17--I_{CEO}--appears to be the best failure indication; however, the total range of less than 1 nA cannot be reliably distinguished by the tester.)

either Test 18 (V_{CE} = 1V, I_C = 1 mA) or Test 23 (V_{CE} = 5V, I_C = 1 mA). The most significant shifts occurred for the h_{FE} tests; the higher the collector current, the less was the shift.

- Leakage currents (I_{CEO} and I_{CBO}) were often unaffected by the HTRB. As shown in Figure 2, all leakage readings were less than 1 nA.

- BV_{CBO} shifted upward somewhat, representing a "walkout" of the "knee" of the BV_{CBO} curve. This walkout could sometimes be observed on a curve tracer at room temperature; its magnitude was underestimated in the original hand analysis. Once the computer program was available, upward shifts of 20 percent were found to be common, and most units were found to shift. Since I_{CBO} was unaffected with 70 volts applied, the decision was made that shifting would not be deemed a cause of failure unless the value of BV_{CBO} was less than 75 volts.

- Upward shifts in V_{BE}Sat and V_{CE}Sat occurred on many devices and escaped notice in the original hand analysis. The magnitude of the shift was as high as 30 mV on either test and represented a 2-to-3-percent shift for V_{BE}Sat and a 20-to-50-percent shift for V_{CE}Sat.

  The shift in saturation voltages occurred mainly with Singapore transistors after heat had been applied. Its cause was "purple plague," a dark purple-to-black gold-aluminum intermetallic compound which forms in the presence of silicon. The construction of these 2N2222A transistors (both Dallas and Singapore) includes internal gold wires which connect the aluminum metallization on the chip to the gold-plated Kovar posts. The plague formed at the gold-wire bond to the aluminum metallization of the chip, thus causing increased contact resistance at the bond and raising the saturation voltages. Plague formation is accelerated by heat. An internal visual examination of several devices revealed that the plague was present on all units (Dallas, Singapore, baked, and unbaked), and the extent to which the saturation voltages shifted apparently was dependent upon the amount of the plague present.

  In retrospect, this particular group of 2N2222A transistors probably was not an ideal choice for performing high-temperature experiments because gold wires were used in the internal construction; however, the discovery of the plague problem occurred after the project was well under way, and the decision was made that the presence of purple plague alone would not be deemed a rejection criterion. Thus a transistor was considered a saturation-voltage failure only if it exceeded the limits established for that particular test.

The first of the preceding points represents a departure from conventional methods of determining failures which consider only the absolute value of a parameter and compare it to a predetermined limit based on usage requirements.[2] The conclusion was reached, however, that the reliability of a transistor which drastically changes its h_{FE} characteristics must be suspect. An argument for the use of a delta-shift failure criterion is made in Appendix C; by this method, a transistor for which h_{FE} shifts more than ±10 percent at I_C = 1 mA is considered a failure. Absolute limits should be placed on other tests, which is usually the case.

After defining what would constitute a failure, an analysis of the step-stress results, similar to that shown in Table 1, was conducted. A transistor was counted as a failure at the first point at which any failure criterion was exceeded: for example, Device 21 failed I_{CEO} at A04, then later failed h_{FE} and I_{CBO} at A20; this unit was counted as a failure at A04 and at all subsequent tests.

The absolute limits used for the tests were derived by first evaluating the initial distribution of test results for a large number of devices subjected to a particular test, then placing a limit on each end of that distribution.

Since all groups of transistors were selected in the same way, conditioned in the same way, and had approximately the same number of failures after being treated, they were evaluated by comparing the cumulative percent failures for each group at a particular temperature to that of the other groups. Figure 3 shows the results obtained for the three step-stress groups; a breakdown of the failures with respect to time is shown in Table 2. The three curves have the same general shape; however, since the 55-V group has significantly more failures at 225 and 250°C than the other two groups, a slight preference exists for using a 55-V V_{CB}. This voltage was therefore selected for use in the stress-in-time experiments.

That failing transistors always failed the 10-percent-delta-shift criterion for low-current h_{FE} at some point in the testing sequence is also noteworthy. Some devices failed other tests as well, but had the delta shift been the only measure of failure, all of the units failing other tests would have been detected.

Stress-In-Time Tests at V_{CB} = 55 V to Determine Optimum Time and Temperature

After the electrical condition most likely to activate failures of the 2N2222A transistor had been determined, a group of transistors at this condition was placed on HTRB at a designated temperature for a long period of time. From the data obtained, a failure-rate-versus-time-on-test curve was drawn for that

Table 1. Failures After Step-Stress HTRB at V_{CB} = 55V (Test Codes A18-A24)

2N2222A Serial Number	Test Failed*								
	I_{CBO}(17) Conditions: V_{CB} = 40 V Limits: 0 to 10 nA	h_{FE}(18) Conditions: V_{CE} = 1 V, I_C = 1 mA Limits: ±10 Percent or 55 to 200	h_{FE}(23) Conditions: V_{CE} = 5 V I_C = 1 mA Limits: ±10 Percent or 55 to 300	I_{CBO}(9) Conditions: V_{CB} = 70 V Limits: 0 to 10 nA	BV_{CBO}(10) Conditions: I_C = 10 uA Limits: 75 to 300 V	BV_{CEO}(14) Conditions: I_C = 30 mA Limits: 37 to 300 V	V_{BE}Sat (28) Conditions: I_B = 5 mA, I_C = 50 mA Limits: 0.750 to 0.800 V	V_{CE}Sat (31) Conditions: I_B = 50 mA, I_C = 50 mA Limits: 0.032 to 0.080 V	h_{FE}(27) Conditions V_{CE} = 5 V, I_C = 500 mA Limits ±10 Percent or 40 to 140
13		A23	A23						
14		A22	A22						
15	A04	A04	A04	A04					
16		A22	A22						
17		A23	A22						
18		A22	A22						
19	A04	A04	A04						
20		A23	A23						
21	A04	A20	A20	A20	A21				
120		A22	A22						
121		A24	A24						
122		A22	A22						
123		A20	A20						
124		A21	A21						
125		A22	A22			A23			A24
126**									
127		A21	A21						A24
128		A23	A23						
3026		A24	A24						
3027		A21	A21						
3028	A19	A04	A04	A04	A21				A23
3070		A21	A21						
3071		A24	A24						
3072		A24	A24						

*Refer to Appendix B for explanation of test codes. All blank spaces indicate the device did not fail the test at any point in the testing sequence.
**This unit was removed after A22 for evaluation.

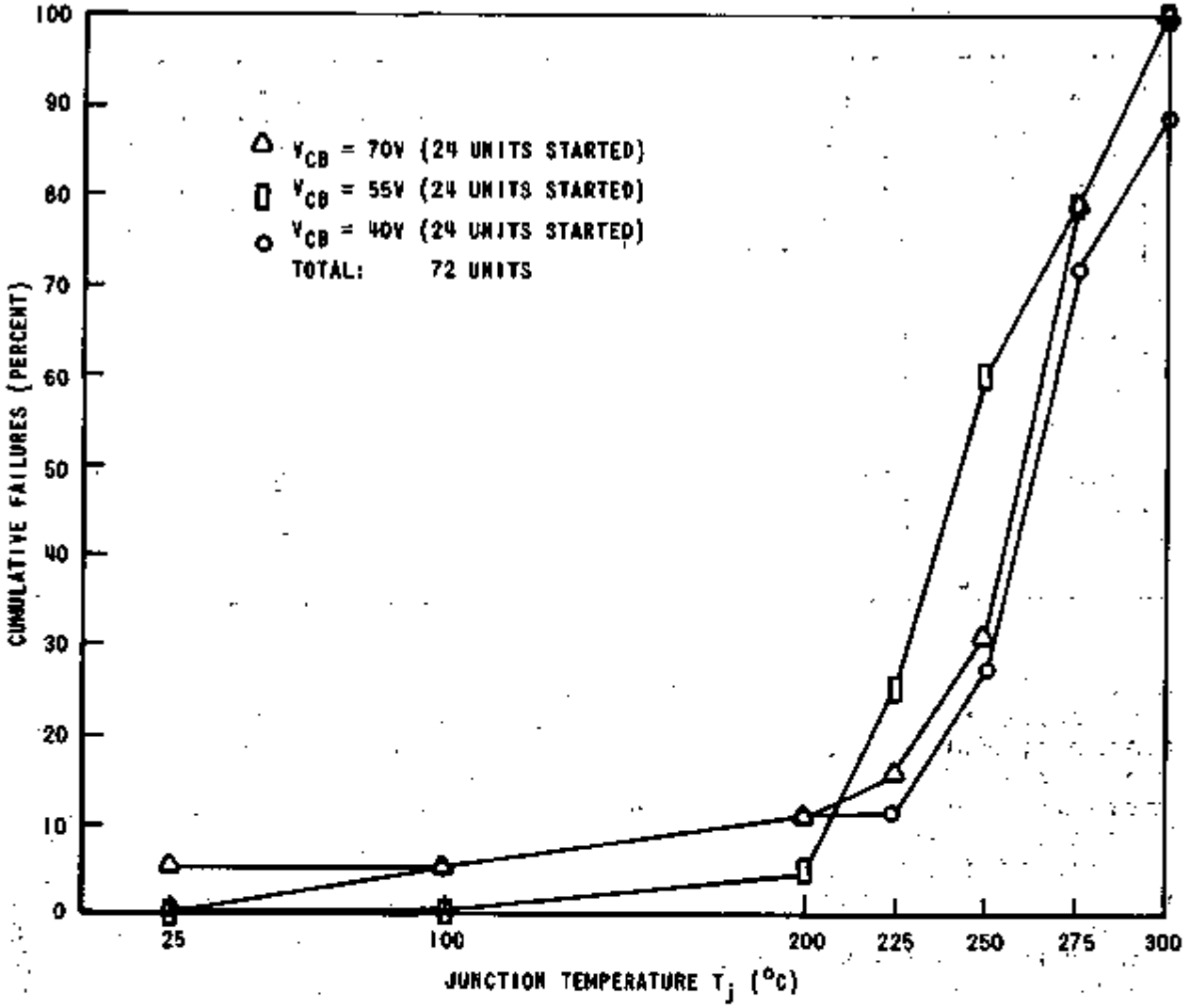


Figure 3. Comparison of Failures for Three Step-Stress HTRB Groups (Note large difference at 250°C between the 55-V group and the other two groups.)

particular temperature. By extending this procedure to include several temperatures, a choice of the optimum temperature and time-on-test was made.

Figure 4 illustrates the procedure that was used. Ninety-six transistors were started in each group. Groups were tested at each of six temperatures for 24 to 840 hours and were taken off HTRB periodically for electrical testing. When the units were not at high temperature (while they were being transported to the tester), the collector-base was maintained with a reverse bias of 6 V to preserve the effects of the HTRB.

Table 2. Step-Stress HTRB Failures by V_{CB} Group

Junction Temperature (°C)	Time on Test (Hours)	Number of Failures		
		V_{CB} = 40 V	V_{CB} = 55 V	V_{CB} = 70 V
	After Treatment	5	4	5
25	16	0	0	1
100	16	1	0	0
200	16	1	1	1
225	16	0	4	1
250	16	3	7	3
275	16	8	3	9
300	16	3	4	4

Kemeny[3] has verified experimentally that a failure-rate-versus-time curve has at least two distinct regions: the "early failures" region; and the "constant failure rate" region. The early-failures region extends from the beginning of the test (t = 0) to the point where the constant-failure-rate region beings. It is characterized by a high failure rate which decreases rapidly with time. In the constant-failure-rate region, the rate levels off, ideally at a very low value, and becomes static with time. In addition to these two regions, a "wearout" region, in which the failure rate increases rapidly because of wearout of the transistors, is usually present. Figure 5 shows the general shape of an idealistic curve. The failure rate λ is given by the following equation.

$$\lambda = \frac{k}{N_s \, \Delta t} , \qquad (1)$$

where k is the number of failures occurring during the time interval, N_s is the number of transistors surviving at the time of the last measurement, and Δt is the time interval.

The optimum time to use with a particular HTRB temperature is clearly the time required to endure early failures. The remaining devices then can be expected to fail at some constant, low rate.

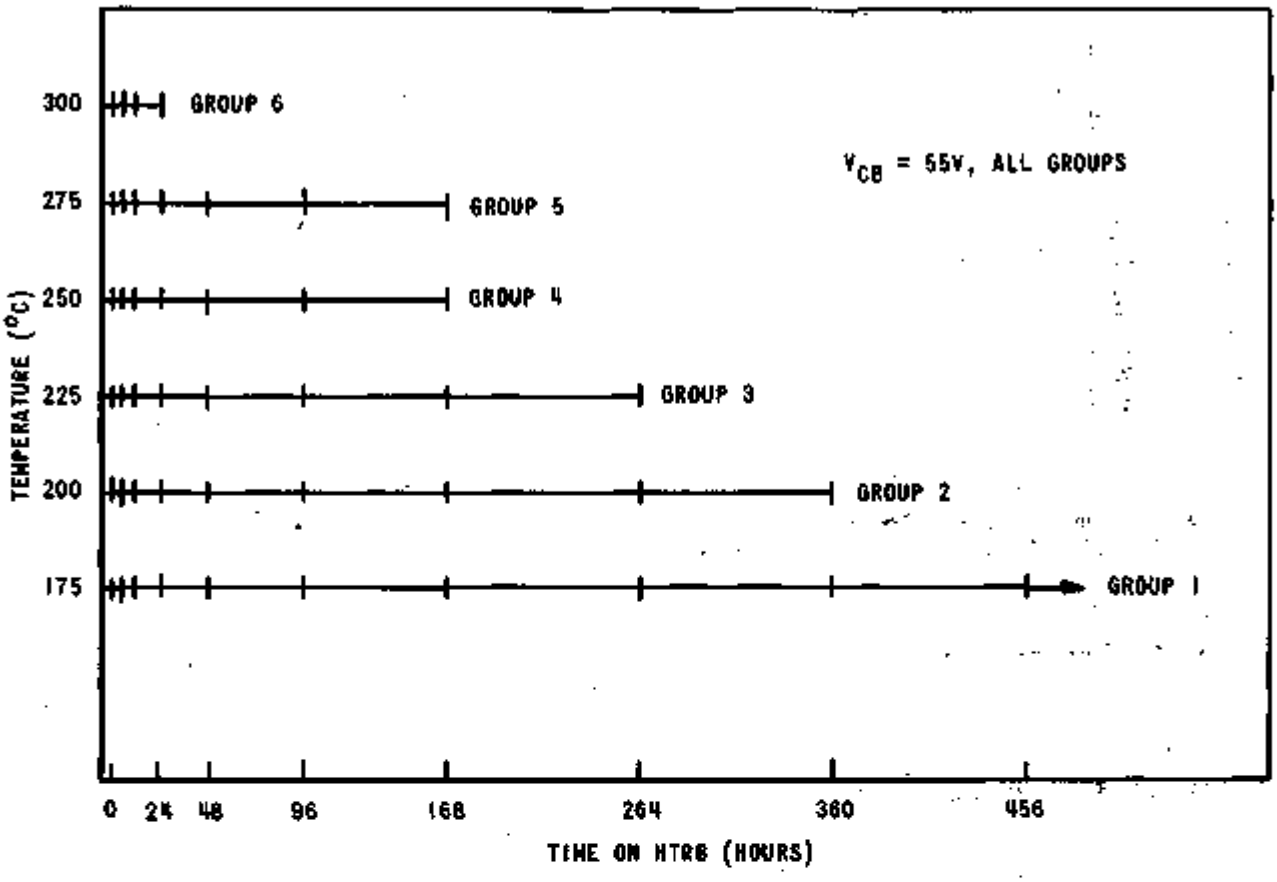


Figure 4. Stress-In-Time HTRB (Vertical lines indicate points at which the groups were removed from HTRB for electrical testing.)

Experimental Results

Figures 6 through 11 are the HTRB failure-rate-versus-time curves for each of the temperatures used in the experiments. Although there is statistical variation in the data, each of the curves has the general shape of the idealistic curve shown in Figure 5. In each, the failure rate is high at first, then drops to a reasonably constant lower value. In Figures 10 and 11, data are not shown after 24 and 6 hours, respectively. Because of the small number of remaining transistors, the data were considered insignificant.

Statistical variations from the ideal curve were expected in these experiments since the sample sizes used were relatively small. To generate the ideal curve, failures would have to be determined for a large number of devices with measurements made at very

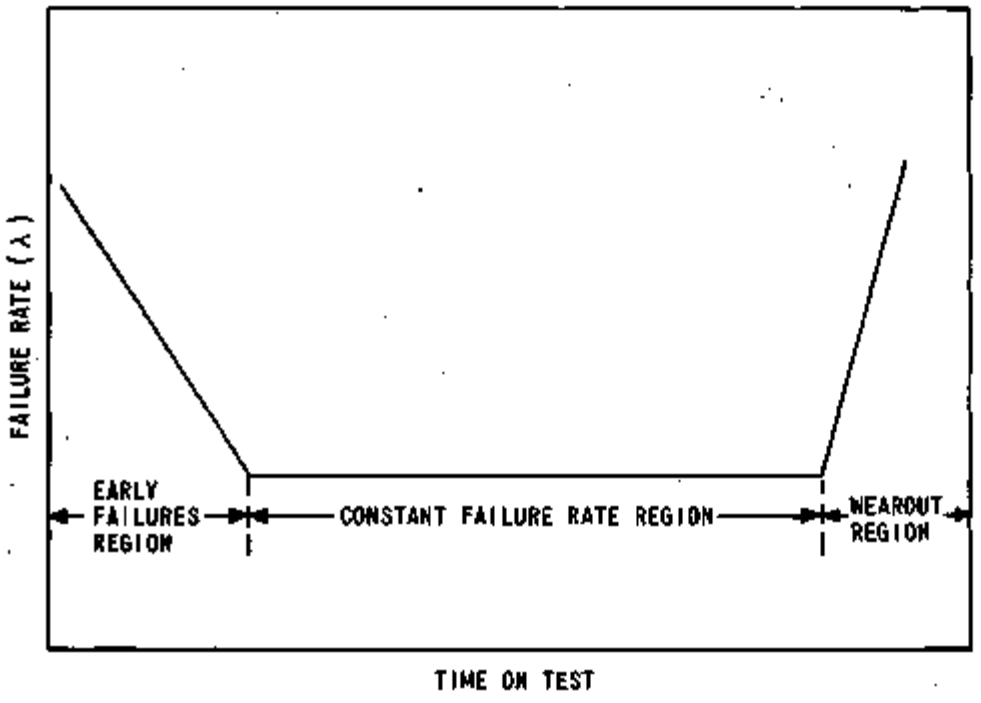


Figure 5. Idealistic Failure-Rate-Versus-Time Curve

short time intervals. Because of the cost involved, this was not done.

The horizontal line (λ_{AV}) drawn on each curve is the geometrical average of all the points that are considered to be in the constant-failure-rate region. Its value is obtained by the following equation.[4]

$$\lambda_{AV} = \frac{\sum_{t = t_{ef}}^{t_{tot}} k}{N_{tm} (t_{tot} - t_{ef})}, \qquad (2)$$

where the numerator represents the total number of failures from the end of the early-failures region (t_{ef}) to the end of the testing (t_{tot}), and N_{tm} is the number of surviving transistors at the geometrical mean time $(t_{ef} \cdot t_{tot})^{1/2}$.

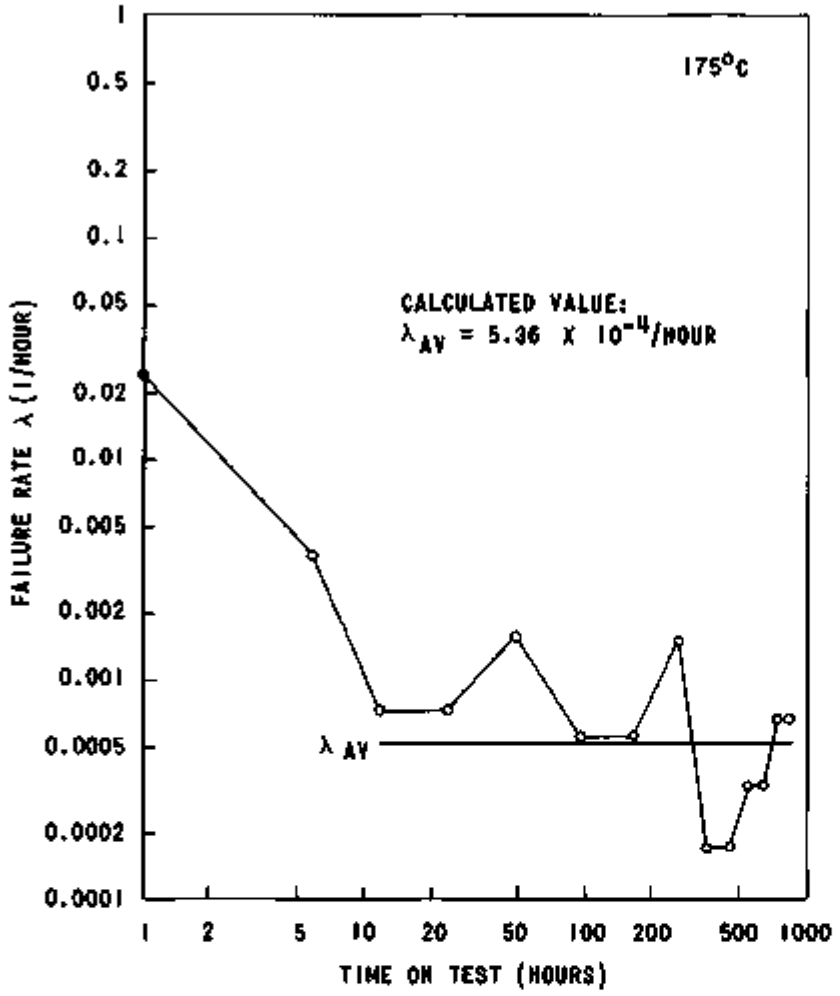


Figure 6. Failure Rate Versus Time for 175°C HTRB

To test the consistency of these data, an Arrenius plot of log λ_{AV} versus 1000/T was made. When this plot turns out to be a straight line of slope B and Y-axis intercept log C,

$$\log \lambda_{AV} = - \frac{1000B}{T} + \log C. \qquad (3)$$

The equation then may be transformed by taking the exponential of both sides to obtain

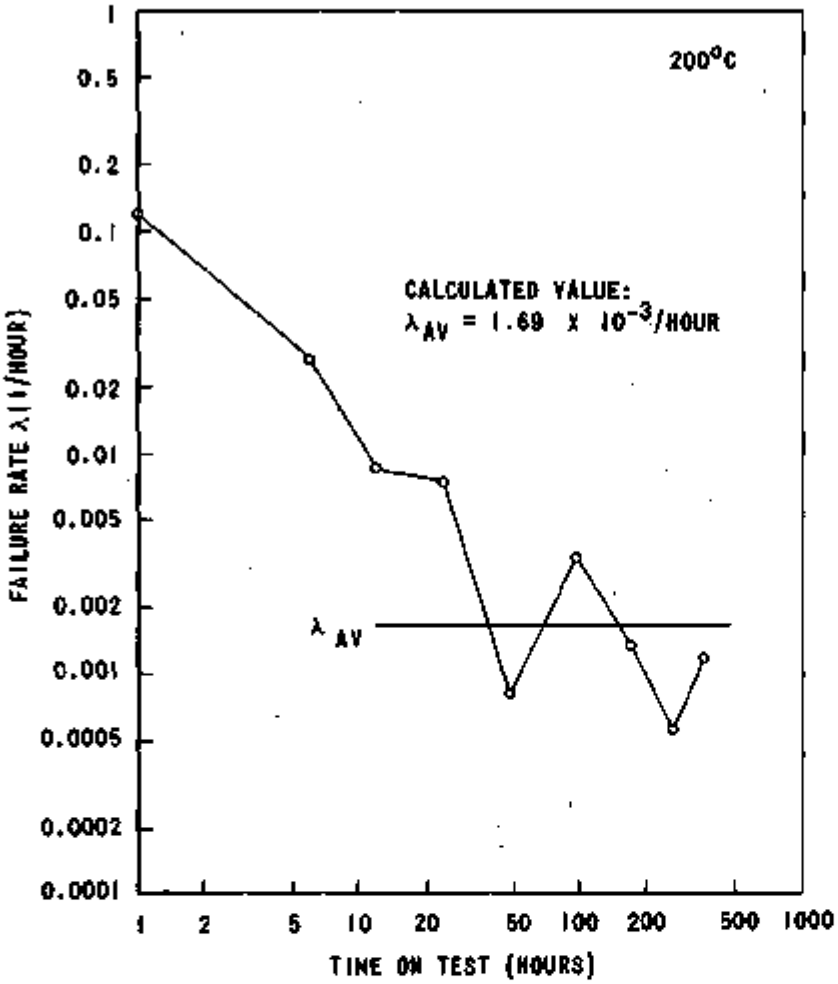


Figure 7. Failure Rate Versus Time for 200°C HTRB

$$\lambda_{AV} = C \exp(-1000B/T), \quad (4)$$

where C and B are constants, and T is the absolute temperature.

If the constant is set at $B = E_a/1000k$, where E_a is an activation energy and k is Boltzmann's constant, then

$$\lambda_{AV} = C \exp(-E_a/kT). \quad (5)$$

This is Arrhenius' equation which defines the rate at which a chemical reaction will occur. Since most processes that cause transistor

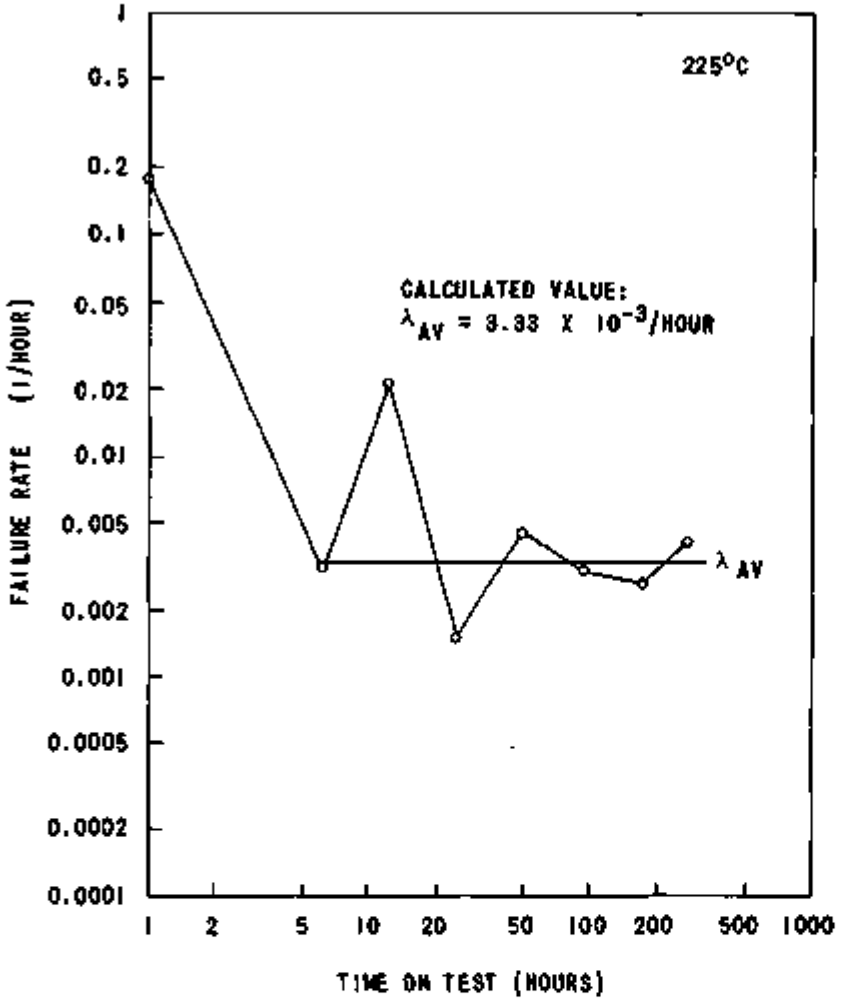


Figure 8. Failure Rate Versus Time for 225°C HTRB

failure after the early-failures period (for example, the diffusion of sodium ions) are long-term chemical reactions, the data can be expected to fit this equation. Moreover, the activation energy for this failure mechanism can be expected to approximate 1.1 eV, since this activation energy has been reported by many observers of silicon surface-degradation phenomena.[5]

The Arrhenius plots shown in Figure 12 illustrate two cases. The first is the conventional procedure of using fixed limits for all tests, including h_{FE}, as a means of defining failures. The second also uses fixed limits for all tests, but adds the delta-shift criterion for low-current h_{FE}, as described in Appendix C. That the data fit a straight line indicates that Arrhenius' equation holds true. Graphical determination of the slope of

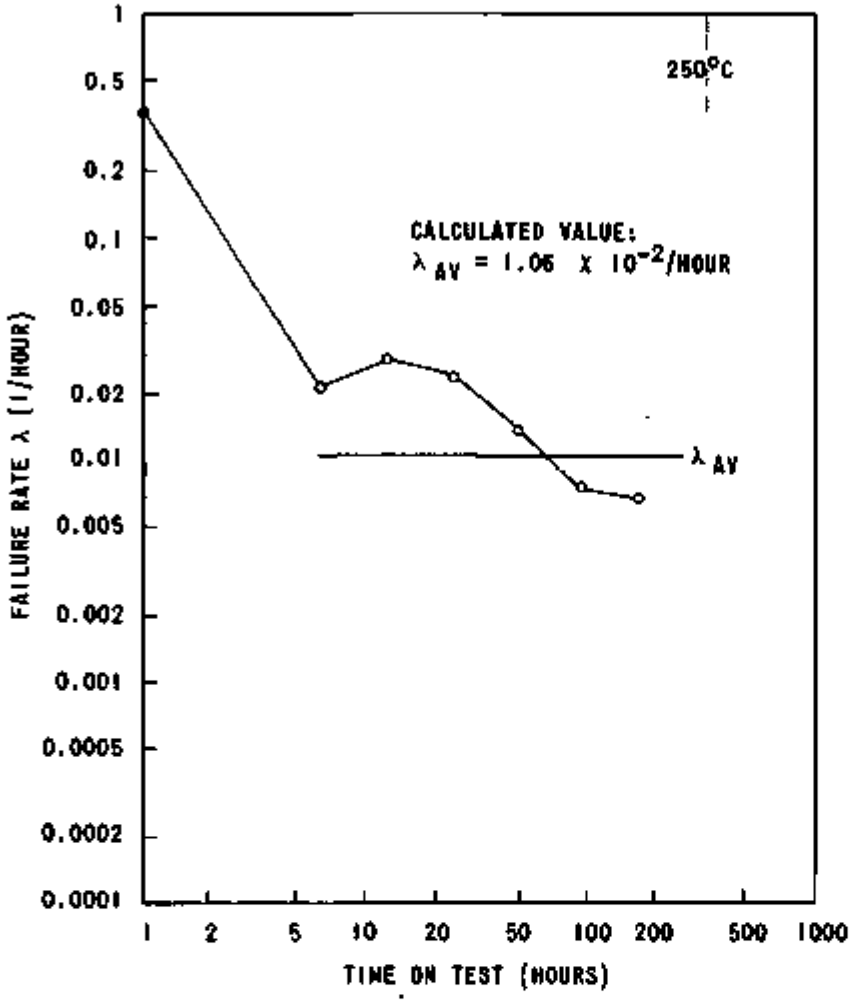


Figure 9. Failure Rate Versus Time for 250°C HTRB

the lines yielded the value E_a = 1.18 eV when only fixed limits were used, and the value E_a = 1.06 eV when the delta-shift criterion was added. These values compare favorably with the 1.1-eV activation energy obtained by others.[6] As anticipated, the relatively consistent results obtained using either criterion indicated that the same failure mechanism was operating in both cases. The use of the delta-h_{FE} method, however, produced higher failure rates than the fixed-limit method, thus indicating that the delta-h_{FE} method is more effective for determining which individual transistors are potentially unreliable.

The value of C in Arrhenius' equation (Equation 5) is the Y-axis intercept in Figure 12. This was determined to be 2.06 x 10^{-9}/hr for the fixed-limit method and 2.99 x 10^{-8}/hr for the delta-h_{FE}

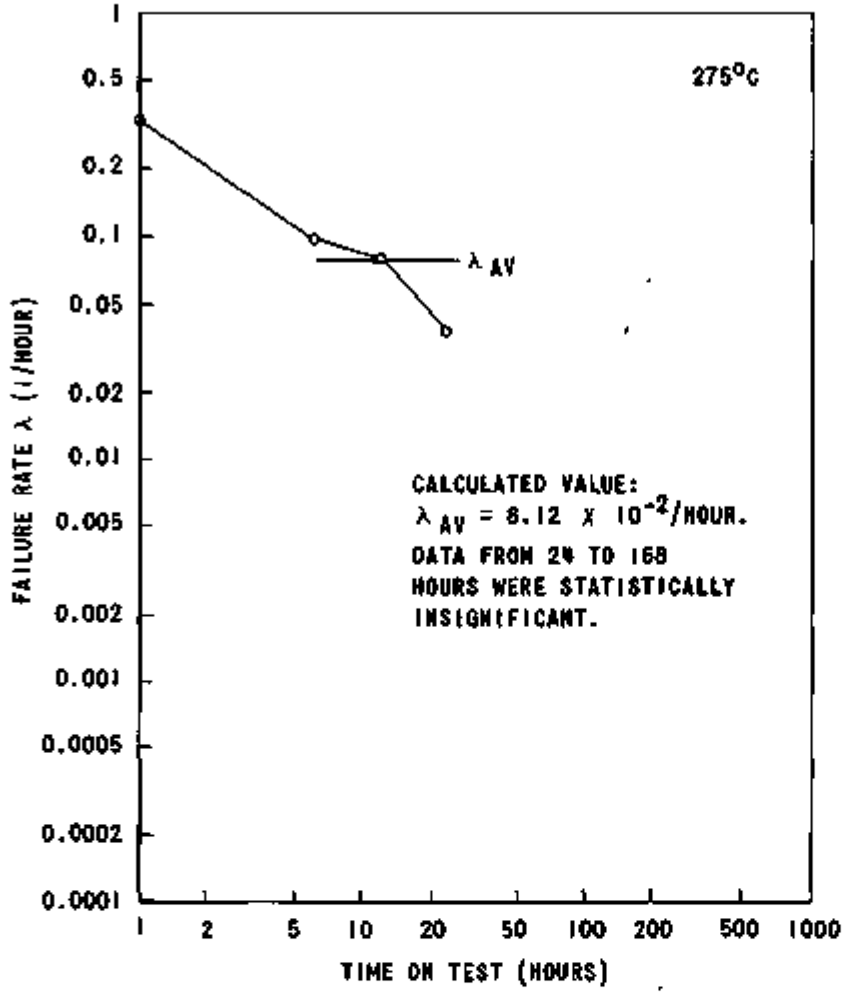


Figure 10. Failure Rate Versus Time for 275°C HTRB

method. By using these values of C and the activation energies mentioned above in Arrhenius' equation, the 2N2222A failure rates can be projected to lower temperatures with the results shown in Table 3.

Kemeny[7] predicts a value of 1.5×10^{-8}/hr at 60°C for one type of silicon planar transistor, the BFY33, which approximates the value obtained at Bendix by using the delta-h_{FE} criterion. Peck[8] has predicted a failure rate of 0.001 percent per 1000 hours (10^{-8}/hr) for high-quality, conventional silicon devices at 125°C.

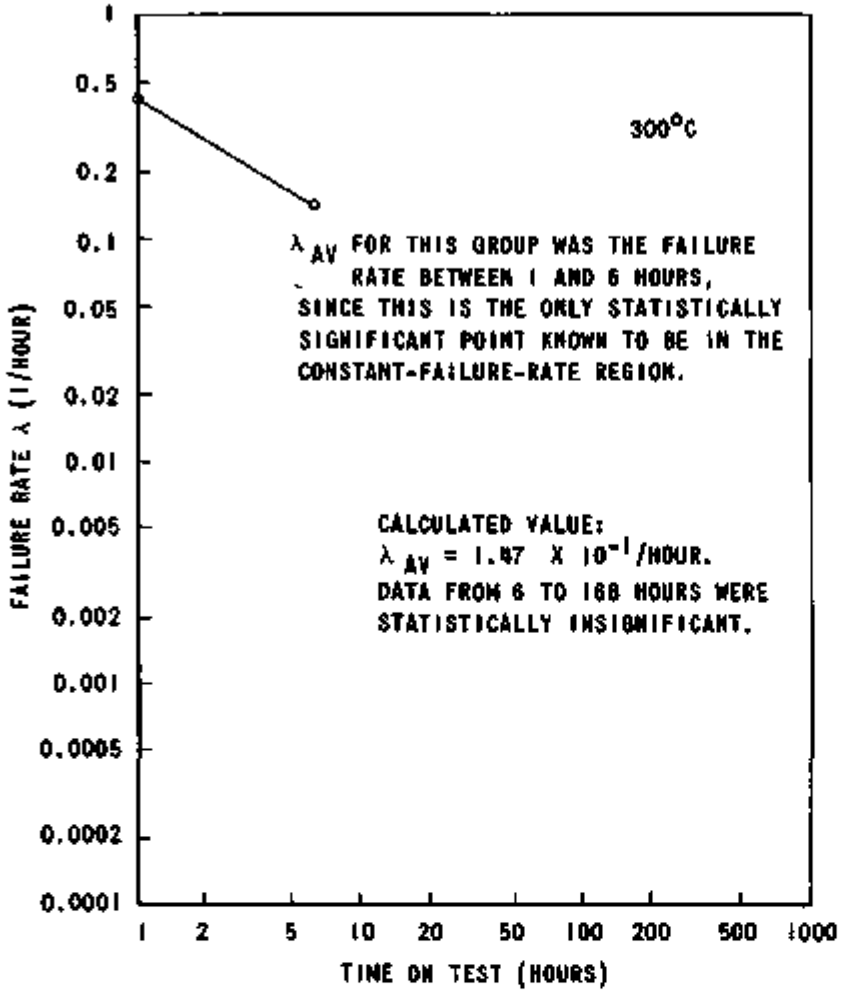


Figure 11. Failure Rate Versus Time for 300°C HTRB

Table 3. Projected Failure Rates for Lower Temperatures

Method	Failure Rates	
	60°C	125°C
Fixed Limits	2.8×10^{-9}/hr	2.4×10^{-6}/hr
Fixed Limits Plus Delta h_{FE}	2.7×10^{-8}/hr	1.1×10^{-5}/hr

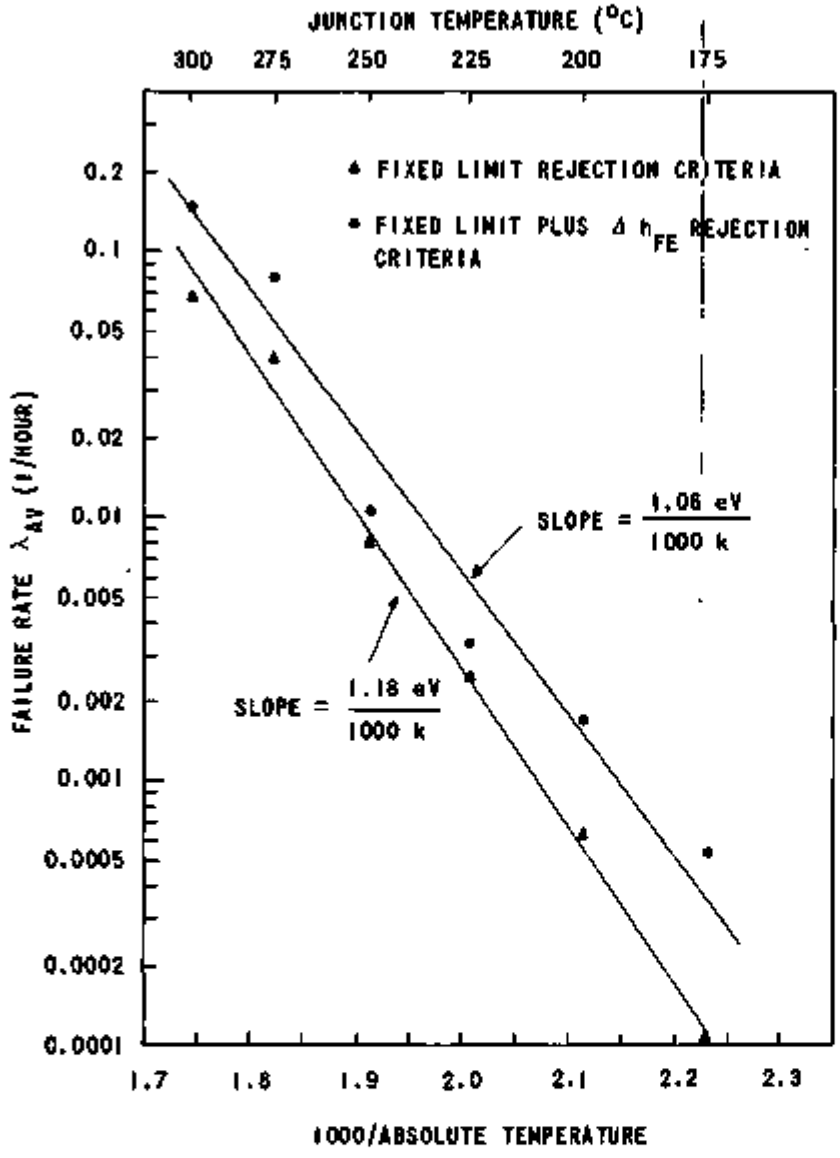


Figure 12. Arrhenius Plots of Stress-In-Time HTRB Results

The graphs of Figures 6 through 11 show that the optimum HTRB times are relatively short at high temperatures. By inspection of each figure, the estimate of the optimum HTRB times (t_{ef}) shown in Table 4 was made. These values of t_{ef} are valid when the delta h_{FE} criterion of Appendix C is used. When only fixed-limit criteria are used, the values of t_{ef} must be increased. Later data have indicated that at 175°C t_{ef} is 24 hours, using fixed limits only.

Table 4. Optimum HTRB Times for High Junction Temperatures (Using Delta h_{FE} Failure Criterion)

Junction Temperature (°C)	t_{ef} (hr)
175	6 to 12
200	6 to 12
225	1 to 6
250	1 to 6
275	1 to 6
300	0 to 6

For the 300°C test, the failure rates calculated for the one-hour and the six-hour points were relatively close, thus indicating that the optimum time may be less than one hour.

Accomplishments, HTRB

The failure-rate-versus-time curves clearly show that there is an optimum time which should be used for HTRB. This time, t_{ef}, is the time required to eliminate the early failures and get into the constant-failure-rate region for the temperature used. Moreover, extending the HTRB time beyond t_{ef} is a waste of resources, since the failure rate is not lowered by such an extension. The values of t_{ef} which should be used for the 2N2222A transistor are tabulated in Table 4. The higher number of hours shown should be used for all temperatures except 300°C where, as noted, the value of t_{ef} may be less than one hour.

All of the times involved are feasible and are economical compared to the present methods used, so any of these temperatures could be selected. The lowest temperature (175°C for 12 hours) would probably minimize oven-maintenance problems and extend their lifetime; however, if oven space and turn-around time are more critical problems than oven maintenance, 6 hours at 225°C would be a better choice.

The Arrhenius plot of Figure 12 shows that the data are reasonably consistent, the mechanism causing failure is a process which follows Arrhenius' equation (consistent with the failure mode proposed in Appendix C), and the mechanism has an activation energy very close to the 1.1 eV reported by many observers of silicon surface-degradation phenomena. When the analysis is extended to a temperature of 60°C, a failure rate of 2.7×10^{-8}/hr is obtained. This agrees with the value predicted for a different type of silicon planar device.[9]

Power Burn-In of 2N2222A Transistor

Step-Stress Tests to Determine Optimum Electrical Conditions

Step-stress burn-in tests were performed on each of three groups of 24 transistors selected in the same manner as for the step-stress HTRB experiments. Failures were also defined in the same manner by using the ±10-percent-shift criterion for the h_{FE} tests. The groups were stressed under electrical conditions of approximately 100, 300, and 500 mW to determine which condition proved optimum for inducing failures.

In Figure 13, which shows the results obtained, the junction temperature T_j is the sum of the ambient temperature and the temperature produced by the electrical power dissipated in the transistor. Appendix D contains a description of the method by which the junction temperatures were obtained. Figure 13 clearly shows that more failures are induced with increased power dissipation; therefore, the highest power dissipation (500 mW) is the one which should be selected for the stress-in-time experiments.

Stress-In-Time Tests at 500-mW Power Dissipation to Determine Optimum Time and Temperature

Four groups of 48 transistors were tested at different junction temperatures (150, 175, 200, and 225°C) for times ranging from 264 to 552 hours in a manner similar to that shown in Figure 4. The groups were periodically removed for testing to the electrical tests listed in Appendix A and the failure-rate-versus-time-on-burn-in curves (Figures 14 through 17) were compiled in a manner similar to that used for the HTRB curves (Figures 6 through 11).

At first glance, the results appear to be a departure from the previous HTRB analysis and from the results of Kemeny's operational studies of germanium devices up to a maximum junction temperature of 105°C.[10] The early-failures region is distorted at the two lower temperatures. For the T_j = 150°C test, the failure rate after one hour was lower than the rate for the next five hours; and for the 175°C test, no failures occurred during

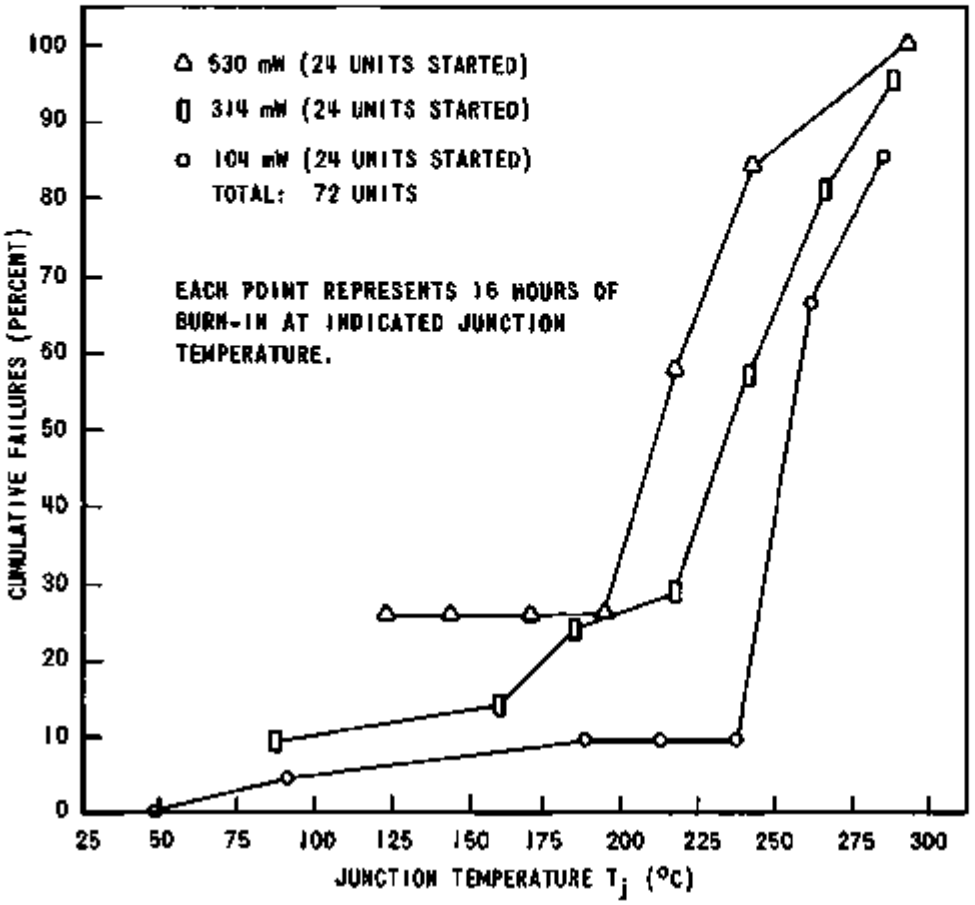


Figure 13. Comparison of Failures for Three Step-Stress Burn-In Groups (Note increase in failures at increased power levels.)

the first hour, but a large number occurred during the next five hours. Moreover, after the first hour at these two lower temperatures, the failure rate decreased approximately linearly with time on the log-log plot and no constant-failure-rate region appears to exist in the curve. The latter condition is, in part, an illusion created by the log-log plot. If the dependence is linear on such a plot, then

$$\log \lambda = \log A + B \log t, \qquad (6)$$

where log A is a constant and represents the Y-axis intercept, B is the constant slope, and t is the time on burn-in. Then

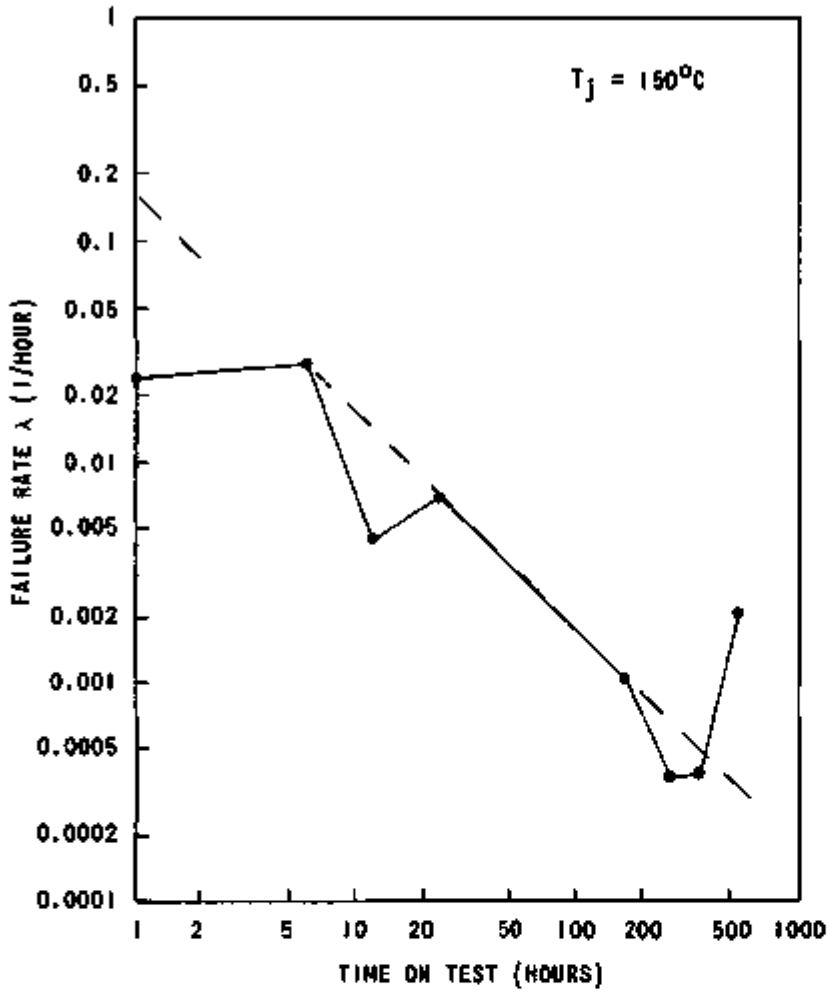


Figure 14. Failure Rate Versus Time for 150°C Burn-In (Failure rate at 1 hour was less than that at 6 hours.)

$$\log \lambda/A = \log t^B,$$

and

$$\lambda = A\, t^B. \qquad (7)$$

The values of A and B, determined graphically for each temperature in Figures 14 through 17, are shown in Table 5.

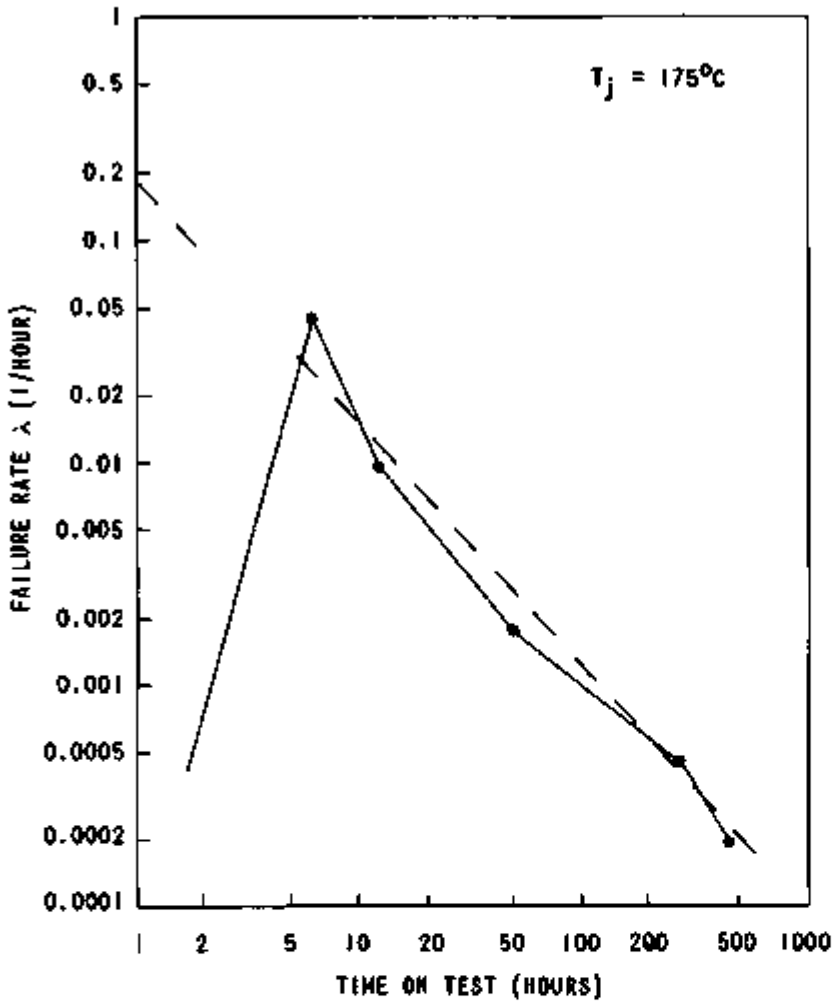


Figure 15. Failure Rate Versus Time for 175°C Burn-In (No failures occurred during the first hour; the last three points on the right represent cumulative failure rates; no failures occurred at several test points.)

The values of B appear to be independent of the junction temperature and reasonably close to a value of -1 (the mean of the four values is -1.00). Thus from Equation 7, the failure rate λ is approximately proportional to 1/t. If λ is plotted as a function of t, as in Figure 18, the curve again looks similar to the ideal curve of Figure 5. Thus the illusion of a linearly decreasing failure rate is explained; however, the constant-failure-rate

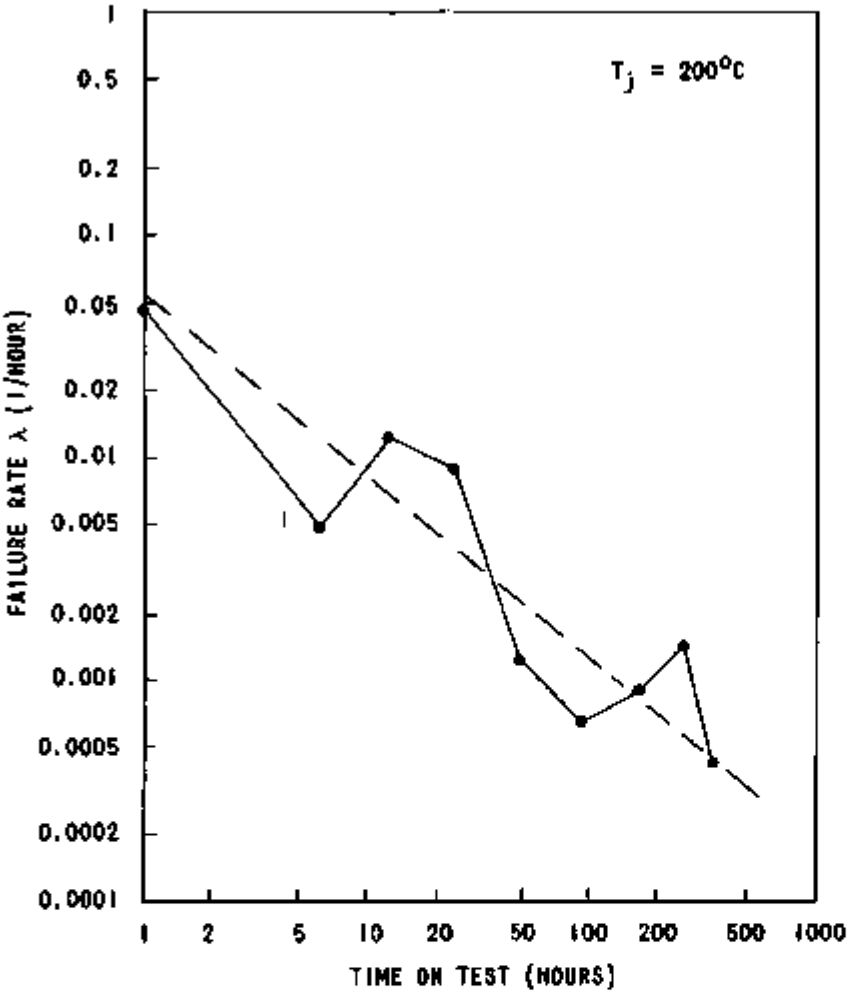


Figure 16. Failure Rate Versus Time for 200°C Burn-In

Table 5. Graphical Determination of A and B for Burn-In

Junction Temperature (°C)	Y-Intercept A	Slope B
150	0.161	-0.98
175	0.180	-1.09
200	0.054	-0.82
225	0.287	-1.12

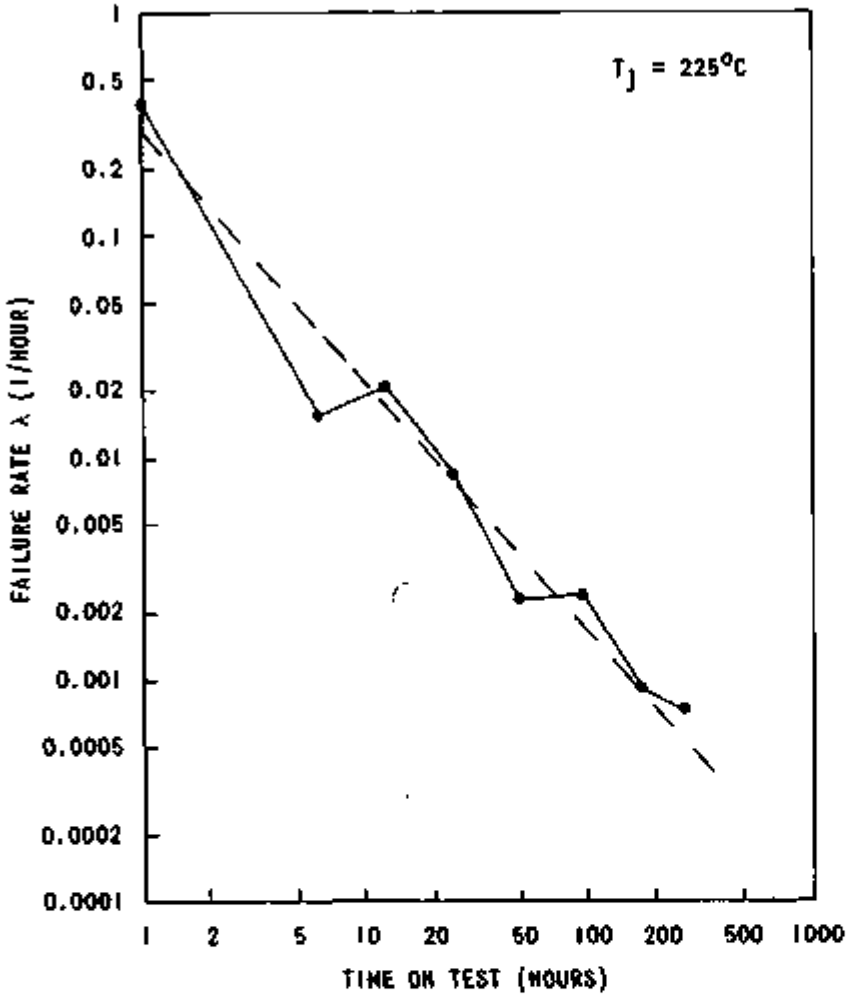


Figure 17. Failure Rate Versus Time for 225°C Burn-In

region cannot be simply described as *constant; slowly decreasing* perhaps would be a better term.

The remarkable thing about the burn-in results is the similarity in the variation of the failure rate with time for the four junction temperatures represented by Figures 14 through 17. In each case, values of the slope and intercept are close and indicate that the failure rate for burn-in is practically independent of the junction temperature under these input power conditions. The Arrhenius relationship (Equation 5) does not hold.

One possible explanation for these results is that during burn-in a large emitter current density is present which causes an electric

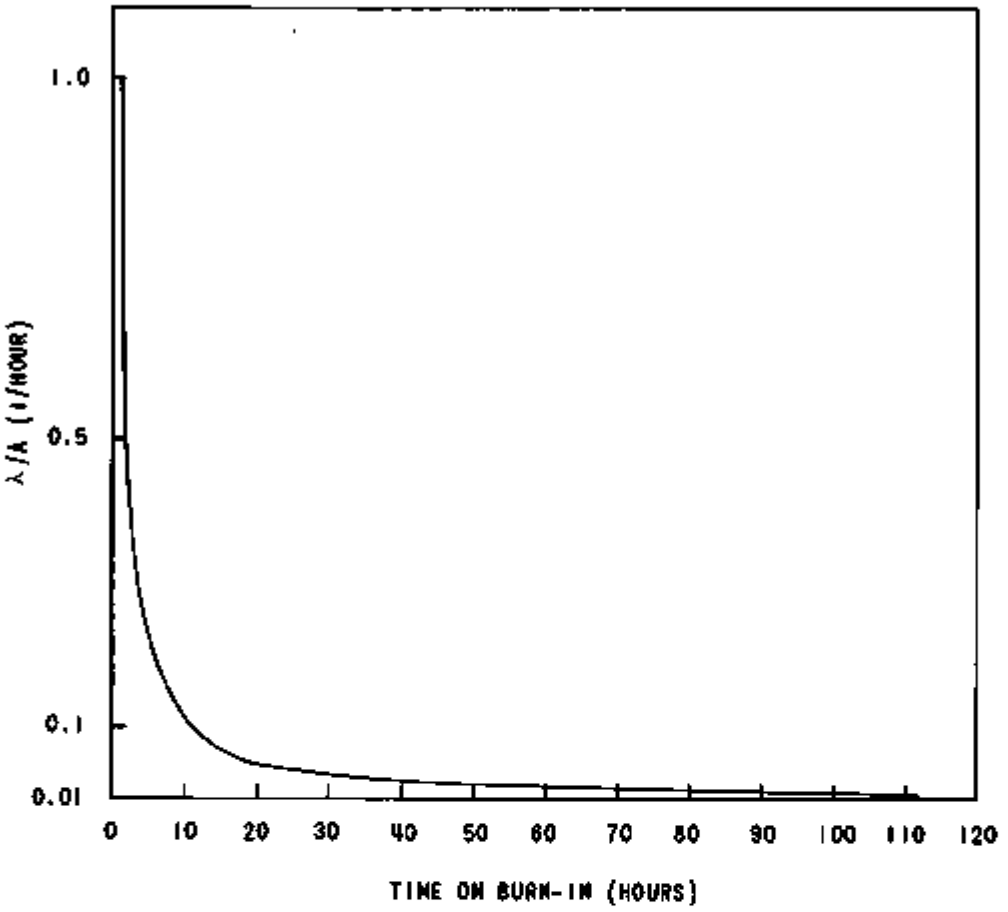


Figure 18. Failure Rate 1/t-Dependence Upon Time (Note slow decrease in failure rate after 20 hours.)

field due to the large space charge in the emitter-base junction transition region. According to Ohwada and Nishi[11], this electric field can become very intense, reaching a magnitude of 10^6 volts per centimeter. For an NPN transistor with contaminating positive ions in its silicon dioxide layer, the effect of such a field would be to attract the positive ions toward the area of the oxide immediately over the emitter-base junction. As the ions diffused preferentially toward that area, the current gain would drift, as described in Appendix C. In this case, normal random movement of ions by diffusion, which depends on temperature, would be overshadowed by a strong tendency of the ions to drift preferentially with the electric field. This tendency would reduce the dependence of the failure rate on temperature. At lower emitter current densities, the electric field due to a space charge in the junction transition region may be negligible,

and ions in the oxide therefore might migrate mainly through a random diffusion process. In such a case of lower power, the Arrhenius equation is likely to hold once again.

In contrast to the determination of optimum HTRB time, the optimum burn-in time under conditions of high power dissipation depends strongly upon the reliability required by the end-use of the transistor. For HTRB, the reliability cannot be improved beyond the optimum time, since the failure rate becomes constant. For burn-in, however, the failure rate decreases continuously. Since the burn-in failure rate has approximately a 1/t dependence on burn-in time, 10 hours on burn-in will reduce the failure rate by one order of magnitude, 100 hours will reduce it two orders of magnitude, etc.

In the absence of end-use considerations, the optimum burn-in time is the time required to get past the steep part of the curve shown in Figure 18 where the failure rate decreases rapidly with time. This occurs at approximately 20 hours with λ decreasing to 0.05 of its value at 1 hour. After 20 hours, λ decreases very slowly. For administrative reasons, an extension of the time to 24 hours might be desirable.

The 1-hour point has been excluded from consideration in the calculation of slopes and intercepts for the 150°C and 175°C tests. Statistical variation may account for the variations shown, but the probability is not great. For example, if the best-fit lines on Figures 14 and 15 are extended, the failure rate is approximately 10^{-1} per hour for 150°C and 2×10^{-1} per hour for 175°C at 1 hour. Thus, by using from 40 to 50 transistors, 4 or 5 failures could be expected in the first hour at 150°C. Only one occurred. Similarly, 8 to 10 failures could be expected at 175°C, where none occurred. The lower failure rate in the first hour is therefore probably real and not due to statistical variations in the small number of parts.

Accomplishments, Power Burn-In

The failure-rate-versus-time curves indicate that the failure rate for power burn-in is approximately inversely proportional to the time on burn-in, and the failure rate is practically independent of the junction temperature for the specific electrical conditions applied. This independence may be due to ion movement in the device oxide toward the emitter base junction, a condition which is caused by a space charge of electrons in the junction transition region setting up a strong attractive electric field for the ions, as previously described.

The optimum time for burn-in depends upon the end-use reliability requirements for the transistor since, because of the dependence of the failure rate upon 1/t, longer times produce lower failure rates.

In the absence of end-use requirements, a time of 24 hours on burn-in at the maximum power-dissipation rating of the devices is recommended. At 24 hours, the failure rate is reduced to approximately 0.042 the failure rate at one hour; further time on burn-in reduces the failure rate very slowly (at 100 hours, the failure rate is 0.01 the failure rate at one hour). Also, a 24-hour burn-in time makes administration of the program less complicated.

No advantage is realized in raising the ambient temperature of the transistors or the temperature of the burn-in above room temperature.

The lower failure rates in the first hour of the 150 and 175°C tests suggest that, below T_j = 175°C, a short period of time is required to activate failures; however, the evidence for this is neither strong nor conclusive.

Determination of Sequence for HTRB and Burn-In

Procedure

After the optimum conditions were determined for HTRB and burn-in, an experiment was performed to determine whether HTRB and burn-in should be performed in a particular sequence.

Two groups of 2N2222A transistors were selected in identical ways. Each group consisted of 96 transistors, 75 percent of which were Dallas (Lot 009) and 25 percent were Singapore (Lot 7024A). Half of both subgroups were treated, as previously described.

Electrical tests, described in Appendix A, had been performed on each group prior to treatment. These tests were then repeated on the transistors which had been treated. Because considerable time elapsed between the initial testing and the experimental use, the tests of Appendix A were repeated and several low-current h_{FE} tests (at 10, 100, and 500 μA) were added to the sequence.

One group of transistors, designated Group I, was subjected to 48 hours of 200°C-HTRB at V_{CB} = 55 V, followed by electrical tests. It was then subjected to 24 hours of 25°C-ambient burn-in dissipating 500 mW power, followed by electrical tests. The other group, designated Group II, received the same stress, except in reverse order: burn-in was performed first, followed by HTRB. Assuming homogeneity of the groups, if a particular sequence of HTRB and burn-in is more effective in activating failures, then either Group I or Group II could be expected to have a significantly higher failure rate.

Experimental Results

Of the 96 transistors started in Group I, on which HTRB was performed first, 3 failed initial tests, 17 failed tests after the static preconditioning previously described, 7 failed tests after HTRB, and 15 more failed after burn-in.

Of the 96 transistors started in Group II, on which burn-in was performed first, 5 failed initial tests, 16 failed tests after static preconditioning, 11 failed tests after burn-in, and 4 more failed after HTRB.

The failures in both groups were very similar to the failures previously encountered in other 2N2222A HTRB and burn-in experiments. Most failed delta h_{FE} first, and a few of these later failed some leakage-current test. The predominating failure mode again appeared to be base-surface degradation due to positive ionic contamination in the silicon dioxide.

Table 6 summarizes the failure results in terms of percentage. Each percentage listed is the number of electrical failures after the stress divided by the number of good units at the beginning of the stress. The most significant disparity between the two groups is the difference of almost 13 percent (31.9 percent for Group I versus 19.1 percent for Group II) in the untreated portions of each group. This caused a difference of approximately 8 percent in the total failures (28.6 percent for Group I versus 20.0 percent for Group II). This difference may be due to sampling variation, since it is derived from 15 untreated failures in Group I versus 9 in Group II.

To determine the consistency of these results, Table 7 compares the failure rates for these two groups with similar data taken during the HTRB and burn-in stress-in-time experiments. The burn-in failure rates for both Group I and Group II are comparable to those obtained during the 200°C stress-in-time tests; however, the HTRB failure rates for both groups are lower. They, in fact, approximate the average failure rate in the constant-failure-rate region (λ_{AV}). The reason for this inconsistency may be the larger-than-expected number of failures between 12 and 24 hours for the 200°C stress-in-time group (Figure 7).

Accomplishments, HTRB and Burn-In Sequence

Table 6 indicates no differences in test results between Group I and Group II that could not be accounted for by sampling variation, nor does the static preconditioning performed on part of each group offer any obvious improvement in the failure rate. The conclusion must therefore be reached that HTRB and power burn-in need not be performed in a particular sequence in order to enhance reliability; however, since burn-in produces more than

Table 6. Percentages of Failures for HTRB and Burn-In Sequence Tests

Failing Devices	Point of Failure					
	Group I			Group II		
	After HTRB (Percent)	After Burn-In (Percent)	Combined (Percent)	After Burn-In (Percent)	After HTRB (Percent)	Combined (Percent)
Treated	6.7	17.9	23.3	10.7	12.0	21.4
Untreated	10.6	23.8	31.9	17.0	2.6	19.1
Total	9.1	21.4	28.6	14.7	6.3	20.0

Table 7. Comparison of Failure Rates (1/hr) for Sequence Test Groups and 200°C HTRB and Burn-In Stress-In-Time Groups

Test Compared	Group Compared			
	Group I ($\bar{\lambda}$)	Group II ($\bar{\lambda}$)	200°C Stress-In-Time ($\bar{\lambda}$)	200°C Stress-In-Time (λ_{AV})
HTRB	0.001893	0.001302	0.007401	0.001687
Burn-In	0.008928	0.006111	0.009689	- -

twice as many failures as HTRB, burn-in should be performed first so that failures can be eliminated earlier in the processing.

HTRB and Power Burn-In of Beam Lead Transistors

Seven types of beam lead transistors, GT2219, GT2907, GT2369, GT3829, HT918, GT2484, and GT3965, were procured from Texas Instruments for analysis through HTRB and power burn-in. These devices are electrically equivalent to devices bearing corresponding "2N" numbers (for example, GT2907 is equivalent to 2N2907). The testing was designed to determine the potential failure modes which might be present in devices built with the new technology and to find out whether, as with conventional transistors, HTRB and power burn-in can effectively accelerate such failure mechanisms.

Beam Lead Device Construction

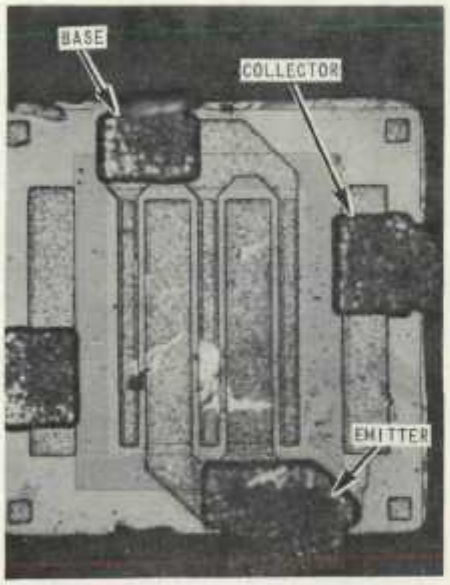
The three distinct types of chip construction which were present among the seven types of beam lead transistors that were analyzed are illustrated in Figures 19 through 21. These basic chip constructions are referred to as Type 1, Type 2, and Type 3. Generalized cross sections of beam lead devices are shown in Figures 22 and 23.

Procedure

From 75 to 100 transistors of each type of device were started into the test sequence. Initial characterization included 39 to 40 tests, described in Appendix E. Data were punched on cards by one of two Fairchild 600D transistor testers in a manner very similar to the process used for the 2N2222A transistors (Appendix B).

HTRB was performed on each type of device at a junction temperature of 150°C and at approximately 80 percent of the rated collector-base breakdown voltage. All groups accumulated 168 hours of HTRB under these conditions. Electrical tests (Appendix E) were performed at intermediate times for some of the groups and were repeated at the completion of 168 hours. A reverse bias was held on the collector-base junction while the transistors were cooling from 150°C to room temperature and during the time they were being transported to the tester.

HTRB was followed by power burn-in at a power dissipation of 658 mW and an ambient temperature of 25°C for all device types. This power dissipation was obtained by applying either V_{CE} = 14.4 V, I_E = 47 mA (on the GT3829, HT918, and GT2484), or V_{CE} = 10 V, I_E = 67 mA (on the GT2905, GT2219, and GT3965). All groups accumulated 168 hours of power burn-in. In addition to the final tests after 168 hours of burn-in, electrical tests were performed at intermediate times of 24, 48, and 96 hours.



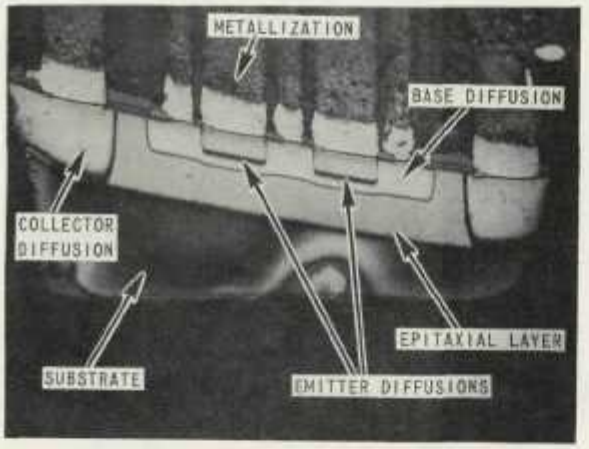


Figure 19. Type 1 Chip Construction, Used for GT2219 and GT2905 (Above, Geometry, 150X Magnification; Below, Cross Section, 200X Magnification. Cross section lapping was performed at an angle of 11 degrees with the surface.)

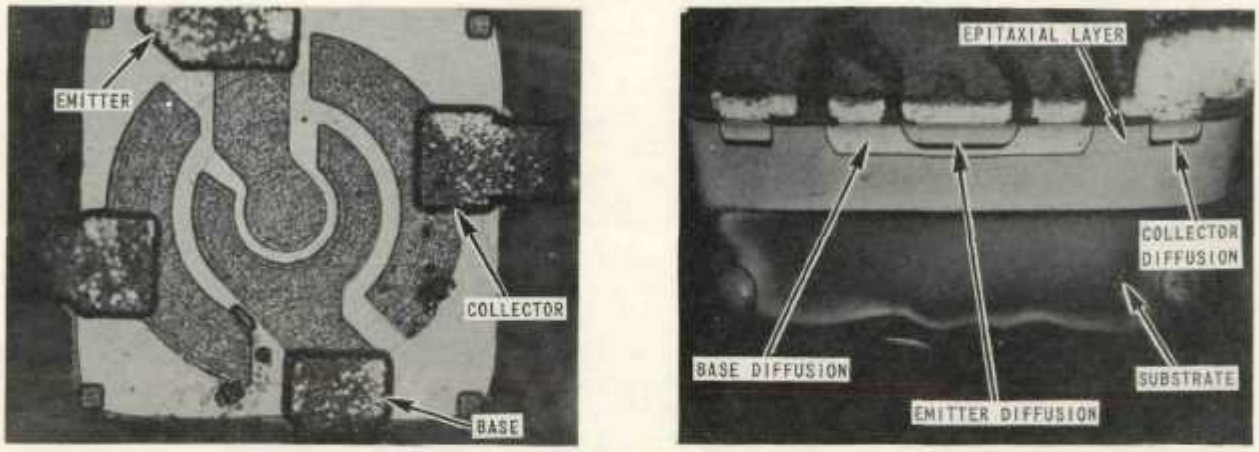


Figure 20. Type 2 Chip Construction, Used for GT2484 and GT3965 (Left, Geometry, 150X Magnification; Right, Cross Section, 200X Magnification. Cross section lapping was performed at an angle of 11 degrees with the surface.)

Analysis of Type 1 Devices (GT2219, GT2905)

The two Type 1 devices constitute an NPN-PNP complementary pair having similar electrical characteristics. The GT2219 is also very similar electrically to the 2N2222A and the SA1825 transistors. The construction of the Type 1 devices is illustrated in Figure 19.

Five of the 80 GT2219 (NPN) transistors which were started into the testing sequence failed initial electrical tests. The tests and the fixed test limits are shown in Appendix E, Table E-1. A device was subsequently counted as a failure if it failed the fixed limits of any test, or if h_{FE} shifted after HTRB or burn-in more than 10 percent at I_C = 1 mA, 20 percent at I_C = 100 μA, or 25 percent at I_C = 10 μA, as described in Appendix C. Only six transistors failed these criteria, five during HTRB and one during burn-in. All six failures were detected with either a collector-base leakage test or a collector-base breakdown-voltage test, although most of the failures also shifted more than the allowable amount on the h_{FE} tests.

The remaining 69 transistors in the group passed all tests, and the amount of h_{FE} variation was well within acceptable limits (Figure 24), thus indicating that the subsequent reliability for these devices should be very high. Failure rates during burn-in and HTRB were much lower for the GT2219 than for the 2N2222A transistor. (This is discussed later.)

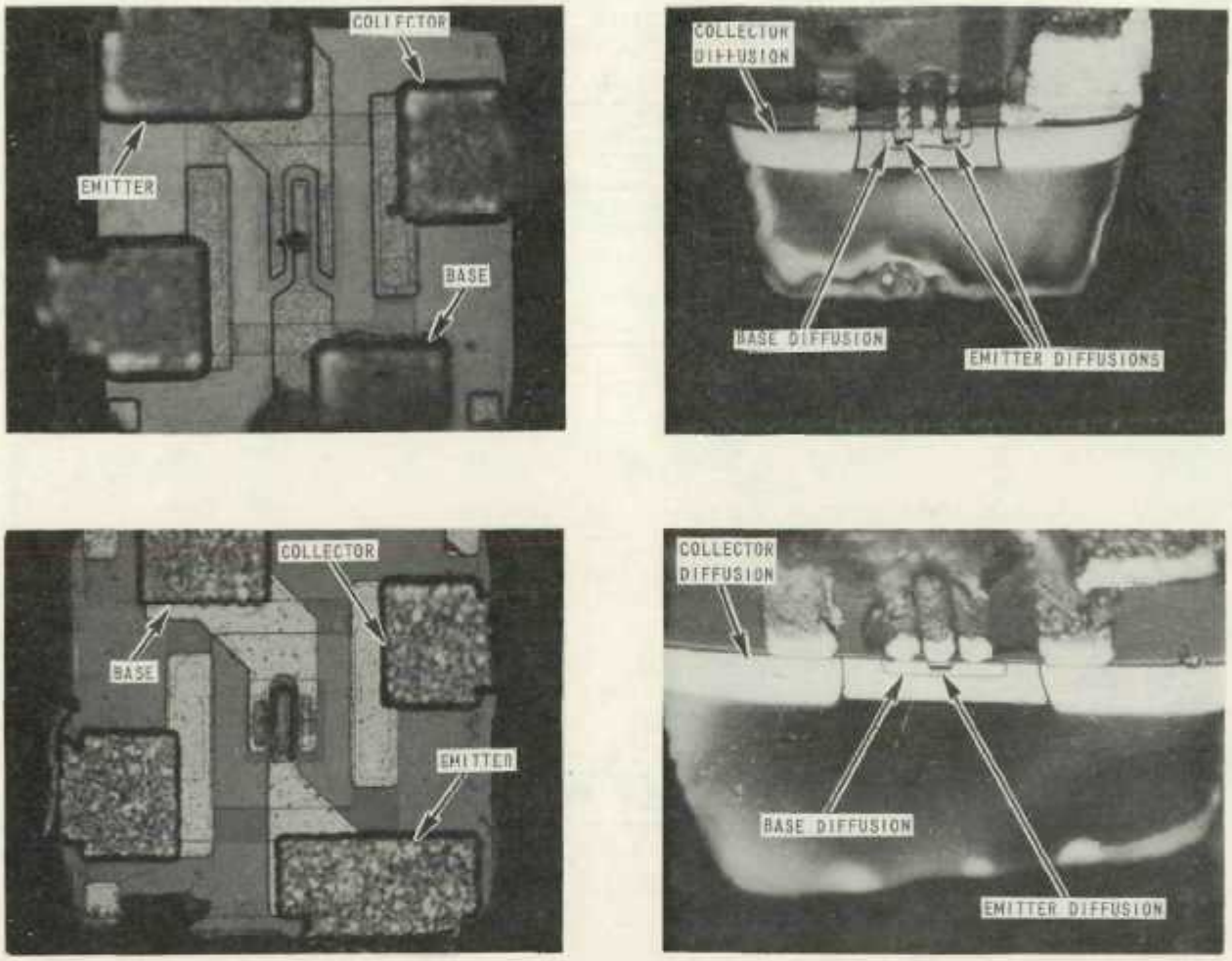


Figure 21. Type 3 Chip Construction, Upper Used for GT2369 and GT3829, Lower Used for HT918 (Upper Left, Geometry; Upper Right, Cross Section; Both 200X Magnification. Lower Left, Geometry, 200X Magnification; Lower Right, Cross Section, 250X Magnification.)

Seven of the 77 GT2905 (PNP) transistors which were started failed initial electrical tests. The tests and the test limits are shown in Appendix E. Table E-2. The same delta h_{FE} limits were used as were used for the GT2219 transistors. During HTRB, 11 of the remaining 70 transistors failed; all were failed for I_{CBO} and I_{CEO}, but some of those showing the highest leakage also failed delta h_{FE}. During burn-in, 21 additional devices failed, all during the first 48 hours of the 168-hour period. Nineteen of these 21 failed only I_{CEO} at 30 V. Many were barely over the 100-nA maximum limit, although all units had been well within

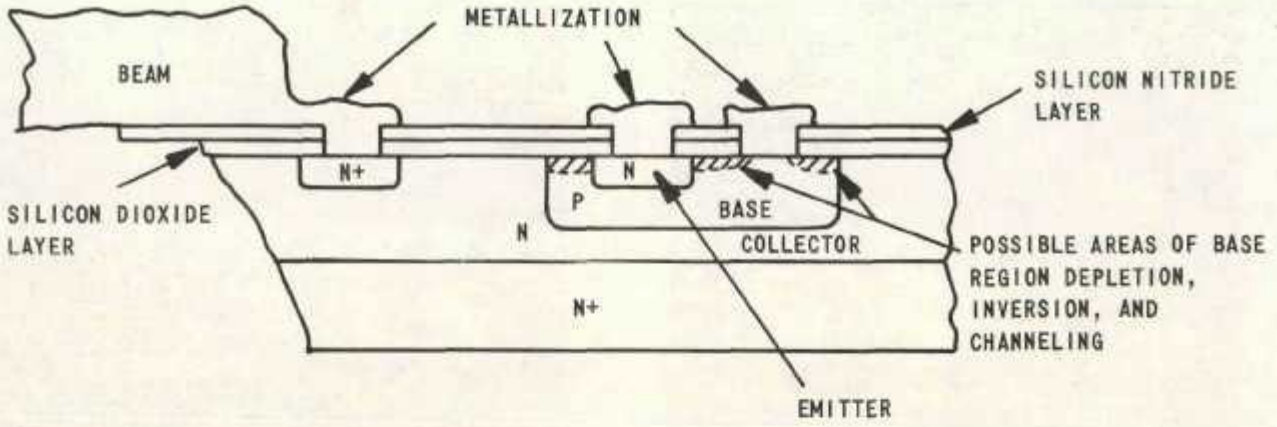


Figure 22. Generalized Cross Section of an NPN Beam Lead Transistor Showing Possible Areas Affected by Positive Ionic Contamination

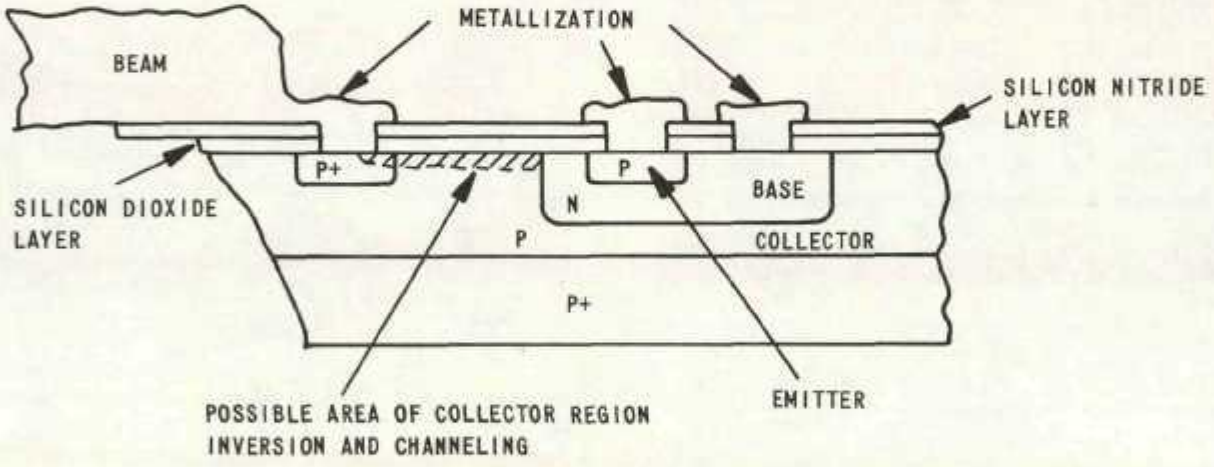


Figure 23. Generalized Cross Section of a PNP Beam Lead Transistor Showing Possible Area Affected by Positive Ionic Contamination

this limit initially (the mean I_{CEO} initially was 17.4 nA with a standard deviation of 6.3 nA).

Figure 25 indicates that neither HTRB nor burn-in had an appreciable effect on the h_{FE} of nonfailing devices. The failure rates for the GT2905 were very similar to those encountered on the 2N2222A. (This is discussed later.)

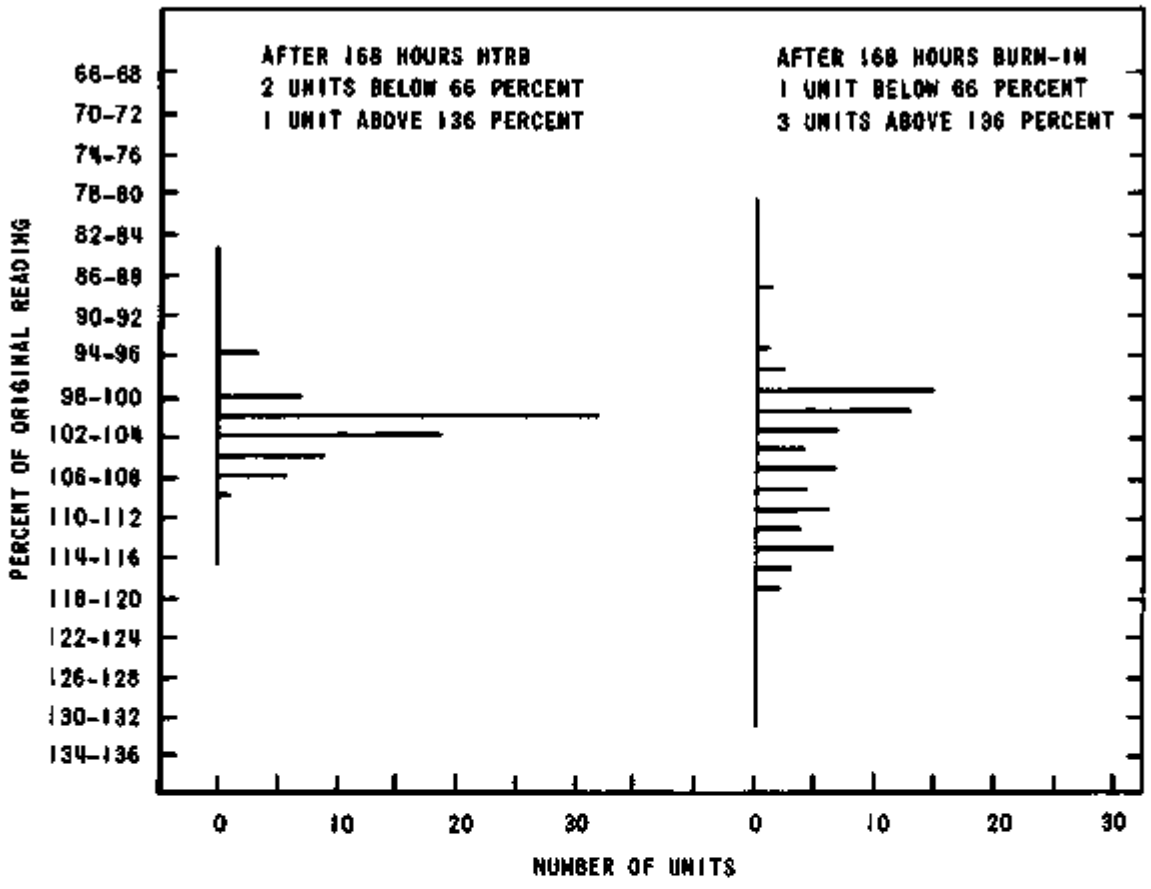


Figure 24. GT2219 Histograms of Percent Change in h_{FE} (Test 22, V_{CE} = 5 V, I_C = 10 μA. A value of 100 percent indicates no change; devices below 75 or above 125 percent are considered failures.)

Analysis of Type 2 Devices (GT2484, GT3965)

The GT2484 and GT3965 devices constitute an NPN-PNP complementary pair having similar electrical characteristics. Their construction is shown in Figure 20.

One of the 80 GT2484 (NPN) transistors which were started failed initial electrical tests. The tests and test limits are shown in Appendix E, Table E-4. The same delta h_{FE} limits were used as were used for the GT2219 transistors. During HTRB, 7 of the remaining 79 transistors failed: 4 failed only I_{CBO} or I_{CEO}, 2 failed only delta h_{FE}, and 1 failed both leakage and delta h_{FE}. During the 168 hours of burn-in, a total of 18 additional devices failed: 13 failed only I_{CEO} or I_{CBO}, 3 failed only delta h_{FE}, and 2 failed both leakage and delta h_{FE}.

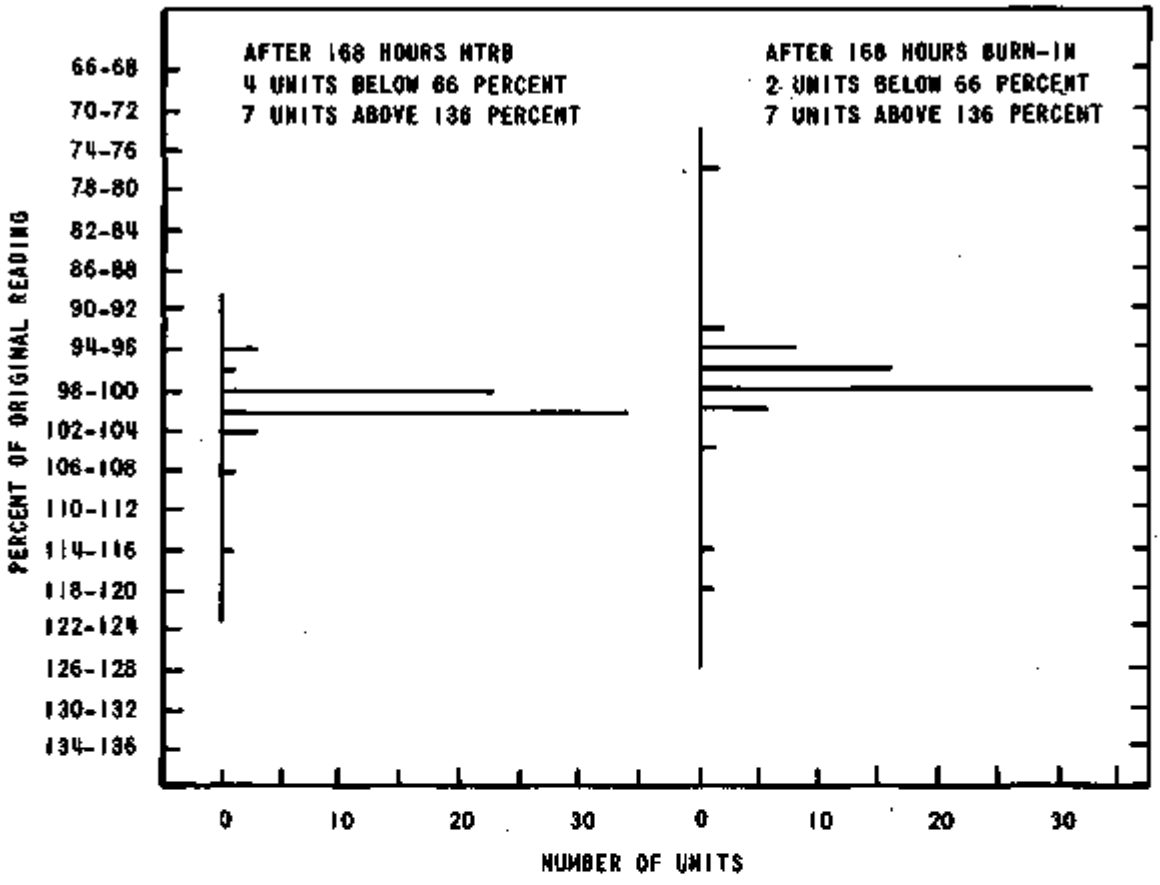


Figure 25. GT2905 Histograms of Percent Change in h_{FE} (Test 22, V_{CE} = 5 V, I_C = 10 μA.)

The h_{FE} behavior of several devices is illustrated by Figure 26. Each of the two types of failures encountered, leakage current (Units 4 and 13) and delta h_{FE} (Units 1 and 14), is compared to a nonfailing device (Unit 17). If both HTRB and burn-in are considered to accelerate the same type of failure mechanism, then the curves of the failing devices are similar. Units 1, 4, and 13 are very much alike in that HTRB caused the initial degradation of h_{FE}. Unit 14 was relatively unaffected by HTRB, but burn-in caused degradation which may not have proceeded to the extent that h_{FE} began to increase as it did with the other devices. Unit 17 did not fail any criterion at any point in the testing.

The shape of the h_{FE} curves in Figure 26 is very similar to the predicted h_{FE} variation of an NPN transistor with positive ionic contamination in the oxide over the base region, as illustrated in Figure 22 (Appendix C, Figures C-1 and C-2). This mechanism is assumed to be the cause of failure. Figure 27 indicates that although most nonfailing units in the group shifted somewhat on

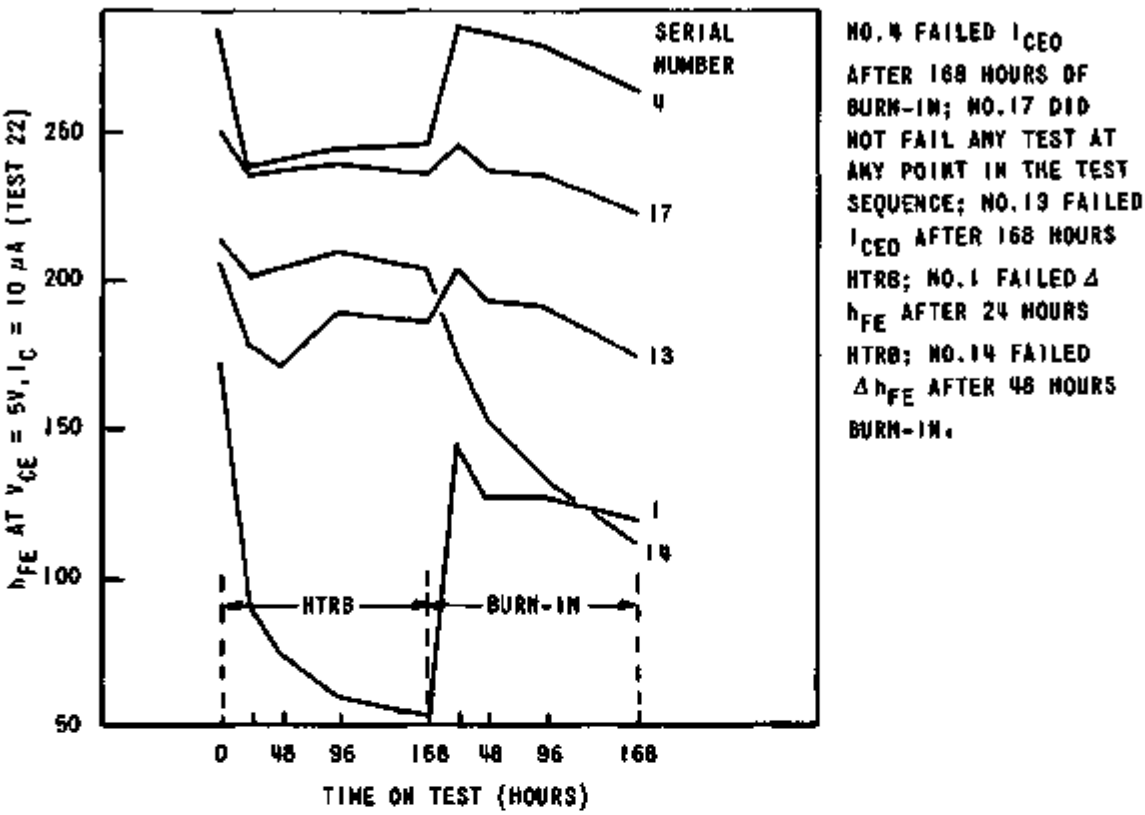


Figure 26. GT2484 Plots of h_{FE} Versus Time on HTRB and Burn-In

h_{FE} during burn-in, they were well within the allowable ±25 percent limits for this test.

One of the 78 GT3965 (PNP) transistors which were started failed initial tests. The tests and the test limits are shown in Appendix E, Table E-3. The same delta h_{FE} limits were used as were used for the other beam lead devices. During HTRB, 33 of the remaining 77 transistors failed. All of the remaining 44 units failed during burn-in: 11 failed during the first 96 hours and 33 failed during the final 72 hours. All units failed either I_{CBO} or I_{CEO}, or both. The worst leakers also failed delta h_{FE} (approximately 40 percent of the group). The transistors which did not have excessive leakage current did not shift on h_{FE}. The stability of their gain is illustrated by Figure 28.

As with the GT2484 transistor, these results are explainable if a positive ionic contamination of the silicon dioxide over the collector surface is assumed. For a PNP device like the GT3965, the collector and emitter surfaces would be affected by positive

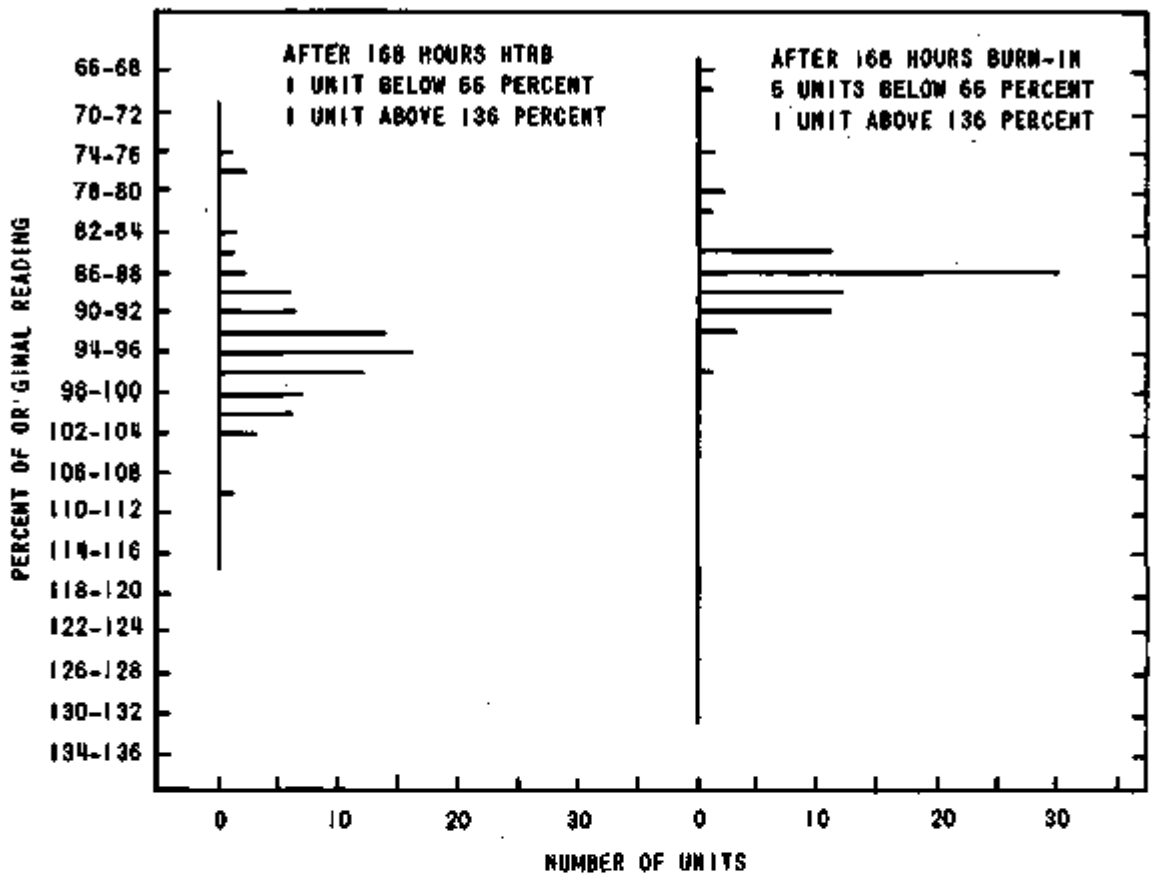


Figure 27. GT2484 Histograms of Percent Change in h_{FE} (Test 22, V_{CE} = 5 V, I_C = 10 µA.)

ions in the oxide as illustrated by Figure 23. Collector inversion and collector-base channeling could result. GT3965 failures, while more numerous, were very similar in nature to the GT2905 failures. As noted previously, the GT2905 is also a PNP device.

To test this theory, two of the GT3965 failures were examined. First, Unit 48, which had failed I_{CBO} and h_{FE} after HTRB and had continued to fail through burn-in, was analyzed. After the ceramic cap and enough of the RTV filler had been removed to expose the beam lead chip, the conformal coating protecting the chip was removed by soaking in Uresolve-Plus. After the unit was air-dried, it exhibited an I_{CBO} of 80 µA at V_{CB} = 40 V. Visual examination of the silicon nitride lip under the beams showed that the emitter nitride was intact with no cracks; however, the base nitride showed cracks.

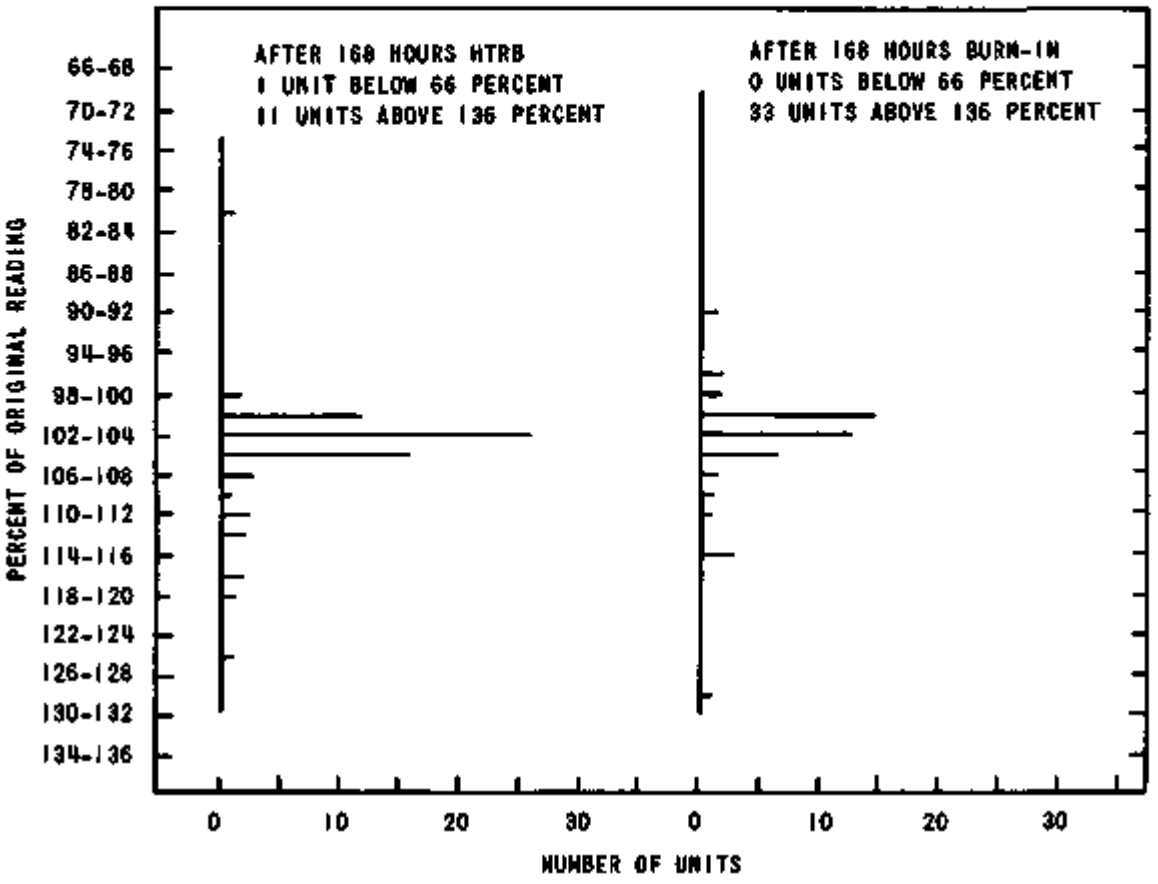


Figure 28. GT3965 Histograms of Percent Change in h_{FE} (Test 21, V_{CE} = 5 V, I_C = 10 µA. There was an upward shift in h_{FE} when leakage current became significant. Units above 136 percent represent worst leakage current failures.)

After the unit was vacuum-baked at 150°C for 30 hours, I_{CBO} had decreased to 100 nA at V_{CB} = 40 V. Examination of the unit on a curve tracer showed walking BV_{CBO}. The decrease in I_{CBO} after baking is consistent with annealing and redistributing a concentration of mobile positive ions in the silicon dioxide over the collector surface, thus dissipating the inversion layer and channel between the collector and the base of the device.

The presence of cracks in the nitride lip offered the additional possibility that moisture or foreign material caused leakage between the base beam and the collector. To eliminate this possibility, another device (Unit 26) was selected for analysis. It had failed I_{CBO} and h_{FE} after 48 hours of burn-in following HTRB. After the conformal coating was removed, visual examination

disclosed that both the base and emitter nitride lips were intact. The unit had an I_{CBO} of 84 μA at V_{CB} = 40 V. After vacuum-baking at 150°C for 30 hours, I_{CBO} had decreased to 200 nA.

The chip was then removed from the header and the front side was visually examined. It appeared to be clean, and no defects were noted. The failure therefore was not caused by cracks in the nitride lip, but rather by surface contamination which was dissipated by the high-temperature exposure.

Analysis of Type 3 Devices (GT2369, GT3829, HT918)

The GT2369 (NPN) and GT3829 (PNP) transistors constitute a complementary pair having similar electrical characteristics. The HT918 is an NPN transistor which has a slightly different geometry than the other two, but which is similar enough to the GT2369 to warrant consideration in this analysis. The construction of these devices is illustrated in Figure 21.

Two of the 80 GT2369 (NPN) transistors which were started failed initial tests. The tests and test limits are shown in Appendix E, Table E-6. The same delta h_{FE} limits were used as were used for the other beam lead devices. During HTRB, 21 of the remaining 78 transistors failed some combination of I_{CEO} (Test 6) or delta h_{FE} (Test 22, 26, or 30), with I_{CEO} failures being the more prevalent. During burn-in, 52 of the remaining 57 units failed, with delta h_{FE} being the predominant failure mode. Of these failures, 51 occurred between 24 and 48 hours.

Figure 29 shows the effect of HTRB and burn-in on a few devices from the GT2369 group. As with the previously described GT2484 group, the h_{FE} variation was very similar to that predicted in Appendix C (Figures C-1 and C-2) for an NPN device with positive ionic contamination of the base surface near the emitter. The histograms shown in Figure 30 indicate that the same type of h_{FE} variation occurred for nearly all of the devices in the group. Similar changes in h_{FE} because of burn-in have been reported by others.[12]

The mean of the h_{FE} degradation after 48 hours of burn-in is approximately 80 percent of the initial reading (Figure 29), whereas the fail-point for Test 22 (h_{FE} at I_C = 10 μA) is 75 percent. For Test 30 (h_{FE} at I_C = 1 mA), the mean at 48 hours is approximately 87 percent with a fail-point of 90 percent. Thus most units were barely acceptable for Test 22 criteria and barely unacceptable for Test 30 criteria. This indicates the basic compatibility of the two criteria. It also illustrates the importance of choosing an h_{FE} test at a collector current close to that of the expected application of the transistor.

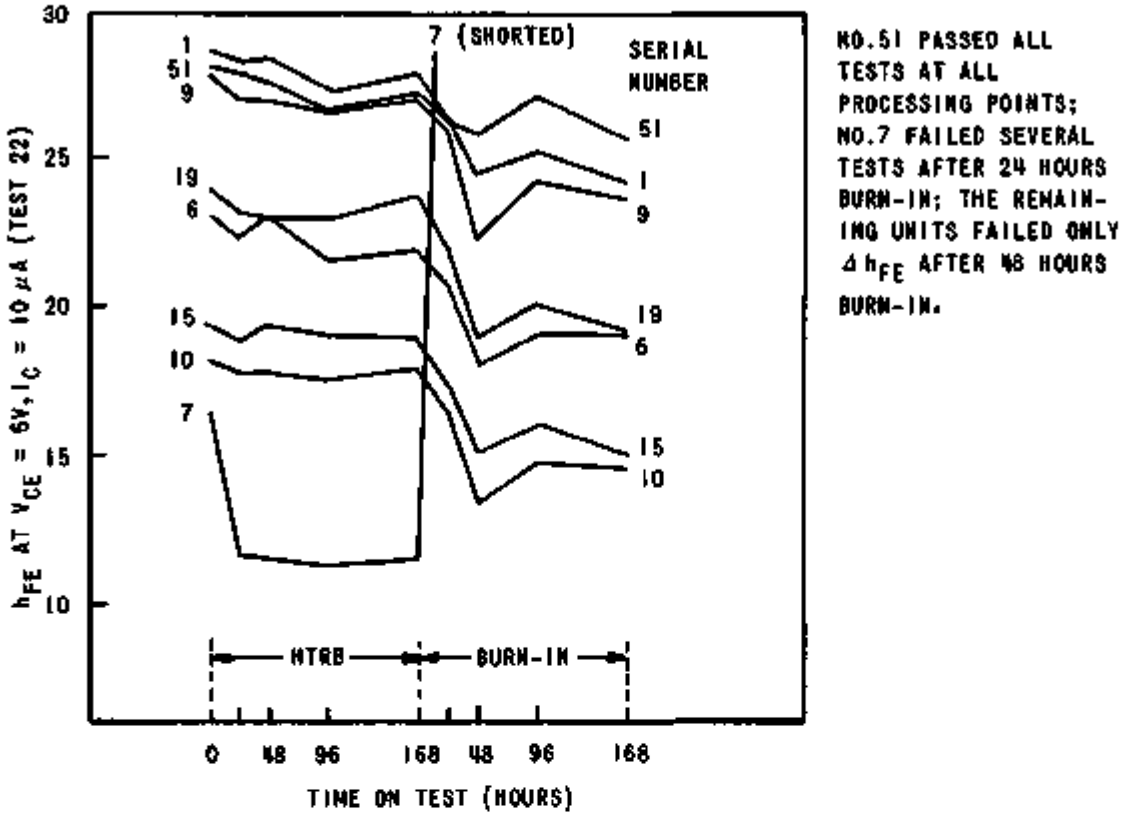


Figure 29. GT2369 Plots of h_{FE} Versus Time on HTRB and Burn-In

The HT918 (NPN) transistor, having a construction and characteristics somewhat similar to those of the GT2369, showed similar results. Only one of the 100 starting units failed during HTRB, but 97 of the remaining 99 failed delta h_{FE} during the first 24 hours of burn-in. The last two devices failed between 48 and 96 hours of burn-in. Tests and test limits for the HT918 are tabulated in Appendix E, Table E-5. Figures 31 and 32 illustrate the same type of h_{FE} variation in the HT918 that was observed in the GT2369, and a similarity to the curves shown in Appendix C (Figures C-1 and C-2). Again, the cause of the variation was positive ionic contamination which affected the base surface near the emitter.

Seventy-five GT3829 (PNP) transistors were started into HTRB. Electrical tests and test limits are tabulated in Appendix E, Table E-7. Eight transistors failed during HTRB, six of which failed I_{EBO} and some combination of I_{CBO}, I_{CEO}, or delta h_{FE}. The remaining two HTRB failures were for delta h_{FE} only, and

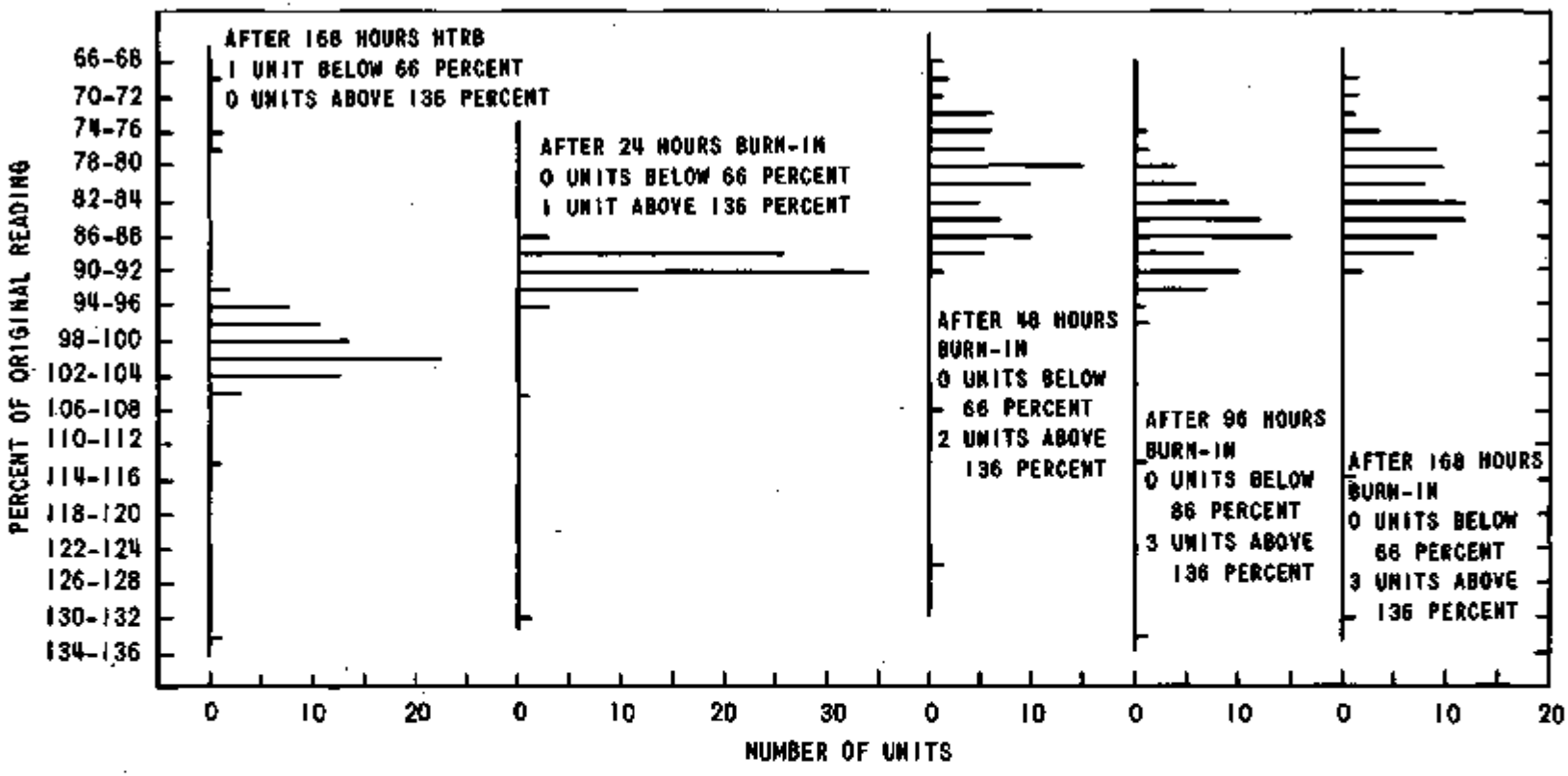


Figure 30. GT2369 Histograms of Percent Change in h_{FE} (Test 22, V_{CE} = 5 V, I_C = 10 μA. Group variation is similar to individual device variation in Figure 29.)

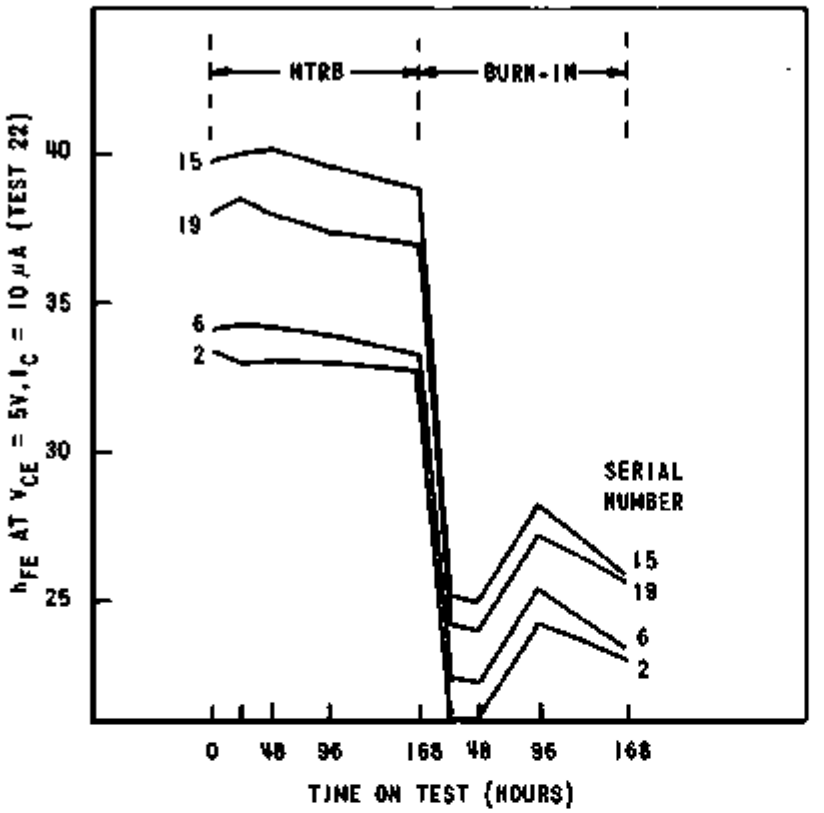


Figure 31. HT918 Plots of h_{FE} Versus Time on HTRB and Burn-In

they were very similar to later burn-in failures. During burn-in, an additional 27 devices failed, seven of which failed some combination of I_{EBO}, I_{CBO}, and I_{CEO}; the remainder failed only delta h_{FE}.

Figure 33 illustrates the types of failures that were encountered. The 13 failures like Unit 2 appear very similar to failures in the other PNP transistor groups (GT2905, GT3965), and they can be explained by positive ionic contamination in the oxide over either the collector or emitter surface causing collector-base or emitter-base channeling (Figure 23).

The other transistors shown in Figure 33, however, do not fit this failure mode; they appear to have failed because of negative ionic contamination which caused depletion and inversion of the base surface. This failure mode also might explain failures similar to that of Unit 2, but this explanation is not readily accepted since mobile negative ionic contamination in silicon dioxide is comparatively rare. Another possibility, suggested

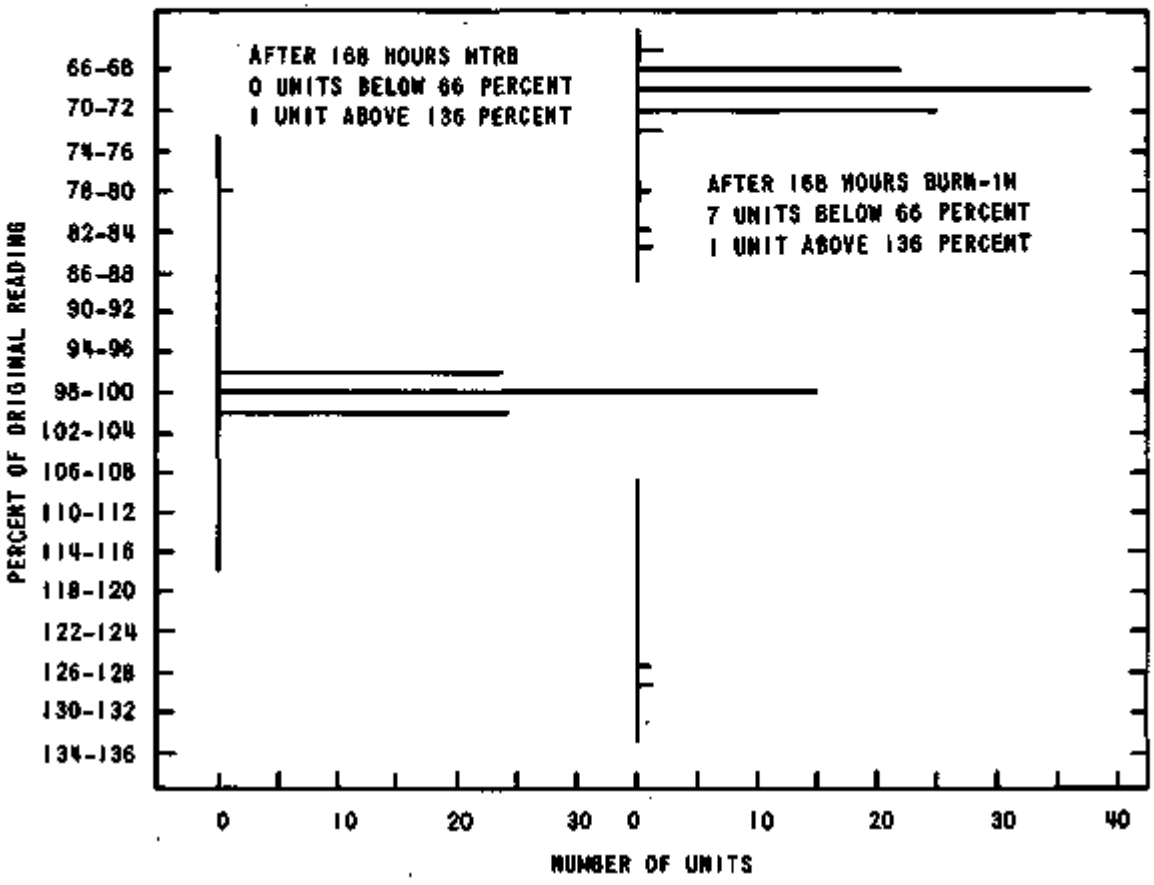


Figure 32. HT918 Histograms of Percent Change in h_{FE} (Test 22, V_{CE} = 5 V, I_C = 10 μA.)

by the shape of the curves for Units 62, 16, and 20, is that a "reverse" contamination effect caused ions to be driven away from the silicon-oxide interface by the burn-in.

In any case, although the exact failure mechanism cannot be pinpointed, the GT3829 failures appear to be related to ionic contamination problems similar to those encountered on the other beam lead devices. Figure 34 indicates that most of the units were unaffected by HTRB, and their behavior during burn-in was similar to that of one of the devices shown in Figure 33. Figure 35 shows that this is a low-current effect which disappears at collector currents of 1 mA and above.

Accomplishments, Beam Lead Transistors

Table 8 compares the cumulative HTRB failure rates of the beam lead devices with cumulative failure rates observed for the 2N2222A and the SA1825 transistors. Table 9 offers a similar

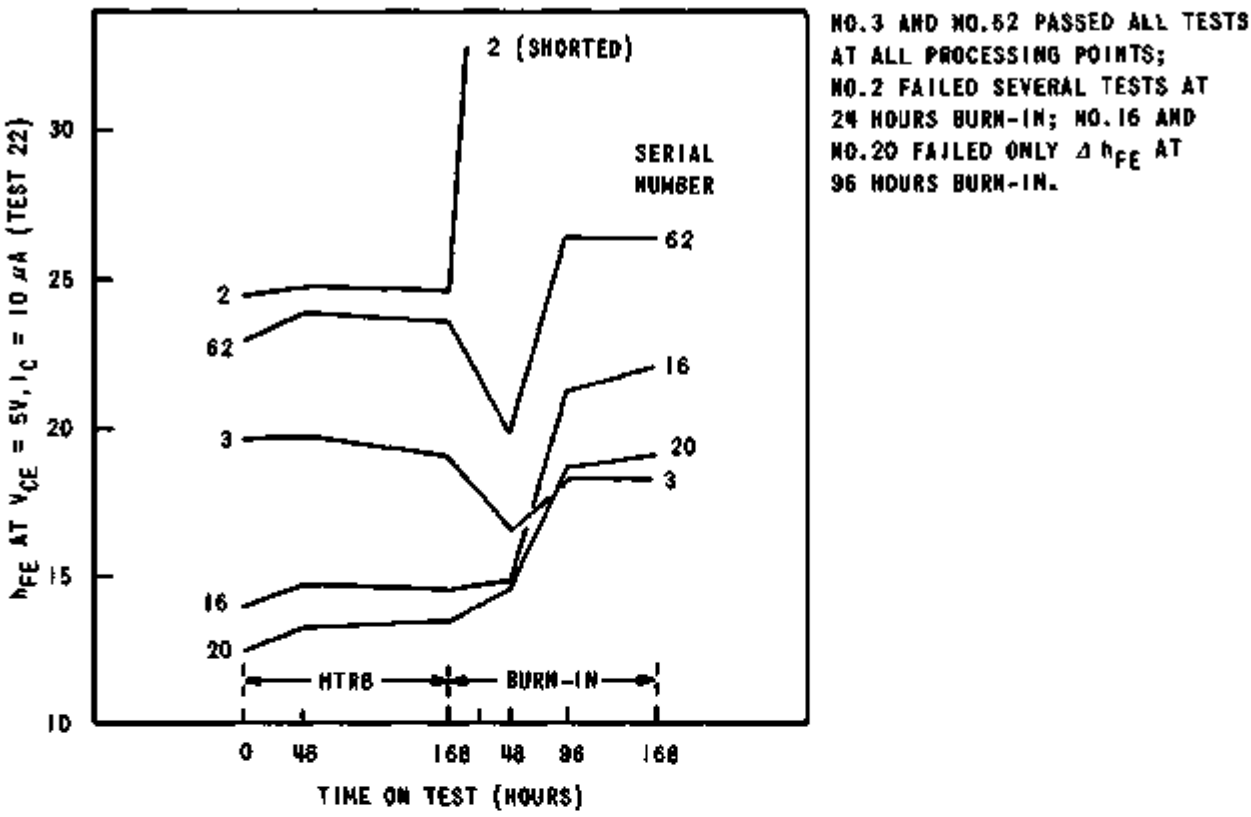


Figure 33. GT3829 Plots of h_{FE} Versus Time on HTRB and Burn-In

comparison for power burn-in. The cumulative failure rate is defined as the fraction of the starting devices which failed divided by the number of hours on HTRB or burn-in. For burn-in, the number of starting devices is the number which has passed all tests through HTRB. The cumulative failure rate normally is expected to decrease with time on HTRB or burn-in since the early failures are averaged over an increased amount of time.

On HTRB, five of the seven groups of beam lead devices (150°C, HTRB) had failure rates which were considerably lower than those for the 2N2222A transistors (175°C, HTRB). The GT3965 failure rate after 168 hours was 2.5 times and the GT2369 failure rate was 1.6 times that of the 2N2222A transistors. As previously noted, the predominant failure mode for all three of these devices was attributed to mobile positive ionic contamination in the silicon dioxide.

On burn-in, three groups of beam lead devices (GT3965, HT918, and GT2369) were encountered in which all or nearly all of the devices failed. Three other groups (GT2905, GT2484, and GT3829)

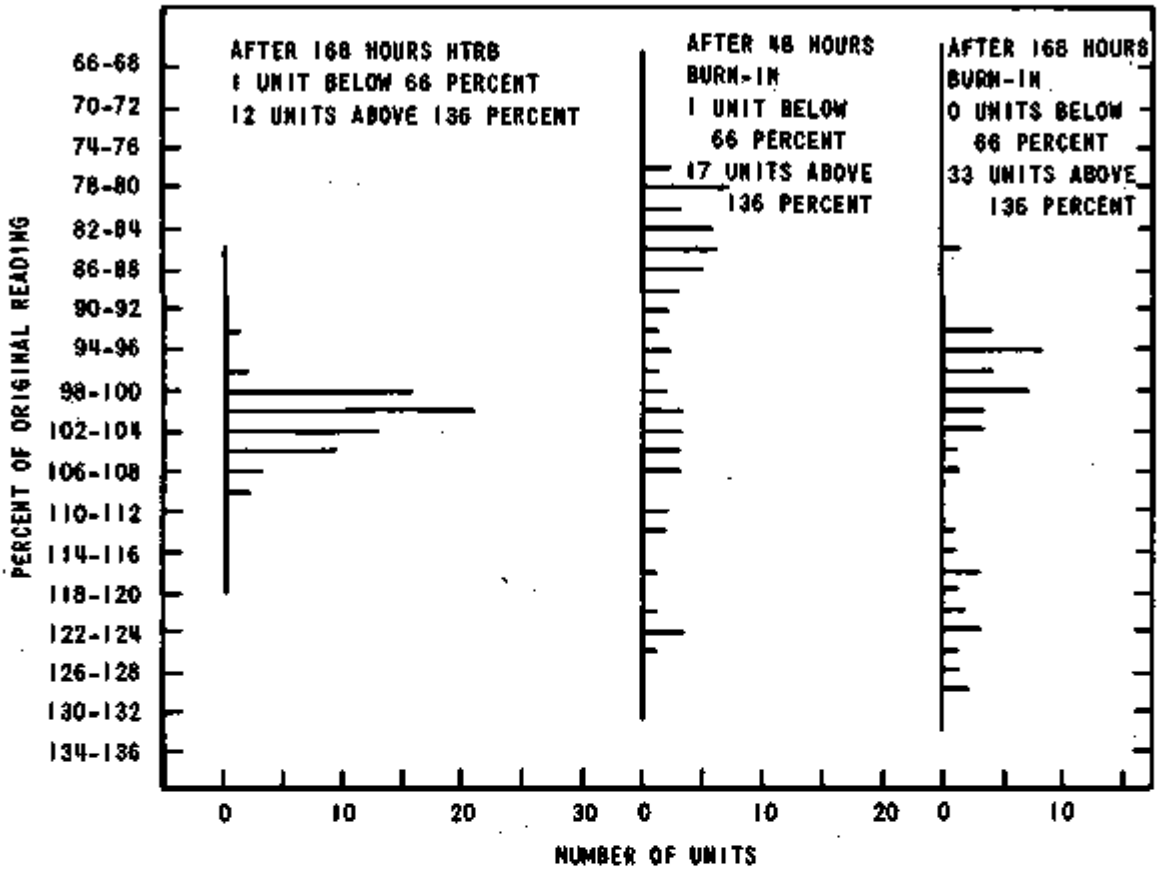


Figure 34. GT3829 Histograms of Percent Change in h_{FE} (Test 22, V_{CE} = 5 V, I_C = 10 μA. Gain was unaffected by HTRB, significantly affected by burn-in.)

had failure rates which were comparable to those of the 2N2222A transistors. Only the GT2219 devices were clearly superior to the 2N2222A, and they were superior by more than two orders of magnitude. Later experiments on similar types of beam lead devices indicated that they are capable of handling power levels up to 360 mW with much greater reliability. The possibility therefore exists that the burn-in results reported herein were caused by an overrating of the devices by the manufacturer.

An interpretation of the test results would seem to warrant the following conclusions.

- The presence of silicon nitride passivation does not necessarily make the transistor impervious to degradation caused by ionic contamination. If the nitride were thin or laced

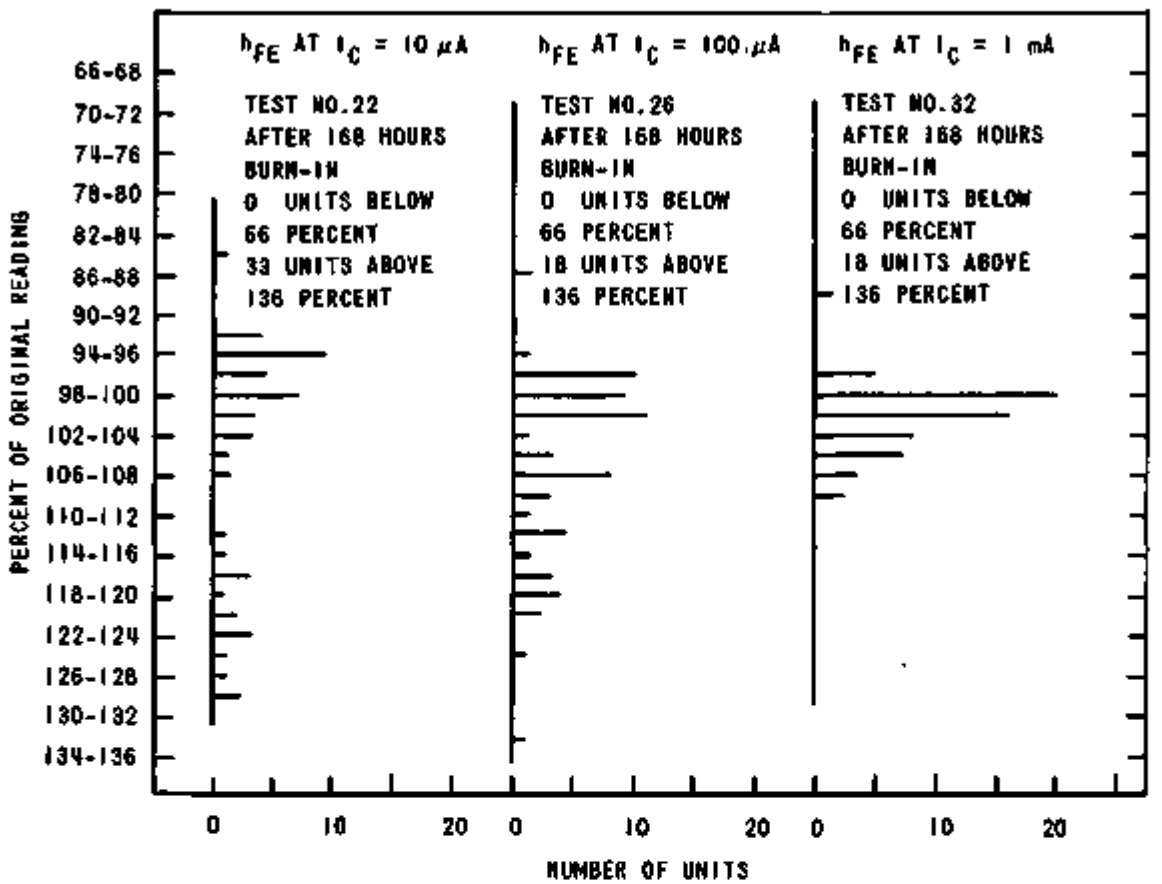


Figure 35. GT3829 Histograms Showing h_{FE} Degradation at Different Levels of Collector Current After 168 Hours of Burn-In

with pinholes, or if contaminants were present prior to the silicon nitride deposition, reliability could be greatly reduced. In contrast, McDonald[13] has shown that devices having sufficiently thick nitride overlapping the silicon dioxide at the edges of the contact windows will withstand gross contamination for 1000 hours of HTRB at 300°C without h_{FE} degradation. Test results from the GT2219 transistors also indicate the potential of a device sealed with silicon nitride passivation. However, at the time these devices were built (circa late 1971), the technology clearly had not reached its full potential.

- Beam lead devices have a built-in design problem: the necessity for placing the collector contact on the front side of the chip makes a PNP beam lead device much more

Table 8. Comparison of Cumulative HTRB Failure Rates ($\bar{\lambda}$) for 2N2222A, SA1825, and Beam Lead Transistors

Time On Test (Hours)	Device and Junction Temperature								
	2N2222A 175°C (1/Hour)	SA1825 150°C (1/Hour)	GT2905 150°C (1/Hour)	GT2219 150°C (1/Hour)	GT3965 150°C (1/Hour)	GT2484 150°C (1/Hour)	HT918 150°C (1/Hour)	GT2369 150°C (1/Hour)	GT3829 150°C (1/Hour)
24	0.003012	0.011072							
48	0.002259							0.001337	0.000833
96	0.001380							0.001335	
168	0.001004		0.000935	0.000396	0.002551	0.000527	0.000059	0.001002	0.000634

Table 9. Comparison of Cumulative Burn-In Failure Rates ($\bar{\lambda}$) for 2N2222A, SA1825, and Beam Lead Transistors

Time On Test (Hours)	Device and Power Dissipation									
	2N2222A 500 mW T_j = 150°C (1/Hour)	2N2222A 500 mW T_j = 200°C (1/Hour)	SA1825 400 mW (1/Hour)	GT2905 658 mW (1/Hour)	GT2219 658 mW (1/Hour)	GT3965 658 mW (1/Hour)	GT2484 658 mW (1/Hour)	HT918 658 mW (1/Hour)	GT2369 658 mW (1/Hour)	GT3829 656 mW (1/Hour)
24	0.010658	0.009686	0.002467	0.009587	0	0.000946	0.004630	0.040824	0.000730	
48				0.007415	0	0.003875	0.002894		0.019005	0.001554
96						0.003205	0.001881			0.004042
168	0.002214	0.001937		0.002118	0.000085	0.013888	0.001571			0.002398

susceptible to collector-surface channeling than its conventional counterpart. Such channeling occurred on all three of the PNP devices investigated. The deep P+ diffusion under the collector contact extends laterally for a short distance under the oxide and helps to retard potential channels, but such diffusions are graded and, especially when the extension under the oxide is short, can be inverted. Apparently, unless the silicon nitride completely seals the oxide from contaminants, a guard ring should be installed on PNP transistors.

- The HTRB test results indicate that beam lead devices are capable of long-term-storage failure rates comparable to the commercial 2N2222A transistor. In view of the stringent packaging requirements required for the 2N2222A (hermetically sealed under very clean conditions in an inert atmosphere), the use of beam lead devices represents an improvement in transistor technology.

- Care must be exercised in the selection of full-power ratings for beam lead transistors. Poor test results were obtained from some device types when the manufacturer's data were used to select a full-power value of 658 mW. Subsequent experiments have indicated that some of these transistor types are capable of sustained operation with low failure rates at full-power values of 360 mW or less.

Power Burn-In and HTRB of SA1825 Transistor

The SA1825 transistor is a high-reliability version of the 2N2222A transistor. This investigation was conducted to determine whether such high-reliability devices offer any advantage over carefully screened devices built on conventional commercial manufacturing lines.

The SA1825 transistors procured for this study were manufactured by Texas Instruments under strict controls placed on the assembly process. These controls were the same as those used for other "SA" devices manufactured by Texas Instruments at that time. The date code of this group was 7110.

Procedure

Because this group of transistors was intended for use in electronic systems, significant deviations from the SA1825 specifications were not allowed. Thus, burn-in and HTRB were performed at the temperatures, times, and electrical conditions defined in the Product Specification. The power dissipation for burn-in was 400 mW at 25°C ambient for 24 hours. HTRB was performed at 150°C for 24 hours at V_{CB} = 48 V. Both of these preconditioning tests were interrupted after 1, 6, 12, and 24 hours for the

electrical tests described in Appendix E, Table E-8. As with the 2N2222A and beam-lead transistor experiments, an h_{FE} shift greater than 10 percent at I_C = 1 mA (Test 9) was a failure criterion.

Experimental Results

Burn-in was performed first, and it produced nine failures among the 152 starting transistors within the 24-hour test period (seven in the first hour and two more between 12 and 24 hours). Eight of the nine failed delta h_{FE}, thus indicating surface-contamination problems. One device showed a 60-percent upward shift in V_{CE} Sat and a 10-percent upward shift in V_{BE} Sat, as well as degradation of high-current gain (Tests 12 and 13). Although this device was not further analyzed, many other transistors from the same lot which were analyzed later had defective (cracked) metallization on the chip at the oxide steps, a problem which caused this lot of SA1825's to be scrapped except for a limited quantity which was used in a noncritical application. The assumption therefore was made that cracked metallization also was the failure mode for the burn-in failure. Figure 36 compares the burn-in failure rate for the SA1825 transistor with that of the 2N2222A (2N2222A previously shown in Figure 14).

HTRB, performed after burn-in, produced 38 additional failures (one after 1 hour, nine between 1 and 6 hours, 27 between 6 and 12 hours, and one between 12 and 24 hours). All failures were for I_{CBO}, I_{CEO}, or delta h_{FE}. Figure 37 compares the HTRB failure rate for the SA1825 transistor with that of the 2N2222A (2N2222A previously shown in Figure 6).

The high failure rates through the first 12 hours of HTRB indicate the presence of a large group of early failures or freaks in the distribution. This can be better understood by analyzing the same data in a different way, using the method of Peck.[14] Figure 38 shows plots of the cumulative failures versus the time on HTRB using scales by which a straight line indicates a log-normal distribution. The S-shape of the 2N2222A curve shows that a population of early failures predominated during the first few hours of HTRB; the curve then changes slope as the early failures are averaged over longer periods of time. A straight line (log-normal distribution) is apparent in the upper portion of the curve. Using this analysis, the optimum HTRB time is the inflection point of the S-shaped curve. For the 2N2222A at 175°C, the inflection occurs at approximately 10 hours which agrees with the 6 to 12 hours previously obtained.

The SA1825 data plotted in Figure 38 show a much larger population of early failures than were present among the 2N2222A transistors. Since the HTRB time was not extended beyond the 24 hours of the

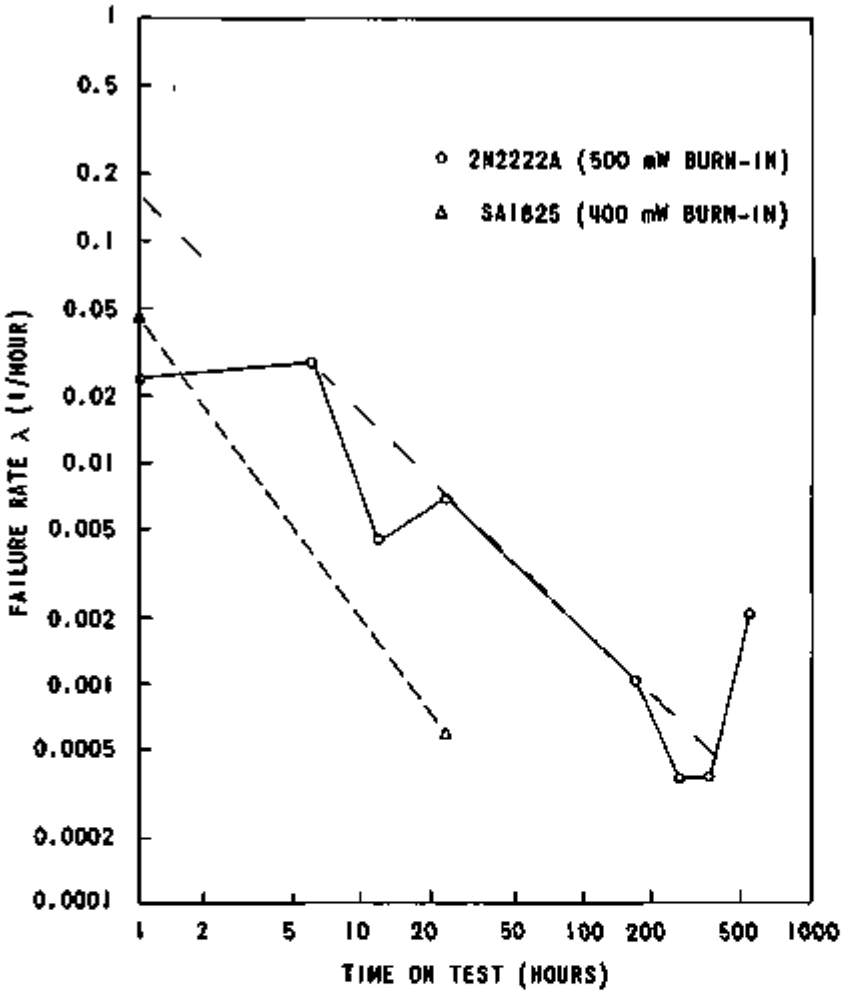


Figure 36. Comparison of Burn-In Failure Rates for 2N2222A and SA1825 Transistors

specification, the exact shape of the upper portion of the SA1825 curve is unknown; however, 24 hours appears to be very close to the inflection point. Thus the SA1825 early failures comprise approximately 27 percent of the group, as compared to approximately 6 percent early failures in the 2N2222A group.

As previously mentioned, a large number of SA1825 transistors were later discovered by other methods to have defective metallization at the oxide steps on the chip. This failure mode was not activated by HTRB, and burn-in produced only one such failure.

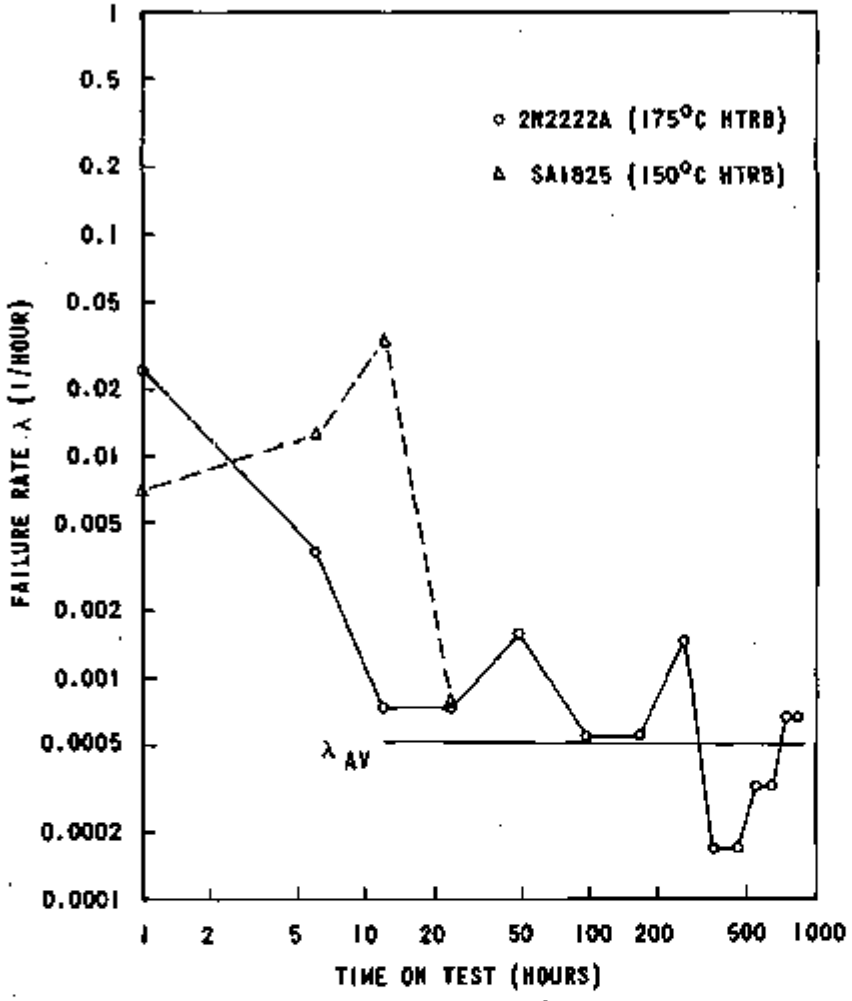


Figure 37. Comparison of HTRB Failure Rates for 2N2222A and SA1825 Transistors

Accomplishments, SA1825

Two failure modes were distinguished in the SA1825 lot. The usual surface contamination problems caused all but one failure which occurred because of defective chip metallization. Since only one such failure occurred because of HTRB or burn-in, the activation energy for the metallization failure mode is apparently considerably higher than the 1.1 eV associated with surface contamination.

Full-power operation of the SA1825 (400 mW) produced a failure-rate-versus-time-on-burn-in curve having a slope very similar to

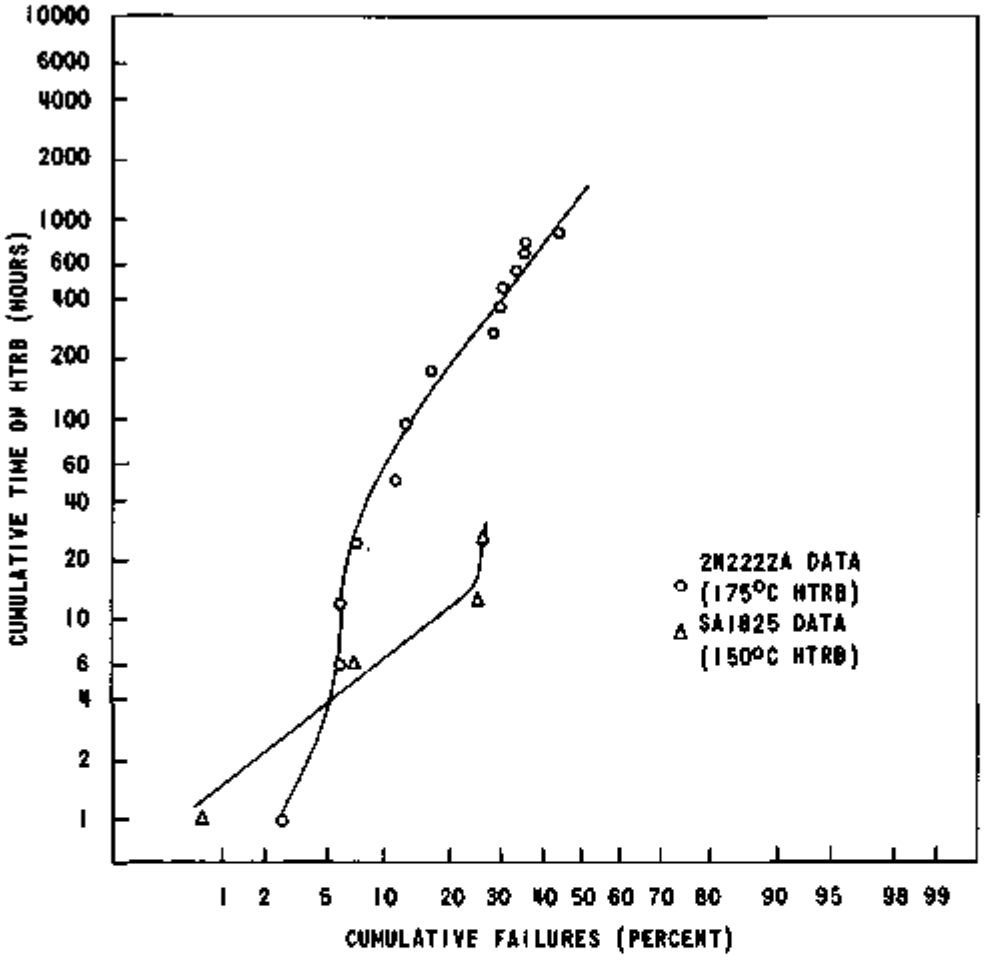


Figure 38. HTRB Failure Rates for 2N2222A and SA1825 Transistors Compared by Peck's Method

the 2N2222A curves. This indicated that the SA1825 failure rate was approximately inversely proportional to time, as was also the case for the 2N2222A. Burn-in failure rates for the SA1825 were about one order of magnitude less than for the 2N2222A; however, the 2N2222A tests were performed at a higher power dissipation (500 mW).

The HTRB results showed that a large population of early failures (27 percent, as compared to 6 percent for the 2N2222A) was present in the SA1825 group. The failures were caused by ionic contamination in the silicon dioxide layer of the chip. Clearly, the quality of this particular lot of high-reliability transistors was not as high as was the quality of the two lots of commercial grade transistors which made up the 2N2222A group.

While the ultimate reliability of this group cannot be established with complete certainty without additional data, the failure rate of the SA1825 at 24 hours has been reduced to the same level as that of the 2N2222A (Figure 37). Since the SA1825 specifications include preconditioning tests which remove the early failures prior to the ultimate use of the lot, the reliability of the transistors that are used may be high.

FUTURE WORK

The knowledge gained and the techniques developed during this project are expected to form the basis of many future reliability studies at both Bendix and Sandia. These methods can be applied to integrated circuits, diodes, and field-effect transistors, as well as to other bipolar types of transistors. Study is needed on all of these semiconductor devices to ascertain whether long-term system reliability requirements will be met.

REFERENCES

[1]MIL-STD-883, *Test Methods and Procedures for Microelectronics*, Method 1014, Test Condition C, Step I and Step II, May 1, 1968.

[2]C. H. Zierdt, Jr., "Procurement Specification Techniques for High Reliability Transistors," *Proceedings of 1967 Annual Symposium on Reliability.* Washington: IEEE Catalog Number 7C50, January, 1967.

[3]A. P. Kemeny, "Experiments Concerning the Life Testing of Transistors - I," *Microelectronics and Reliability*, Volume 10, 1971, pp 169-194.

[4]Ibid, p 175.

[5]Zierdt.

[6]Zierdt.

[7]Kemeny, pp 169-194.

[8]D. S. Peck, "Reliability of Beam Lead Sealed Junction Devices," *Proceedings of 1969 Annual Symposium on Reliability.* New York: IEEE Catalog Number 69C8-R.

[9]Kemeny, pp 169-194.

[10]Kemeny, pp 169-194.

[11]A. Ohwada and Y. Nishi, "A Stability Improvement of Current Gain in Silicon Planar Transistors," *IEEE Transactions on Electron Devices*, Volume ED-16, Number 2, February, 1969, pp 222-224.

[12]Ibid, pp 222-224.

[13]B. A. McDonald, "Three h_{FE} Degradation Mechanisms and Their Associated Characteristics," *Proceedings of 1970 Annual Symposium on Reliability Physics.* Las Vegas, Nevada: IEEE Catalog Number 70C59PHY.

[14]D. S. Peck, "The Analysis of Data From Accelerated Stress Tests," *Proceedings of 1971 Annual Symposium on Reliability Physics.* Las Vegas, Nevada: IEEE Catalog Number 71C9PHY.

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BIBLIOGRAPHY

Grutchfield, H. B. "Measurement of the Thermal Resistance and Thermal Response of Diffused Silicon Transistors." *Fairchild Semiconductor Application Bulletin*, Number APP-53, January, 1963.

Kemeny, A. P. "Experiments Concerning the Life Testing of Transistors - I." *Microelectronics and Reliability*, Volume 10, 1971.

McDonald, B. A. "Three h_{FE} Degradation Mechanisms and Their Associated Characteristics." *Proceedings of 1970 Annual Symposium on Reliability Physics*. Las Vegas, Nevada: IEEE Catalog Number 70C59PHY.

MIL-STD-883, *Test Methods and Procedures for Microelectronics*, Method 1014, Test Condition C, Step I and Step II, May 1, 1968.

Ohwada, A., and Y. Nishi. "A Stability Improvement of Current Gain in Silicon Planar Transistors." *IEEE Transactions on Electron Devices*, Volume ED-16, Number 2, February, 1969.

Peck, D. S. "The Analysis of Data From Accelerated Stress Tests." *Proceedings of 1971 Annual Symposium on Reliability Physics*. Las Vegas, Nevada: IEEE Catalog Number 71C9PHY.

Peck, D. S. "Reliability of Beam Lead Sealed Junction Devices." *Proceedings of 1969 Annual Symposium on Reliability*. New York: IEEE Catalog Number 69C8-R.

Reddi, V. G. K. "Influence of Surface Conditions on Silicon Planar Transistor Current Gain." *Solid State Electronics*, Volume 10, 1967.

Sello, H., and others (Fairchild Semiconductor). *A Study of Failure Mechanisms in Silicon Planar Epitaxial Transistors*, Technical Report Number RADC-TR-66-36. New York: Rome Air Development Center Research and Technology Division, Griffiss AFB, May, 1966.

Zierdt, C. H., Jr. "Procurement Specification Techniques for High Reliability Transistors." *Proceedings of 1967 Annual Symposium on Reliability*. Washington, D.C.: IEEE Catalog Number 7C50, January, 1967.

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Appendix A

ELECTRICAL TESTS FOR 2N2222A TRANSISTOR

The tests shown in Table A-1 were performed on each 2N2222A transistor initially and thereafter at selected points on the transistor flow chart. The tests always were performed in the sequence listed.

Table A-1. Electrical Tests for 2N2222A Transistor

Test Number	Test Type	Test Conditions	Comments
1	$V_{BE}Sat$	I_B = 5 mA, I_C = 50 mA	
2	$V_{BE}Sat$	I_B = 5 mA, I_C = 50 mA	Repeat of Test 1
3	$V_{CE}Sat$	I_B = 5 mA, I_C = 50 mA	
4	$V_{CE}Sat$	I_B = 5 mA, I_C = 50 mA	Repeat of Test 3
5	I_{CBO}	V_{CB} = 15 V	
6	I_{CBO}	V_{CB} = 30 V	
7	I_{CBO}	V_{CB} = 45 V	
8	I_{CBO}	V_{CB} = 60 V	
9	I_{CBO}	V_{CB} = 70 V	
10	BV_{CBO}	I_C = 1 µA	
11	BV_{CBO}	I_C = 10 µA	
12	BV_{CEO}	I_C = 10 µA	
13	BV_{CEO}	I_C = 10 mA	
14	BV_{CEO}	I_C = 30 mA	
15	I_{CEO}	V_{CE} = 10 V	
16	I_{CEO}	V_{CE} = 25 V	
17	I_{CEO}	V_{CE} = 40 V	

Table A-1 Continued. Electrical Tests for 2N2222A Transistor

Test Number	Test Type	Test Conditions	Comments
18	h_{FE}	V_{CE} = 1 V, I_C = 1 mA	
19	h_{FE}	V_{CE} = 1 V, I_C = 20 mA	
20	h_{FE}	V_{CE} = 1 V, I_C = 100 mA	
21	h_{FE}	V_{CE} = 1 V, I_C = 200 mA	
22	h_{FE}	V_{CE} = 1 V, I_C = 500 mA	
23	h_{FE}	V_{CE} = 5 V, I_C = 1 mA	
24	h_{FE}	V_{CE} = 5 V, I_C = 20 mA	
25	h_{FE}	V_{CE} = 5 V, I_C = 100 mA	
26	h_{FE}	V_{CE} = 5 V, I_C = 200 mA	
27	h_{FE}	V_{CE} = 5 V, I_C = 500 mA	
28	V_{BE}Sat	I_B = 5 mA, I_C = 50 mA	Repeat of Test 1
29	V_{BE}Sat	I_B = 10 mA, I_C = 100 mA	
30	V_{BE}Sat	I_B = 50 mA, I_C = 500 mA	
31	V_{CE}Sat	I_B = 5 mA, I_C = 50 mA	Repeat of Test 3
32	V_{CE}Sat	I_B = 10 mA, I_C = 100 mA	
33	V_{CE}Sat	I_B = 50 mA, I_C = 500 mA	
34	I_{CBO}	V_{CB} = 30 V	Repeat of Test 6

Tests 1 through 4 were performed to detect open or shorted devices and so that the testing could be stopped before other potentially damaging tests were performed. The plan did not work, however, since very few devices were encountered which were defective enough to fail the limits established for the tests (0.2 to 1.0 V for V_{BE}Sat, 0.02 to 0.6 V for V_{CE}Sat). The tests were retained through all of the 2N2222A experiments so that the tests for later runs would be in the same position on the data cards as they were originally. Test 34 was added to make certain that the transistors were not damaged by the tester during Tests 6 through 33.

All tests were performed with one of two Fairchild 600D automatic transistor testers which punched data on the cards in a coded language peculiar to the tester. A computer program was written which translated the Fairchild 600D language into standard engineering language and repunched the data on a new set of cards in a format suitable for the project analysis programs.

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Appendix B

DATA CARD FORMAT AND TEST CODE IDENTIFICATION FOR 2N2222A TRANSISTOR

As previously stated, all data were recorded on punched cards by the Fairchild 600D automatic transistor tester. A three-digit code was punched on each card which identified the flow-chart position that the card represented. For example, the code A51 on a card indicates that the data on that card are from the tests performed on the 175°C HTRB stress-in-time group after one hour on HTRB (Table B-2).

The data on the cards punched by the tester were in a test-code format which is unique to the Fairchild 600D. A computer program was written to translate the Fairchild language into standard engineering language and to punch a new set of cards. The new cards were used in the data analysis programs, and the original cards punched by the tester were discarded. Table B-1 shows the format of the converted cards.

Table B-1. Format of Converted 2N2222A Data Cards

Column	Description
1-6	Serial Number
7-9	Blank
10-13	Data for Test 1 (three digits and a decimal point)
14-15	Units for Test 1 (NA, UA, MA, V_ or_ _)
16-17	Blank
18-25	Repeat of 10-17 for Test 2
26-33	Repeat of 10-17 for Test 3
34-41	Repeat of 10-17 for Test 4
42-49	Repeat of 10-17 for Test 5
50-57	Repeat of 10-17 for Test 6
58-65	Repeat of 10-17 for Test 7
66-73	Repeat of 10-17 for Test 8
74-76	Flow-Chart Position Code
77-80	Card Sequence Number

Tests 9 through 34 are contained on four additional cards with eight tests on each except the last card which has two tests. The same format is used, except that the serial number is not repeated on these cards. The sequence numbers in Columns 77-80 provide for the rearrangement of the cards in the event they should become mixed. Tables B-2 through B-6 indicate the codes used for the various tests.

Table B-2. Test Codes for Stress-In-Time Experiments

Time Increment	Stress-In-Time HTRB Junction Temperature (°C)						Stress-In-Time Burn-In Junction Temperature (°C)			
	175	200	225	250	275	300	150	175	200	225
Initial Tests	A01	A01	A01	A01	A01	A01	A01	A01	A01	A01
Tests After Treatment	A04	A04	A04	A04	A04	A04	A04	A04	A04	A04
Tests After (Hours)										
1	A51	A58	A65	A72	A79	A86	04A	15A	25A	34A
6	A52	A59	A66	A73	A80	A87	05A	16A	26A	35A
12	A53	A60	A67	A74	A81	A88	06A	17A	27A	36A
24	A54	A61	A68	A75	A82	A89	07A	18A	28A	37A
48	A55	A62	A69	A76	A83	A90	08A	19A	29A	38A
96	A56	A63	A70	A77	A84	A91	09A	20A	30A	39A
168	A57	A64	A71	A78	A85	A92	10A	21A	31A	40A
264	A95	A98	01A				11A	22A	32A	41A
360	A96	A99					12A	23A	33A	
456	A97						13A	24A		
552	63A						14A			
648	64A									
744	65A									
840	66A									

Table B-3. Test Codes for Step-Stress HTRB

Junction Temperature	V_{CB} (Volts)		
	40	55	70
Initial Tests	A01	A01	A01
Tests After Treatment	A04	A04	A04
Tests After (°C)			
25	A11	A18	A25
100	A12	A19	A26
200	A13	A20	A27
225	A14	A21	A28
250	A15	A22	A29
275	A16	A23	A30
300	A17	A24	A31

Table B-4. Test Codes for Step-Stress Burn-In at 100-mW Power Dissipation

Junction Temperature	Power = 100 mW
Initial Tests	A01
Tests After Treatment	A04
Tests After (°C)	
47	A32
92	A33
188	A34
212	A35
236	A36
261	A37
285	A38

Table B-5. Test Codes for Step-Stress Burn-In at 300-mW Power Dissipation

Junction Temperature	Power = 300 mW
Initial Tests	A01
Tests After Treatment	A04
Tests After (°C)	
87	A39
170	A40
184	A41
218	A42
242	A43
266	A44
290	02A

Table B-6. Test Codes for Step-Stress Burn-In at 500-mW Power Dissipation

Junction Temperature	Power = 500 mW
Initial Tests	A01
Tests After Treatment	A04
Tests After (°C)	
122	A45
145	A46
170	A47
195	A48
219	A49
243	A50
293	A94

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Appendix C

USE OF A DELTA-SHIFT FAILURE CRITERION FOR h_{FE}

Mobile ions, if present in sufficient quantities in the silicon dioxide layer of a transistor, have long been known to cause degradation of important electrical characteristics of the device. Scrupulously clean work areas and complicated handling procedures are required in the manufacture of transistors to prevent such ionic contamination from becoming excessive. When such measures fail, the effect on the reliability of a group of transistors can be disastrous. One manufacturer* describes such changes in the oxide passivating layer or the silicon-oxide interface as the largest failure mode in the manufacture of their transistors.

A survey of the available literature indicates that the following results may be caused by mobile ionic charges in or on the surface of the silicon dioxide passivation layer.

- Depletion or accumulation of the silicon directly beneath the oxide in which charges are present
- Inversion of the silicon in the affected area from P-type to N-type or from N-type to P-type
- Channel formation

All three of these results are basically the same thing, differing primarily in degree and location. Their location in the transistor structure determines the electrical characteristics, if any, that will be affected.

McDonald** and Reddi*** have described how mobile ionic contamination in the oxide layer can affect current gain. Using specially

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*H. Sello and others (Fairchild Semiconductor), *A Study of Failure Mechanisms in Silicon Planar Epitaxial Transistors*, Technical Report Number RADC-TR-66-36. New York: Rome Air Development Center Research and Technology Division, Griffiss AFB, May, 1966.

**B. A. McDonald, "Three h_{FE} Degradation Mechanisms and Their Associated Characteristics," *Proceedings of 1970 Annual Symposium on Reliability Physics*. Las Vegas, Nevada: IEEE Catalog Number 70C59PHY.

***V. G. K. Reddi, "Influence of Surface Conditions on Silicon Planar Transistor Current Gain," *Solid State Electronics*, Volume 10, 1967, pp 305-334.

designed and fabricated transistors with metal electrodes over the emitter-base junction, surface potentials near the junction were modified in a controlled manner to simulate the effects of ionic oxide contamination. Reddi, in particular, made measurements of the effects on several different designs of transistors, and his article describes in detail the ways in which depletion and inversion of the base surface near the emitter can affect h_{FE}. He has concluded that the effect on h_{FE} depends primarily on the base-surface doping concentration and, if the base-surface potential due to contamination is assumed to increase steadily during a life test, a plot of h_{FE} versus time during the test will be similar to Figure C-1. Quantitative data, estimated from Reddi's figures, are shown in Table C-1. From Reddi's data and Figure C-1, the prediction can be made that the h_{FE} degradation will be less at higher I_C values, as illustrated by Figure C-2.

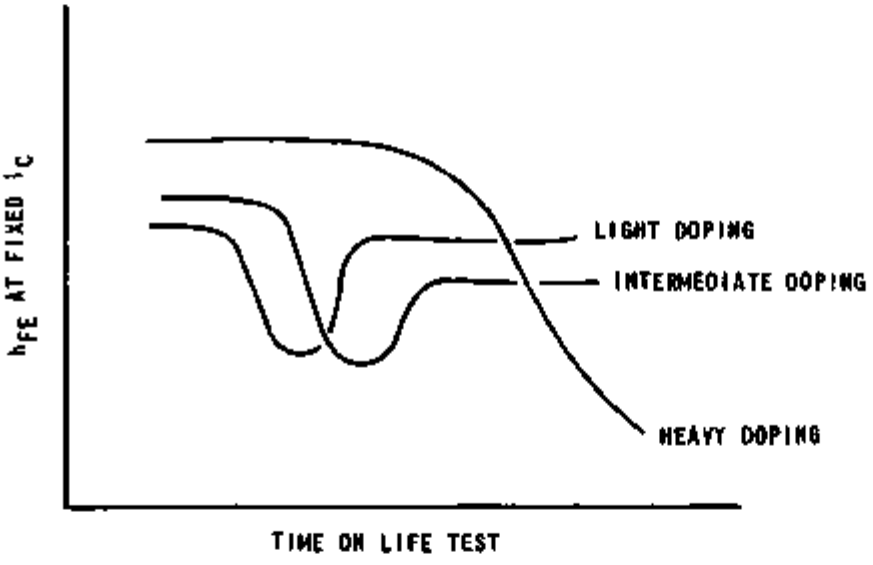

Figure C-1. Effect of Life Test on h_{FE} of a Contaminated Device for Different Base-Surface Doping Concentrations, Assuming No Channeling (Reddi)

The interpretation of the h_{FE} variation in a real situation is clearly more complicated than thus far has been described. Only the possibility of base-surface depletion and inversion near the emitter has been considered. Neither emitter-base and collector-base channeling nor depletion and inversion of the emitter surface has been discussed. Furthermore, the possibility exists

Table C-1. Effect of Different Contamination Levels on Transistors Having Light, Medium, and Heavy Base-Surface Doping Concentrations

I_C	h_{FE}*		
	V_G = 0**	V_G = +40 V***	V_G = +80 V
Reddi's Transistor A (NPN, double emitter, base-surface doping concentration 1 x 10^{18} atoms/cm^3)†			
5.9 µA	315	280 (-11)	
270 µA	769	742 (-3.5)	
Reddi's Transistor B (NPN, double emitter, base-surface doping concentration 3 x 10^{18} atoms/cm^3)††			
10 µA	281	80 (-72)	210 (-25)
100 µA	503	231 (-54)	399 (-20)
1 mA	670	503 (-25)	600 (-10)
Reddi's Transistor D (NPN, double emitter, base-surface doping concentration 6 to 7 x 10^{18} atoms/cm^3)†††			
10 µA	161	53.2 (-67)	1 (-99)
100 µA	281	126 (-55)	5 (-98)
1 mA	498	289 (-42)	24 (-95)

*Numbers in parentheses are the percentages of shift from the V_G = 0 condition.

**V_G = 0 represents the "flat band" or uncontaminated condition of the device.

***V_G = +44 V for Transistor B only.

†Data estimated from Reddi's Figure 8. Base surface is strongly inverted at V_G = +40 V.

††Data estimated from Reddi's Figure 10. Base surface has reached maximum depletion (minimum h_{FE} at V_G = +44 V; it is strongly inverted at V_G = +80 V.

†††Data estimated from Reddi's Figure 13. Base surface is mildly depleted at V_G = +40 V; it is near maximum depletion at V_G = +80 V.

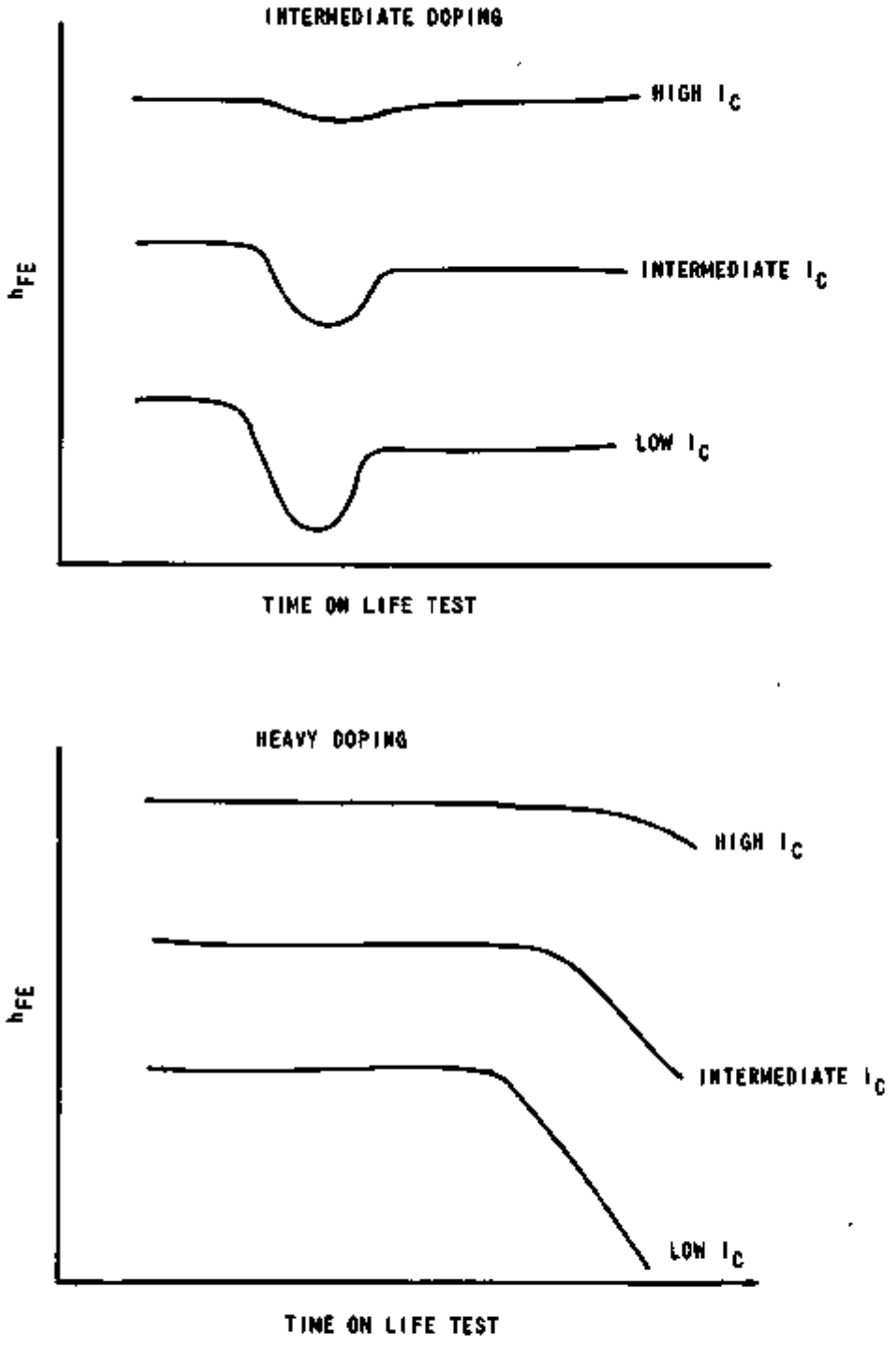

Figure C-2. Effect of Life Test on h_{FE} at Different Collector Currents, Assuming a Fixed Base-Surface Doping Concentration

that, because of previous processing, a charge buildup in the oxide may already have begun prior to the beginning of the life test; in particular cases, h_{FE} therefore might appear to actually increase during the life test. In any event, changes in h_{FE} (either an increase or a decrease) are a measure of the defectiveness of a transistor, and lower current (I_C) h_{FE} tests are a more sensitive measure of the defectiveness than are higher current tests.

The practical problem in a real situation is to determine how to use the knowledge that h_{FE} variation is a measure of transistor defectiveness. In these experiments, the first type of data analysis tried was the use of fixed h_{FE} limits as failure criteria. The limits were selected by tightly specifying both ends of the initial distribution of the h_{FE}. In addition, fixed limits were similarly applied to other tests (breakdown voltages, leakages, and saturation voltages). Table C-2 shows the 2N2222A transistors that failed and the tests that were failed after the total of 96 starting transistors had completed 360 hours of HTRB at a junction temperature of 200°C. All failures were detected by the combination of the I_{CEO} test (Test 17) and the I_C = 1 mA h_{FE} tests (Tests 18 and 23).

To test the validity of this type of analysis, a study was made of the devices which remained after the failures had been removed. Figure C-3 charts the mean h_{FE} (Test 23) and the standard deviation from the mean of the "good" transistors; no significant abnormalities are indicated in either the total group or any of its four subgroups. At this point, the temptation was to conclude that the failures had been removed and that only "good" devices remained. However, a check of some of the individual "good" units showed that h_{FE} had shifted drastically on some of them, even though no limit had been failed.

A computer program was therefore developed to analyze the parameter shifts as well as the absolute values of the readings. Figure C-4 is a sample output from the program. The h_{FE} reading of each device after 360 hours on HTRB (Code A99) is divided by its original reading (Code A01). Multiplying this answer by 100 gives the percentage of each device's original reading. A value of 100 percent indicates that the device did not change at all, a value of 50 percent indicates that the device has 50 percent of its original h_{FE}, ... The results of the calculations for all 96 transistors in the group are summarized by the histogram.

At this point, a new, arbitrary definition of an h_{FE} failure was made: a device which shifts more than 10 percent on h_{FE}. If the devices below 90 percent and above 110 percent are counted on Figure C-4, 52 h_{FE} failures will be found among the 96 transistors

Text continued on page 99.

Table C-2. Failure List of 2N2222A Transistors After 360 Hours HTRB at 200°C Junction Temperature

Subgroup. Devices Failed. Total Devices	Serial Number**	Test, Conditions, Limits								
		I_{CEO}*** V_{CE} = 40 V (0-10 nA)	h_{FE} V_{CE} = 1 V I_C = 1 mA (55-300)	h_{FE} V_{CE} = 5 V I_C = 1 mA (55-300)	I_{CBO} V_{CB} = 70 V (0-10 nA)	BV_{CBO} I_C = 10 µA (75-300 V)	BV_{CEO} I_C = 30 mA (37-300 V)	V_{BE}Sat I_B = 5 mA I_C = 50 mA (0.750-0.900 V)	V_{CE}Sat I_B = 50 mA I_C = 50 mA (0.032-0.080 V)	h_{FE} V_{CE} = 5 V I_C = 500 mA (40-140)
Dallas Preconditioned 12 of 36 Failed	386	*	*							
	388	*	*	*	*	*				
	393	*								
	396	*			*	*				
	397	*								
	400		*	*						
	401	*			*	*				
	407	*			*	*				
	409	*								
	413		*							
	414	*	*	*	*	*				
	416		*	*						
Dallas Unpreconditioned 6 of 36 Failed	856		*	*						
	859		*							
	860		*	*						
	870		*	*						
	874		*	*						
	875		*	*						
Singapore Unpreconditioned 3 of 12 Failed	3168		*	*						
	3176		*	*						
	3179		*	*						
Singapore Preconditioned 6 of 12 Failed	3565		*	*						
	3567	*								
	3568		*	*			*			
	3571		*	*						
	3574	*								
	3579	*	*							

*Indicates device failed test
**All units passed all initial tests.
***All I_{CEO} failures except 3574 occurred after preconditioning and prior to HTRB, 3574 failed I_{CEO} after one hour HTRB

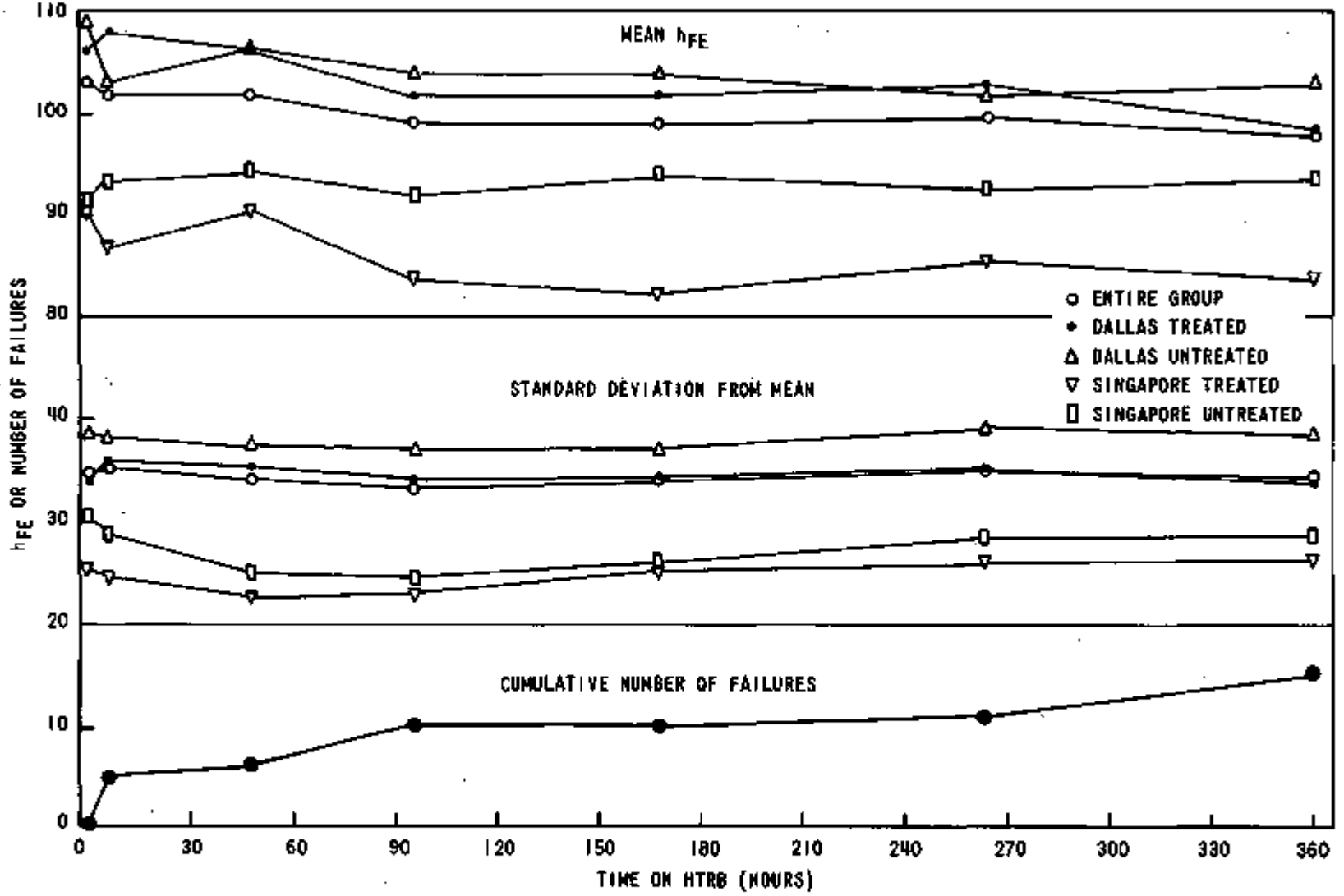

Figure C-3. Variation of the Mean h_{FE} (Test 23), Standard Deviation, and Cumulative Number of Failures With Time-On-HTRB for the 200°C-HTRB Stress-In-Time Group Which Passed Fixed Rejection Limits of 55-200

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                                ENGINEERING TEST GROUP HISTOGRAM

TEST NO. 23          ADJ DATA EXPRESSED AS A PERCENT OF ADJ DATA          200 DEG C HTRB  AFTER 360 HOURS
HFE AT VCE=5V, IC=1MA

BELOW 50 PERCENT =  0     ABOVE 150 PERCENT =  1

                  0         10        20        30        40        50        60        70        80        90       100 UNITS
                  |....|....|....|....|....|....|....|....|....|....|....|....|....|....|....|....|....|....|....|....|
 50.0-  52.0 PCT|*
 52.0-  54.0 PCT|
 54.0-  56.0 PCT|*
 56.0-  58.0 PCT|**
 58.0-  60.0 PCT|
 60.0-  62.0 PCT|*
 62.0-  64.0 PCT|*
 64.0-  66.0 PCT|*
 66.0-  68.0 PCT|***
 68.0-  70.0 PCT|**
 70.0-  72.0 PCT|**
 72.0-  74.0 PCT|*
 74.0-  76.0 PCT|*
 76.0-  78.0 PCT|*
 78.0-  80.0 PCT|*
 80.0-  82.0 PCT|**
 82.0-  84.0 PCT|**
 84.0-  86.0 PCT|**
 86.0-  88.0 PCT|********
 88.0-  90.0 PCT|***
 90.0-  92.0 PCT|*********
 92.0-  94.0 PCT|************
 94.0-  96.0 PCT|*******
 96.0-  98.0 PCT|********
 98.0- 100.0 PCT|********
100.0- 102.0 PCT|*
102.0- 104.0 PCT|*
104.0- 106.0 PCT|*
106.0- 108.0 PCT|
108.0- 110.0 PCT|*
110.0- 112.0 PCT|***
112.0- 114.0 PCT|*
114.0- 116.0 PCT|
116.0- 118.0 PCT|
118.0- 120.0 PCT|
120.0- 122.0 PCT|
122.0- 124.0 PCT|
124.0- 126.0 PCT|*
126.0- 128.0 PCT|*
128.0- 130.0 PCT|*
130.0- 132.0 PCT|
132.0- 134.0 PCT|
134.0- 136.0 PCT|*
136.0- 138.0 PCT|
138.0- 140.0 PCT|
140.0- 142.0 PCT|
142.0- 144.0 PCT|
144.0- 146.0 PCT|
146.0- 148.0 PCT|
148.0- 150.0 PCT|

QUANTITY OF UNITS =  96
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Figure C-4. Sample Computer Output: 200°C-HTRB After 360 Hours

after 360 hours, whereas only 15 will be discovered with the "limits" analysis previously described. If, in fact, the assumption is made that the 15 "limits" failures are the 15 lowest units on Figure C-4 (the worst case), units having as low as 66 percent of their original gain will be accepted. Clearly, the use of fixed h_{FE} limits alone is insufficient for providing a true indication of the quality of the devices.

Quantitative estimates of the allowable h_{FE} shifts at low currents can be determined from Reddi's* data, shown in Table C-1. Note the differences in h_{FE} variation for the different base-surface doping concentrations. For example, at a gate voltage (V_G) of 40-44 V, which corresponds to some particular level of contamination, the lightly doped base (Transistor A) is strongly inverted, but the h_{FE} is fairly close to its "uncontaminated" (V_G = 0) value. The medium-doped base (Transistor B) reached maximum depletion of the surface (minimum h_{FE}) at about the same contamination level, while the heavily doped base (Transistor D) is moderately depleted with severely degraded h_{FE}.

While no fixed percentage of allowable h_{FE} shift covers all of these cases, most of them can be covered by attempting to detect inversion on a medium-doped base such as Transistor B in Table C-1. *Thus, a ±10 percent shift of h_{FE} is allowed at I_C = 1 mA, a ±20 percent shift is allowed at I_C = 100 μA, or a ±25 percent shift is allowed at I_C = 10 μA.* These allowable shifts will detect depletion of the lightly doped bases and both depletion and inversion of the medium and heavily doped bases. Clearly, inversion of the lightly doped base would not be detected unless significant channeling occurred since the h_{FE} shift is small (Table C-1, Transistor A).

An I_{CBO}, I_{CES}, or I_{CEO} test and an I_{EBO} test should be used with the delta h_{FE} criterion as an added means of detecting channel formation. Channel formation occurs when a surface-inversion layer extends under the oxide so that two metal contacts are bridged, thus providing a current path around a junction. Emitter-base junction channeling is analogous to placing a resistor between the emitter and the base. If the surface is slightly inverted (a large value of resistance), a small current will bypass the junction, but h_{FE} may be relatively unaffected--especially on a lightly doped base. *An I_{EBO} test is required to detect this situation.* As the surface becomes more strongly inverted, the bypass current, which adds to I_B, becomes significantly large and causes h_{FE} degradation (since $h_{FE} = I_C/I_B$). The bypass current also makes the E-B forward characteristics

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*Reddi, pp 305-334.

"soft," possibly enough to affect I_{CEO}. Collector-base channeling is similar, except that the C-B bypass current adds to I_{CBO}, thus causing I_C to increase, I_B to decrease, and h_{FE} to increase. *An I_{CBO}, I_{CES}, or I_{CEO} test is required to detect changes in I_{CBO} which are too small to affect h_{FE}.*

The 2N2222A transistors used for these experiments exhibited many of the described characteristics of positive ionic contamination in the oxide. These characteristics were revealed by either HTRB or burn-in. Figure C-5 shows a generalized cross section of the 2N2222A transistor chip. The presence of positively charged ionic contamination in the oxide over the base region near the emitter and collector junctions could cause depletion or inversion of the base. If the contamination extended inward to the base metallization, current channels would be provided around the junctions.

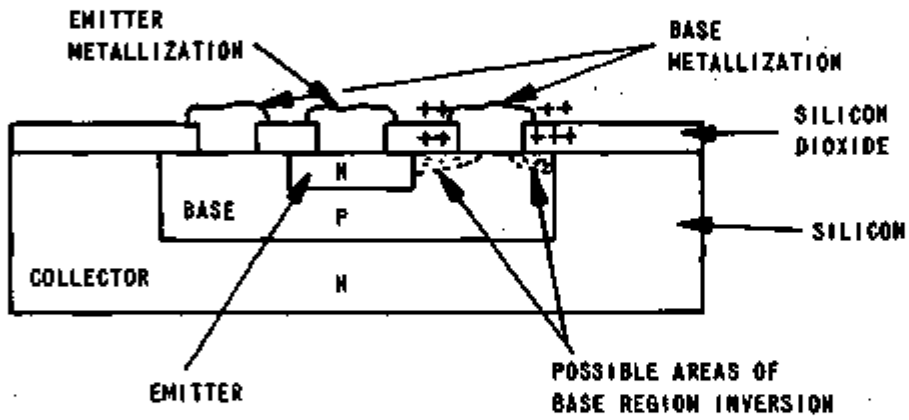

Figure C-5. Generalized Cross Section of 2N2222A Transistor Chip

Figures C-6 through C-8 show the effects of emitter-base channeling on Unit 14 from the 55-V step-stress HTRB group. (Parameters are plotted for this device in Figure 2.) Comparison is made to a "fresh" device, Unit 3410. Note the severely degraded h_{FE} at low current on Unit 14, the high reverse leakage (emitter-base), and the soft emitter-base forward characteristics. In contrast, the collector-base characteristics appear normal (leakage less than 1 nA, breakdown voltage greater than 75 V).

Unit 14 is typical of one kind of failure encountered in the 2N2222A experiments. Many times, this type of failure could be detected only by an h_{FE} delta-shift criterion since an I_{EBO} test

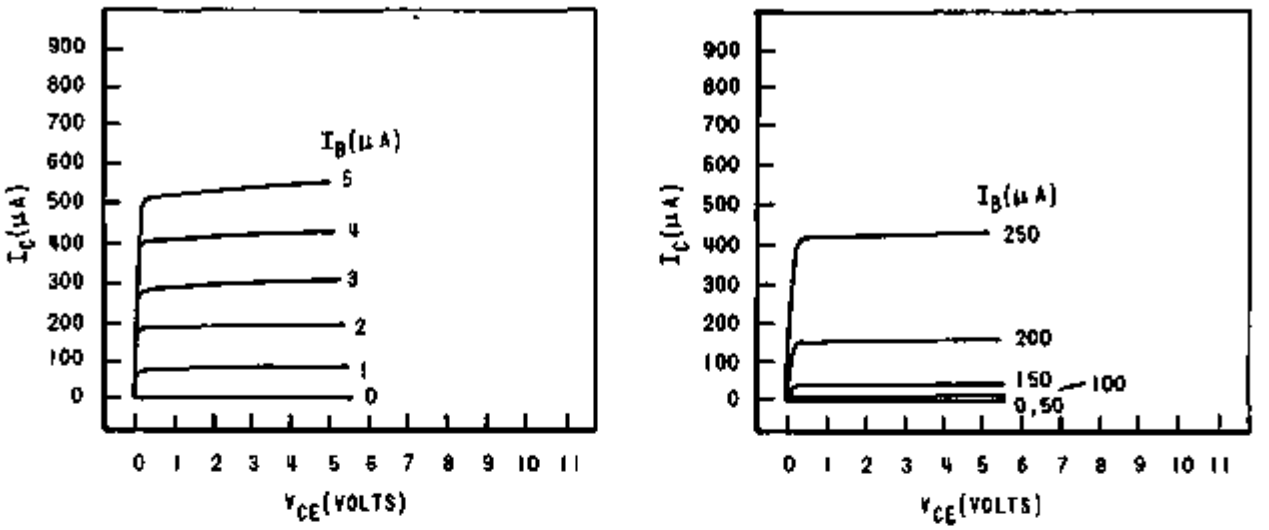

Figure C-6. Low-Current h_{FE} Characteristics of Unit 3410 (Left) and Unit 14 (Right) (Even spacing of Unit 3410 steps indicates uniformity of gain with collector current; Unit 14 gain decreases rapidly with collector current.)

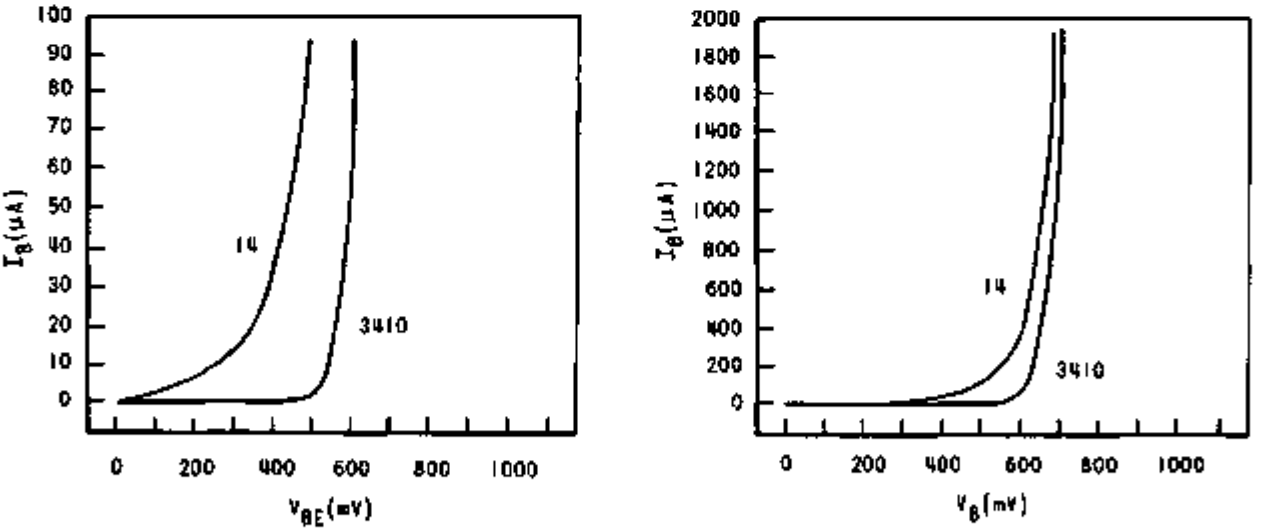

Figure C-7. Emitter-Base Forward Characteristics for Units 14 and 3410 (Forward voltages are significantly higher at I_B = 10 μA than those at higher currents.)

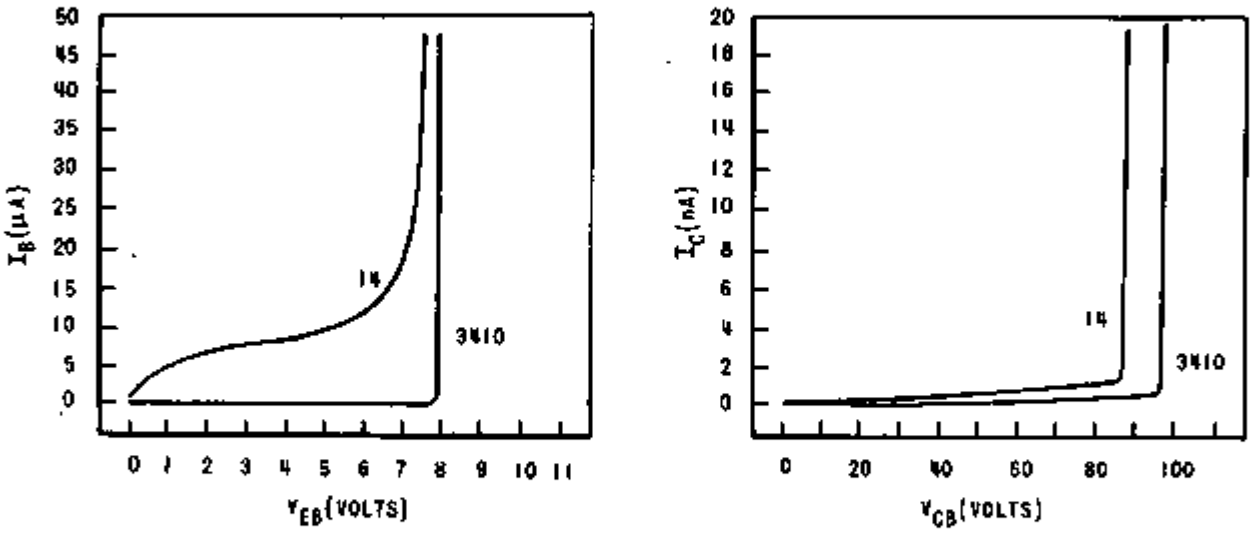

Figure C-8. Emitter-Base Reverse Characteristics (Left) and Collector-Base Reverse Characteristics (Right) for Units 14 and 3410 (Note high emitter-base leakage on Unit 14.)

was not performed, and since the h_{FE} degradation often was not severe enough to cause a failure of the minimum h_{FE} limit.

In brief, a delta-shift criterion for low-current h_{FE} (±10 percent at I_C = 1 mA, ±20 percent at I_C = 100 μA, or ±25 percent at I_C = 10 μA) will detect depletion and inversion of the base or emitter surface due to ionic contamination in the oxide after preconditioning tests (HTRB or power burn-in). The addition of an I_{EBO} test and either an I_{CBO}, I_{CES}, or I_{CEO} test will insure the detection of channel formation on light- to medium-doped bases as well as along the collector surface.

Appendix D

POWER BURN-IN METHODS AND DETERMINATION OF JUNCTION TEMPERATURE FOR 2N2222A TRANSISTOR

All power burn-in tests for the 2N2222A, the SA1825, and the beam lead transistors were performed in a common-base circuit in which the transistor was operating in its active region with the collector-base junction reverse-biased and the emitter-base junction forward-biased. Figure D-1 shows the basic circuit used for all types of devices. The values shown are the conditions which will produce a power dissipation of 500 mW in the 2N2222A transistor.

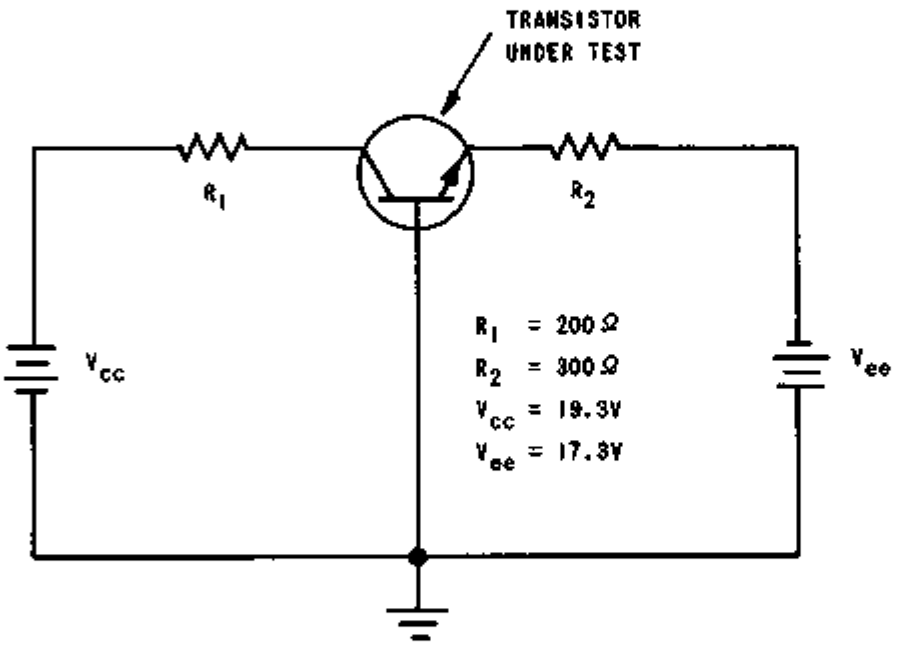

Figure D-1. Circuit Configuration for Power Burn-In Experiments (Given values are for stress-in-time experiments.)

One goal of the power burn-in experiments was to determine the optimum junction temperature (T_j). T_j, which is the sum of the ambient temperature and the temperature rise produced by the electrical power dissipated inside the transistor, therefore had to be accurately measured. The ambient temperature can be easily and accurately measured; however, the temperature produced by the dissipated electrical power must be measured indirectly by

using a temperature-sensitive parameter having a known temperature-dependence. Following Grutchfield*, the forward voltage drop of the base-emitter junction was used as the temperature-sensitive parameter.

As a first step, thermocouples were welded to the case of several transistors so that the case temperature could be accurately measured. The transistors then were mounted on a burn-in board and placed in an oven. A Tektronix Model 576 curve tracer was connected to the board and was used to apply the same electrical conditions that were used for the step-stress and stress-in-time burn-in, except that pulsed rather than sustained dc voltage was applied. The pulses were of 300-μs duration with a duty cycle of less than 2 percent. When the voltage was pulsed in this manner, there was no rise in the junction temperature as a result of the electrical conditions; thus, the case temperature and the junction temperature were identical. The case temperature and the base-emitter forward voltage were measured at several oven-ambient temperatures from room temperature to 300°C.

Figure D-2 shows the variation of V_{BE} with the junction (case) temperature for two of the sample transistors at three different power levels. V_{BE} was very consistent among different transistors up to a temperature of about 250°C. At higher temperatures, V_{BE} varied considerably from one device to another. The junction temperatures below 250°C used in the HTRB, power burn-in, and sequence experiments were estimated to be within ±5°C of the actual junction temperatures of the individual devices.

A particular junction temperature can now be obtained for a group of transistors by placing them on a burn-in board in an oven, applying the desired power level, then adjusting the oven-ambient temperature until the V_{BE} which corresponds to the desired junction temperature (from Figure D-2) is obtained. For example, a 2N2222A transistor dissipating 500 mW of dc power in the oven environment required an ambient temperature of 109°C to obtain a junction temperature of 200°C (V_{BE} = 400 mV); three other 2N2222A transistors dissipating 500 mW of power in still air at 25°C during the sequence experiments had junction temperatures ranging from 197 to 200°C (V_{BE} = 407 mV to 400 mV). The difference between these two examples can be attributed to the oven fan which, in the latter case, circulated the air to provide a cooling action which was not present when the air was still. Junction temperatures of transistors under power can be changed significantly by

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*H. B. Grutchfield, "Measurement of the Thermal Resistance and Thermal Response of Diffused Silicon Transistors," *Fairchild Semiconductor Application Bulletin*, Number APP-53, January, 1963.

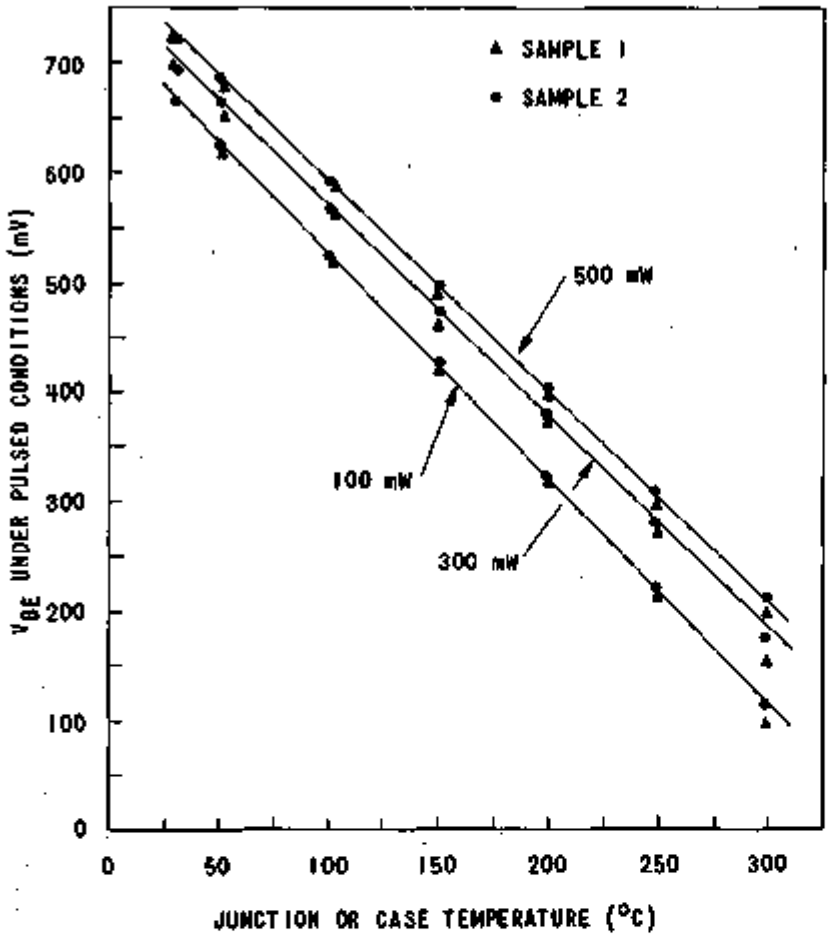

Figure D-2. Variation of V_{BE} With Junction Temperature for the 2N2222A Transistor

even a small amount of circulating air. In any event, monitoring V_{BE} and converting to the junction temperature by using Figure D-2 provides an accurate way of determining T_j, regardless of external conditions.

One note of caution must be introduced: the use of this method assumes that when a curve similar to that of Figure D-2 is generated, the case temperature and the junction temperature are the same. Some transistors, however, have been observed to have a rise in junction temperature within even a 300-μs pulse at high power levels. This condition will make the actual junction temperature higher than the case temperature and will produce inaccuracy in the curve. An oscilloscope can be used to monitor V_{BE} during the pulse to determine whether such a problem exists with a particular transistor.

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Appendix E

TEST CODES AND ELECTRICAL TESTS FOR SA1825 AND BEAM LEAD TRANSISTORS

Data cards for all tests were punched by the Fairchild 600D tester and were reformatted exactly as described in Appendix B for the 2N2222A transistor. The electrical test sequences performed on the different types of devices at each flow-chart position are listed in Tables E-1 through E-8.

As with the 2N2222A transistor, a unique three-digit test code was punched on each data card to identify the flow-chart position which the card represents. The codes for all SA1825 and beam lead transistor tests are tabulated in Tables E-9 and E-10.

Table E-1. Tests, Conditions, and Limits Used for GT2219 Beam Lead NPN Transistor

Test Number	Test Type	Conditions	Limits	
			Minimum	Maximum
1	I_{EBO}	V_{EB} = 4 V	0	1.0 nA
2	I_{CBO}	V_{CB} = 30 V	0	10 nA
3	I_{CES}	V_{CE} = 30 V	0	10 nA
4	I_{CER}	V_{CE} = 30 V R = 1000 Ω	0	10 nA
5	I_{CER}	V_{CE} = 30 V R = 10000 Ω	0	10 nA
6	I_{CEO}	V_{CE} = 30 V	0	100 nA
7	$V_{VE}Sat$	I_B/I_C = 0.1/1 mA	0.640 V	0.680 V
8	$V_{CE}Sat$	I_B/I_C = 0.1/1 mA	0.010 V	0.020 V
9	$V_{CE}Sat$	I_B/I_C = 0.3/3 mA	0.011 V	0.021 V
10	$V_{BE}Sat$	I_B/I_C = 1/10 mA	0.720 V	0.760 V
11	$V_{CE}Sat$	I_B/I_C = 1/10 mA	0.015 V	0.030 V
12	$V_{CE}Sat$	I_B/I_C = 3/30 mA	0.025 V	0.050 V
13	$V_{BE}Sat$	I_B/I_C = 10/100 mA	0.810 V	0.850 V
14	$V_{CE}Sat$	I_B/I_C = 10/100 mA	0.070 V	0.100 V
15	$V_{CE}Sat$	I_B/I_C = 20/200 mA	0.130 V	0.170 V
16	$V_{BE}Sat$	I_B/I_C = 50/500 mA	0.920 V	0.970 V
17	$V_{CE}Sat$	I_B/I_C = 50/500 mA	0.300 V	0.400 V
18	$V_{BE}Sat$	I_B/I_C = 80/800 mA	0.900 V	1.10 V
19	$V_{CE}Sat$	I_B/I_C = 80/800 mA	0.500 V	0.600 V
20	BV_{CEO}	I_C = 30 mA	35.0 V	100 V

Table E-1 Continued. Tests, Conditions, and Limits Used for GT2219 Beam Lead NPN Transistor

Test Number	Test Type	Conditions	Limits	
			Minimum	Maximum
21	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 10 µA	0.490 V	0.550 V
22	h_{FE}	V_{CE} = 5 V, I_C = 10 µA	60.0	120
23	h_{FE}	V_{CE} = 5 V, I_C = 30 µA	70.0	135
24	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 100 µA	0.540 V	0.600
25	h_{FE}	V_{CE} = 5 V, I_C = 100 µA	100	160
26	h_{FE}	V_{CE} = 5 V, I_C = 300 µA	110	170
27	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 1 mA	0.600 V	0.660 V
28	h_{FE}	V_{CE} = 5 V, I_C = 1 mA	120	180
29	h_{FE}	V_{CE} = 5 V, I_C = 3 mA	130	190
30	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 10 mA	0.600 V	0.700 V
31	h_{FE}	V_{CE} = 5 V, I_C = 10 mA	130	190
32	h_{FE}	V_{CE} = 5 V, I_C = 30 mA	160	220
33	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 100 mA	0.770 V	0.830 V
34	h_{FE}	V_{CE} = 5 V, I_C = 100 mA	140	200
35	h_{FE}	V_{CE} = 5 V, I_C = 200 mA	130	190
36	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 500 mA	0.770 V	0.830 V
37	h_{FE}	V_{CE} = 5 V, I_C = 500 mA	50.0	130
38	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 800 mA	0.790 V	0.850 V
39	h_{FE}	V_{CE} = 5 V, I_C = 800 mA	30.0	90.0
40	BV_{CBO}	I_C = 100 µA	80.0 V	200 V

Table E-2. Tests, Conditions, and Limits Used for GT2905 Beam Lead PNP Transistor

Test Number	Test Type	Conditions	Limits	
			Minimum	Maximum
1	I_{EBO}	V_{EB} = 4 V	0	1.0 nA
2	I_{CBO}	V_{CB} = 30 V	0	10 nA
3	I_{CES}	V_{CE} = 30 V	0	10 nA
4	I_{CER}	V_{CE} = 30 V R = 1000 Ω	0	10 nA
5	I_{CER}	V_{CE} = 30 V R = 10000 Ω	0	10 A
6	I_{CEO}	V_{CE} = 30 V	0	100 nA
7	V_{BE}Sat	I_B/I_C = 0.1/1 mA	0.640 V	0.680 V
8	V_{CE}Sat	I_B/I_C = 0.1/1 mA	0.010 V	0.020 V
9	V_{CE}Sat	I_B/I_C = 0.3/3 mA	0.011 V	0.030 V
10	V_{BE}Sat	I_B/I_C = 1/10 mA	0.720 V	0.760 V
11	V_{CE}Sat	I_B/I_C = 1/10 mA	0.020 V	0.040 V
12	V_{CE}Sat	I_B/I_C = 3/30 mA	0.030 V	0.060 V
13	V_{BE}Sat	I_B/I_C = 10/100 mA	0.830 V	0.870 V
14	V_{CE}Sat	I_B/I_C = 10/100 mA	0.090 V	0.150 V
15	V_{CE}Sat	I_B/I_C = 20/200 mA	0.150 V	0.240 V
16	V_{BE}Sat	I_B/I_C = 50/500 mA	0.950 V	1.05 V
17	V_{CE}Sat	I_B/I_C = 50/500 mA	0.390 V	0.570 V
18	V_{BE}Sat	I_B/I_C = 80/800 mA	1.00 V	1.20 V
19	V_{CE}Sat	I_B/I_C = 80/800 mA	0.600 V	1.20 V
20	BV_{CEO}	I_C = 30 mA	35.0 V	100 V

Table E-2 Continued. Tests, Conditions, and Limits Used for GT2905 Beam Lead PNP Transistor

Test Number	Test Type	Conditions	Limits	
			Minimum	Maximum
21	$V_{BE}ON$	V_{CE} = 5 V, I_C = 10 µA	0.490 V	0.550 V
22	h_{FE}	V_{CE} = 5 V, I_C = 10 µA	120	250
23	h_{FE}	V_{CE} = 5 V, I_C = 30 µA	120	260
24	$V_{BE}ON$	V_{CE} = 5 V, I_C = 100 µA	0.540 V	0.600 V
25	h_{FE}	V_{CE} = 5 V, I_C = 100 µA	140	270
26	h_{FE}	V_{CE} = 5 V, I_C = 300 µA	100	260
27	$V_{BE}ON$	V_{CE} = 5 V, I_C = 1 mA	0.600 V	0.660 V
28	h_{FE}	V_{CE} = 5 V, I_C = 1 mA	100	260
29	h_{FE}	V_{CE} = 5 V, I_C = 3 mA	100	260
30	$V_{BE}ON$	V_{CE} = 5 V, I_C = 10 mA	0.600 V	0.710 V
31	h_{FE}	V_{CE} = 5 V, I_C = 10 mA	100	260
32	h_{FE}	V_{CE} = 5 V, I_C = 30 mA	140	300
33	$V_{BE}ON$	V_{CE} = 5 V, I_C = 100 mA	0.400 V	0.800 V
34	h_{FE}	V_{CE} = 5 V, I_C = 100 mA	130	250
35	h_{FE}	V_{CE} = 5 V, I_C = 200 mA	100	200
36	$V_{BE}ON$	V_{CE} = 5 V, I_C = 500 mA	0.770 V	0.830 V
37	h_{FE}	V_{CE} = 5 V, I_C = 500 mA	50.0	130
38	$V_{BE}ON$	V_{CE} = 5 V, I_C = 800 mA	0.830 V	0.930 V
39	h_{FE}	V_{CE} = 5 V, I_C = 800 mA	20.0	70.0
40	BV_{CBO}	I_C = 100 µA	60.0 V	200 V

Table E-3. Tests, Conditions, and Limits Used for GT3965 Beam Lead PNP Transistor

Test Number	Test Type	Conditions	Limits	
			Minimum	Maximum
1	I_{EBO}	V_{EB} = 4 V	0	1.0 nA
2	I_{CBO}	V_{CB} = 40 V	0	10 nA
3	I_{CES}	V_{CE} = 40 V	0	10 nA
4	I_{CER}	V_{CE} = 40 V R = 1000 Ω	0	10 nA
5	I_{CER}	V_{CE} = 40 V R = 10000 Ω	0	10 nA
6	I_{CEO}	V_{CE} = 40 V	0	150 nA
7	$V_{BE}Sat$	I_B/I_C = 5/50 μA	0.570 V	0.600 V
8	$V_{CE}Sat$	I_B/I_C = 5/50 μA	0.025 V	0.075 V
9	$V_{CE}Sat$	I_B/I_C = 0.1/1 mA	0.030 V	0.100 V
10	$V_{BE}Sat$	I_B/I_C = 0.1/1 mA	0.660 V	0.695 V
11	$V_{CE}Sat$	I_B/I_C = 0.3/3 mA	0.040 V	0.110 V
12	$V_{CE}Sat$	I_B/I_C = 1/10 mA	0.070 V	0.130 V
13	$V_{BE}Sat$	I_B/I_C = 1/10 mA	0.760 V	0.810 V
14	$V_{CE}Sat$	I_B/I_C = 3/30 mA	0.155 V	0.230 V
15	$V_{CE}Sat$	I_B/I_C = 10/100 mA	0.765 V	0.910 V
16	$V_{BE}Sat$	I_B/I_C = 10/100 mA	0.920 V	0.960 V
17	$V_{CE}Sat$	I_B/I_C = 20/200 mA	0.170 V	0.360 V
18	$V_{BE}Sat$	I_B/I_C = 20/200 mA	1.00 V	1.07 V
19	BV_{CEO}	I_C = 10 mA	55.0 V	150 V
20	$V_{BE}ON$	V_{CE} = 5 V, I_C = 10 μA	0.500 V	0.570 V

Table E-3 Continued. Tests, Conditions, and Limits Used for GT3965 Beam Lead PNP Transistor

Test Number	Test Type	Conditions	Limits	
			Minimum	Maximum
21	h_{FE}	V_{CE} = 5 V, I_C = 10 µA	210	500
22	h_{FE}	V_{CE} = 5 V, I_C = 30 µA	230	510
23	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 100 µA	0.570 V	0.625 V
24	h_{FE}	V_{CE} = 5 V, I_C = 100 µA	250	510
25	h_{FE}	V_{CE} = 5 V, I_C = 300 µA	250	510
26	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 1 mA	0.630 V	0.680 V
27	h_{FE}	V_{CE} = 5 V, I_C = 1 mA	250	510
28	h_{FE}	V_{CE} = 5 V, I_C = 3 mA	250	510
29	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 3 mA	0.660 V	0.710 V
30	h_{FE}	V_{CE} = 5 V, I_C = 5 mA	230	470
31	h_{FE}	V_{CE} = 5 V, I_C = 10 mA	230	470
32	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 10 mA	0.690 V	0.740 V
33	h_{FE}	V_{CE} = 5 V, I_C = 30 mA	200	440
34	h_{FE}	V_{CE} = 5 V, I_C = 50 mA	160	400
35	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 50 mA	0.710 V	0.760 V
36	h_{FE}	V_{CE} = 5 V, I_C = 100 mA	40.0	100
37	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 100 mA	0.750 V	0.800 V
38	h_{FE}	V_{CE} = 5 V, I_C = 200 mA	10.0	25.0
39	BV_{CBO}	I_C = 10 µA	65.0	150

Table E-4. Tests, Conditions, and Limits Used for GT2484 Beam Lead NPN Transistor

Test Number	Test Type	Conditions	Limits	
			Minimum	Maximum
1	I_{EBO}	V_{EB} = 4 V	0	1.0 nA
2	I_{CBO}	V_{CB} = 30 V	0	10 nA
3	I_{CES}	V_{CE} = 30 V	0	10 nA
4	I_{CER}	V_{CE} = 30 V R = 1000 Ω	0	10 nA
5	I_{CER}	V_{CE} = 30 V R = 10000 Ω	0	10 nA
6	I_{CEO}	V_{CE} = 30 V	0	100 nA
7	$V_{BE}Sat$	I_B/I_C = 5/50 μA	0.550 V	0.620 V
8	$V_{CE}Sat$	I_B/I_C = 5/50 μA	0.020 V	0.050 V
9	$V_{CE}Sat$	I_B/I_C = 0.1/1 mA	0.020 V	0.065 V
10	$V_{BE}Sat$	I_B/I_C = 0.1/1 mA	0.660 V	0.695 V
11	$V_{CE}Sat$	I_B/I_C = 0.3/3 mA	0.030 V	0.080 V
12	$V_{CE}Sat$	I_B/I_C = 0.5/5 mA	0.040 V	0.095 V
13	$V_{BE}Sat$	I_B/I_C = 0.5/5 mA	0.700 V	0.770 V
14	$V_{BE}Sat$	I_B/I_C = 1/10 mA	0.740 V	0.800 V
15	$V_{CE}Sat$	I_B/I_C = 1/10 mA	0.060 V	0.120 V
16	$V_{BE}Sat$	I_B/I_C = 3/30 mA	0.800 V	0.850 V
17	$V_{CE}Sat$	I_B/I_C = 3/30 mA	0.110 V	0.170 V
18	$V_{BE}Sat$	I_B/I_C = 5/50 mA	0.840 V	0.900 V
19	$V_{CE}Sat$	I_B/I_C = 5/50 mA	0.200 V	0.270 V
20	BV_{CEO}	I_C = 10 mA	45.0 V	100 V

Table E-4 Continued. Tests, Conditions, and Limits Used for GT2484 Beam Lead NPN Transistor

Test Number	Test Type	Conditions	Limits	
			Minimum	Maximum
21	$V_{BE}ON$	V_{CE} = 5 V, I_C = 10 μA	0.500 V	0.560 V
22	h_{FE}	V_{CE} = 5 V, I_C = 10 μA	150	500
23	h_{FE}	V_{CE} = 5 V, I_C = 30 μA	175	500
24	$V_{BE}ON$,	V_{CE} = 5 V, I_C = 30 μA	0.530 V	0.590 V
25	h_{FE}	V_{CE} = 5 V, I_C = 50 μA	200	500
26	h_{FE}	V_{CE} = 5 V, I_C = 100 μA	200	500
27	$V_{BE}ON$	V_{CE} = 5 V, I_C = 100 μA	0.560 V	0.620 V
28	h_{FE}	V_{CE} = 5 V, I_C = 300 μA	225	500
29	h_{FE}	V_{CE} = 5 V, I_C = 500 μA	225	500
30	$V_{BE}ON$	V_{CE} = 5 V, I_C = 500 μA	0.600 V	0.660 V
31	h_{FE}	V_{CE} = 5 V, I_C = 1 mA	225	500
32	$V_{BE}ON$	V_{CE} = 5 V, I_C = 1 mA	0.620 V	0.680 V
33	$V_{BE}ON$	V_{CE} = 5 V, I_C = 3 mA	0.640 V	0.700 V
34	h_{FE}	V_{CE} = 5 V, I_C = 3 mA	250	500
35	h_{FE}	V_{CE} = 5 V, I_C = 40 mA	225	500
36	$V_{BE}ON$	V_{CE} = 5 V, I_C = 40 mA	0.680 V	0.740 V
37	$V_{BE}ON$	V_{CE} = 5 V, I_C = 50 mA	0.680 V	0.740 V
38	h_{FE}	V_{CE} = 5 V, I_C = 50 mA	225	500
39	BV_{CBO}	I_C = 100 μA	95.0 V	150 V

Table E-5. Tests, Conditions, and Limits Used for HT918 Beam Lead NPN Transistor

Test Number	Test Type	Conditions	Limits	
			Minimum	Maximum
1	I_{EBO}	V_{EB} = 2 V	0	1.0 nA
2	I_{CBO}	V_{CB} = 15 V	0	10 nA
3	I_{CES}	V_{CE} = 12 V	0	10 nA
4	I_{CER}	V_{CE} = 12 V R = 1000 Ω	0	10 nA
5	I_{CER}	V_{CE} = 12 V R = 10000 Ω	0	10 nA
6	I_{CEO}	V_{CE} = 12 V	0	10 nA
7	$V_{BE}Sat$	I_B/I_C = 5/50 μA	0.640 V	0.700 V
8	$V_{CE}Sat$	I_B/I_C = 5/50 μA	0.050 V	0.100 V
9	$V_{CE}Sat$	I_B/I_C = 10/100 μA	0.050 V	0.100 V
10	$V_{BE}Sat$	I_B/I_C = 10/100 μA	0.660 V	0.720 V
11	$V_{CE}Sat$	I_B/I_C = 30/300 μA	0.050 V	0.100 V
12	$V_{CE}Sat$	I_B/I_C = 0.1/1 mA	0.050 V	0.100 V
13	$V_{BE}Sat$	I_B/I_C = 0.1/1 mA	0.730 V	0.790 V
14	$V_{CE}Sat$	I_B/I_C = 0.3/3 mA	0.050 V	0.100 V
15	$V_{CE}Sat$	I_B/I_C = 0.5/5 mA	0.050 V	0.100 V
16	$V_{BE}Sat$	I_B/I_C = 1/10 mA	0.820 V	0.880 V
17	$V_{CE}Sat$	I_B/I_C = 1/10 mA	0.060 V	0.110 V
18	$V_{BE}Sat$	I_B/I_C = 5/50 mA	0.940 V	0.980 V
19	$V_{CE}Sat$	I_B/I_C = 5/50 mA	0.150 V	0.250 V
20	BV_{CEO}	I_C = 30 mA	20.0 V	50.0 V

Table E-5 Continued. Tests, Conditions, and Limits Used for HT918 Beam Lead NPN Transistor

Test Number	Test Type	Conditions	Limits	
			Minimum	Maximum
21	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 10 µA	0.600 V	0.660 V
22	h_{FE}	V_{CE} = 5 V, I_C = 10 µA	20.0	60.0
23	h_{FE}	V_{CE} = 5 V, I_C = 30 µA	20.0	60.0
24	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 30 µA	0.630 V	0.690 V
25	h_{FE}	V_{CE} = 5 V, I_C = 50 µA	25.0	60.0
26	h_{FE}	V_{CE} = 5 V, I_C = 100 µA	25.0	60.0
27	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 100 µA	0.660 V	0.720 V
28	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 300 µA	0.690 V	0.750 V
29	h_{FE}	V_{CE} = 5 V, I_C = 300 µA	25.0	60.0
30	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 1 mA	0.720 V	0.780 V
31	h_{FE}	V_{CE} = 5 V, I_C = 1 mA	30.0	65.0
32	h_{FE}	V_{CE} = 5 V, I_C = 3 mA	30.0	65.0
33	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 3 mA	0.750 V	0.810 V
34	h_{FE}	V_{CE} = 5 V, I_C = 5 mA	30.0	65.0
35	h_{FE}	V_{CE} = 5 V, I_C = 10 mA	35.0	75.0
36	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 10 mA	0.780 V	0.840 V
37	h_{FE}	V_{CE} = 5 V, I_C = 30 mA	30.0	70.0
38	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 50 mA	0.830 V	0.890 V
39	h_{FE}	V_{CE} = 5 V, I_C = 50 mA	20.0	50.0
40	BV_{CBO}	I_C = 10 µA	50.0 V	100 V

Table E-6. Tests, Conditions, and Limits Used for GT2369 Beam Lead NPN Transistor

Test Number	Test Type	Conditions	Limits	
			Minimum	Maximum
1	I_{EBO}	V_{EB} = 4 V	0	10 nA
2	I_{CBO}	V_{CB} = 15 V	0	10 nA
3	I_{CES}	V_{CE} = 15 V	0	10 nA
4	I_{CER}	V_{CE} = 15 V R = 1000 Ω	0	10 nA
5	I_{CER}	V_{CE} = 15 V R = 10000 Ω	0	10 nA
6	I_{CEO}	V_{CE} = 15 V	0	20 nA
7	V_{BE}Sat	I_B/I_C = 5/50 μA	0.580 V	0.650 V
8	V_{CE}Sat	I_B/I_C = 5/50 μA	0.220 V	0.310 V
9	V_{CE}Sat	I_B/I_C = 0.1/1 mA	0.155 V	0.210 V
10	V_{BE}Sat	I_B/I_C = 0.1/1 mA	0.675 V	0.720 V
11	V_{CE}Sat	I_B/I_C = 0.3/3 mA	0.145 V	0.200 V
12	V_{CE}Sat	I_B/I_C = 1/10 mA	0.140 V	0.190 V
13	V_{BE}Sat	I_B/I_C = 1/10 mA	0.760 V	0.810 V
14	V_{CE}Sat	I_B/I_C = 3/30 mA	0.160 V	0.210 V
15	V_{CE}Sat	I_B/I_C = 10/100 mA	0.280 V	0.345 V
16	V_{BE}Sat	I_B/I_C = 10/100 mA	0.940 V	0.985 V
17	V_{CE}Sat	I_B/I_C = 20/200 mA	0.500 V	1.00 V
18	V_{BE}Sat	I_B/I_C = 20/200 mA	1.05 V	1.20 V
19	V_{CE}Sat	I_B/I_C = 50/500 mA	0	9.99 V
20	BV_{CEO}	I_C = 10 mA	15.0 V	100 V

Table E-6 Continued. Tests, Conditions, and Limits Used for GT2369 Beam Lead NPN Transistor

Test Number	Test Type	Conditions	Limits	
			Minimum	Maximum
21	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 10 μA	0.530 V	0.590 V
22	h_{FE}	V_{CE} = 5 V, I_C = 10 μA	10.0	40.0
23	h_{FE}	V_{CE} = 5 V, I_C = 30 μA	12.0	50.0
24	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 30 μA	0.560 V	0.615 V
25	h_{FE}	V_{CE} = 5 V, I_C = 50 μA	14.0	55.0
26	h_{FE}	V_{CE} = 5 V, I_C = 100 μA	16.0	60.0
27	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 100 μA	0.590 V	0.650 V
28	h_{FE}	V_{CE} = 5 V, I_C = 300 μA	20.0	70.0
29	h_{FE}	V_{CE} = 5 V, I_C = 500 μA	22.0	80.0
30	h_{FE}	V_{CE} = 5 V, I_C = 1 mA	25.0	90.0
31	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 1 mA	0.645 V	0.710 V
32	h_{FE}	V_{CE} = 5 V, I_C = 3 mA	35.0	100
33	h_{FE}	V_{CE} = 5 V, I_C = 10 mA	45.0	115
34	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 10 mA	0	1.00 V
35	h_{FE}	V_{CE} = 5 V, I_C = 30 mA	50.0	130
36	h_{FE}	V_{CE} = 5 V, I_C = 100 mA	45.0	115
37	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 100 mA	0.710 V	0.780 V
38	h_{FE}	V_{CE} = 5 V, I_C = 200 mA	15.0	35.0
39	V_{BE}^{ON}	V_{CE} = 5 V, I_C = 200 mA	0.875 V	0.950 V
40	BV_{CBO}	I_C = 10 μA	50.0 V	100 V

Table E-7. Tests, Conditions, and Limits Used for GT3829 Beam Lead PNP Transistor

Test Number	Test Type	Conditions	Limits	
			Minimum	Maximum
1	I_{EBO}	V_{EB} = 4 V	0	1.00 nA
2	I_{CBO}	V_{CB} = 18 V	0	10.0 nA
3	I_{CES}	V_{CE} = 18 V	0	10.0 nA
4	I_{CER}	V_{CE} = 18 V R = 1000 Ω	0	10.0 nA
5	I_{CER}	V_{CE} = 18 V R = 10000 Ω	0	10.0 nA
6	I_{CEO}	V_{CE} = 18 V	0	10.0 nA
7	V_{BE}Sat	I_B/I_C = 5/50 µA	0.620 V	0.700 V
8	V_{CE}Sat	I_B/I_C = 5/50 µA	0.110 V	0.190 V
9	V_{CE}Sat	I_B/I_C = 0.1/1 mA	0.110 V	0.190 V
10	V_{BE}Sat	I_B/I_C = 0.1/1 mA	0.700 V	0.780 V
11	V_{CE}Sat	I_B/I_C = 0.3/3 mA	0.110 V	0.190 V
12	V_{CE}Sat	I_B/I_C = 1/10 mA	0.110 V	0.190 V
13	V_{BE}Sat	I_B/I_C = 1/10 mA	0.780 V	0.860 V
14	V_{CE}Sat	I_B/I_C = 3/30 mA	0.130 V	0.210 V
15	V_{CE}Sat	I_B/I_C = 10/100 mA	0.250 V	0.600 V
16	V_{BE}Sat	I_B/I_C = 10/100 mA	0.930 V	1.01 V
17	V_{CE}Sat	I_B/I_C = 20/200 mA	0.500 V	1.40 V
18	V_{BE}Sat	I_B/I_C = 20/200 mA	0.900 V	1.30 V
19	V_{CE}Sat	I_B/I_C = 50/50 mA	0.00 V	9.99 V
20	BV_{CEO}	I_C = 100 µA	20.0 V	100 V

Table E-7 Continued. Tests, Conditions, and Limits Used for GT3829 Beam Lead PNP Transistor

Test Number	Test Type	Conditions	Limits	
			Minimum	Maxinum
21	$V_{BE}ON$	V_{CE} = 5 V, I_C = 10 µA	0.580 V	0.660 V
22	h_{FE}	V_{CE} = 5 V, I_C = 10 µA	8.0	40.0
23	h_{FE}	V_{CE} = 5 V, I_C = 30 µA	10.0	40.0
24	$V_{BE}ON$	V_{CE} = 5 V, I_C = 30 µA	0.600 V	0.680 V
25	h_{FE}	V_{CE} = 5 V, I_C = 60 µA	10.0	40.0
26	h_{FE}	V_{CE} = 5 V, I_C = 100 µA	10.0	40.0
27	$V_{BE}ON$	V_{CE} = 5 V, I_C = 100 µA	0.640 V	0.720 V
28	h_{FE}	V_{CE} = 5 V, I_C = 300 µA	15.0	40.0
29	$V_{BE}ON$	V_{CE} = 5 V, I_C = 300 µA	0.660 V	0.740 V
30	h_{FE}	V_{CE} = 5 V, I_C = 600 µA	15.0	40.0
31	$V_{BE}ON$	V_{CE} = 5 V, I_C = 1 mA	0.700 V	0.780 V
32	h_{FE}	V_{CE} = 5 V, I_C = 1 mA	15.0	40.0
33	$V_{BE}ON$	V_{CE} = 5 V, I_C = 3 mA	0.720 V	0.800 V
34	h_{FE}	V_{CE} = 5 V, I_C = 3 mA	20.0	45.0
35	h_{FE}	V_{CE} = 5 V, I_C = 10 mA	20.0	45.0
36	$V_{BE}ON$	V_{CE} = 5 V, I_C = 10 mA	0.760 V	0.840 V
37	h_{FE}	V_{CE} = 5 V, I_C = 100 mA	15.0	40.0
38	$V_{BE}ON$	V_{CE} = 5 V, I_C = 200 mA	0.900 V	1.01 V
39	h_{FE}	V_{CE} = 5 V, I_C = 200 mA	10.0	40.0
40	BV_{CBO}	I_C = 100 µA	30.0 V	100 V

Table E-8. Tests, Conditions, and Limits Used for SA1825 Conventional NPN Transistor

Test Number	Test Type	Conditions	Limits	
			Minimum	Maximum
1	V_{BE}Sat	I_B/I_C = 5/50 mA	0.745 V	0.880 V
2	V_{BE}Sat	I_B/I_C = 5/50 mA	0.745 V	0.880 V
3	V_{CE}Sat	I_B/I_C = 5/50 mA	0.032 V	0.080 V
4	V_{CE}Sat	I_B/I_C = 5/50 mA	0.032 V	0.080 V
5	BV_{CEO}	I_C = 30 mA	37.0 V	300 V
6	I_{CBO}	V_{CB} = 60 V	0	10.0 nA
7	I_{EBO}	V_{EB} = 4 V	0	10.0 nA
8	I_{CEO}	V_{CE} = 25 V	0	10.0 nA
9	h_{FE}	V_{CE} = 5 V, I_C = 1 mA	50.0	200
10	h_{FE}	V_{CE} = 5 V, I_C = 20 mA	80.0	240
11	h_{FE}	V_{CE} = 5 V, I_C = 20 mA	80.0	240
12	h_{FE}	V_{CE} = 5 V, I_C = 200 mA	60.0	200
13	h_{FE}	V_{CE} = 5 V, I_C = 500 mA	40.0	140

Table E-9. Test Codes Used for Beam Lead Transistors

Test Point	Beam Lead Transistor Type						
	GT2219 (Code)	GT2905 (Code)	GT3965 (Code)	GT2484 (Code)	HT918 (Code)	GT2369 (Code)	GT3829 (Code)
Initial	G01	F01	I01	H01	E01	D01	C01
After 48 hours HTRB						D05	C05
After 96 hours HTRB						D06	
After 168 hours HTRB	G07	F07	I07	H07	E07	D07	C07
After 24 hours burn-in	G10	F10	I10	H10	E10	D10	
After 48 hours burn-in	G11	F11	I11	H11	E11	D11	C11
After 96 hours burn-in	G12	F12	I12	H12	E12	D12	C12
After 168 hours burn-in	G13	F13	I13	H13	E13	D13	C13

Table E-10. Test Codes Used for SA1825 Transistor

Test Point	Test Code
Initial	B01
After 1 hour burn-in	B02
After 6 hours burn-in	B03
After 12 hours burn-in	B04
After 24 hours burn-in	B05
After 1 hour HTRB	B06
After 6 hours HTRB	B07
After 12 hours HTRB	B08
After 24 hours HTRB	B09

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