FAST PULSE SIGNAL AVERAGING

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FAST PULSE SIGNAL AVERAGING*

W. E. Wilson

Radiological Physics Section
Radiological Sciences Department

Battelle Memorial Institute
Pacific Northwest Laboratory
Richland, Washington

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Abstract

This report describes a system which couples a sampling oscilloscope with a small digital computer. This combination makes it possible to digitally record very high frequency (up to 1GHz) and low-level (down to mV) electronic waveforms. By having the data in digital form in a computer, it is possible to do elementary calculations on individual waveforms or process many repetitions of a waveform (signal average). Some familiarity with sampling techniques and digital computers is assumed.

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- Appendix 1. Data Address and Multiplexer Details
- Appendix 2. Cable and Device Selector Details

1.0--Introduction

1.1--Data Sampling

When electronic waveforms contain frequency components which exceed the bandwidth of normal recording devices, one can sometimes resort to sampling techniques to record or display data. Thus when one has high frequency repetitive signals of known phase, one can use a sampling oscilloscope to observe the waveform when conventional display techniques fail. A sampling oscilloscope employs a fast diode gate between the input and the grid of the first tube in the vertical preamplifier. This diode gate when briefly pulsed (10^{-12} seconds) allows a charge q to pass through and be collected on the stray capacitance of the grid of the first amplifying tube. This charge, which is proportional to the instantaneous voltage at the input, is then amplified by conventional slow electronics and becomes a voltage analog of the input at the instant of sampling. On the next appropriate repetition of the waveform, the diode gate is pulsed slightly later in relative phase, thus taking a later sample. In this manner, the oscilloscope obtains a histogram of high frequency repetitive electronic waveforms.

1.2--Data Averaging

Data averaging to enhance signal-to-noise ratio is receiving widespread application. The basic operation is the algebraic summation of many repetitions of the waveform being analyzed. If the signals are added in phase, the sum of N repetitions is just N times an individual signal. The sum for noise, which is incoherent with the signal, is $N^{1/2}$ times that for a single repetition. One therefore achieves an enhancement of the signal-to-noise ratio by $N^{1/2}$. This particularly simple result actually holds exactly only for a special class of noise spectra; Ernst⁽¹⁾ and Ernst and Anderson⁽²⁾ have given theoretical discussions of time averaging.

1.3--Digital Storage

Averaging of data is perhaps most accurately done with the data in digital form. Commercially available digital devices called digital oscilloscopes are often used for this purpose. The time required for the memory cycle of these devices sets the upper bandwidth limit. For example a typical 10 microsecond cycle time puts an upper limit on the frequency components of the signals that one can measure at about 100 kHz.

The sampling technique as exemplified by the sampling oscilloscope can be thought of as a method for slowing signals that are too fast for conventional display methods. They can be used here to slow signals too fast for conventional data averaging systems. This report describes the marriage of a sampling oscilloscope with a small digital computer (PDP-8) for the purpose of employing simultaneously both sampling and averaging techniques.⁽³⁾ In one sense the computer provides a digital memory for the sampling scope. Alternatively one can think of the oscilloscope as a high speed linear gate and stretcher in front of the conventional slow ADC of the computer. In any case the system provides a versatile means of recording high-speed (GHz) and low-level (mV) waveforms under circumstances where conventional means are impossible.

2.0--Interface Description

2.1--General

The system we have assembled employs a Tektronix Model 561 display unit with plug-in sampling modules 3S76 and 3T77. This combination was used because the components were readily available and more familiar to us; presumably any similar sampling oscilloscope would work equally well. The automatic time slewing feature of the sampling scope was not altered so that the only requirement for the interface was to get the data into the computer in a useable form. Some triggering control is required in order to achieve this.

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2.2--3S76 to ADC

The principal features of the system are presented in Figure 1. The Tektronix 3S76 module has available on the front panel, a voltage analog of the vertical deflection. This signal is passed through a current amplifier for impedance matching and presented to the direct access input of the analog-to-digital converter (ADC). The current amplifier has a gain of approximately -0.3 because full-scale deflection on the oscilloscope produces +10 volts at A-out and our ADC will handle 0 to -3 volts; no further processing of the input is required.

2.3--Data Strobe

The 3T77 horizontal timing unit can use either internal or external triggering. The normal trigger-out signal is presented to the interface where the signal is delayed and shaped to provide a data strobe which commands the ADC to digitize the signal present at the data input.

2.4--Trigger Hold-Off

Simultaneously the trigger-out signal sets a flip-flop which provides a hold-off signal to incapacitate the triggering circuitry in the 3T77. This flip-flop is automatically reset by the PDP-8 following completion of the data transfer from the ADC into the PDP-8 via 3-cycle data break.

2.5--3T77 Modifications

To connect into the hold-off in the 3T77, a single transistor (2N1308) is added to the triggering circuitry within the 3T77 (refer to Figure 2). The collector of the transistor is connected between R26 and R27 in the trigger hold-off circuitry of the 3T77. Tunnel diode D25 is normally in its high state and switches to its low state when the 3T77 is triggered. The plug-in cannot be retriggered until D25 returns to its high state. This is prevented by holding the collector of the 2N1308 at ground potential.

2.6--3-Cycle Data Break

The data transfer from the ADC to the PDP-8 uses the 3-cycle data break facility of the computer. This means that the computer obtains the memory storage *location* for the datum from an internal register which automatically increments after each datum is accepted. Therefore the computer automatically assigns successive memory locations to successive points or samples from the oscilloscope. The *magnitude* of the datum is obtained from the ADC output registers and is the digital measure of the analog input.

2.7--Sweep State

At the end of one complete sweep, the sampling oscilloscope notifies the computer of this fact via the sweep-output signal of the 3T77. This signal is shaped in the interface and connects into the program interrupt buss in the PDP-8. A service routine is therefore necessary as part of the computer program to answer this program interrupt. A simple service routine would transfer the data (a single sweep) from temporary buffer memory locations to permanent locations in the computer memory, erase the buffer region and remove the trigger hold-off so that data accumulation may continue.

2.8--Module Layout

Figures 2 and 3 show in more detail the modules required to carry out the function of the interface. The trigger-in signal from the 3T77 is converted to computer logic levels by a W520 module and is then delayed. The delay is necessary to allow the sweep output signal at the beginning of a sweep to condition points F and J in the next level of modules. After this delay, the trigger-in sets the trigger hold-off flip-flop and the

output from this flip-flop, in turn, is shaped and returned as a trigger hold-off to the 3T77. The flip-flop is reset from the computer or from an external pulser if desired.

The trigger-out also provides the data strobe pulse for the ADC. The sweep-output level conditions a delay module which further delays the trigger signal, the pulse is lengthened and amplified to provide a strobe pulse for the ADC.

Figure 3 shows details of the modules necessary to provide the break requests, enable-disable and clear ADC for the data break facility between the ADC and PDP-8. The requirements here are unique to our particular ADC-computer combination and will not be discussed in any detail. Also shown is the interrupt flag which is set by the sweep-state and reset under program control. Device selector, cabling and multiplexer connections are given in the appendices.

3.0--System Operation

This section presents a collection of illustrations of the operation of the system.

3.1--Waveform Recording

A high frequency pulse approximately 10 ns wide and 300 mV high from an RIDL mercury pulser was applied to the input of the sampling oscilloscope. A single repetition of the waveform on the sampling oscilloscope is shown in Figure 4a. The horizontal scale is 2 ns and the vertical scale 100 mV per division. This repetitive waveform was fed into the sampling oscilloscope and digitally recorded by the PDP-8 computer. A single trace recorded by the computer is pictured in Figure 4b. The horizontal and vertical scales are arbitrary in this case except that each dot represents

0.2 ns which is the same as Figure 4a. The system was set to accumulate 4000 repetitions of the waveform and the result is shown in Figure 4c. The waveform is much smoother, i.e. statistically averaged. The rise and fall times are more precisely defined and the flat top of the signal shows much less spurious signal, because of the averaging of the random noise.

3.2--Memory Assignments

A single sweep from the sampling oscilloscope is recorded via data break in successive memory locations in a buffer memory region in the computer. In the program used here the beginning location is 2000₈ and the next successive 128 memory locations are reserved for recording the 100 samples in a single oscilloscope sweep. Figure 5a shows the complete memory assignments. The figure shows at the left a single sweep which occupies 100 of the first 128 channels. The next 256 channels comprise a permanent memory. The middle 128 channels comprise the least significant and the upper 128 make up the most significant portion of the double precision permanent memory. Figure 5a shows the computer display following two successive sweeps of the square pulse input. The waveform at the left is a record of the last of the two sweeps and the middle portion of the display shows the sum of the two sweeps. With only two repetitions, the least significant portion of the double precision memory has not yet overflowed so that an intelligible form is still apparent. Figure 5b shows the same memory region after 4096 successive repetitions of the sweep. Again the left 128 shows the last trace recorded and the right most 128, the most significant portion of the permanent memory, shows an averaged waveform. The least significant portion now is incomprehensible due to each channel overflowing many, many times.

The picture Figure 4b is an expanded display of the left 128 of 5b, and Figure 4c is an expanded version of the right most 128 of Figure 5b.

These modes of display and data handling are arbitrary and can be varied by reprogramming to fit one's needs. For convenience 128 rather than 100 channels were assigned to handle the 100 data points in a single sweep when the sampling scope is in the 10 samples/div mode. To operate in the 100 samples/div mode, one would need to change a few constants in the program and reassign the memory locations in a suitable fashion. There is nothing fundamental about the design of the system preventing one from using it in the 100 samples/div mode.

3.3--Time-Domain-Reflectometry

An example was made using time-domain-reflectometry to illustrate how one might use the coupled sampling scope-computer for on-line analysis on waveforms. The 10 ns pulse was injected into a 2 ns long delay line with open termination (General Radio type 874-W03 terminator). The resulting pulse and reflections were observed with the sampling oscilloscope and recorded with the computer. Figure 6a is the result for about 4000 successive repetitions of the sweep. Figure 6b shows the resulting waveform and reflections when the 2 nanosecond delay line is capacitively terminated. With the addition of appropriate subroutines for mathematical analysis of the waveforms computer assisted engineering design of delay line circuitry could be achieved.

4.0--Service Program

4.1--Program Description

This program services the sampling oscilloscope when it is interfaced with the computer. It provides for interrupts from the oscilloscope and keyboard only. The program presented here is an overlay to DODAD;⁽⁴⁾

therefore, most of the commands are identical with DODAD. The system uses 3-cycle data break with the word count register (WCR) at 0176 and current address register (CAR) at 0177. The content of CAR (initially 2000) determines the starting location of a buffer memory region wherein each individual scope trace is stored. Via program interrupt at the completion of each sweep, this service routine transfers the data from this buffer region to a permanent storage region, erases the buffer and then resumes. Transfer to permanent memory means *add* the present sweep to those previously accumulated in permanent memory so that input waveforms may be "averaged." Other methods of handling the data in the buffer region would only require reprogramming.

4.2--Loading Instructions

4.2.1--Load DODAD via the binary loader or from DECTAPE.

4.2.2--Load SCOPE via the binary loader.

4.2.3--Enter 0200 into switch register, press load address and start.

4.2.4--To enable sampling scope, type XM; to disable, type NM.

4.3--Notes

4.3.1--Memory location 0174 contains minus the number of sweeps (octal) desired. It is initially set for 10 (decimal). To obtain any other number of sweeps (up to 4096) toggle in minus the octal number desired into both 0174 and 0175.

4.4--Listing (Pages 13, 14 and 15)

5.0--Appendix

5.1--Device Selector

Appendix Figure 1 shows the device selector board (W103) which fixes the sampling oscilloscope as device 40. The three program control signals are identified. One signal goes eventually to the skip buss in the computer, the other two are used respectively to *set enable* and *clear enable* of the sampling oscilloscope.

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/SIGNAL AVERAGING PROGRAM

*1

INTER, KSF /IS IT THE KEYBOARD?

IMP .+2 /NO

IMP I CMAND/YES

SCS /IS THE SWEEP FINISHED?

IMP .+3

CES /YES, CLEAR ENABLE SCOPE

IMP I TRANS

IMP I ERROR

*20

CONTIN, JMS CRLF

IAD SAVEAC /RESTORE ACCUM

IDN /ENABLE PI

IMP I INTER-1 /EXIT

*200

BEGIN, KCC /CLEAR FLAGS

ICF

CES /CLEAR ENABLE SCOPE

MCO /CLEAR M OVERFLOW INTERRUPT

FCE MCE /CLEAR ADC ENABLES

IAD BELL /RING BELL

JMS PRINT1

JMS CRLF

*311

ENABLE, JMS I SIDES

CLA

SZL

IMP .+2

IMP CONTIN

MCA /CLEAR M ADC& TRIGGER-HOLD-OFF

SES /SET ENABLE SCOPE

IMP CONTIN

*400

TRANSF, DCA SAVEAC

JMS RESET /INITIALIZE

TAD CAR /SET UP CHANNEL #2200

TAD CHNLNO

DCA HLD1

CLA CLL

TAD I CAR

TAD I HLD1

DCA I HLD1

SZL /DID DATA OVERFLOW?

JMP CARRY /YES, CARRY ONE

CARION, ISZ CAR /NO, GO ON

ISZ HLD1

ISZ CCTR /LAST CHANNEL?

JMP .-9 /NO, DO NEXT CHANNEL

ISZ SCIR /YES, IS THIS THE LAST SWEEP?

JMP ERASE /NO, ERASE THIS SWEEP AND GO ON

JMS RESET /YES, INITIALIZE

TAD MSRP /GET READY TO TAKE ANOTHER SET

DCA SCIR

JMP CONTIN+1

CARRY, TAD HLD1 /SET UP DOUBLE PRECISION CHNL NO

TAD CHNLNO

DCA HLD2 /CARRY ONE

ISZ I HLD2

JMP CARION /NO OVERFLOW, CARRY ON

HLT /DOUBLE PRECISION DATA OVERFLOWED! HALT!

ERASE, JMS RESET /ERASE 2000 TO 2177 FOR NEXT SWEEP

CLA

DCA I CAR

ISZ CAR

ISZ CCTR /LAST CHANNEL?

JMP .-4 /NO

JMS RESET /YES, GET READY FOR NEXT SWEEP

SES /SET ENABLE SCOPE

MCA /CLEAR M ADC & TRIG HOLD OFF

JMP CONTIN+1

RESET, 0000

CLA

TAD MCHNL /LOAD MINUS # OF CHANNELS

DCA CCTR /DEPOSIT IN CHNL COUNTER

TAD CHNLST /LOAD FIRST CHNL #

DCA CAR /DEPOSIT IN CURRENT ADD REGISTER

JMP I RESET /EXIT

HLD1, 0000

HLD2, 0000

*1156
DSABLE, JMS I SIDES
SZL
IMP .+2
IMP CONTIN
CES /DISABLE SCOPE
IMP CONTIN

*41
PRINT1, 0000
*50
CRLF, 0000
*61
CHNLNO, 0200
*234
BELL, 0207
*166
SIDES, SIDE
*365
SIDE, 0000
*151
SAVEAC, 0000
*155
CHNLST, 2000
*165
CMAND, CMMAND
*173
MCHNL, 7601
*174
MSRP, 7766
*176
CCTR, 7601
*177
CAR, 2000
*154
TRANS, TRANSF
*160
ERROR, ERRORS
*571
ERRORS, KCC
*210
CMAND, DCA SAVEAC
CES=6404
SES=6402
SCS=6401
FCE=6322
MCU=6332
MCA=6334
MCE=6324
\$

5.2--Cabling

Also shown in Appendix Figure 1 are details of the three cables required to interconnect the various components of the system.

5.3--Data Address Selection, etc.

Appendix Figure 2 shows the details of the DI IN and DI ADD connections. The data address is hard-wired to 0176 (octal) which fixes the word count register (WCR) as memory location 176. This automatically defines memory location 177 to be the current address register (CAR). Biasing levels are also shown to identify three-cycle data break and direction of data input-output. All of these details are unique to our particular system and are presented here only for completeness.

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FIGURE 1

FIGURE 2

FIGURE 3

(A) Single Sweep on Sampling Oscilloscope. 100 mV/div, 2nS/div.

(B) Single Sweep Stored in Digital Memory of Computer.

(C) 4000 Repetitions of the Above Waveform.

FIGURE 4

(A) 2 Sweeps

(B) 4096 Sweeps

FIGURE 5
Memory Allocations

(A) Unterminated 2nS Line

(B) Capacitively Terminated 2nS Line

FIGURE 6
Time-Domain-Reflectometry

APPENDIX I

APPENDIX 2

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