COMPUTING TECHNOLOGY CENTER

MASTER

USER'S MANUAL: UCARDS

UNION CARBIDE AUTOMATIC ROUTING
AND DESIGN SYSTEM
FOR PRINTED CIRCUIT BOARDS

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by

J. F. Jamison

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ABSTRACT

USER'S MANUAL: UCARDS

UNION CARBIDE AUTOMATIC ROUTING
AND DESIGN SYSTEM
FOR PRINTED CIRCUIT BOARDS

UCARDS is a computer aided design system for producing component layout, conductor layout, and other aids to the fabrication of printed circuit boards. This manual is intended to serve as a guide to the proper use of the system, and supersedes report K-1736.

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INTRODUCTION

The word UCARDS is an acronym for the title Union Carbide Automatic Routing and Design System. As the title implies, UCARDS is an automated design system for producing component layout, conductor layout, and other aids for the fabrication of printed circuit boards. This manual is intended to serve as a guide to the proper use of the system.

The motivating philosophy behind UCARDS is the conviction that a flexible, easy to use system of computer programs can relieve the design engineer from many of the tedious tasks inherent to the design of printed circuit boards. In keeping with this philosophy a simple language has been developed that will aid the designer in communicating his intentions to the system. It allows the designer to control the performance of the various functions and capabilities of the UCARD System. For example, the designer can use the language to request (among other things) automatic placement of components on the circuit board, automatic generation of conductor paths, and generation of magnetic and punched tape information to control numerically controlled drills and drafting machines.

The remaining pages of this manual are devoted to a detailed description of the capabilities and use of UCARDS. The terms "designer", "design engineer" and "engineer" are used frequently and are taken to mean synonymously "one who prepares layout for fabrication of printed circuit boards." The term "design program" should be taken to mean "the language input to UCARDS necessary to design a single printed

circuit board." Other terms are defined as they first appear in the text. A glossary in the appendix provides an easy reference to most of the unusual terminology that has been employed.

Figure 1

CHAPTER 1

UCARDS CAPABILITIES

The UCARD System is divided into sections or modules, each of which contains the logic corresponding to a specific capability within the system. In most cases a module is subdivided into submodules which perform specific tasks necessary to the overall function of the module. Figure 1 depicts the capabilities of UCARDS and the logical connection between modules and submodules, and illustrates the relationship of the language described in Chapter 2 to these capabilities. By describing UCARDS capabilities in detail, this chapter will aid the designer in choosing the capabilities necessary to design a particular board.

Compilation of the Design Program

Every design program submitted to UCARDS passes through a compilation phase. This feature is automatic and the designer has no control over its use. The purpose of the Compile Feature is two fold. First, the design program language is scanned for syntactical errors and appropriate error messages are generated. These messages are described in detail in Chapter 4 and enable the designer to correct the design program before resubmitting it to UCARDS. The second function of the Compile Feature is to translate the design program (once it is free of errors) into data structures and instructions that can be processed by the various UCARDS modules.

Automatic Placement Capability

The Automatic Placement Feature is invoked at the designer's request. Its purpose is to consider electrical relationships between components, component sizes, conductor width, and board dimensions and to calculate from this information a position for each component on the circuit card. The calculated position information is then used to produce an assembly drawing of the circuit board and to print a list of components and their locations on the board to aid in fabrication.

Absolute Placement Capability

The Absolute Placement Feature is invoked at the designer's request. This feature allows the designer to specify the locations of components on the circuit board. When using this feature, UCARDS expects the design program to contain information locating the components on the board; hence, it bypasses the lengthy calculations necessary in the Automatic Placement Capability. This capability cannot be used in conjunction with Automatic Placement.

Routing Capability

The Routing Feature is invoked at the designer's request. After placement of the components has been performed, UCARDS automatically calculates which components must be connected together. The routing modules use this data to try to locate the shortest paths between these components. Routing can take place on either surface of the card and if necessary portions of a conductor path may be located on

different sides of the card. However, an attempt is made to keep the number of holes that must be drilled to a minimum.

The routing modules are not always successful in locating a path between two pins. If this happens, an appropriate message is printed to the designer. The import of this is that with the given board configuration (i.e., with the components in their present positions and with the conductor paths generated to this point already on the board) no path exists between the pins in question that does not violate some tolerance restrictions. Thus, the designer must resort to a subsequent run through UCARDS utilizing the Update Capability.

Update Capability

Update is also an optional feature. The module containing the Update Capability is comprised of five submodules which (1) remove conductor paths or portions of paths from the board, (2) remove holes from the board, (3) insert conductor paths or portions of paths onto the board, (4) insert holes into the board, and (5) reserve areas on the board for labeling at fabrication time. These features can be used by the designer to alter previously designed boards and to correct errors in previously designed boards.

Predefinition Capability

The Predefinition Capability is invoked at the designer's request. This feature is the same as items (3), (4), and (5) of the Update Capability, except that it is invoked prior to placement and can be

used to insert fixed bus lines onto the board, to insert mounting holes into the board, and to void or reserve areas on the board for later labeling.

Drilling Machine Capability

The Drilling Machine Capability is invoked at the designer's request. Within the module providing this capability there are two submodules, one of which produces information necessary to create a punched control tape for a Pratt-Whitney numerically controlled drill, and the second of which does the same for a Moog numerically controlled drill. When the designer requests this capability, a punched control tape is generated that contains information necessary to automatically drill in the board all holes required at fabrication-time. This includes all holes required to mount components on the board in addition to the holes inserted during routing for paths passing from one surface to another.

Gerber Drafting Machine Capability

If this capability is requested in the design program, a punched control tape is produced that will control a Gerber Model 75 numerically controlled drafting machine. The Gerber Model 75 is equipped with a light head so that photographic tracings can be made. Hence, when this capability is used, a tape is generated that can be used to create a photomaster of the circuit board. It is invoked at the designer's request.

Benson-Lehner Drafting Machine Capability (Optional)

When this feature is requested, a magnetic control tape is produced that causes the Benson-Lehner drafting machine to draw on paper a picture of both sides of the circuit board and a layout diagram showing the hole pattern in the board. If there were no failures during execution of the routing capability, then this capability is executed if the designer supplied a DRAFT/ statement in his design program.

Multi-Layer Capability

In the event that the designer wishes to design a laminated or stacked circuit board, he can do so by requesting this feature. The number of layers in the design is completely optional and is specified by the designer in the design program.

Batch Process Capability

This capability is invoked at the designer's request and allows him to process several design programs in one computer run. When this feature is used, the design programs are stacked one behind the other and are processed in order by UCARDS. If syntax errors are discovered during the compile phase in one design program, the appropriate error messages are generated and the next design program in the stack is then processed.

Board Type Option Capability

In order to design a circuit card, information must be supplied to

UCARDS describing the shape and dimensions of the board and the input-output connector strip. UCARDS has provision for a library of up to six such board configurations that can be permanently embedded in the system. This is of utility whenever a certain type card is used frequently by the designer. In lieu of requesting one of the board shapes in the library, the designer has the option of specifying the shape of the board and its dimensions in the design program. The result is that the designer has complete freedom in selecting the shape of the card that will hold the printed circuit being designed.

Line Drawing Capability

Occasionally the designer may need to require that certain lines other than conductor paths be drawn on the card during the execution of the drafting phase. An example of this is the underscoring of label information. This can be accomplished by use of the Line Drawing capability. The language necessary to accomplish this is given in Chapter 2.

Label Capability

The designer can request that labeling information be etched into the circuit card at fabrication time. The Label capability allows him to specify any such information and its position on the card via the design program so that the photomaster ultimately produced will contain the information.

CHAPTER 2

UCARDS LANGUAGE

It has already been stated in the introduction that the design program serves as the method of communication between the designer and the UCARD System. It is therefore essential that the designer become familiar with the language used to write the design program. This language is intended to be flexible, easy to use, and hopefully unambiguous.

As was described earlier, the UCARD System is divided into program modules each of which performs an overall function. Within each module there may be submodules which perform specific tasks related to the overall objective. Hence, some words in the UCARDS language are related to the overall activity of a module, while others are more specific and invoke activity in one or more submodules.

As is the case with any language, no matter how simple, there are certain rules of grammar that must be adhered to in order to prevent communication errors and ambiguity. This chapter describes the UCARDS language and specifies the few rules of grammar and syntax that must be observed.

General Format

Every statement in the design program has the same general format:

[UCARDS WORD]/{FIELD1,FIELD2,FIELD3,...};

that is, a UCARDS vocabulary word followed by a slash which in turn may

be followed by one or more fields separated by commas. The contents of each field, if present, is a modifier or datum depending on the word to the left of the slash. In writing the UCARDS statement, there are no positional restrictions; i.e., the statement can be positioned anywhere in the card. UCARDS ignores all blanks so the designer can put spaces between fields to make the design program listing more readable.

In the descriptions that follow, brackets, [], indicate fields that must be present in the UCARDS statement and braces, { }, indicate fields whose presence is optional in the UCARDS statement. If the field contents are optional, the optional choices are listed in a vertical stack within the braces or brackets. For example, in the statement description

MACHINE/	<div style="display: inline-block; vertical-align: middle;"> <div style="border-left: 1px solid black; border-right: 1px solid black; padding: 0 5px; margin: 0 5px;"> MOOG PRATTW GERBER </div> </div>
----------	---

the brackets indicate that one of the three words in the vertical stack must be supplied after the slash. All UCARDS vocabulary is written in capital letters.

UCARDS statements must eventually be punched into 80 column IBM cards; hence, it may happen that a particular statement will not fit on one card. UCARDS provides for this eventuality by allowing statements to be continued on a subsequent card or cards. This is done by punching the characters CONT into columns 77 through 80 of the card. For example, the following is a valid UCARDS statement:

Col. 1

Col. 77 78 79 80

CARD #1

MACHINE/

CONT

CARD #2

GERBER

A maximum of 5 continuation cards may be used for a single UCARDS statement.

Arbitrary Nodes

Format: [ARBITRARY NOD]/[n_1], { $n_2, n_3, \dots$ }

Description: There must be at least one integer number following the slash. The numbers $n_1, n_2, \dots$ are node numbers as specified in component definitions and represent circuit nodes that must be routed to some I/O point but that it is immaterial to the design which I/O point is used.

Function: To allow the designer to specify that certain circuit nodes may be routed arbitrarily to I/O points; that is, to I/O points that have not been designated for specific connections in the ONE SIDED IO or TWO SIDED IO statements. I/O points that are free to be used in this arbitrary fashion are designated by inserting the value zero (0) in the corresponding node number field of the I/O definition card.

Board Type

Format: BOARD TYPE/[n]

Description: n is an integer between one and six, $1 \leq n \leq 6$.

Function: To signal UCARDS that the circuit under design is to be placed on one of the six board configurations in the permanent library of board shapes.

Default Option: If this statement does not appear in the design program, UCARDS expects a FRAME statement and a IOSTRIP statement to be present. If none of these are present, an error condition prevails and the design program will not be executed.

Component Definition (Absolute Placement)

Format:

CAPACITOR DIODE HOLE MODULE ONE SIDED IO PAD MODULE RESISTOR TRANSISTOR TWO SIDED IO	/[name],	$\begin{bmatrix} T \\ B \end{bmatrix}$,	[k ₁ ,k ₂ ,...,k _n],	[I ₁ ,
				J ₁ ,I ₂ ,J ₂ ,...,I _n ,J _n]

Description: The words in the vertical stack to the left of the slash are used to define components to be mounted on the board. ONE SIDED IO is used to define a connector strip that is insulated from any connector that may be defined on the reverse side of the card. TWO SIDED IO is used to define a connector strip that is electrically connected by a drilled hole to a mirror image on the reverse side of the card. When defining IO

strips, always define them from left to right. PAD MODULE is used to define an integrated module that does not require holes for mounting as opposed to HOLE MODULE which describes an integrated module that requires holes for mounting. [name] is any one to four character identifier that the designer wishes to use. A "T" in the second field means the component is to be mounted on the top side of the board and a "B" means it is to be mounted on the bottom side. The third field is the first of n fields $k_1, k_2, \dots, k_n$ which contain the numbers of the nodes to which pins 1, 2, ..., n of the component connect, where n is the number of pins on the component. The fourth set of brackets represents $2n$ fields containing grid coordinate¹ pairs representing the location on the circuit board of each pin 1, 2, ..., n .

Function: To describe a component and associated circuit information to UCARDS.

Example:

Col. 1

DIODE/D1, T, 1, 2, 10, 5, 10, 15

Here the component is a diode called D1 to be mounted on the top side of the circuit board. Pin one connects to node 1 of the circuit and pin 2 connects to node 2 of the circuit. Pin one

¹ For a description of grid coordinates, see Chapter 3.

is located 10 grid cells from the top of the board and 5 grid cells from the left hand edge while pin two is located 10 grid cells from the top and 15 cells from left.

Component Definition (Automatic Placement)

Format:	CAPACITOR	/[name], $\begin{bmatrix} T \\ B \end{bmatrix}$ [k ₁ ,k ₂ ,...,k _n] {H, W}
	DIODE	
	HOLE MODULE	
	ONE SIDED IO	
	PAD MODULE	{X ₁ , Y ₁ , X ₂ , Y ₂ , ..., X _n , Y _n }, {Label}
	RESISTOR	
	TRANSISTOR	
	TWO SIDED IO	

Description: The words in the vertical stack to the left of the slash have the same meaning as for absolute placement, as do the first two fields to the right of the slash. The optional fields beginning with the fourth field after the slash are as follows: H is a decimal number equal to the height of the component, W is a decimal number equal to the width of the component², X₁, Y₁, X₂, Y₂, ..., X_n, Y_n, are the coordinate location in inches of pins 1, 2, ..., n, on this component,

² Automatic placement views all components as if they were rectangles.

Figure 2

assuming the origin to be the center of the component, see Figure 2. The fields $k_1, k_2, \dots, k_n$ are the numbers of the nodes in the circuit to which pins 1, 2, ..., n, respectively, connect. In the case of I/O strips, only those I/O points which are to be connected to specific nodes should have positive node numbers assigned. The remainder should have zeroes (0) in the corresponding node field. The final field in the card is optional but must be present if the previous optional fields {H, W}, and $\{X_1, Y_1, \dots\}$ are omitted. It contains any one to four character identifier and, if present, tells UCARDS that the component description data has been omitted from this card and may be found on a DESCRIBE card bearing this label. The DESCRIBE card format is explained later in this chapter.

Function: To describe a component and associated circuit information to UCARDS when automatic placement has been requested.

Examples:

Col. 1

DIODE/D1, T, 1, 2, .5, .125, 0., .25, 0., -.25

Col. 1

DIODE/D1, T, 1, 2, \$1

DESCRIBE/\$1, .5, .125, 0., .25, 0., -.25

Cell Size

Format: [CELL SIZE]/[X]

Description: X is a decimal number equal to the length of one side of a square grid cell.

Function: To tell UCARDS the dimensions of a grid cell. This statement is used for both absolute and automatic placement. When automatic placement has been requested, the smaller of the CELL SIZE and the LAND DIAMETER is used to determine the grid system.

Default Option: If not specified, the cell size is assumed to be .1 inch.

Define

Format: [DEFINE]/

Function: This statement signals UCARDS that absolute placement is to be performed and that component definition cards will appear next in the design program.

Delete Hole

Format: [DELETE HOLE]/[I₁, J₁, I₂, J₂, ...]

Description: This statement is used when updating a previously designed circuit board. The fields to the right of the slash

contain grid coordinate locations of holes to be removed from the board.

Function: To activate the hole delete module of UCARDS so that specified holes can be removed from a previously designed circuit board.

Delete Path

Format: [DELETE PATH]/ $\begin{bmatrix} T \\ B \end{bmatrix}$, $[I_1, J_1, I_2, J_2]$, $\{ \begin{matrix} T \\ B \end{matrix}, [I_3, J_3, I_3, J_3] \}, \dots$

Description: The first field to the right of the slash contains a "T" or a "B" indicating that the path segments in this statement are to be removed from the top or bottom, respectively, of a previously designed circuit board. At least two pairs of grid coordinates must follow the first field. These coordinates are the locations of the end points of a horizontal or vertical path segment to be removed. Several path segments can be deleted with a single DELETE PATH statement. In order to delete a path connecting two pins one must decompose it into its horizontal and vertical components and specify each of these in a DELETE PATH statement.

Function: To activate the path delete module of UCARDS and provide data necessary to remove circuit paths from a previously designed circuit board.

Describe

Format: [DESCRIBE]/[Label], [H, W], [X₁, Y₁, X₂, Y₂, ..., X_n, Y_n]

Description: The first field to the right of the slash contains a one to four character label that appeared in a component definition card. In the remaining fields, H is a decimal number equal to the height of the component, W is a decimal number equal to the width of the component, and X₁ and Y₁ are decimal numbers that represent the coordinate location of pin one of the component, assuming the origin to be at the center of the component. X₂ and Y₂ are similarly defined for pin 2 of the component, and so on.

Function: To describe the geometry of a component to be placed on the circuit board by the automatic placement capability. This statement has utility when a number of components with identical dimensions are to be mounted on the board.

Dimension

Format: [DIMENSION]/ [A₁, B₁]

Description: A₁ and B₁ are decimal numbers equal to the dimension in inches of the rectangular area on the circuit board available for component mounting and path layout. In Figure 3, A₁=X₈-X₁ and B₁=Y₁₀-Y₁.

Figure 3

Function: This statement supplies the placement and routing modules of UCARDS with the dimensions of the usable area of the board under design.

Draft

Format: [DRAFT]/

Function: This statement activates the drafting machine modules in UCARDS. the MACHINE/ statement is then used to specify which machines are to be used.

Draft Option

Format: [DRAFT OPTION]/ $\begin{bmatrix} \text{ON} \\ \text{OFF} \end{bmatrix}$

Function: Same as PUNCH OPTION except for drafting.

Default Option: Same as for PUNCH OPTION.

Drawline

Format: [DRAWLINE]/ $\begin{bmatrix} \text{T} \\ \text{B} \end{bmatrix}$, [I₁, J₁, I₂, J₂], { $\begin{bmatrix} \text{T} \\ \text{B} \end{bmatrix}$, I₃, J₃, I₄, J₄ },...

Description: The "T" or "B" following the slash is used to indicate on which surface the line segments specified in this statement are to be drawn. At least two pairs of grid coordinates must follow the surface field. These represent the end points in grid coordinates of a line segment to be etched on the circuit

board. Additional line segments are optional.

Function: To enable the designer to draw line segments on the board other than those paths generated by UCARDS. For example the statement can be used to underline label information.

Exit

Format: [EXIT]/

Description: UCARDS ignores any information appearing to the right of the slash in this statement; hence, it may be used by the designer to supply appropriate comments.

Function: This statement signals to UCARDS that the design program has been completely executed and no more design programs are to be executed at this time.

Example: EXIT/ END OF DESIGN PROGRAM P19354

Failure Limit

Format: [FAILURE LIMIT]/[X]

Description: X is an integer number representing the maximum number of failures that will be tolerated during routing.

Function: To supply an upper bound to the number of routing failures that will be tolerated.

Default Option: If this statement does not appear in the design program, UCARDS will not tolerate any failures during routing. Consequently if a failure occurs, execution of the design program stops.

File

Format: [FILE]/[file number]

Description: The field to the right of the slash must contain an integer between one and ten ($1 \leq \text{file number} \leq 10$). No decimal point can be present.

Function: UCARDS files a model of each design in a 10 entry file.

The designer can use any one of these entries or slots to file a given design. He can at any time override an entry in the file with a new entry by supplying in the new design program a FILE/ statement containing the file number of the old design.

In this case the old design is destroyed. The designer must specify which slot in the file is to be used for a particular design or the model of the design will not be filed for future reference.

Frame

Format: [FRAME]/[$X_1, Y_1, X_2, Y_2, \dots, X_n, Y_n$]

Description: The pairs (X_i, Y_i) to the right of the slash are the coordinate locations in inches of corner points in the outline of the board under design. The points are tabulated starting at any corner and then moving counterclockwise around the frame. The origin is assumed to be at the lower left corner of a rectangle enclosing the board. (See Figure 3).

Function: To supply dimension and outline data about the board shape on which the circuit under design is to be placed.

Default Option: If this statement does not appear, UCARDS assumes that a BOARD TYPE/n statement appears elsewhere in the design program. If neither occurs an unresolvable error condition exists and the design program will not be executed.

Gridsize

Format: [GRID SIZE]/ [I, J]

Description: I is an integer count of the number of grid cells in the vertical direction. J is an integer count of the number of grid cells in the horizontal direction.

Function: To provide UCARDS with dimensional information about the grid network being used for this design. When automatic placement is being used, this statement is ignored if present in the design program. See Chapter 3 for a complete description of grid networks.

Insert Hole

Format: [INSERT HOLE]/ [I₁, J₁, I₂, J₂, ..., I_n, J_n]

Description: The pairs of numbers to the right of the slash are integers representing grid coordinate locations of positions where holes are to be drilled on the circuit board.

Function: This statement signals UCARDS that during updating or during predefinition holes are to be inserted in the board at the specified locations.

Insert Path

Format: [INSERT PATH]/ [$\begin{bmatrix} T \\ B \end{bmatrix}$, P₁, I₁, J₁, I₂, J₂], { $\begin{bmatrix} T \\ B \end{bmatrix}$,
[P₂, I₃, J₃, I₄, J₄]},...

Description: As indicated above, at least six fields must follow to the right of the slash. Additional groups of six fields are optional. The first field in each group must be a "T" or a "B" indicating to UCARDS on which side of the circuit board the path specified is to be placed. P₁, P₂,... are decimal numbers that are used by UCARDS to identify the path segment. They are referred to as path identification numbers. The integer pairs (I₁, J₁, I₂, J₂,...) are pairs of grid coordinates specifying the end points of a horizontal or vertical path segment. Hence, in each group of six fields either I₁ = I₂ or J₁ = J₂.

Function: This statement may be used when either updating or predefining. During predefinition, it can be used to insert bus lines on the board in cases where many components connect to the same node. During updating, it can be used to connect previously unconnected components. The path identification numbers are very important. Chapter 3 describes these numbers and their function in more detail.

IO Height

Format: [IO HEIGHT]/[X]

Description: "X" is a decimal number equal to the vertical height of the connector strip at the bottom of the board. In Figure 3, $X = Y2 - Y5$.

Function: UCARDS assumes during routing that the circuit board is a rectangle with a connector strip containing input-output points located on one or more edges. Hence, for plug-in circuit cards such as the one in Figure 3 the designer must specify the vertical height of the connector strip so that UCARDS can take this into account when producing control tapes for the drilling and drafting machines.

Default Option: If this statement does not appear in the design program, UCARDS assumes that there is no connector strip.

IO Strip (short form)

Format: [IO STRIP]/ [X, Y, INC, H, n]

Description: The pair (X, Y) is the coordinate location in inches of the center of the pad at the top of the left most connector in the strip. "INC" is the distance in inches between the centers of adjacent pads on the strip. "H" is the height of the connectors on the strip and "n" is the number of connectors on the strip.

Function: To supply dimension data to UCARDS so that the connector strip or plug portion of the card can be drawn.

Default Option: Same as for FRAME/ statement.

IO Strip (long form)

Format: [IO STRIP]/ [X₁, Y₁, X₂, Y₂, ..., X_n, Y_n]

Description: Each pair (X, Y) is the coordinate in inches of the center of a pad on a connector in the strip. This form must be used when the I/O strip is not amenable to definition using the short form. For example, some circuit board plug strips require that holes be drilled in the P/C board connectors both at the top and bottom of each connector. Also this type of plug often requires that the connectors be staggered, hence, the short form could not be used since

it provides only for holes along the top of each connector in the strip and also that they be in a straight line.

Function: Same as for the short form.

Default Option: Same as for the FRAME/ statement.

Label

Format: [LABEL]/[X, Y], [size], $\begin{bmatrix} H \\ V \end{bmatrix}$, [alphameric data]

Description: X and Y are decimal numbers equal to the coordinates in inches of the point at which the alphameric data are to be placed. "size" is a decimal number equal to the length of one side of a square that will contain the characters in the alphameric data. The presence of an H means the alphameric data is to be drawn from left to right horizontally. Similarly, V means the alphameric data is to be drawn from bottom to top vertically starting at the point X, Y.

Function: To allow the designer to specify the label information that is to appear on the circuit board.

Land Diameter

Format: [LAND DIAMETER]/[X]

Description: X is a decimal number equal to the maximum diameter of lands necessary for hole drilling.

Function: To supply UCARDS with the maximum land diameter of all the lands that must be etched on the circuit board.

Default Option: If this statement does not appear in the design program, UCARDS assumes that the largest land has a diameter of .1 inch.

Machine

Format: [MACHINE]/

NAWIDE
MOOG
PRATTW
GERBER

Description: The options in the vertical stack to the right of the slash are names by which UCARDS recognizes a particular numerically controlled machine. MOOG refers to a MOOG drilling machine, PRATTW refers to a Pratt-Whitney drill, and GERBER refers to a Gerber drafting machine equipped with photographic light head. The particular machines used will be dictated by the design installation and need not be the ones mentioned here. If an installation prefers other machines, the highly modularized construction of UCARDS

makes it relatively easy for a computer programmer to supply the proper routines for generating punched tape for these machines and to embed the corresponding machine names into the UCARDS vocabulary.

Margins

Format: [MARGINS]/[k, r, t, b]

Description: When automatic placement is to take place, a DIMENSION statement is used to define the dimensions of a rectangular area available for component placement. The MARGINS statement provides for margins within this rectangle as follows: k = width of margin at left side of placement area, r = width of margin at right side of placement area, t = width of margin at top side of placement area, b = width of margin at bottom side of placement area.

Function: To allow the designer to specify margins within the placement area so that labels or bus lines can be etched along the edges and not interfere with components.

Newcase

Format: [NEWCASE]/

Function: To signal UCARDS that a design program ends with this card and a new program immediately follows this program.

Offset

Format: [OFFSET]/[X, Y]

Description: X and Y are the amount of translation in the horizontal and vertical directions that is to be applied when drilling the holes in the fabricated board.

Function: X and Y are measured in inches from the origin of the drill bed. The purpose is to prevent the drill from operating in the same portion of the drill bed all of the time. This is critical only in shops where the particular drill is used exclusively for small printed circuit boards so that constant operation in a restricted portion of the drill bed would produce uneven wear on the machine.

Default Option: If this statement does not appear in the design program, UCARDS assumes an offset of zero inches.

Place

Format: [PLACE]/

Function: This statement signals UCARDS that automatic placement is to be performed and that component definition cards will appear next in the design program.

Predefine

Format: [PREDEFINE]/

Function: This statement signals UCARDS that the designer will

use the VOID, INSERT PATH, or INSERT HOLE statements before component definition and routing. By utilizing this feature, the designer can preset certain board areas to conditions of his own choosing.

Punch

Format: [PUNCH]/

Function: This statement signals UCARDS that the designer requires punched control tapes so that numerical controlled drills can be used to drill holes in the circuit board.

Punch Option

Format: [PUNCH OPTION]/^{ON}[_{OFF}]

Function: Normally if failures occur during routing, the designer does not then require punched control tapes, since the design is not yet complete. However, the control tapes and associated computer listings can sometimes be helpful in updating the board; hence, UCARDS provides the option of obtaining control tapes even though routing failures have occurred. PUNCH OPTION/ON means provide control tapes regardless of results during routing. The PUNCH OPTION/ statement is ignored unless a PUNCH/ statement also appears in the design program.

Default Option: The punch option is assumed ON if no PUNCH OPTION/OFF appears in the design program.

Remark

Format: [REMARK]/[any alphanumeric information]

Function: This statement is used to supply descriptive comments in the design program. It has no effect on the execution of the design program.

Example:

```

:
:
REMARK/This design uses an apar card
:
BOARD TYPE/6
:
:

```

Route

Format: [ROUTE]/

Function: This statement signals UCARDS that routing is to take place and hence, activates the routing modules.

Scale

Format: [SCALE]/[X]

Description: "X" is a decimal number equal to the scale factor to be used when preparing layout drawings and drill control tape output. The photomasters are always produced at actual size.

Function: To provide scaling data to UCARDS. For example, if a 2 to 1 paper drawing is desired in addition to the actual size picture the statement would read SCALE/2.0 .

Default Option: If no scale statement appears; only actual size output will be produced.

Search

Format: [SEARCH]/[FILE NUMBER]

Description: File number is an integer between 1 and 10 corresponding to the file number used in the "FILE/file number" statement when this circuit board was originally submitted to UCARDS for design.

Function: This statement provides UCARDS with the file key corresponding to a particular previous design and commands UCARDS to obtain that design from the file.

Title

Format: [TITLE]/ {alphameric data}

Description: The field after the slash may contain any alphameric data whatever.

Function: This statement provides the designer with the means for titling all listings, punched tapes, and photomasters associated

with the design of a particular board.

Update

Format: [UPDATE]/

Function: This statement signals UCARDS that the design program in which it appears is intended to alter a previously designed circuit board that is on file and hence, activates the update modules.

Void

Format: [VOID]/ $\begin{bmatrix} T \\ B \\ TB \end{bmatrix}$, $[I_1, J_1, I_2, J_2, I_3, J_3]$

Description: The first field to the right of the slash must contain a T, B, or TB corresponding to whether the area to be reserved lies on the top, bottom or both top and bottom of the board. The three coordinate pairs, (I_1, J_1) , (I_2, J_2) , and (I_3, J_3) are grid coordinate pairs representing any three corners of a rectangular area on the circuit board.

Function: To enable the designer to reserve rectangular areas of the circuit board for labeling.

CHAPTER 3

USE OF UCARDS

The UCARD System employs a discrete cellular environment to construct a digital computer model of a printed circuit board. In the area where printed circuitry is permitted, a grid system is constructed and unique coordinates are assigned to each grid cell with the origin of the coordinate system assumed to be at the upper left hand corner of the circuit board (see Figure 4). When absolute placement is being done, the designer has the responsibility for constructing this grid system so that he can specify the location of components within it. If automatic placement is to be performed, then UCARDS constructs the grid system internally. The size of the cells is a function of wire width and tolerance.

The grid system is also utilized during the routing phase of processing. UCARDS, in attempting to locate the most direct path between two pins, examines all cells in the grid system and attempts to locate a chain of previously unused cells that link the two pins together. If it is successful in doing this, the same decimal number is assigned to each cell in the chain. This number is unique for each distinct path and is referred to as the path identification number. The functions of this number are basic to UCARDS. It is of utmost importance to the designer when updating previously designed circuit boards.

TYPICAL GRID SYSTEM

Constructing the Grid System

In many cases, the question of where to place components on the circuit board is answered by the designer simply by glancing at the circuit schematic. When this is the case, the lengthy calculations of automatic placement can be avoided by specifying in the design program the grid system and absolute location of components in it. To do this the designer must construct the grid system.

The grid system is easily constructed by considering three questions (1) What is the required minimum diameter of a conductor for this board?, (2) What is the required minimum spacing between conductors for this board?, and (3) What is the minimum land diameter allowable? Since UCARDS considers all conductors to be centered in a horizontal and/or vertical chain of grid cells, it is necessary to choose a grid cell size at least large enough so that if two conductors run parallel, they will not violate the spacing tolerance. In general, spacing is equal to the minimum conductor width so that by choosing the grid cell size equal to twice the minimum conductor width no tolerances will be violated.

In order to determine the dimensions of the grid system, simply divide the width (see Figure 4) of the circuit board in inches by the grid cell size decided upon. The largest integer smaller than the quotient is the number of grid cells in the horizontal direction. Similarly, the number of cells in the vertical direction is equal to the largest integer smaller than the quotient of the height of the

board in inches divided by the grid cell size.¹ This information is now used in the GRID SIZE/ and CELL SIZE/ statements.

For example, suppose the width of the circuit board is 3.1 inches and the height is 4.15 inches. In addition suppose the cell size used is .1 inches. Then the number of cells in the horizontal direction will be $[3.1 \div .1] = [31] = 31$. Similarly, the number of cells in the vertical direction will be $[4.15 \div .1] = [41.5] = 41$. Hence, the GRID SIZE statement would read:

GRID SIZE/ 41, 31

Using the Routing Capability

This capability is perhaps the simplest to use of all the UCARDS capabilities. After writing the component definition statements the designer needs only to write the statement ROUTE/ in his design program in order to invoke the routing capability. When UCARDS encounters this statement in the design program, it automatically begins to connect the components in the proper fashion.

As a standard part of the computer output, the designer receives a printer plot of the conductor configuration at the end of each connection. Also the path identification number used for the connection is printed out. In addition, after all connections have been attempted by UCARDS a list of any failures is printed and a list of each pin of

¹ Note that the connector strip is not included; only that part of the board available for conductor routing is considered.

each component together with the path identification number used at each pin (if any) is printed. This information is extremely useful to the designer when updating the circuit board since he must supply path identification numbers when using the INSERT PATH statement.

Using the Describe Capability

When using Automatic Placement, it is necessary to supply UCARDS with data about the height, width, and relative pin locations on the component. This is done in the component definition statements. It is not unusual for a circuit board to have many components of the same description on it, hence, by using the Describe Feature the designer need only specify the component description once for each component type.

For example if the circuit board under design will have ten .1 x .3 inch resistors mounted on it, the designer can choose a label, say \$1, and use it in a DESCRIBE statement as detailed in Chapter 2. Then when writing the component definition statements he can describe the component geometry by simply using the label \$1 instead of detailing all of the information in each statement.

Using the Drilling Machine Capability

UCARDS provides the option of calling for control tapes to operate either one or both of two numerical controlled drills, a MOOG drill and a Pratt-Whitney drill. The PUNCH statement activates the UCARDS modules that prepare these control tapes. However, the designer must

tell UCARDS via a MACHINE statement which machines are to be used. The MACHINE statement can be used to invoke only one machine so that if tapes for both drills are required, two MACHINE statements must appear in the design program. If an OFFSET statement is used to translate the drill coordinates, then the same translation amount applies to all machines requested. Similarly, if a SCALE statement is used, scaled control tapes will be produced, in addition to the actual size tapes, for all machines requested.

If the designer does not wish to obtain control tapes when failures occur during routing, he must supply in the design program the statements:

PUNCH OPTION/OFF

PUNCH/

MACHINE/[machine name].

Using the Drafting Machine Capability

UCARDS provides the option of calling for control tapes to operate either one or both of two numerically controlled drafting machines, a Benson Lehner Electro Plotter and a Gerber Model 75 drafting machine equipped with a lighthead. The DRAFT statement activates the UCARDS modules that prepare these control tapes. In the case of the Benson Lehner drafting machine, the control tape is a magnetic tape and in the case of the Gerber, the control tape is a punched paper or mylar tape.

Whenever the statement DRAFT/ appears in the design program, UCARDS

will produce a control tape for the Benson Lehner drafting machine provided no failures occurred during routing. Note that no MACHINE/ statement is required. However, in order to activate the Gerber drafting machine modules, the statements

DRAFT/

MACHINE/GERBER

must appear in the design program.

If the designer does not wish to obtain pictures of the circuit board when failures occur during routing, the following statements must appear in the design program:

DRAFT OPTION/OFF

DRAFT/

MACHINE/GERBER

Programming note: Pictures are quite often helpful in updating a design that was unsuccessful on the first attempt. Hence, it is generally recommended that the following statements be present in the design program on the first attempt:

DRAFT OPTION/ON

DRAFT/

In this case, a Benson Lehner drawing can be made which will give the designer a better idea of the path configurations generated. Of course, the statement,

MACHINE/GERBER

may also be present at the designer's option.

Using the Update and Predefinition Capability

The successful layout of a circuit board is contingent upon many factors such as component placement, component and conductor density and the order in which conductor paths are laid out on the board. The human designer has the advantages of intuition, experience and forethought when attempting a design; no computer aided design system can possess any of these with present day computers.

In an attempt to offset this seemingly prohibitive disadvantage, UCARDS provides an update capability which allows the designer to impose his intuition, experience and forethought on the design. For example, before submitting the design program to UCARDS, the designer might notice that a number of component pins reside on the same node in the circuit schematic. Hence, he would be led to consider the possibilities of "predefining" a bus line around some portion of the border of the board which would tend to make those component pins connect to the bus line thereby reducing conductor density in the center of the board. The UCARDS PREDEFINE statement, together with the INSERT PATH and INSERT HOLE statements, supplies the option for doing this.

On the other hand, it is not infrequent that the first design attempt is unsuccessful in that one or two conductor paths cannot be placed on the board. The Update Capability allows the designer to alter conductor paths on the original design so that UCARDS can complete the design on a second attempt.

For example, the designer might notice that had the paths been laid out in a different order during the routing phase, circuit trees

would have built up in a different manner thereby allowing all connections to be made. Since he has no control over the order in which connections are attempted (UCARDS does this) he must use the update capability to alter the paths into an equivalent tree structure that will allow the remaining connections to be done.

When UCARDS completes the processing of a design program, it files a model of the circuit card using the file number in the FILE/ statement. If the designer wishes to update the circuit board at a later time, he must request that model by supplying the file number in a SEARCH/[file number] statement.

Hence, if the designer wished to alter a previous design that had been filed under the file number 9 and to refile the altered design under file number 9, his design program would contain the statement:

```

:
:
SEARCH/9
:
:

```

Once the desired previous design has been obtained, UCARDS is ready to perform the updating tasks requested by the designer. It has been mentioned earlier that the path identification number associated with each conductor path is of utmost importance during updating. In particular, when the designer wishes to insert a new path onto the board he must be careful to choose a path identification number that is unique, i.e. one that has never been used before. One can always do this by counting the number of connections made in the previous design and adding 50 to that result. All numbers greater than this will not have been used in the previous design.

On the other hand, if the designer wishes to insert a conductor path that is to join some conductor tree established in the previous design, he must use a path identification number in his INSERT PATH statement that is the same as that used by UCARDS when the original tree was developed in the previous design. In order to expedite this choice by the designer, UCARDS prints at the end of each design, a table showing the pin location of each component and the associated path identification number.

Using the Multi-Layer Capability

This capability is intended to give the designer the ability to design laminated or stacked circuit boards. No provision is made for forcing particular conductors or circuits to be on a given surface. In order to do this, the designer must submit separate design programs for each surface and stack them at fabrication time.

The designer uses the multi-layer capability when designing boards that must be compact and yet at the same time have many conductors. In this case, it is usually immaterial to the designer which layer a particular conductor lies on. The UCARDS multi-layer capability processes all connections, attempting to place them all on one layer; if this cannot be done, the remaining connections are attempted on the second layer and so on until either all connections have been completed or the maximum number of allowable layers has been exhausted. The fact that multi-layer processing is to take place and the maximum number of layers that will be tolerated are specified by the statement

MULTI-LAYER/[n].

Notice that if it is possible, UCARDS will complete the design on less than "n" layers.

Using the New Case Capability

This capability allows the designer to "batch process" design programs. In order to utilize the capability the designer merely ends each design program in the stack with the exception of the last one with the statement:

NEW CASE/ .

If any one of the design programs fails to compile, UCARDS passes on to the next program in the stack after printing appropriate error messages.

Using the Automatic Placement Capability

This capability relieves the designer from the task of deciding where each component must be placed on the circuit board. The criterion used by UCARDS in selecting a position for each component on the circuit board is that of minimum wire length. That is, the components are placed so that the total path length of conductors is a minimum.

In order to use this capability, the designer must first describe in the design program the area available for placement via the statements:

DIMENSION/

MARGINS/

These statements are described in detail in Chapter 2. After this, the statement:

PLACE/

may appear. Its appearance signals UCARDS that Automatic Placement is to take place. The component definition statements must appear after this statement. Component definition statements are detailed in Chapter 2.

Before using this capability, the designer should read about the DESCRIBE statement since its use can greatly reduce the effort necessary to write the component definition statements. In addition the parts list should be checked for component sizes. If the board to be designed contains one or more components that are very large relative to the remaining components, then absolute placement is advised over automatic placement.

Using the Absolute Placement Capability

Since it is often an easy matter for the designer to decide where components should be placed on the circuit board, UCARDS provides the absolute placement feature so that the lengthy calculations of automatic placement can be avoided. There is another reason for providing this feature. Automatic placement uses the criterion of minimum wire length to compute an "optimal" position for each component on the circuit board. It may happen that even though this criterion can be satisfied and a component arrangement computed, the resulting arrangement prevents certain connections from being made during the

routing phase. If this occurs and produces a serious updating problem, the designer would do well to change the design program to use Absolute Placement so that he can impose his intuition and skill on the problem.

In order to use this capability, the designer must first select a grid network as described in the section: Constructing the Grid System. Using the appropriate UCARDS statements, this grid network is then described in the design program after which the statement:

DEFINE/

may appear. This will signal UCARDS that the design program contains component placement data. Following this statement the component definition statements must appear. These statements are described in Chapter 2.

Defining Components

The statements and their formats necessary to define components to be mounted on the circuit board are described in Chapter 2. The method of definition varies depending on whether the designer wishes to use the Automatic Placement feature or the Absolute Placement feature. In either case the user must assign a symbolic name to the component, (e.g. R1 might signify a resistor, C2 might represent a capacitor, etc.). Also the designer must decide which surface (top or bottom) of the card the component is to be mounted on.

When using the Absolute Placement feature, the designer must provide two additional sets of data. First, he must specify to which node on the circuit each pin of the component connects. In order to do

this he should take the circuit schematic and assign a unique integer number to each node. The node information for each component can then be read directly off of the circuit schematic. Figure 5 illustrates how this might be done. Secondly, the designer must supply the location in grid coordinates (see the section Constructing the Grid System in this chapter) of each pin in the component. It is imperative that the pin locations be given in the same order as the node information.

Defining components when using the Automatic Placement feature is the same as for Absolute Placement except that no grid coordinate information is supplied. Instead a geometric description of the component is given. This description is described in Chapter 2 and illustrated in Figure 2.

○ REPRESENTS NODE NUMBER

CHAPTER 4

UCARDS ERROR MESSAGES

This chapter contains a list of the error messages that can be generated by UCARDS. In addition to errors in the design program itself, it can happen that errors occur during routing due to the board being too densely packed with conductor paths and components. In order to facilitate the diagnosis of such events, appropriate error messages are generated.

1. MESSAGE: ROUTING FAILURE

CAUSE: No path exists between the pins being connected that does not violate tolerances.

UCARDS ACTION: Processing continues, unless the allowable limit of failures is exceeded, on the next connection. This connection is saved and listed at the end of processing together with any others that may have failed.

USER ACTION: An Update must be made on the final board configuration and the connection that failed must be manually inserted with INSERT PATH statements.

2. MESSAGE: **** THERE IS A FORMAT ERROR IN THE ABOVE CARD ****

CAUSE: The UCARDS statement is incorrectly written.

UCARDS ACTION: The design program will not be executed, but the error scan continues.

USER ACTION: Check the statement in question against the format detailed in Chapter 2. Correct the statement and resubmit the design program to UCARDS.

3. MESSAGE: **** WARNING --- TOOL TRANSLATION AMOUNT IS ZERO ****

CAUSE: The OFFSET/ statement does not have a translation amount specified, hence the statement is redundant.

UCARDS ACTION: This is a warning only. UCARDS continues its error scan and executes the design program if no further errors occur.

USER ACTION: If no translation amount is desired then no action is required. Otherwise the statement must be changed and the design program resubmitted to UCARDS.

4. MESSAGE: **** SURFACE NOT SPECIFIED IN ABOVE CARD ****

CAUSE: One of the fields in the statement specified should contain a T, B, or TB but none appears.

UCARDS ACTION: The design program will not be executed but the error scan continues.

USER ACTION: Check the statement against the format detailed in Chapter 2. Correct it and resubmit the design program to UCARDS.

5. MESSAGE: **** COORDINATE DATA INCORRECT IN ABOVE CARD ****

CAUSE: The number of coordinate fields in the statement specified is incorrect.

UCARDS ACTION: The design program will not be executed but the error scan continues.

USER ACTION: Check the statement against the format detailed in Chapter 2. Correct it and resubmit the design program to UCARDS.

6. MESSAGE: **** MACHINE NOT AVAILABLE ****

CAUSE: The machine name in the MACHINE/statement is not MOOG,
PRATTW, or GERBER.

UCARDS ACTION: The design program will not be executed. Error
scan continues.

USER ACTION: Correct the statement and resubmit the design
program to UCARDS.

7. MESSAGE: **** THE WORD IN THE ABOVE CARD IS NOT PART OF THE
UCARDS VOCABULARY ****

CAUSE: The word to the left of the slash in the statement specified
is misspelled.

UCARDS ACTION: The design program will not be executed, but the
error scan continues.

USER ACTION: Correct the statement and resubmit the design program
to UCARDS.

8. MESSAGE: **** THE INTERCONNECT TABLES HAVE OVERFLOWED ****

CAUSE: More than 200 connections are called for in this design
program.

UCARDS ACTION: The design program will not be executed, but the
error scan continues.

USER ACTION: The designer can break the design program into two
programs and use the NEW CASE/ statement. This will produce
effectively two circuit boards that can be stacked. If this is
not acceptable, see a computer programmer and have him increase
the lengths of the CMPH, CMPT, IHSUB, and ITSUB arrays.

9. MESSAGE: **** NO DELIMITER IN THE ABOVE CARD ****
- CAUSE: Either a slash (/) or a comma is missing in the statement specified.
- UCARDS ACTION: The design program will not be executed but the error scan continues.
- USER ACTION: Correct the statement and resubmit the design program to UCARDS.
10. MESSAGE: **** PAD DIAMETER TOO LARGE FOR THIS GRID ****
- CAUSE: The pad diameter specified in the LAND DIAMETER/ statement is greater than ten times the width of a grid cell as specified in the CELL SIZE/ statement.
- UCARDS ACTION: Execution of the design program is stopped.
- USER ACTION: Check the LAND DIAMETER and CELL SIZE statements for errors.
11. MESSAGE: **** THE INSERT AND DELETE TABLE HAS OVERFLOWED ****
- CAUSE: The total number of path segments being inserted or deleted is greater than 500.
- UCARDS ACTION: All processing stops immediately.
- USER ACTION: Make two separate update runs through UCARDS.
- Submit part of the path deletes and/or inserts on the first run and the remaining ones on the second run. The same FILE/ statement must be used in both update runs.
12. MESSAGE: **** THE VOID TABLE HAS OVERFLOWED ****
- CAUSE: More than 9 rectangular areas are being reserved on the board in VOID/ statements.

UCARDS ACTION: All processing stops immediately.

USER ACTION: Try to consolidate some of the reserve areas into a single area.

13. MESSAGE: **** CONTINUATION NOT ALLOWED FOR MORE THAN FIVE CARDS ****

**** ALL THE FOLLOWING CONTINUATION CARDS WILL BE IGNORED ****

CAUSE: More than five continuation cards were used.

UCARDS ACTION: The design program will not be executed, but the error scan continues.

USER ACTION: Write new UCARDS statements containing the data in the excess continuation cards.

14. MESSAGE: **** INCORRECT NUMBER OF INTEGER FIELDS IN THE ABOVE CARD ****

CAUSE: The statement specified has an incorrect number of fields containing numbers without decimal points.

UCARDS ACTION: The design program will not be executed, but the error scan continues.

USER ACTION: Check the statement format against the format detailed in Chapter 2. Correct and resubmit the design program to UCARDS.

15. MESSAGE: **** INCORRECT NUMBER OF NON-INTEGER FIELDS IN THE ABOVE CARD ****

CAUSE: The statement specified has an incorrect number of fields containing numbers with decimal points.

UCARDS ACTION: The design program will not be executed, but the error scan continues.

USER ACTION: Check the statement against the format detailed in Chapter 2. Correct and resubmit the design program to UCARDS.

16. MESSAGE: **** PLOT OPTION NOT SPECIFIED. IT HAS BEEN TURNED ON ****

CAUSE: No DRAFT OPTION/ statement appears in the design program.

UCARDS ACTION: UCARDS assumes drafting is desired even if failures occur during routing.

USER ACTION: None.

17. MESSAGE: **** COMPONENT TYPE IS NOT EXPLICITLY DEFINED AND ITS

TYPE NAME **** DOES NOT APPEAR IN A DESCRIBE STATEMENT ****

CAUSE: During component definition for Automatic placement, the Describe Feature was used. The statement specified contains a Describe label as detailed in Chapter 2, but no DESCRIBE statement appears bearing that label.

UCARDS ACTION: The design program will not be executed, but the error scan continues.

USER ACTION: Refer to Chapter 2 and write a correct DESCRIBE statement bearing the proper label. Resubmit the design program to UCARDS.

18. MESSAGE: **** GRID DIMENSIONS NOT SPECIFIED ****

CAUSE: Absolute Placement has been requested but no GRID SIZE/ statement appears in the design program.

UCARDS ACTION: Execution of the design program stops.

USER ACTION: Refer to Chapter 2 and write a correct GRID SIZE/ statement and resubmit the design program to UCARDS.

19. MESSAGE: **** BOARD TYPE NOT SPECIFIED ****

CAUSE: None of the statements BOARD TYPE/, FRAME/, and IOSTRIP/ appears in the design program.

UCARDS ACTION: Execution of the design program stops.

USER ACTION: Refer to Chapter 2 and write the correct statement or statements. Resubmit the design program to UCARDS.

20. MESSAGE: **** I/O SIZE NOT SPECIFIED ****

CAUSE: No IO HEIGHT/ statement appears in the design program.

UCARDS ACTION: Execution of the design program stops.

USER ACTION: Refer to Chapter 2 and write a correct IO HEIGHT statement. Resubmit the design program to UCARDS.

21. MESSAGE: **** PLACEMENT DIMENSIONS NOT SPECIFIED ****

CAUSE: No DIMENSION/ statement appears in the design program in which automatic placement was requested.

UCARDS ACTION: The design program is not executed.

USER ACTION: Refer to Chapter 2 and write the correct DIMENSION/ statement. Resubmit the design program to UCARDS.

22. MESSAGE: **** DEFINITION CANNOT TAKE PLACE UNTIL THE GRID SIZE HAS BEEN SPECIFIED ****

CAUSE: The statement GRID SIZE/ should appear before the statement DEFINE/ in the design program.

UCARDS ACTION: The design program will not be executed.

USER ACTION: Correct the order of the statements and resubmit the design program to UCARDS.

APPENDIX 1

SUGGESTED PROCEDURES

The following pages contain a flow chart of the steps one should follow when writing the design program. The following legend interprets the symbols in the flow chart.

LEGEND

Connecting block - identifies point where flow is continued from a previous page.

Connecting block - identifies point where flow will be continued on a following page.

Decision block - represents a decision point requiring a choice between two or more paths.

Processing block - if the rectangle contains a UCARDS statement or word in capital letters, it means "write the necessary statements of the form noted in the block."

Otherwise the literal instructions in the block are to be carried out.

APPENDIX 2

EXAMPLES OF DESIGN PROGRAMS

TITLE/ TEST CASE
 FILE/ 10
 GRID SIZE/ 28, 30
 FAILURE LIMIT/ 99
 BOARD TYPE/ 6
 IO HEIGHT/ .375
 CELL SIZE/ .1
 SCALE/ 2.
 PLOT OPTION/ ON
 PUNCH OPTION/ ON
 PREDEFINE/
 VOID/ TB, 2, 2, 2, 30, 5, 30
 DEFINE/
 TWO SIDED IO/ TS, T, 1, 2, 3, 4, 5, 28, 5, 28, 10, 28, 15, 28, 20, 28, 25
 DIODE/ CR1, T, 2, 6, 14, 5, 14, 9
 RESISTOR/ R1, T, 6, 3, 14, 12, 18, 12
 CAPACITOR/ C1, T, 6, 7, 12, 12, 8, 12
 TRANSISTOR/ Q1, T, 8, 7, 1, 12, 18, 13, 17, 14, 18
 RESISTOR/ R2, T, 8, 3, 16, 13, 20, 13
 RESISTOR/ R3, T, 8, 4, 16, 17, 20, 17
 RESISTOR/ R4, T, 1, 5, 16, 21, 20, 21
 ROUTE/
 DRAFT/
 MACHINE/ GERBER
 PUNCH/
 MACHINE/ MOOG
 EXIT/

Example 1: Design program using Absolute Placement

REMARK/ EXAMPLE OF USE OF UPDATE
FILE/ 9
TITLE/ UPDATE OF BOARD 101
SEARCH/ 10
UPDATE/
LABEL/ .2, 2.675, .15, H, CIRCUIT NO. 101
DRAFT/
SCALE/ 2.
MACHINE/ GERBER
EXIT/

Example 2: Design Program using the Update Feature

TITLE/ P19355
SEARCH/ 3
FILE/ 3
UPDATE/
DELETE HOLE/ 10, 15, 8, 17
DELETE PATH/ T, 5, 3, 5, 20, T, 10, 5, 20, 5
INSERT HOLE/ 6, 7
INSERT PATH/ T, 21., 6, 7, 6, 10
DRAFT/
LABEL/ 1.5, 3.5, .1, H, DECADE COUNTER
SCALE/ 2.
MACHINE/ GERBER
PUNCH/
MACHINE/ PRATTW
OFFSET/ 1,3
EXIT/ END OF UPDATE DESIGN

Example 3: Design Program Using Update Feature

```

REMARK / EXAMPLE OF STACKED DESIGN PROGRAMS
TITLE / TEST CASE
GRID SIZE / 28, 30
FAILURE LIMIT / 99
BOARD TYPE / 6
IO HEIGHT / .375
CELL SIZE / .1
SCALE / 2.
DRAFT OPTION / ON
PUNCH OPTION / ON
PREDEFINE /
VOID / TB, 2, 2, 10, 2, 2, 10
DEFINE /
REMARK / ABSOLUTE COMPONENT DEFINITION
TWO SIDED IO / TS, T, 1, 2, 3, 4, 5, 28, 5, 28, 10, 28, 15, 28, 20, 28, 25
DIODE / CR1, T, 2, 6, 14, 5, 14, 9
RESISTOR / R1, T, 6, 3, 14, 12, 18, 12
CAPACITOR / C1, T, 6, 7, 12, 12, 8, 12
TRANSISTOR / Q1, T, 8, 7, 1, 12, 18, 13, 17, 14, 18
RESISTOR / R4, T, 1, 5, 16, 21, 20, 21
ROUTE /
DRAFT /
MACHINE / GERBER
PUNCH /
MACHINE / MOOG
NEW CASE /
TITLE / PLACEMENT - TEST CASE
DIMENSION / 3.0, 3.0
MARGINS / .1, .1, .1, .2
BOARD TYPE / 6
LAND DIAMETER / .1
SCALE / 2.
IO HEIGHT / .375
REMARK / COMPONENT DEFINITION FOR AUTOMATIC PLACEMENT
PLACE /
REMARK / EXAMPLE OF USE OF DESCRIBE FEATURE
RESISTOR / R1, T, 2, 6, $2
CAPACITOR / C1, T, 8, 3, $3
CAPACITOR / C2, T, 3, 19, $3
CAPACITOR / C5, T, 19, 5, $3
DIODE / CR1, T, 11, 12, $3
DIODE / CR2, T, 18, 4, $3
TRANSISTOR / Q1, T, 8, 7, 9, $4
REMARK / EXAMPLE OF USE OF CONTINUATION CARDS
TWO SIDED IO / TS, T, 1, 2, 3, 4, 5, 12, 19, .75, 0., 1.0, 0., 1.25, 0., 1.5, CONT
., 1.75, 0., 2.0, 0., 2.25, 0.
DESCRIBE / $2, .3, .1, 0., .12, 0., -.12
DESCRIBE / $3, .15, .05, 0., .07, 0., -.07
DESCRIBE / $4, .25, .25, 0., -.12, .12, 0., 0., .12
ROUTE /
DRAFT /
PUNCH /
MACHINE / PRATTW
EXIT /

```

Example 4

TITLE / PLACEMENT - TEST CASE
 DIMENSION / 3.0, 3.0
 MARGINS / .1, .1, .1, .2
 BOARD TYPE / 6
 LAND DIAMETER / .1
 SCALE / 2.
 IO HEIGHT / .375
 PLACE /
 REMARK / EXAMPLE OF USE OF DESCRIBE FEATURE
 RESISTOR / R1, T, 2, 6, \$2
 CAPACITOR / C1, T, 8, 3, \$3
 CAPACITOR / C2, T, 3, 19, \$3
 CAPACITOR / C5, T, 19, 5, \$3
 DIODE / CR1, T, 11, 12, \$3
 DIODE / CR2, T, 18, 4, \$3
 TRANSISTOR / Q1, T, 8, 7, 9, \$4
 REMARK / EXAMPLE OF USE OF CONTINUATION CARDS
 TWO SIDED IO / TS, T, 1, 0, 3, 4, 0, 12, 0, .75, 0., 1.0, 0., 1.25, 0., 1.5, CONT
 ., 1.75, 0., 2.0, 0., 2.25, 0.
 REMARK / EXAMPLE OF USE OF ARBITRARY NOD
 ARBITRARY NOD / 2, 5, 19
 DESCRIBE / \$2, .3, .1, 0., .12, 0., -.12
 DESCRIBE / \$3, .15, .05, 0., .07, 0., -.07
 DESCRIBE / \$4, .25, .25, 0., -.12, .12, 0., 0., .12
 ROUTE /
 DRAFT /
 PUNCH /
 MACHINE / NAWIDE
 EXIT /

```

TITLE / PLACEMENT - ROUTING TEST CASE
DIMENSION/ 4.0, 4.0
MARGINS / .1, .1, .1, .2
BOARD TYPE / 6
LAND DIAMETER / .1
SCALE / 2.
IO HEIGHT/ .375
PLACE /
RESISTOR / R1, T, 2, 6, $2
RESISTOR / R2, T, 6, 3, $2
RESISTOR / R3, T, 6, 7, $2
RESISTOR / R4, T, 8, 3, $2
RESISTOR / R5, T, 1, 9, $1
RESISTOR / R6, T, 9, 10, $2
RESISTOR / R7, T, 10, 19, $2
RESISTOR / R8, T, 11, 19, $2
RESISTOR / R9, T, 12, 13, $2
RESISTOR / R10, T, 13, 19, $2
RESISTOR / R11, T, 13, 14, $2
RESISTOR / R12, T, 1, 16, $1
RESISTOR / R13, T, 15, 19, $2
RESISTOR / R14, T, 16, 17, $2
RESISTOR / R15, T, 17, 5, $2
RESISTOR / R16, T, 18, 5, $2
CAPACITOR / C1, T, 8, 3, $3
CAPACITOR / C2, T, 3, 19, $3
CAPACITOR / C3, T, 10, 11, $3
CAPACITOR / C4, T, 15, 19, $3
CAPACITOR / C5, T, 19, 5, $3
CAPACITOR / C6, T, 17, 18, $3
DIODE / CR1, T, 11, 12, $3
DIODE / CR2, T, 18, 4, $3
TRANSISTOR / Q1, T, 8, 7, 9, $4
TRANSISTOR / Q2, T, 15, 14, 16, $4
DESCRIBE / $1, .5, .125, 0., .2, 0., -.2
DESCRIBE / $2, .3, .1, 0., .12, 0., -.12
DESCRIBE / $3, .15, .05, 0., .07, 0., -.07
DESCRIBE / $4, .25, .25, 0., -.12, .12, 0., 0., .12
END /
ROUTE /
DRAFT/
MACHINE/GERBER
EXIT/

```

Example 5: Design Program Using Automatic Placement

APPENDIX 3

EXAMPLES OF UCARDS OUTPUT

TERMINAL DEFINITIONS

NAME	PINS	LOCATION	SURFACE
R1	1	4, 4	T
R1	2	4, 6	T
R2	1	4, 13	T
R2	2	4, 15	T
R3	1	4, 31	T
R3	2	4, 33	T
R4	1	19, 13	T
R4	2	19, 15	T
R5	1	12, 3	T
R5	2	12, 7	T
R6	1	4, 22	T
R6	2	4, 24	T
R7	1	19, 22	T
R7	2	19, 24	T
R8	1	18, 22	T
R8	2	18, 24	T
R9	1	25, 24	T
R9	2	25, 22	T
R10	1	33, 31	T
R10	2	33, 33	T
R11	1	11, 31	T
R11	2	11, 33	T
R12	1	10, 3	T
R12	2	10, 7	T
R13	1	26, 31	T
R13	2	26, 33	T
R14	1	19, 6	T
R14	2	19, 4	T
R15	1	34, 4	T
R15	2	34, 6	T
R16	1	32, 4	T
R16	2	32, 6	T
C1	1	18, 13	T
C1	2	18, 14	T
C2	1	26, 13	T
C2	2	26, 15	T
C3	1	11, 22	T
C3	2	11, 24	T
C4	1	25, 31	T
C4	2	25, 32	T
C5	1	33, 22	T
C5	2	33, 24	T
C6	1	26, 4	T
C6	2	26, 6	T
CR1	1	26, 23	T
CR1	2	26, 24	T

Example 6:- Example of Terminal Definition List

DESIGN RESULTS - / PLACEMENT - ROUTING TEST CASE

BOARD SIZE - X DIRECTION 4.00
 Y DIRECTION 4.00

MARGINS - LEFT 0.10, RIGHT 0.10, TOP 0.10, BOTTOM 0.20

NUMBER OF I/O POINTS 7
 NUMBER OF MOVABLE COMPONENTS 26

COMPONENT LOCATIONS

COMP NUMBER	X POS	Y POS	NO. LUGS	X SIZE	Y SIZE
1	0.57	3.52	2	0.30	0.10
2	1.52	3.52	2	0.30	0.10
3	3.42	3.52	2	0.30	0.10
4	1.52	1.94	2	0.30	0.10
5	0.57	2.67	2	0.50	0.13
6	2.47	3.52	2	0.30	0.10
7	2.47	1.93	2	0.30	0.10
8	2.47	2.07	2	0.30	0.10
9	2.47	1.31	2	0.30	0.10
10	3.42	0.48	2	0.30	0.10
11	3.42	2.76	2	0.30	0.10
12	0.57	2.85	2	0.50	0.13
13	3.42	1.18	2	0.30	0.10
14	0.57	2.00	2	0.30	0.10
15	0.57	0.41	2	0.30	0.10
16	0.57	0.55	2	0.30	0.10
17	1.45	2.04	2	0.15	0.05
18	1.52	1.24	2	0.15	0.05
19	2.47	2.76	2	0.15	0.05
20	3.35	1.28	2	0.15	0.05
21	2.47	0.48	2	0.15	0.05
22	0.57	1.24	2	0.15	0.05
23	2.55	1.20	2	0.15	0.05
24	1.52	0.48	2	0.15	0.05
25	1.52	2.76	3	0.25	0.25
26	3.42	2.00	3	0.25	0.25

INPUT/OUTPUT LOCATIONS

I/O NUM	X POS	Y POS
1	0.75	0.0
2	1.00	0.0
3	1.25	0.0
4	1.50	0.0
5	1.75	0.0
6	2.00	0.0
7	2.25	0.0

Example 7: Example of Automatic Placement Results

THE FOLLOWING IS A LIST OF CONNECTIONS TO BE MADE

TS	1	R5	1
TS	1	R12	1
TS	2	R1	1
TS	3	R2	2
TS	3	R4	2
TS	3	C1	2
TS	3	C2	1
TS	4	CR2	2
TS	5	R15	2
TS	5	R16	2
TS	5	C5	2
TS	6	R9	1
TS	6	CR1	2
TS	7	R7	2
TS	7	R8	2
TS	7	R10	2
TS	7	R13	2
TS	7	C2	2
TS	7	C4	2
TS	7	C5	1
R1	2	R2	1
R1	2	R3	1
R3	2	Q1	2
R4	1	C1	1
R4	1	Q1	1
R5	2	R6	1
R5	2	Q1	3
R6	2	R7	1
R6	2	C3	1
R8	1	C3	2
R8	1	CR1	1
R9	2	R10	1
R9	2	R11	1
R11	2	Q2	2
R12	2	R14	1
R12	2	Q2	3
R13	1	C4	1
R13	1	Q2	1
R14	2	R15	1
R14	2	C6	1
R16	1	C6	2
R16	1	CR2	1

Example 8: Example of Connection List

7

After Definition (Top Side)

BOTTOM SIDE

```

*****
*
*
*   O O       O O       O O       O O   *
*
*
*
*
*
*   O   O       O       O O       O O   *
*
*   O   O       O       O O       O O   *
*
*
*
*
*
*
*
*
*
*   O O       O O       O O       O O   *
*
*   O O       O O       O O       O O   *
*
*
*
*
*
*
*
*
*
*   O O       O O       O O       O O   *
*
*   O O       O O       O O       O O   *
*
*
*
*
*
*
*
*
*
*
*****

```

STATUS AT END OF DEFINITION PHASE

Example 10: Printer Plot of Board Configuration

After Definition (Bottom Side)

PATH IDENTIFICATION NUMBER TABLE

NAME	PINS	LOCATION	SURF	PATHNO
R1	1	4, 4	T	2.00
R1	2	4, 6	T	21.00
R2	1	4, 13	T	21.00
R2	2	4, 15	T	3.00
R3	1	4, 31	T	3.00
R3	2	4, 33	T	23.00
R4	1	19, 13	T	23.00
R4	2	19, 15	T	3.00
R5	1	12, 3	T	1.00
R5	2	12, 7	T	26.00
R6	1	4, 22	T	26.00
R6	2	4, 24	T	27.00
R7	1	19, 22	T	27.00
R7	2	19, 24	T	27.00
R8	1	18, 22	T	29.00
R8	2	18, 24	T	29.00
R9	1	25, 24	T	29.00
R9	2	25, 22	T	31.00
R10	1	33, 31	T	31.00
R10	2	33, 33	T	31.00
R11	1	11, 31	T	31.00
R11	2	11, 33	T	33.00
R12	1	10, 3	T	1.00
R12	2	10, 7	T	34.00
R13	1	26, 31	T	34.00
R13	2	26, 33	T	34.00
R14	1	19, 6	T	34.00
R14	2	19, 4	T	38.00
R15	1	34, 4	T	38.00
R15	2	34, 6	T	38.00
R16	1	32, 4	T	39.00
R16	2	32, 6	T	39.00
C1	1	18, 13	T	39.00
C1	2	18, 14	T	3.00
C2	1	26, 13	T	3.00
C2	2	26, 15	T	3.00
C3	1	11, 22	T	3.00
C3	2	11, 24	T	29.00
C4	1	25, 31	T	29.00
C4	2	25, 32	T	29.00
C5	1	33, 22	T	29.00
C5	2	33, 24	T	29.00
C6	1	26, 4	T	38.00
C6	2	26, 6	T	39.00
CR1	1	26, 23	T	29.00
CR1	2	26, 24	T	29.00

Example 11: Path Identification Number Table

GERBER MOD 75 OUTPUT

PAGE# 1

N	G	X	Y	D	M
100	01	+00500	+00000	02	
101	54			12	
102	01	+03500	+00000	01	
103		+03500	+00500		
104		+04000	+00500		
105		+04000	+04500		
106		+00000	+ 4500		
107		+0000	+ 500		
108		+00500	+00500		
109		+00500	+00000		
110	54			15	
111	01			02	
112		+00650	+03450	02	
113		+01150	+03450	01	
114		+00150	+02950	02	
115		+00350	+02950	01	
116		+01450	+02850	02	
117		+03250	+02850	01	
118		+00650	+02750	02	
119		+01350	+02750	01	
120		+00350	+02650	02	
121		+00450	+02650	01	
122		+00450	+01850	02	
123		+00650	+01850	01	
124		+01250	+01450	02	
126		+02150	+00650	02	
127		+03050	+00650	01	

EXAMPLE OF NUMERICAL CONTROL TAPE LISTING.

THIS LISTING WAS OBTAINED BY
GIVING THE FOLLOWING UCARDS
STATEMENTS-

-
-
-
- DRAFT/
- MACHINE/GERBER
-
-
-

Example 12: Listing of Numerical Control Tape

APPENDIX 4

GLOSSARY OF TERMS

The definitions given in this glossary are not intended to be universal. Instead, the terms are only defined relative to their usage in this report.

Computer Aided Design - a general term referring to the act of using the computer to enhance a design process.

Compilation - the function performed by UCARDS that scans all input data for errors and establishes the steps in the design process.

Conductor Path - the path found by the UCARDS routing module joining two component pins on the circuit card, and which represent the position of a conductor on the fabricated board.

Connector Strip - the area of the circuit card containing the input and output pads. On a plug-in type card, the connector strip is the plug portion of the card.

Decimal Number - as used in this report, a number having a decimal point associated with it. (e.g. 7. or 8.5).

Design Program - the collection of UCARDS statements necessary to accomplish the computer aided design of a circuit board.

Designer - the person (draftsman, engineer, etc.) writing the design program.

Field - as used in this report, data appearing between commas in a UCARDS statement.

Grid System - the network of horizontal and vertical lines used by

UCARDS to locate components and conductor paths. (See Figure 4).

Grid Cell - one square in the grid system. (See Figure 4).

Integer Number - as used in this report, a number appearing with no decimal point. (e.g. 7 or 8).

IO Strip - Same as connector strip.

Land - the area around a hole or lead on a component that will eventually be plated at fabrication time to provide for solder joints between the component pins and the circuit card.

Module - a group of subroutines in UCARDS that work together to accomplish a given task in the design process.

Node - a point in an electrical circuit to which one or more component leads attach.

Numerical Control - the control and operation of machine tools via computer generated punched tapes or magnetic tapes.

Pad - same as land.

Photomaster - the positive or negative photograph used at fabrication time to expose the conductor paths and pads onto board stock for etching purposes.

Punched Control Tape - a paper or mylar tape containing punched EIA code used for controlling numerical controlled machine tools.

UCARDS - Union Carbide Automatic Routing and Design System.

UCARDS Statement - a statement written in the vocabulary and according to the formats described in Chapter 2.