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RESEARCH IN RADIATION MONITORING
SURVEY INSTRUMENTATION

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ABSTRACT

Two low-power solid-state prototype readout units were developed, an LED display and a LCD display. The display output was in a bar-graph format, covering four-decades of information, with 10-segments per decade. The displays accept a frequency input, which is standardly available from several portable radiation-survey instruments. Both readout units will operate on two D-cell batteries (3.0 Volt), with a typical current drain requirement of 0.3 MA for the LED display and 30 μ A for the LCD display.

A wide-range electrometer circuit was also developed. The circuit covers an input current range from 10^{-13} A to 10^{-8} A. The output signal is a pulse whose frequency is directly proportional to input current. The circuit requires no high-megohm resistors, and is autoranging. Several candidate input amplifiers were analyzed and evaluated for use with the electrometer circuit.

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CHAPTER I

INTRODUCTION

This report covers work performed for the Oak Ridge National Laboratory (ORNL) by the University of Tennessee (UTK) Electrical Engineering Department, Knoxville, Tennessee. The research was directed toward improvements in nuclear radiation portable survey instrumentation, for which ORNL was directly subcontracted to the U.S. Navy Department as part of an overall Radiac development program.

The research at UTK involved two definite TASKS in radiation monitoring survey instrumentation:

- (1) The first, and foremost, TASK involved development of a low-power solid state readout device, which would ultimately replace analog meters now in use on battery-operated survey instruments. The circuit requirements were that at least three decades of indication be provided, in a linear graphical output technique (usually referred to as a "bar-graph" display).
- (2) A subordinate TASK was to examine the possibility of a wide-range low-power solid-state electrometer circuit, suitable for hybrid microcircuit construction, that would measure input currents from ionization chambers in the range of 10^{-13} ampere to 10^{-8} ampere, without the use of high-megohm resistors, and without the requirement of switching between ranges. The output signal was to be compatible with the readout device of TASK 1.

To accomplish TASK I required investigation of available light-emitting-diodes (LED) and liquid crystal display (LCD) devices, and their interface with low power CMOS digital circuits. Details of the results are covered in the following Chapters.

CHAPTER II

SOLID STATE DISPLAY SYSTEMS - LED

The primary task of our research was to implement a low-power solid-state display system, which would accept an input signal proportional to radiation and display an output in incremental bar-graph form, using commercially available solid-state devices. At present one is limited (for low-power use) to either an LED display or a liquid crystal display. The discussion that follows is related to research performed using each of these devices, where the input signal to the display was a pulse train with frequency proportional to radiation level. This type of input was deemed more representative of both low-and high-range survey instruments available, or currently under development.

Advantages of LEDs

The commercial availability of a large variety of low-price light emitting diodes (LED), the wide temperature operating range (-55 to 100°C), and the reliability of the diodes have motivated the development of LED display systems to satisfy the requirements in this portable radiation-monitoring survey instrumentation project. The salient disadvantage of the LED as a display element is its large power requirement, typically 1000 times greater than the power needed for liquid crystal displays. However, if the LED is used in a "pointer" display system (Fig. 1) where a single LED is pulsed on for a few milliseconds (4 to 10 ms) at a low repetition rate (4 to 10 Hz), the power consumption can be sufficiently low to allow the use of the LED as the readout element in low-power survey instruments.

1	2	3	4	5	6	7	8	9
0	0	0	0	0	0	0	0	0

LED "BLINKS" WITH ON TIME MUCH LESS
THAN OFF TIME FOR -

1. LOW POWER CONSUMPTION
2. STIMULATION OF OPERATOR AWARENESS

Figure 1. LED Used as a Pointer.

The pointer type LED display system is discussed in this section. LED drivers are discussed and the digital logic developed for interfacing the drivers with the processed radiation signal is described.

LED Drivers

The basic LED driver circuit is shown in Figure 2. The LED should be supplied with a current pulse of amplitude and duration that changes little with power supply voltage and ambient temperature variations. The logic selects a specific LED by saturating a bipolar transistor chosen for low saturation voltage (typically less than 0.2V for $I_c < 10$ mA). The current-source pulse timing is determined either by a low-power astable multivibrator or a signal derived from a digital clock such as would usually already be in the display system for control of the logic interface.

A low-power LED driver timed by an astable multivibrator was developed and is shown in Figure 3. The entire circuit uses about 1 mW of power for a 9 mA LED current pulse, 7.2 ms duration, occurring at a 5 Hz repetition rate, when the battery voltage V_B is 2.8 volts. The temperature compensation due to V_{BE} tracking of Q_5 and Q_6 causes the LED current amplitude to change a

Figure 2. LED Current Driver Configuration.

negligible amount over the required temperature range of -40 to $+50^{\circ}\text{C}$. If the timing capacitors and resistors are selected for low temperature coefficients, the pulse duration and repetition rate will be sufficiently constant over the temperature range. The LED current pulse timing depends slightly on V_B , but the pulse amplitude is a strong function of V_B , typically changing about 40% for a 30% change in V_B .

The variation of the LED pulse characteristics with V_B in the circuit of Figure 3 can be minimized by replacing the Q_5 , Q_6 circuit with a current regulated LED that has recently become available. The device is the National Semiconductor NSL4944 that has a diffused-lens red LED in series with an IC

Q1, Q2, Q3, Q4, Q7, are 2N5962

Q5, Q6 are 2N4250

Figure 3. Low-power Astable Multivibrator and LED Driver.

current regulator all incapsulated in a plastic package. The LED current is fixed at about 13 mA over a voltage range of approximately 2.4 to 18 volts. We have demonstrated proper operation of the device in the pulsed mode; however, the diffused lens is not as bright in the pointer

configuration as other clear lens LED's we have used. The NSL4944 current regulated LED can easily be switched with astable or digital clock timing by low-saturation voltage ($V_{CE} < 0.2V$) bipolar transistors placed in series with the current path. This new current-regulated LED is the best candidate for use in the LED display system if it can be obtained in a brighter lens configuration.

We have also analytically and experimentally investigated the National Semiconductor low-cost LM3909 LED flasher-oscillator monolithic circuit for possible use in LED displays. The circuit has appeal because of its capability of operation over a battery voltage range of 1 to 5 volts. The low-voltage operation is accomplished by a novel circuit that uses the timing capacitor of an astable multivibrator for voltage multiplication to a level sufficient to exceed the GaAs LED forward threshold voltage even when the battery supply voltage is as low as about one volt. We do not, however, suggest using the flasher-oscillator as an LED driver for the following reasons: (1) A large value ($\approx 30\mu F$) external timing capacitor is necessary for the required low repetition rates, and (2) the LED current pulse amplitude and timing are very sensitive functions of the battery voltage.

The LED driver configuration we have developed for our LED multiplexed breadboard display is shown in Figure 4. The 4 Hz output of the logic clock IC13 provides the timing pulses for starting the monostable multivibrator IC15. The monostable output pulse is set to about an 8 msec width by the R15-C6 timing network. Thus, for about 8 msec the base-collector terminals of the transistor Q_1 (operating as a diode) are connected to ground through the resistor R3. The resistor R4 and one of the resistors R5, R6, R7, or R8 then fix the current amplitude in the LED of the appropriate decade selected by one of the IC16 transmission gates. The amplitude of the LED

current is held reasonably constant with temperature because of the base-emitter junction compensation of the Q1 - Q2 (3,4, or 5) circuit. However, the current amplitude is still a strong function of the battery voltage; this problem would be eliminated in future designs by using IC current regulated LED's.

Digital Logic Operation

A more detailed discussion of the logic for the LED display circuit of Figure 4 follows below.

The LED display logic interfaces the processed transducer signal with the LED array. In this case, the processed signal is a pulse frequency directly proportional to the transducer signal. The display logic performs the interface function in the following manner:

1. The input signal pulses are counted for 1 sec.
2. The count is transferred to a memory.
3. All the counting logic is reset.
4. A new count is accumulated while the previous count is displayed.

While performing this task, the logic must use low power. To meet the low power requirement, CMOS devices are used and only one LED is conducting at a time. This requires additional logic to determine the highest decade in which a count appears.

Timing. For the display to function properly, three timing signals are necessary. The signals are CLK, RESET 1, and RESET 2. CLK transfers the count and decade selection information into memory. RESET 1 initiates the counting logic while RESET 2 initiates the decade selection logic. These

timing signals are generated by the series connection of RC controlled monostables. First a 2048 Hz signal is generated by an RC controlled astable, IC 12 in Figure 4) then the 2048 Hz signal is divided by a binary counter, IC13 (Figure 4), to produce a 1 Hz signal. The falling edge of the 1Hz signal triggers the first of four series connected monostables. Each monostable triggers on the falling signal edge from the preceding one. The output of each monostable is a $5\mu\text{s}$ wide pulse. The first monostable generates the CLK signal, the second provides some delay to assure the transfer is complete before any logic is reset, the third generates RESET 1, and the fourth monostable generates RESET 2.

The transfer and reset all take place in approximately $20\mu\text{s}$. This is much less than the shortest period input to the display, therefore the transfer and reset can take place without stopping the input and there will be a very low probability of missing a count. Figure 5 illustrates the sequence of signals required for proper operation.

Counting. The counting of input pulses is performed by the ripple connection of 4 BCD counters as illustrated by IC1 and IC2 in Figure 4. Using this method we can count from 0 to (10^4-1) pulses in one sec, therefore frequencies from 0 to $(10^4-1)\text{Hz}$ can be measured in increments of 1Hz.

Multiplexing. The number of output lines can be reduced by multiplexing. Instead of using 39 output lines, one for each display LED and one for the driver, the multiplexed logic system of Figure 4 only requires 15, one for each decimal digit 0-9, one for overflow, and one for each of the 4 decades. The display flashes only the most significant decimal digit, therefore only the counter representing the highest decade in which a count appears need be placed into memory.

Figure 5. Signal Sequence for LED Operation.

Four, 4-to-1 multiplexers (IC6 and IC7 in Figure 4) were used to connect the proper counter with memory. Each multiplexer receives four bits from each counter. Additional logic, to be discussed later, generates multiplexer control signals S1 and S2.

Decade Selection and Multiplexer Select Logic. It is necessary to determine the highest decade in which a count appears so the proper decade in the display can be driven and so the proper counter can be multiplexed into memory. By connecting the first bit of each counter, except for the first counter, to the "SET" input of an RS flip flop, we can determine which decades have had a count. By using combinational logic the RS outputs are decoded to generate the control signals (MS1 and MS2) for the multiplexers. Table 1 below illustrates the function of the combinational logic.

The logic network for generating MS1 and MS2 is at the lower left hand section of Figure 4. The RS flip flops are in IC3.

RS1	RS2	RS3	MS1	MS2
0	0	0	0	0
1	0	0	1	0
1	1	0	0	1
1	1	1	1	1

Table 1. Truth table for MS1 and MS2.

The decade selection also uses the RS flip flops. First the conditions of the RS flip flops are stored in memory on the CLK pulse, then combinational logic generates a high level on the proper decade line.

Table 2 below illustrates the function of the combinational logic in generating the decade selection. The logic circuit is in the upper center section of Figure 4.

RS1	RS2	RS3	DS1	DS2	DS3	DS4
0	0	0	1	0	0	0
1	0	0	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

Table 2. Truth table for decade selection.

Overflow Indication. When a count of 10,000 or greater occurs, a JK flip-flop (IC5, Fig.4) is set. This indicates the count has exceeded the range of the display. The output of the JK FF is stored into memory and used to inhibit any count from reaching the display and also used to light the 10,000+ LED.

Memory. The counter memory is provided by a 4 bit latch on a CMOS 4514 chip. The decade selection and overflow memory is provided by 4 D type latches. The input to these devices is latched to the output on the CLK pulse and does not change until the next CLK pulse. IC8 and IC4 in Figure 4 are the memory devices.

In addition to the 4 bit latch on the CMOS 4514 device (IC8 in Figure 1), there is a 4-to-16 decoder. Therefore, the count is immediately decoded when latched into memory. This converts the 4-bit BCD count to a high-on-one line corresponding to the BCD input 0-to-9. At this point the logic function is complete; the proper decade and decimal digit have been selected. Next, these are used to light the appropriate display LED.

Display Section. The display section conveys the count information to the eye. The display is accurate to 10% of full scale; this is due to the fact that only the most significant decimal digit is displayed. For example, if the count was 234, the 200 LED would flash. The LED's are arranged in four decades with nine LED's in each decade plus the overflow in the fourth decade and the zero in the first decade. The LED array is illustrated on the right-hand side of Figure 4.

As can be seen in Figure 4, the output lines of the decoder connect to a bipolar switch. A $33k\Omega$ resistor in the base of the transistor assures saturation when a high level appears at the decoder output. The overflow line is connected to the bipolar switch with a $33k\Omega$ resistor. The overflow also goes to the INH input of the decoder; thus when an overflow occurs the outputs of the decoder go low keeping the switches to the decimal digits off. Only one switch is on at a time.

The LED's are in the collectors of the bipolar switches. With the exception of the zero and overflow, there are four LED's, all with the same decimal digit but in different decades. The LED's are connected to a current source for the proper decade. Each decade has a current source controlled by the decade-select logic through a transmission gate. When the decade-select line is high for a certain decade, the appropriate current source is connected to the drive signal. Only one current source is connected at a time. Each decade is connected to nine LED's plus the zero in the first and overflow in the last; for instance, the second decade has the 10, 20, 30, 40, 50, 60, 70, 80, 90 cathodes connected to the second-decade current source. This is illustrated in the upper right section of Figure 4.

If a count of 431 occurred, the first BCD counter would have a count of 1, a second counter would have a count of 3, and the third would have a 1, the fourth has no count. The first two RS flip flops are set, generating an $MS1=0$, and a $MS2=1$, which then multiplexes the third counter to the inputs of the four-bit latch on the CMOS 4514. When the CLK pulse occurs, the RS FF outputs are latched into memory, generating a high level on DS3 which connects the drive signal to the third-decade current source. Also, the count of 4 on the third counter is latched into the 4514 unit and decoded, causing the S4 line to go high, which turns on the switch at the anode of 90 LED's 4, 40, 400, and 4000. Since the third decade current source is on, a current path through LED 400 occurs. This is the correct operation of the LED display.

CHAPTER III

SOLID STATE DISPLAYS - LCD

In this chapter the construction and theory of operation for Liquid Crystal Display (LCD) devices will be presented, and an operating LCD system will be discussed.

Construction of LCD Devices

All types of liquid crystal displays have the same basic construction. There are two glass plates separated by a spacer, with the edges sealed and a filling hole left in the edge or in the back. This construction is shown in Figure 6.

Figure 6. Construction of LCD Devices.

The space between the plates is filled with a liquid crystal material and the filling hole then sealed. The glass plates have patterns of tin or indium oxide deposited on them in the shape of the desired display. If the display is to be operated in the reflection mode, the back electrode is a mirror of evaporated metal such as aluminum. For operation in the transmission mode, both electrodes are transparent. This allows the display to be lit from the back with the light shining through to the viewer. These two forms of transmission are shown in Figure 7 (Ref. T3).

Figure 7. Lighting Methods for Liquid Crystal Displays.

The spacer for the display is a high quality controlled precision spacer with a width of between 10 and 20 μm . The seal quality strongly influences the display lifetime. The material must not react with the liquid crystal fluid and must have a temperature coefficient compatible with the other materials in the display. The practice now is to use glass frit sealants, as they fit these requirements best. Other sealants used include thermo setting resins, glass to metal seals, and thermoplastic materials (Refs. 6, 8, 9, 13).

Types of LCD Devices

There are two important types of LCDs commercially available, (1) dynamic scattering, and (2) twisted nematic displays. To understand the differences between these types of displays, the basic chemistry of liquid crystal materials must be considered.

A liquid crystal material is a liquid which has the chemical structure and polar properties which enable the molecules within the liquid to align in the same direction. This behavior is caused by long rod shaped organic molecules which contain dipole groups. The dipoles align the molecules in a certain direction which is the property making the liquid crystal useful in display technology.

In the dynamic scattering display a liquid which has a negative dielectric anisotropy is used. In this material, the molecules of the liquid crystal will align perpendicularly to an electric field. When there is no field applied to the dynamic scattering LCD, the display appears optically transparent because the light is passing through the aligned molecules. An electric field causes conductive ionic dopants to disturb the alignment of the molecules and set up a hydrodynamic turbulence. This turbulent

layer contains large numbers of refracting boundaries giving it the appearance of frosted glass. This is illustrated below in Figure 8.

Figure 8. Dynamic Scattering LCD.

In a twisted nematic display, a liquid which has a positive dielectric anisotropy is used. This means that the molecules of the liquid crystal are aligned parallel to the electric field. Two different mechanisms are used to make the twisted nematic display work. First the surface of the plates adjacent to the liquid are treated so that the molecules of the liquid crystals align themselves with the plates. This is done by either rubbing the surfaces vigorously in one direction with cotton wool or lens tissue, or by the oblique evaporation of SiO or similar materials in a high vacuum. The plates are then assembled with the aligned directions

in an orthogonal relationship. The second mechanism involves the use of polarizers to allow only light twisted by the molecules of the liquid crystals to pass through the display. This is done by using polarizers which are also twisted by 90° . This is demonstrated by the series of drawings, in Figure 9.

Figure 9. The Twisted Nematic LCD .

In Figure 9(a), the first polarizer admits only polarized light. The liquid crystal then twists the light because the molecules line up with the etching on the two plates which twists the light 90° . The Figure 9(b) polarizer then admits this light since the light and the last polarizer are twisted 90° with respect to the original polarized light. In Figure 9(b) an electric field is applied to the plates which aligns all the molecules parallel to the field despite the etching of the plates. This causes the light to pass through the liquid crystal without being twisted. This light is then blocked by the last polarizer, since the light is not polarized in the same direction as the polarizer (Refs. 2, 3, 6, 7, 8).

LCD Drivers

To preserve the lifetime of a liquid crystal display it must be driven in a special way. For a liquid crystal to function, an electric field must be established between the electrodes of the display. However, a dc voltage can cause electrolysis in the liquid crystal. Although most liquid crystal materials have high resistivity, there may be some impurities in the liquid, such as water. These impurities may react with the anode to make the LCD inoperable.

It is therefore necessary to drive the LCD with an ac signal. This signal frequency should be in a range of about 20- 400 HZ, depending on the type of liquid crystal material used. By constantly switching polarities, the ac drive prevents electrolysis; however, any dc voltage component contaminating the ac signal must not exceed a value of about 20 mV.

The ac drive can be implemented by impressing a square wave of voltage on one electrode and a square wave 180° out of phase on the opposite electrode. This causes the liquid crystal material to always see a voltage of

twice the peak-to-peak voltage of the square wave. When a segment is not addressed, the same square wave is fed into both electrodes, causing the liquid crystal to see zero net voltages, as shown by Figure 10.

Back Electrode Wave form

Front Electrode Wave form - Turned on

Front Electrode Wave form - Turned off

Signal Seen By Turned on LCD Segment

Figure 10. AC Drive for the LCD.

In a direct drive implementation, exclusive OR gates are used to drive the segments as shown in Figure 11.

Figure 11. Direct Exclusive-OR Drive for an LCD

In this implementation a high signal on one input of the exclusive OR gate causes the output to be the inverse of the other input square wave. By using a common signal to one input of each gate and the backplane of

the display, it is possible to feed the same signal, or a 180° phase shifted signal, to the front segment as is seen at the backplane electrode.

In a multiplexing scheme using liquid crystals there are some serious disadvantages. A liquid crystal is fed by an rms voltage which means that in a time division multiplexing scheme, the number of segments which can be scanned is limited. In other words, as the number of segments scanned is increased, the time which a signal is present at a particular segment is reduced over a repetition cycle. This reduces the rms voltage seen by a segment. As the number of segments scanned is increased, the rms voltage across the segments will be reduced below V_{Tn} , the voltage necessary to turn on a segment. The situation is further complicated by the fact that V_{Tn} is a function of temperature. This means that the display may work at room temperature, but as the temperature is decreased, V_{Tn} will increase and the segments will not get enough voltage to turn them on.

Time division multiplexing is not the only means of multiplexing the liquid crystal displays, but other methods have similar drawbacks. One other method investigated was the matrix address multiplexing scheme.

To multiplex a four-decade display, fifteen lines are brought out, as opposed to 42 lines for a direct driven implementation. In the matrix addressed multiplexing, the "ones" from all four decades are connected as well as the "twos", "threes" etc. This makes a total of nine less lines brought out. Then there is one line for zero, one line for 10,000 at the top of the fourth decade, and four lines for the backplanes. Information as to which decade is on is conveyed by switching a square-wave into the active decade backplane and a dc voltage of half the peak-to-peak square wave voltage, into the inactive decade backplanes. This causes the active segment to see twice the square-wave voltage, while the inactive

segments see only the square-wave voltage. The threshold voltage, V_{th} , must be around 1 1/2 times the RMS voltage of the input square wave so that it is bracketed by the rms voltage of the input square wave and twice that voltage. The waveforms in this scheme are shown in Figure 12.

Figure 12. Drive Waveforms in a Matrix Addressed Multiplexing Scheme.

An important disadvantage of the matrix addressed multiplexing scheme is that V_{th} varies with the temperature and will drift out of the narrow range of voltages necessary for proper performance.

There are other multiplexing methods which use square-waves as inputs to the backplanes and segments which have appropriate phase relationships. These methods accomplish much the same as the matrix addressed technique described above and may be found in the references (Refs. 1, 3, 8, 11).

LCD Power And Temperature Requirements

In this section the twisted nematic type display will be the only type liquid crystal display discussed because it is most easily implemented in a low-power display configuration.

The low-power requirements of the liquid crystal display are one of its most desirable features. The low-power operation arises from two basic properties of the twisted nematic display. First, the nematic liquid crystal material is almost nonconductive. This means that very low current will flow through the material in the display. This is in contrast to the scattering display in which a current must flow through the material to cause scattering. For this to happen the material is doped with impurities to give it a higher conductivity. Secondly, a very low voltage is required across the twisted nematic display, since all that is needed is a voltage large enough to disrupt the fragile twisted alignment of the twisted nematic display. This is in contrast with the dynamic scattering type display in which the orderly arrangement of dipole molecules must not only be disturbed but disrupted to a larger extent so that light will be scattered by a random arrangement of these molecules.

The temperature requirements are basically a result of two characteristics of the liquid crystal material. First, for the liquid crystal to work it must be in the nematic range of the liquid crystal. At a lower temperature the material freezes into a solid, and at a higher temperature the liquid crystal material goes into the isotropic range. To illustrate this, the binary phase diagram of a liquid crystal material, MBBA (component A) and EBBA (component B), is shown in Figure 13.

Figure 13. Binary Phase Diagram of a Liquid Crystal Material.

For the liquid crystal to work properly, it must remain in the nematic region. It is clear from Figure 13 that different materials will have different nematic regions. Obtaining a material which will have a high isotropic-nematic phase change temperature is not a difficult problem and has been solved. However, obtaining a low nematic-solid phase change temperature has proved to be a more difficult problem. A liquid crystal material is basically an organic liquid, and as such it has obvious limitations on its freezing point. Materials are available which will go below -20°C , with hope that this temperature will soon be pushed to -30°C . This is the basic limitation of a liquid crystal material when used in low temperature applications.

The second characteristic which governs the use of liquid crystal materials in low temperature applications is the response time of the material. The LCD material has a turn-on time and a turn-off time given by (Ref. 7).

$$\text{Rise time, } T_A = n \left[\epsilon_0 \Delta \epsilon E^2 - \frac{k\pi^2}{d^2} \right]^{-1}, \quad (1)$$

$$\text{Fall time, } T_D = nd^2/k\pi^2, \quad (2)$$

where,

n = average viscosity
 E = electric field strength
 d = electrode spacing
 $\Delta \epsilon$ = dielectric anisotropy

$k = k_{11} + 1/4 (k_{33} - 2k_{22})$
 k_{11} = elastic constant for splay
 k_{22} = elastic constant for twist
 k_{33} = elastic constant for bend

These equations indicate that for a particular display the rise and fall times of the response depend directly on the average viscosity of the liquid. This average viscosity is a function of temperature. This means that as the temperature decreases, the viscosity of the liquid crystal material will increase, causing the response time of the display to increase. As the temperature of the liquid crystal material approaches its freezing point, the viscosity of the material begins to radically increase. This means that instead of a response time in milliseconds as at room temperature, a response time of seconds will be found near the freezing point of the material. In most applications a response of seconds is not fast enough for use in LCD devices. The limit on the low temperature at which the display can work is therefore seen to be a function of both the response time needed for a certain application and the freezing point of the liquid crystal material.

There is obviously no way in which a liquid crystal material with a freezing point of from -20°C to -30°C can be operated at -40°C to meet military specifications. The straight forward means of overcoming this limitation is to heat the liquid crystal material until it has the needed response time. The disadvantage of this is that the reason for using a liquid crystal is, in part, for its low power consumption and heating it consumes more power than is saved. Over an extended period, however, the liquid crystal would probably consume less power than other displays since the heater may not often be required. Therefore, the power consumed at these low temperatures would be less than the power saved at higher temperatures. The trade-offs between temperature, power consumption and response time are indicated in Figure 14 which shows the power required by a heater to maintain a certain response time, as a function of temperature.

Figure 14. Power Required to Heat an LCD Display.

This graph is only indicative of the type power requirements needed for a heater. Data was taken for this graph by setting a sweep generator to activate another segment of the thermometer type display every second for a one second response, every two seconds for a two-second response, etc. The temperature was then set at a fixed value and current in the heater was varied until the display responded to the signals. However, the heater used in this experiment heated only about half of the display, so that to heat up a whole four-decade display of the type used, more power would be required. This is offset though by the fact that very little insulation was used around the device to insure that all the heat flow from the heater went to the liquid crystal display. It is quite likely that the power consumptions of a full four-decade display could be substantially decreased from the data on the graph by proper insulation. (Refs. 4, 6, 7, 11, 13).

Circuit For An Operating LCD Display

The circuitry for our constructed liquid crystal bar-graph display consists of several stages, as indicated in Figure 15. All devices are CMOS.

The first stage is a combination of a 4047 multivibrator and a 4040 12-stage ripple counter/divider. These IC units along with an R-C diode differentiator circuit generate the timing and reset signals for the display logic, as well as a 32 Hertz signal to drive the liquid crystal display. The next part consists of four 4017 decade-counters. These are connected in a ripple fashion to count from zero to ten thousand. The next stage comprises ten 4043 S/R flip-flops. When the counters go high, a flip flop is set so that as each additional decade is counted an additional flip-flop is set. These S/R flip-flops are reset along with the counters

by a pulse every second. The next stage consists of seven 4174 hex, D-type latches. These are clocked by the one-Hertz square-wave signal so that the latches hold the same information for a one-second period. This is necessary to keep the display from going back to zero after every reset pulse. The following stage consists of ten 4030 quad, exclusive-OR gates. These have as inputs the output of the D-latches and a 32-Hertz signal. The exclusive-OR gates invert the 32-Hertz input when the D-latch input is high, and pass the signal unaltered when the D latches are low. This drives the LCD display by providing a 32 Hz square-wave signal on the segments which are either the same as the backplane squarewave, or inverted. This is the direct drive method discussed in the previous LCD driver section.

The actual constructed circuit of Figure 15 required approximately 30 microampere of current operating from 2 D-cells (3.0 volts), at 25°C. The circuit would work over a temperature range from +60°C to near -10°C. Operation at lower temperatures would necessitate a heater, as discussed previously.

CHAPTER IV

WIDE-RANGE ELECTROMETER INVESTIGATIONS

The design goal was to produce an electrometer that would cover five to six decades of input current, without the necessity of having a range selection switch. Such an electrometer could be connected to either a solid state detector or an ionization chamber to supply the input current. For example, using a nominal 100 cc chamber (at STP) a range of radiation intensity from 10 mR/Hr to 1000 R/Hr could be covered with an input current to the electrometer from 10^{-13} A to 10^{-8} A. With very low residual input current due to stray leakages, it is theoretically possible to extend the range to 10^{-14} A (1 mR/Hr) if a measurement at higher temperatures (50°C) was not required.

Several other design objectives required were the following:

- a) Accuracy better than 10% over the full temperature range from -40°C to +50°C.
- b) Low-power consumption to permit reasonable operating time on D-cell batteries.
- c) Inexpensive construction utilizing available Hybrid Thick Film technology.
- d) An output signal that would be compatible with either digital displays and/or the solid state analog displays under development.
- e) The elimination of all high-megohm resistors.
- f) Auto-ranging such that an operator scale-change is not required.

During the course of the investigation it was necessary to investigate several new circuit concepts in areas akin to the original scope of work. Several of these are explored in detail in the following summary.

A Proposed Circuit

The wide-range electrometer circuit developed during the one year period of the contract is shown conceptually in Figure 16. The input current is initially amplified by a factor of 10^4 , with the resulting current (10^{-9} to 10^{-4} amp) converted by standard techniques to a frequency output (1 Hz to 100 kHz). This type of output is directly compatible with either a direct digital or solid state analog (bar-graph) display.

It is possible to directly convert the input current to a frequency using a current integrator, however the demands on very low leakage in an input integrating capacitor and on charge-dumping circuits over the required temperature range was considered prohibitive.

A more detailed schematic is illustrated in Figure 17. In this circuit the positive input current I_{in} becomes the collector current of Q1A, due to the logarithmic feedback connection of Q1A-Q1B. Since the collector current of Q1B is constant and equal to I_1 , then from the basic equations for the base-emitter junction

$$V_{O1} = V_{BE}(Q1B) - V_{BE}(Q1A), \quad (1)$$

and since the collector current I_C is related to the reverse saturation current I_S and V_{BE} by

$$I_C = I_S [\exp(qV_{BE}/kT) - 1], \quad (2)$$

then combining Eqs. (1) and (2) gives

$$V_{O1} = \frac{kT}{q} \ln \frac{(I_{C1B} + I_{S1B}) I_{S1A}}{(I_{C1A} + I_{S1A}) I_{S1B}}. \quad (3)$$

Figure 16. Concept for a Wide-Range Electrometer.

Figure 17. Wide-Range Electrometer Details.

Using dual monolithic transistors for Q1 (and Q2), with dielectric isolation and small geometry, one can obtain the condition that

$$I_{S1A} = I_{S1B} = 10^{-15} \text{ A}, \quad (4)$$

hence Eq. (3) reduces to

$$V_{o1} \approx \frac{kT}{q} \ln \left(\frac{I_{C1B}}{I_{C1A}} \right) = \frac{kT}{q} \ln \left(\frac{I_1}{I_{in}} \right). \quad (5)$$

The voltage V_{o1} is applied to the input of Q2A, hence the result is

$$V_{o1} = V_{BE} (Q2A) - V_{BE} (Q2B). \quad (6)$$

Using Eq. (2), and Eq. (5), with similar results as in Eq. (4) leads to

$$\frac{kT}{q} \ln \left(\frac{I_1}{I_{in}} \right) = \frac{kT}{q} \ln \left(\frac{I_2}{I_o} \right), \quad (7)$$

or

$$I_o = I_{in} \left(\frac{I_2}{I_1} \right), \quad (8)$$

and since $I_1 = V_1/R_1$ and $I_2 = V_1/R_2$,

$$I_o = I_{in} \left(\frac{R_1}{R_2} \right). \quad (9)$$

Thus the relative stability of the reference voltage V_1 is unimportant. If the ratio of R_1 to R_2 is equal to 10^4 , we have therefore multiplied the input current by a current gain of 10^4 .

The current I_o is now utilized as the input current to a current-to-frequency conversion circuit, consisting of A3, IC1, IC2 and Q3. The amplifier A3 and C comprise a current integrator with an output change equal to (Q3A is initially non-conducting)

$$\Delta V_{02} = (I_0/C) t_1 . \quad (10)$$

The output voltage V_{02} will rise until the threshold voltage of the Schmitt comparator IC1 is attained. Thus, the comparator will furnish an output trigger pulse to the monostable circuit IC2. The output of the monostable is a positive pulse of width T , which turns-off Q3B, and thereby turns-on the current switch Q3A. Hence, the current I_{REF} [$I_{REF} > I_{0(max)}$] will be supplied to the integrator, with the result that the output of A3 now ramps downward for a time of T seconds, or

$$\Delta V_{02}' = [(I_{REF} - I_0)/C] T . \quad (11)$$

But, $\Delta V_{02} = \Delta V_{02}'$, or from Eqs. (10) and (11),

$$\text{Frequency output} = \frac{1}{(t_1 + T)} = I_0 \left(\frac{1}{I_{REF} T} \right), \quad (12)$$

or from Eq. (9), the final result is

$$\text{Frequency output} = I_{in} \left[\frac{R1/R2}{I_{REF} T} \right] . \quad (13)$$

It is significant to notice that the stability of the integrating capacitor C is not important (it must, however, be a low-leakage type), nor is the absolute stability of either resistors $R1$ or $R2$ (only the ratio is important), nor the threshold voltage of IC1. The absolute stability of both I_{REF} and the pulse width T are important.

Significant sources of error, in addition to changes in I_{REF} or T , would be primarily input leakage current for A1, and leakage in capacitor C . Further, input leakage current of A3 and reverse-bias current for Q3A should be less than 10^{-10} amp for better than 10% accuracy of measurement. Also,

the input currents for op-amps A2A and A2B should be considerably smaller than I_1 or I_2 , respectively. This latter requirement is not a stringent condition with present-day op-amps.

Final Wide-Range Electrometer Circuit

A complete schematic of the wide-range electrometer is shown in Figure 18. Here, the logarithmic transistor pair Q1 is a 2N4044 transistor, constructed by a dielectrically-isolated monolithic technique. The reverse-saturation current I_s is typically 1×10^{-15} amp for this transistor. Similarly, Q2 is a monolithic pair, MAT-01, having a larger geometry than the 2N4044, and therefore better logarithmic tracking at the higher currents of I_0 . The A2 and A3 op-amps are TL062 dual monolithic units, which have ion-implanted JFET inputs for low input leakage current [typically the input currents are below 10 pA (10×10^{-12} A)], and also have a total operating supply current less than 150 microamps for each op-amp. The input current gain of 10^4 is achieved by resistors R1 and R2 of 20 megohm and 2K-ohm, respectively. Thus, with a voltage drop across each resistor of 1-volt (V_1 - V_2), the collector currents for Q1B and Q2A are 50 nA and 0.5 mA, respectively.

The reference current I_{REF} is approximately 0.2 mA, achieved by the constant current reference circuitry of Q7, R5, A3B, Z1, and R6. Effectively, a constant current of 0.2 mA is maintained by the precision band-gap reference voltage of Z1 (1.22V) dropped across resistor R5. Slight adjustments of the output frequency can be made by trimming the value of R5B.

The precision monostable circuit IC2 is a CD4047 CMOS circuit, with the pulse width controlled by the value of R7 and C3. The pulse width is

Figure 18. Schematic of Wide-Range Electrometer.

exceptionally stable against both temperature and power supply variations. The Schmitt comparator IC1 utilizes one section of a quad CMOS Schmitt Nand logic circuit, the MC14093B.

With the connections shown for IC2, if the input current to the current-to-frequency circuitry (I_0) exceeds the value of reset current I_{REF} , then IC2 will function as an astable circuit, with an output frequency of approximately 140 kHz, thereby giving a fail-safe full-scale radiation display. If the output of A3A should attempt to latch at a negative voltage (V_{02}), then the comparator A4 would function, providing a re-charge current of 0.5 MA to bring V_{02} back positive. Under normal operation, the comparator output of A4 is positive, and the current switch Q5 is not conducting.

The reference voltages V1 and V2 for the electrometer are obtained with the simple power-supply of Q8 and references Z2 and Z3.

The entire circuit is designed to operate with power supply voltages ($V+$ and $V-$) between $\pm 4V$ and $\pm 8V$ with a nominal value of $\pm 6V$. The total circuit current drain varies somewhat with the output frequency, with a typical positive supply current of 1.6 MA and a negative supply current of 1.1 MA (at $\pm 6V$) for output frequencies below 10 kHz, with the positive current increasing to 2.1 MA at maximum output frequency of 140 kHz.

In Figure 19 is shown measured data for the characteristics of the current-to-frequency conversion, for output frequency versus input voltage V_{01} . The slope of the curve is the expected theoretical value of -60mv/decade. As stated previously, values of I_0 from $10^{-11}A$ to $10^{-4}A$ would correspond to input currents from $10^{-15}A$ to $10^{-8}A$.

Development of the wide-range electrometer is continuing at ORNL, with further tests and refinements anticipated.

Figure 19. Graph of Output Frequency Versus Input Voltage V_{O1} .

Circuits Suitable For Input Amplifier A1

The most critical part of the wide-range electrometer circuit of Figure 18 is the input dc amplifier, A1. This amplifier must have very low input leakage current ($<10^{-14}$ A), have low offset voltage, be capable of low-power operation, have only one dominant open-loop pole, and be easily and inexpensively constructed with hybrid IC techniques.

We investigated several candidate designs, and experimentally evaluated each of them during the course of the one-year contract. There were three basic designs that could readily be constructed, (1) a bipolar transistor input design, (2) a JFET input design and (3) an MOSFET input design. Each of these, with appropriate experimentally observed characteristics, are detailed below.

The Bipolar Transistor Input Amplifier. The circuit for this amplifier was presented earlier in Quarterly Report No. 2 (ORNL/Sub/7200-2), and has been redesigned for an improved version as shown in Figure 20. Since the circuit is sensitive to stray capacitances at the emitters of the input transistors, it was necessary to implement the design onto a hybrid thick-film IC substrate, packaged in a T0-5 header, to evaluate the design. The entire circuit of Figure 20 was constructed on a 0.16 in. by 0.19 in. ceramic substrate using 5-mil conductors spaced 5-mils apart, and then mounted inside a 10-pin T0-5 header. The principal advantage of this circuit is that it will operate with power supply voltages down to ± 1.2 V, thus allowing operation directly from two D-cell batteries. The input base current for Q1A or Q1B is typically between 1 to 3×10^{-14} ampere, and decreases slightly as temperature increases. The entire circuit required typically 8 μ A supply current at ± 1.5 supply. The main disadvantage of a bipolar input are (1) the noise voltage increases as $1/I_C$, hence operation

$Q1 = Q2 = 2N4044$ (Intersil)
 $Q3 = MAT-01$
 $Q4 = MP5838$ (or $2N3956$)
 $Q5 = \text{Process 55}$ (NSC)
 $OA1 = \mu A776$ (or $CA3078$)

Figure 20. Bipolar Transistor Input Amplifier.

at collector currents of the order of picoamps results in a very noisy output amplifier and (2) the gain-bandwidth product varies directly with I_C , hence low collector currents results in a reduced frequency response for the amplifier. In Figure 21 the output small-signal pulse response of the constructed hybrid IC circuit is shown, for the amplifier connected in a non-inverting unity gain configuration. The output signal rise time (10-90%) was 9 μ sec, corresponding to a 40 kHz gain-bandwidth product. The output noise is quite high, as evidenced by the photograph, corresponding to a 15mV peak-to-peak amplitude.

The JFET Transistor Input Amplifier. The circuit for this amplifier was also presented earlier in Quarterly Report No. 2, and an improved schematic is illustrated in Figure 22. This circuit was constructed in breadboard form (labeled hereafter TF25) using discrete devices, and evaluated. In Figures 23 and 24 some of the characteristics are shown in comparison with a similar commercially available amplifier (AD515). In Figure 23 it is apparent that the total supply current for the TF25 amplifier is considerably lower, and more constant, than for the AD515 unit (the supply current is 32 μ A versus nominally 500 μ A for the AD515). However, reducing the supply current also lowers the slew-rate, as evidenced by Figure 23(b). In Figures 24(a) and (b) it is evident that the common-mode and power-supply rejection ratios (CMRR and PSRR, respectively) are improved over the AD515, for the particular JFET used in the breadboard. The indicated values of PSRR are 25,000/1 (84db) for positive supply variations, and 14,000/1 (83db) for negative supply variations. The CMRR is 30,000/1 (84db). Using three different AD832 units for Q1 of Figure 22 resulted in measured input leakage currents of 1.2, 1.8, and 1.0 $\times 10^{-14}$ amp. With the bootstrapped connection of Q2 the drain-gate and source-gate voltages are invariant,

(a) Output

(b) Input

Figure 21. Pulse Response of the Bipolar Transistor Input Amplifier, in a Unity-Gain Configuration, [50mv/div, 2 msec/div].

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Figure 23. Some Comparisons Between the JFET Amplifier TF 25, and the AD515 Amplifier.

Figure 24. Comparisons Between TF-25 and AD515 (continued).

even though the power supply voltages change. Hence, the input leakage currents did not change for variations in power supply voltages from $\pm 4V$ to $\pm 15V$.

The MOSFET Transistor Input Amplifier. This circuit is basically the same as that of the JFET amplifier of Figure 22, except Q1 is replaced by a dual monolithic P-Channel MOSFET, as shown in Figure 25. In addition, the substrate potential of the MOS device must be biased at a more positive voltage than either the source or drain, which is accomplished by diode D1. In Figures 26 and 27 are shown some of the characteristics of the MOSFET amplifier. Figure 26(a) indicates a power supply current of $60\mu A$ for power supply voltages of greater than $+4.5$ volts and more negative than -0.5 volts. The slew-rate of the circuit is approximately $0.2 V/\mu sec$, as indicated in Figure 26(b). Figure 27(a) indicates values of PSRR of $8000/1$ (73db) for both positive and negative power supply changes, and an exceptional CMRR of $100,000/1$ (100db).

Of course, the PSRR and CMRR depend upon the matching inherent in the input devices, for any type of input, whether bipolar, JFET, or MOSFET. The measured input leakage current for the breadboard MOSFET amplifier was less than $1 \times 10^{-15} A$.

Summary. In summary, comparisons among the three types of input amplifiers would indicate the following:

- (1). The lowest input leakage current is achieved by the MOSFET amplifier, although it will require a power-supply voltage greater than $+4.5$ volt for operation. Further, the MOSFET should have the worst input offset voltage drift with temperature, typically no better than $\pm 50\mu V/^{\circ}C$. The low-frequency noise should be lower than that of the Bipolar

Q1 = 3N190
 Q2 = PROCESS 55 (NSC)
 D1 = 1N914
 IC1 = LM4250
 IC2 = CA3096

Figure 25. The MOSFET Input Amplifier.

Figure 26. Characteristics of the MOSFET Input Amplifier.

Figure 27. MOSFET Amplifier (continued).

circuit, but much higher than that of the JFET circuit. Is a high radiation environment, the threshold voltage of the MOSFET devices will increase requiring a higher power supply voltage.

- (2). The ability to operate with power supply voltages as low as $\pm 1.2\text{V}$ is the only apparent good feature of the Bipolar design. The very high noise of this design drastically restricts its usage.
- (3). The JFET input amplifier would offer the best characteristics in a high radiation environment, since the pinch-off voltage would change very slightly. The equivalent noise voltage of this amplifier is the lowest of the three designs. The circuit will work with a power supply voltage as low as $+3.5\text{V}$, and should have an offset voltage drift with temperature less than $\pm 25\mu\text{V}/^\circ\text{C}$. Unfortunately, one could not expect input leakage currents below 1×10^{-14} amp.

Thus, for greatest sensitivity the MOSFET design must be utilized, but for input current measurements no lower than 10^{-12} amp, the JFET design offers overall better performance.

CHAPTER V

CONCLUSIONS AND RECOMMENDATIONS

The two major TASKS as outlined in Chapter I have been accomplished. Two low-power solid-state read-out devices were developed, an LED unit and a LCD unit. The display is in a bar-graph form, covering four decades of radiation. The current drain required from two D-cells (3.0 volt) was minimal, approximately 0.3 ma for the LED circuit and 30 μ A for the LCD circuit. Both read-out units were packaged at ORNL, and are to be evaluated by Navy personnel.

A wide-range autoranging electrometer covering an input current range from 10⁻¹³A to 10⁻⁸A was developed. The circuit has not been completely evaluated, however, and possibly needs additional refinement. The output of the electrometer is a frequency signal that is directly compatible with either of the solid-state read-out units.

We would recommend the LED read-out circuit be considered as the most promising currently of the two types, primarily because it can operate over the full required temperature range of -40°C to +50°C. The LCD unit is limited to a low temperature operation of near 0°C, unless a power-consuming heater is implemented into the LCD display. Further, it appears that the better LCD material for use at lower temperatures will require a much higher power-supply voltage (>9V) than the present material. Also, multiplexing of present LCD displays is not practicable, for operation over a wide temperature range.

If the solid-state bar-graph type display is to be used for a large number of instruments, the CMOS control electronics must be reduced to a workable LSI chip array. The prototype LED CMOS circuit required 17 IC chips

versus 33 IC chips for the LCD (not multiplexed) display. It is suggested that since the logic used is reasonably standard, it is feasible to consider a 2 or 3 chip set of mask-programmable arrays (Ref. 5). Utilizing a "Master Breadboard" approach would save on both initial prototype costs and on design turnaround time.

The wide-range electrometer circuit offers promise for use in both high-range and low-range Radiac instruments. This could achieve a cost reduction in instrument requirement and inventory by allowing one instrument to cover radiation survey requirements normally allocated to two instruments.

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