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Ernest O. Lawrence Radiation Laboratory

AN INTEGRAL DESIGN TECHNIQUE FOR WIDEBAND MULTISTAGE TRANSISTOR AMPLIFIERS

Berkeley, California
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Larry Scott

December 14, 1961
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ABSTRACT

Presented is a philosophy for designing wideband multistage transistor amplifiers. The amplifier is visualized as an integral unit, the interstage networks constituting the elements of the amplifier unit. By designing the amplifier as a unit and adjusting the overall response (gain and bandwidth) with the interstage time constants, an increase in gain-bandwidth product is realized over the iteratively designed amplifiers. The resulting increase in gain-bandwidth product results from absence of the bandwidth shrinkage factor for multistage amplifiers.

Formulas are derived for both a two- and three-transistor integrally designed wideband amplifier, in which shunt peaking networks are used for coupling. Experimental amplifiers were constructed following these formulas, and the observed performance agreed quite well with the calculations.
I. INTRODUCTION

A greater overall gain-bandwidth product for multistage amplifiers is realizable through a design procedure that characterizes the total amplifier rather than characterizing each stage separately. The design entails picturing the several stages of the amplifier as an integral unit and adjusting the individual time constants to obtain the desired overall response.

The increase in gain-bandwidth product will be shown to result from the absence of the bandwidth shrinkage factor in the calculation. Here the bandwidth shrinkage factor is the ratio of overall amplifier bandwidth to the interstage bandwidth of an iteratively designed amplifier. It is given by \( \frac{1}{(2^{1/N} - 1)^{\frac{1}{2}}} \), where \( N \) is the number of cascaded stages. Absence of the shrinkage factor is owing to an integral-unit design philosophy, rather than an iterative (i.e., identical-stages-cascaded) design. It would seem that the convenience of designing one stage and then cascading costs the designer a fraction of the attainable gain-bandwidth product of the multistage amplifier. The integral-unit philosophy is applied here to the design of both two- and three-transistor amplifiers utilizing shunt-peaked interstage networks. Shunt-peaking interstage networks are selected because of their relative simplicity and conservation of gain-bandwidth product when broadbanded. The gain-bandwidth product of a shunt-peaked interstage is equal to \( f_t \) of the transistor.

As shown in Appendix A, the current gain of a typical shunt-peaked interstage is of the form

\[
A_1 = H \frac{P + z}{P^2 + aP + b},
\]

where \( P = j\omega \), and \( H \) is a constant.
It is possible to factor the denominator polynomial into its two roots and set one of the factors equal to the numerator term \( P + z \), yielding:

\[
A_1 = \frac{H}{P + C} \cdot \frac{P + z}{P + C} = \frac{H}{P + C}.
\]

Now suppose that two such interstages are connected in series. The current gain would be

\[
A_I = \frac{H_1 H_2}{P^2 + a_1 P + b_1} \cdot \frac{P + z_1}{(P + z_1)(P + C_1)} \cdot \frac{P + z_2}{P^2 + a_2 P + b_2},
\]

If we let the first term be factored as before to yield

\[
A_I = \frac{H_1 H_2}{P^2 + a_1 P + b_1} \cdot \frac{P + z_1}{P + z_1} \cdot \frac{P + z_2}{P^2 + a_2 P + b_2},
\]

and let \( C_1 = z_2' \),

then \( A_I = \frac{H_1 H_2}{P^2 + a_2 P + b_2} \).

This current-gain expression shows that the bandwidth is determined only by the second interstage, and the gain by both interstage networks. The two roots of the denominator polynomial may be varied to obtain the shape of response desired, maximally flat magnitude, linear phase, and other results.

For three stages, the final form of the gain is

\[
A_I = \frac{H_1 H_2 H_3}{(P^2 + a_2 P + b_2)(P + C_3)}.
\]

To generalize on this scheme, assume a product of \( n \) shunt-peaked interstage terms

\[
A_I = \prod_{i=1}^{n} \frac{H_i (P + z_i)}{P^2 + a_i P + b_i},
\]
Table I. Table of symbols.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_c$</td>
<td>depletion-layer capacitance of the collector-base junction.</td>
</tr>
<tr>
<td>$r'_b$</td>
<td>extrinsic base resistance of transistor.</td>
</tr>
<tr>
<td>$r_e$</td>
<td>$\frac{kT}{q\bar{I}_e} = 0.026\ \text{volt}$, intrinsic emitter resistance, where $\bar{I}_e$ is the d.c. emitter current.</td>
</tr>
<tr>
<td>$R_L$</td>
<td>$(B_0 + 1) (r_e + R_e)$</td>
</tr>
<tr>
<td>$R_c$</td>
<td>external emitter resistance, unbypassed.</td>
</tr>
<tr>
<td>$R_I$</td>
<td>interstage resistance.</td>
</tr>
<tr>
<td>$L$</td>
<td>interstage inductance.</td>
</tr>
<tr>
<td>$\beta_0$</td>
<td>$\frac{a_0}{(1 - a_0)}$, or low-frequency current gain of a common emitter stage when the load is a short circuit.</td>
</tr>
<tr>
<td>$\omega_\beta$</td>
<td>frequency at which the common emitter current gain has dropped 3 db from $\beta_0$, with a short-circuit load.</td>
</tr>
<tr>
<td>$\omega_t$</td>
<td>$\omega_\beta \beta_0$.</td>
</tr>
<tr>
<td>$\omega_{3\text{ dB}}$</td>
<td>frequency at which the amplifier response is down 3 db from its low-frequency value.</td>
</tr>
<tr>
<td>$D$</td>
<td>$1 + \omega_t (C_c + C_{cb}) (R_L + r_e + R_e)$, a factor that indicates the degradation of bandwidth because of feedback through $C_c$ and $C_{cb}$.</td>
</tr>
</tbody>
</table>
By proper selection of the time constants this can take the form

\[ A_1 = \prod_{i=1}^{n} \frac{H_i}{P^n + a_n P^{n-1} + b_n P^{n-2} + \ldots + Y_n P + Z_n} , \]

which means that the response function for \( n \) stages will contain an \( n \)-th order polynomial in the denominator.

To determine the relative merit of this design, the resulting bandwidth, as determined by the \( n \)-th order denominator polynomial, is multiplied by the low-frequency gain, and this gain-bandwidth product is then compared to that obtained by cascading the same number of transistors in an iterative design. In the iterative design, all stages have the same bandwidth and a single time-constant form of response.

II. ANALYSIS OF INTEGRAL DESIGN

The band-edge frequency of an \( n \)-th order gain function is determined by the shape of the response; for our examples, a maximally flat magnitude response will be specified.

A. Two-Stage Amplifier

For the case of the two-stage amplifier, we have

\[ A_1 = \frac{H_1 H_2}{P^2 + a_2 P + b_2} , \]

as already stated, and

\[ P + z_2 = P + c_1 , \quad \text{or} \quad z_2 = c_1 ; \quad (2) \]

\[ (P + z_1)(P + c_1) = P^2 + a_1 P + b_1 , \quad (3) \]

or \( z_1 + c_1 = a_1 ; \quad z_1 c_1 = b_1 . \quad (4) \)

For maximally flat magnitude we require

\[ a_2^2 = 2b_2 , \quad \text{(5)} \]
and \[ \omega_3 \text{db} = \sqrt{b_2}. \] (6)

The low-frequency gain is expressed by
\[ A_1(0) = \frac{H_1 H_2}{b_2}, \] (7)

and
\[ A_1(0) \omega_3 \text{db} = \frac{H_1 H_2}{\sqrt{b_2}}. \] (8)

In terms of the circuit parameters, we have
\[ H_1 = \frac{\omega t(1)}{D_1}, \]
and
\[ H_2 = \frac{\omega t(2)}{D_2}. \]

and
\[ \omega_3 \text{db} = (b_2)^{1/2} = \left( \frac{\omega t(2)}{D_2} \left[ \frac{R_{1}(2) + R_{1} + r_{b}'}{L_{2}} \right] \right)^{1/2}. \] (9)

or
\[ A_1(0) = \left( \frac{\omega t(1)}{D_1} \times \frac{1}{\omega_3 \text{db}} \right) \left( \frac{\omega t(2)}{D_2} \times \frac{1}{\omega_3 \text{db}} \right), \] (10)

and
\[ A_1(0) \omega_3 \text{db} = \left( \frac{\omega t(1)}{D_1} \times \frac{\omega t(2)}{D_2} \right) \frac{1}{\omega_3 \text{db}}. \] (11)

B. Three-Stage Amplifier

In the case of the three-stage amplifier we have
\[ A_1 = \frac{H_1 H_2 H_3}{(P^2 + a_2 P + b_2)(P + C_3)}, \] (12)

and
\[ P + z_2 = P + C_1 \quad \text{or} \quad z_2 = C_1, \] (13)

and we have
\[ (P + z_1)(P + C_1) = P^2 + a_1 P + b_1. \]
and 

$$(P + z_3)(P + C_3) = P^2 + a_3P + b_3,$$

or

$$z_1 + C_1 = a_1, \quad (14)$$

$$z_1 C_1 = b_1, \quad (15)$$

and

$$z_3 + C_3 = a_3, \quad (16)$$

$$z_3 C_3 = b_3. \quad (17)$$

For a maximally flat magnitude, we require

$$a_2 = \sqrt{b_2}, \quad (18)$$

$$C_3 = a_2, \quad (19)$$

and $\omega_3 \text{db} = (b_2 C_3)^{1/3}. \quad (20)$

The low-frequency gain for three stages is then expressed

$$A_1(0) = \frac{H_1 H_2 H_3}{b_2 C_3}, \quad (21)$$

and

$$A_1(0) \omega_3 \text{db} = \frac{H_1 H_2 H_3}{(b_2 C_3)^{2/3}}. \quad (22)$$

In terms of transistor parameters, we have

$$H_1 = \frac{\omega t(1)}{D_1},$$

$$H_2 = \frac{\omega t(2)}{D_2},$$

and

$$H_3 = \frac{\omega t(3)}{D_3}. $$
We also have
\[ b_2 = \frac{\omega \beta(2)}{D_2} \left( \frac{R_{l(2)} + R_1 + r_b'}{L_2} \right), \]
\[ c_3 = \frac{\omega \beta(3)}{D_3} \left( \frac{R_{l(3)} R_1 + r_b'}{R_{l(3)}} \right), \]
and
\[ \omega_{3 \text{ db}} = (b_2 c_3)^{1/3}, \]
or
\[ A_1(0) = \left( \frac{\omega t(1)}{D_1} \frac{1}{\omega_{3 \text{ db}}} \right)^n \left( \frac{\omega t(2)}{D_2} \frac{1}{\omega_{3 \text{ db}}} \right)^n \left( \frac{\omega t(3)}{D_3} \frac{1}{\omega_{3 \text{ db}}} \right)^n, \]
\[ (23) \]
and
\[ A_1(0) \omega_{3 \text{ db}} = \left( \frac{\omega t(1)}{D_1} \frac{1}{\omega_{3 \text{ db}}} \right)^n \left( \frac{\omega t(2)}{D_2} \frac{1}{\omega_{3 \text{ db}}} \right)^n \left( \frac{\omega t(3)}{D_3} \frac{1}{\omega_{3 \text{ db}}} \right)^n. \]
\[ (24) \]

Generalizing, for \( n \) stages we apply the formula
\[ A_1(0) = \left( \frac{\omega t(i)}{D_i} \frac{1}{\omega_{3 \text{ db}}} \right)^n, \]
\[ (24A) \]

III. ANALYSIS OF ITERATIVE DESIGN

The gain and bandwidth of an iteratively designed amplifier may be derived as follows.

Where the typical interstage gain is
\[ a_i = \frac{K}{P + P_0}, \]
\[ (25) \]
and
\[ \omega_{3 \text{ db}} = P_0, \]
\[ a_i(0) \omega_{3 \text{ db}} = K, \text{ and } K = \frac{\omega_t}{D}. \]
\[ (26) \]

For \( n \) stages cascaded we have
\[ a_1 = \left( \frac{K}{P + P_0} \right)^n, \]
\[ (27) \]
and \( \omega_3 \text{db} = P_0 \cdot S \).

Where we have the shrinkage factor \( S = (2^{1/n} - 1)^{1/2} \),

we have \( a_I(0) = \left( \frac{K}{P_0} \right)^n = \left( \frac{\omega_t}{D \cdot \omega_3 \text{db}} \right)^n S^n \),

and

\[
a_I(0) \omega_3 \text{db} = \left( \frac{\omega_t}{D \cdot \omega_3 \text{db}} \right)^n \omega_3 \text{db} S^n.
\]

IV. COMPARATIVE THEORETICAL PERFORMANCE

By comparing integral equation (24A) and iterative equation (30),
it is seen that the gain of an n-transistor amplifier designed by the integral unit method is \( S^{-n} \) times the gain of the iteratively designed one, where both amplifiers have the same overall bandwidth, and where \( S \) is the shrinkage factor calculated for \( n \) cascaded stages. Table II shows the gain-increase factor for 2-, 3-, and 4-stage amplifiers, in which

\[
G_{\beta \omega, \text{iterative}} = G_{\beta \omega, \text{integral}} S^n
\]

for equal bandwidths.

If we reduce the amplifiers compared to a typical or equivalent inter-stage of each overall design, the difference between them is the exclusion of the shrinkage factor from the integrally designed amplifier interstage. This indicates an improvement in interstage broadbanding efficiency by the amount that the gain-bandwidth product of that stage is increased; namely, the shrinkage factor.

V. EXPERIMENTAL VERIFICATION

The procedures for integral designs, developed in detail in Appendices A and B, were used to design the two- and three-stage amplifiers shown in Figs. 1 and 2. Theoretical and experimental performance of the amplifiers is compared in Table III. The agreement shown is as close as experimental accuracy allows.
Table II. Gain increase factors for 2-, 3-, and 4-stage amplifiers.

<table>
<thead>
<tr>
<th>Stages (n)</th>
<th>S</th>
<th>$S^{-n}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.64</td>
<td>2.4</td>
</tr>
<tr>
<td>3</td>
<td>0.49</td>
<td>8.48</td>
</tr>
<tr>
<td>4</td>
<td>0.425</td>
<td>30.5</td>
</tr>
</tbody>
</table>

Table III. Calculated and measured performances of the amplifiers (Fig. 1 and 2) compared.

<table>
<thead>
<tr>
<th>n</th>
<th>Gain</th>
<th>Bandwidth</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Calculated</td>
<td>Measured</td>
</tr>
<tr>
<td>2</td>
<td>10.</td>
<td>10.</td>
</tr>
<tr>
<td>3</td>
<td>66.</td>
<td>66.</td>
</tr>
</tbody>
</table>
Fig. 1. Schematic of a two-stage integrally designed amplifier.
Fig. 2. Schematic of a three-stage integrally designed amplifier.
VI. CONCLUSION

The philosophy of integral design is a useful technique for circumventing the limitation of gain-bandwidth product for multistage amplifiers. A greater gain-bandwidth product results for the integral design of multistage amplifiers because the bandwidth shrinkage factor is eliminated. This factor is defined as the loss in attainable gain-bandwidth product that results from cascading identically (iteratively) designed stages. By eliminating this loss, an appreciable increase in gain can be realized (see Table II), which could result in the use of fewer transistors to realize the same gain-bandwidth as an iteratively designed amplifier.

Some practical difficulty is encountered with the design because the parameters of the transistors are not accurately known nor uniform from unit to unit. This difficulty can be reduced by more conservative design techniques, and by such devices as the external emitter resistance used in the three-transistor amplifier design. The improvement in gain-bandwidth product realized by this design technique more than offsets these difficulties.
ACKNOWLEDGMENTS

I would like to thank D. O. Pederson of the University of California at Berkeley for his help and encouragement in developing this design technique, and the Lawrence Radiation Laboratory Nuclear Instrumentation Development Group, especially Horace G. Jackson, for frequent discussions.
APPENDICES

A. The Integral Design of a Two-Transistor Shunt-Peaked Amplifier

The gain of a typical shunt-peaked interstage may be derived as follows, (see Fig. 3):

\[ A_i = \frac{i_L}{i_g} = -\frac{\omega_t}{D} \times \frac{P + R_i/L}{P^2 + \left(\frac{R_i + r_b'}{L} + \frac{\omega_\beta}{D}\right) P + \frac{\omega_\beta}{D} \left(\frac{R_i + r_b'}{L}\right)} \]  \hspace{1cm} (A-1)

where

\[ R_i = \beta_0 r_e, \]

\[ C_1 = \frac{1}{\omega_t r_e} + C_{te}, \]

\[ D = 1 + \omega_t (C_c + C_{cb})(R_L + r_e), \]

and

\[ \omega_t = \omega_\beta \beta_0, \text{ as stated in Table I}. \]

The condition for cancellation may be determined by dividing the denominator by the numerator to find:

\[ \frac{P + \frac{r_b'}{L}}{P + \frac{R_i}{L}} \times \frac{\frac{\omega_\beta}{D}}{P^2 + \left(\frac{R_i + r_b'}{L} + \frac{\omega_\beta}{D}\right) P + \frac{\omega_\beta}{D} \left(\frac{R_i + r_b'}{L}\right)} \]

\[ = \frac{P}{P^2 + (R_i/L) P + \frac{\omega_\beta}{D} \left(\frac{R_i}{L}\right) + \frac{R_i r_b'}{L^2}} \cdot \frac{\omega_\beta}{D} \left(\frac{R_i + r_b'}{L}\right) - \frac{R_i r_b'}{L^2} = 0. \]
Fig. 3. Typical shunt-peaked interstage network.
However, the denominator factors into

\[
\left( P + \frac{R_I}{L} \right) \left( P + \frac{r'_b}{L} + \frac{\omega}{D} \right),
\]  

provided that

\[
\frac{\omega}{D} \left[ \frac{R_I + r'_b}{L} \right] - \frac{R_I r'_b}{L^2} = 0,
\]

or if

\[
\frac{R_I}{L} = \frac{\omega}{D} \left[ \frac{R_I + r'_b}{r_b} \right].
\]  

An alternative way to make this division is as follows:

\[
\frac{R_I}{L} + P \left( \frac{\omega}{D} \left( \frac{R_I + r'_b}{L} \right) + \left( \frac{R_I + r'_b}{L} + \frac{\omega}{D} \right) P + P^2 \right)
\]

\[
\frac{\omega}{D} \left( \frac{R_I + r'_b}{R_I} \right) P \]

\[
\left[ \frac{R_I + r'_b}{L} - \frac{\omega}{D} \left( \frac{R_I + r'_b}{R_I} \right) \right] P + P^2
\]

\[
\frac{R_I}{L} P + P^2
\]

\[
\frac{r'_b}{L} - \frac{\omega}{D} \left( \frac{R_I + r'_b}{R_I} \right) = 0.
\]

However, the denominator factors into

\[
\left[ P + \frac{R_I}{L} \right] \left[ P + \frac{\omega}{D} \left( \frac{R_I + R_I + r'_b}{R_I} \right) \right],
\]  

provided that

\[
\frac{r'_b}{L} - \frac{\omega}{D} \left( \frac{R_I + r'_b}{R_I} \right) = 0,
\]
yields the same result as Eq. (A-3). We also see by comparison that if Eq. (A-3) or (A-5) is satisfied, Eq. (A-4) will be equal to Eq. (A-2).

Now consider the case of two integral stages, for which we can derive the gain as follows:

\[ A_l = \frac{\omega t(1)}{D_1} \cdot \frac{\omega t(2)}{D_2} \cdot \frac{P + \frac{R_{l(1)}}{L_1}}{P^2 + \left( \frac{R_{l(1)}}{L_1} + \frac{\omega b(1)}{D_1} \right) P + \frac{\omega b(1)}{D_1} + \frac{R_{l(1)} + R_1 + r_b'}{L_1} \left( \frac{R_{l(1)} + R_1 + r_b'}{L_1} \right)} \]

\[ \left( \frac{R_{l(2)}}{L_2} + \frac{\omega b(2)}{D_2} \right) P + \frac{\omega b(2)}{D_2} + \frac{R_{l(2)} + R_1 + r_b'}{L_2} \bigg] \right) \]

For cancellation we have

\[ \frac{R_{l(1)}}{L_1} = \frac{\omega b(1)}{D_1} \left[ \frac{R_1 + r_b'}{r_b} \right], \]

and

\[ \frac{R_{l(2)}}{L_2} = \frac{r_b}{L_1} + \frac{\omega b(1)}{D_1}. \]

The condition for maximally flat magnitude is

\[ \frac{R_{l(2)}}{L_2} + \frac{r_b}{L_1} + \frac{\omega b(2)}{D_2} = \left[ \frac{2\omega b(2)}{D_2} \left[ \frac{R_{l(2)} + R_1 + r_b'}{L_2} \right] \right] \]

But we have

\[ \omega_{3\text{dB}} = \left[ \frac{\omega b(2)}{D_2} \left( \frac{R_{l(2)} + R_1 + r_b'}{L_2} \right) \right], \]
A systematic design technique now appears in which we progressively:

(a) Pick a bandwidth ($\omega_3$ db) for the amplifier, or pick a gain, and then from Eq. (A-11) find the bandwidth.

(b) Use the shape constraint equation (A-9):

$$\frac{R_l(2) + r_b}{L_2} + \frac{\omega_p(2)\beta(2)}{D_2} = \sqrt{2}\omega_3 \text{ db},$$

and Eq. (A-10), the bandwidth equation, to determine $R_l(2)$ and $L_2$.

(c) Use these data in turn to solve Eqs. (A-7) and (A-8) for $R_l(1)$ and $L_1$.

There is an additional degree of freedom in the design that allows some flexibility in selecting components. This freedom results from varying $\beta_0 r_e$, since $r_e = kT_0 q I_e$, and by changing $I_e$ some flexibility is realizable.

These equations assume that the transistors, $\omega_t$, $\omega_p$, $r_b$, $C_c$, and the optimum biasing conditions, $I_e$, $V_{ce}$, have been specified.

Let us assume an amplifier constructed from two 2N1143 transistors specified to have a bandwidth of 70 Mc. The properties of the transistors are:

<table>
<thead>
<tr>
<th>Q2</th>
<th>Q3</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\beta_0$</td>
<td>$f_t$</td>
</tr>
<tr>
<td>30</td>
<td>300</td>
</tr>
<tr>
<td>50</td>
<td>300</td>
</tr>
</tbody>
</table>
We substitute values as indicated to obtain:

\[
\begin{align*}
D_2 &= 1 + \omega t C_c (R_L + r_e) \\
&= 1 + 2\pi (300 \times 10^6) (1.5 \times 10^{-1})^2 (75 + 13) \\
&= 1 + 0.25 = 1.25, \\
D_3 &= 1 + 2\pi (300 \times 10^6) (1.5 \times 10^{-12})(125 + 3) \\
&= 1.35, \\
\frac{f_t(2)}{D_2} &= 240 \text{ Mc} \\
\frac{f_t(3)}{D_3} &= 222 \text{ Mc},
\end{align*}
\]

and

\[
A_i(0) = \left(\frac{240}{70}\right) \left(\frac{222}{70}\right) = 10.8.
\]

The measured response showed a gain of 10, and 10 to 90% rise time of 5 nsec. A schematic of this amplifier, including a common base stage at the input for matching the source impedance, is shown in Fig. 1.

B. The Integral Design of a Three-Transistor Shunt-Peaked Amplifier

In order to operate the transistors at optimum emitter bias current while still maintaining the freedom to vary \(\beta_0 r_e\), the input resistance of the transistor, a small unbypassed resistance \((R_E)\) is included in the emitter lead. The equivalent circuit is schematized in Fig. 4.

The gain can be derived as follows:

\[
A_i = \frac{A_t}{D} = \frac{P + R_I/L}{P^2 + \left[\frac{R_{I} + R_{E} + r'b}{L} + \frac{\omega \beta}{D}\right]P + \frac{\omega \beta}{D} \left[\frac{R_I + r'b + (1-\alpha)R_E}{L}\right]}
\]

in which

\[
D = 1 + \omega t (C_c + C_{cb})(R_L + R_E).
\]
Fig. 4. Equivalent circuit with unbypassed resistance $R'_E$. 

\[ R'_E = R_E + r_e \]

\[ C = \frac{1}{(\omega_f \omega)R'_E} \]
We now consider the case of three stages, for which we derive the gain as follows:

\[ A_1 = \frac{\omega_1(1)}{D_1} \times \frac{\omega(2)}{D_2} \times \frac{\omega(3)}{D_3} \]

\[
\times \frac{P + R_{1(1)}/L_1}{P^2 \left( \frac{R_{1(1)} + R_{1} + r'}{L_1} + \frac{\omega_1(1)}{D_1} \right) P + \frac{\omega_1(1)}{D_1} \left( \frac{R_{1(1)} + r'}{L_1} + \frac{1}{1-a_0} \right) R_{1}'}
\]

\[
\times \frac{P + R_{1(2)}/L_2}{P^2 \left( \frac{R_{1(2)} + R_{1} + r'}{L_2} + \frac{\omega_1(2)}{D_2} \right) P + \frac{\omega_1(2)}{D_2} \left( \frac{R_{1(2)} + r'}{L_2} + \frac{1}{1-a_0} \right) R_{1}'}
\]

\[
\times \frac{P + R_{1(3)}/L_3}{P^2 \left( \frac{R_{1(3)} + R_{1} + r'}{L_3} + \frac{\omega_1(3)}{D_3} \right) P + \frac{\omega_1(3)}{D_3} \left( \frac{R_{1(3)} + r'}{L_3} + \frac{1}{1-a_0} \right) R_{1}'}
\]

For cancellation we have:

\[
\frac{R_{1(1)}}{L_1} = \frac{\omega_1(1)}{D_1} \left[ \frac{\beta_0 R_1' + r'}{R_1' + r'} \right], \quad (B-3)
\]

\[
\frac{R_{1(2)}}{L_2} = \frac{\omega_1(2)}{D_2} \left[ \frac{\beta_0 R_1' + r'}{R_1' + r'} \right], \quad (B-4)
\]

and

\[
\frac{R_{1(3)}}{L_3} = \frac{r'}{L_3} + \frac{R_{1}(L)}{L_3} + \frac{\omega_1(3)}{D_3}, \quad (B-5)
\]
Then we can derive

\[
A_I = \frac{\left(\frac{\omega t(1)}{D_1}\right) \left(\frac{\omega t(2)}{D_2}\right) \left(\frac{\omega t(3)}{D_3}\right)}{P^2 + \left(\frac{R_l(3) + r_b E}{L_3} + \frac{\omega \beta(3)}{D_3}\right) P + \frac{\omega \beta(3) \left(\frac{R_l(3) + r_b E}{L_3}\right)}{D_3} \left[ P + \frac{r_b E}{L_1} + \frac{\omega \beta(1)}{D_1}\right]}
\]  

(B-6)

For a maximally flat magnitude we have

\[
\left(\frac{R_l(3) + r_b E}{L_3} + \frac{\omega \beta(3)}{D_3}\right) P + \frac{\omega \beta(3) \left(\frac{R_l(3) + r_b E}{L_3}\right)}{D_3} \left[ P + \frac{r_b E}{L_1} + \frac{\omega \beta(1)}{D_1}\right] = \frac{\omega \beta(3)}{D_3} \left(\frac{R_l(3) + r_b E}{L_3}\right)
\]

(B-7)

and

\[
\omega_{3 \text{db}} = \left[\left(\frac{\omega \beta(3)}{D_3} \left(\frac{R_l(3) + r_b E}{L_3}\right)\right) \left(\frac{r_b E}{L_1} + \frac{\omega \beta(1)}{D_1}\right)^{-1}\right]^{1/3}
\]

(B-9)

There are six unknowns \(R_l\) and \(L\) for each stage) and six eqs. (B-3, B-4, B-5, B-7, B-8, and B-9); therefore a solution in only a question of algebra. As in the two-transistor example, the initial step in the design is to specify the bandwidth, or to calculate the bandwidth from the specified gain and the gain-bandwidth product, which is

\[
A_I(0) = \frac{\left(\frac{\omega t(1)}{D_1}\right) \left(\frac{\omega t(2)}{D_2}\right) \left(\frac{\omega t(3)}{D_3}\right)}{\omega_{3 \text{db}}} = \left(\frac{\omega t}{D}\right)^3 \left(\frac{1}{\omega_{3 \text{db}}}\right)^2
\]

(B-10)
An amplifier was constructed following the above design equations (see Fig. 5), with a specified bandwidth of 50 Mc. The gain calculated from Eq. (B-10) is 76 and the measured gain was 66, the difference resulting from losses in the bias circuitry (i.e., the 5 k base resistor). When the resulting 0.85 loss factor is included, the gains compare quite well.

The bandwidth was determined from a pulse rise time method to be

\[ f_{3db} = \frac{0.35}{t_r} = \frac{0.35}{(7.3 \times 10^{-9})} = 48 \text{ Mc}. \]

The amplifier comprised three 2N834 transistors, the system was specified to have a bandwidth of 50 Mc. The properties of the transistors were

<table>
<thead>
<tr>
<th></th>
<th>( \beta_0' )</th>
<th>( f_{t'} ) (Mc)</th>
<th>( r_b' )</th>
<th>( C_c' )</th>
<th>( D )</th>
<th>Gain correction from biasing resistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q2</td>
<td>50</td>
<td>420</td>
<td>60</td>
<td>4 pf</td>
<td>2.13</td>
<td>0.96</td>
</tr>
<tr>
<td>Q3</td>
<td>60</td>
<td>480</td>
<td>60</td>
<td>4 pf</td>
<td>2.13</td>
<td>0.90</td>
</tr>
<tr>
<td>Q4</td>
<td>50</td>
<td>450</td>
<td>60</td>
<td>4 pf</td>
<td>2.13</td>
<td>0.985</td>
</tr>
</tbody>
</table>

These properties yield a calculated gain

\[ A_1 = \left( \frac{450}{2.13 \times 50} \right) \left( \frac{480}{2.13 \times 50} \right) \left( \frac{420}{2.13 \times 50} \right) = 76, \]

which, when including the loss from the biasing resistors, gives us for a amplifier gain:

\[ 76 \times (0.96)(0.90)(0.985) = 66. \]
Fig. 5. Integral design applied to a three-transistor shunt-peaked amplifier.
BIBLIOGRAPHY


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