SERI/TR-8033-2-T1



# CADMIUM SULFIDE/COPPER SULFIDE HETEROJUNCTION CELL RESEARCH

Final Report, February 26, 1979—July 15, 1980

By
John A. Thornton
David G. Cornog

June 30, 1980

Work Performed Under Contract No. AC02-77CH00178

Telic Corporation
Santa Monica, California





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SERI/TR-8033-2-T1
Distribution Category UC-63

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June 30, 1980

Work Performed Under Contract No. XJ-9-8033-2

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## ABSTRACT

This report covers work performed for the period February 26, 1979 to June 15, 1980.

Extensive modifications were made to the multi-source deposition apparatus. These include the installation of a larger vacuum chamber on the existing pumping system. The new chamber provides improved inter-source shielding, an improved substrate mounting and heating system, and a vacuum interlock for introducing substrates.

CdS resistivity control by both In doping and off-stoichiometric deposition has been investigated. Indium doping has been achieved both by diffusion from a pre-deposited In layer and by using In doped sputtering targets. Resistivities in the range 0.1 to 5 $\Omega$-cm have been obtained for target doping levels of from 0.1 to 1 at. percent of In. These resistivities were found to be critically dependent on the $H_2S$ injection rate, apparently because of compensation by Cd vacancies. Off-stoichiometry CdS coatings with solar-illuminated resistivities of about $10^2$ $\Omega$-cm have been deposited, using a cyclic reactive sputtering process where the $H_2S$ injection is periodically switched on and off.

The $Cu_xS$ deposition process was found to be sensitive to the period of cathode operation prior to coating deposition, probably because of the conditioning of cathode and shield surfaces. $Cu_xS$ coatings deposited onto CdS under various conditions have been found to have the same properties as those deposited onto glass substrates in previous studies.

All-sputter-deposited Cd(Zn)S/$Cu_2S$ cells, with Cd(Zn)S layers deposited using a Cd-0.10 Zn target doped with 2 atomic percent In, have yielded efficiencies of $\sim$0.4%. All-sputtered cells with efficiencies of $\sim$0.6% have been fabricated, using undoped CdS deposited by the pulse injection process. Efficiencies of $\sim$1.2% have been achieved for cells with undoped sputter-deposited CdS and CuCl dry processed $Cu_2S$.

# 1. PROJECT DESCRIPTION

## 1.1 Overall Objective

The program objective is to investigate and evaluate the application of cylindrical-post magnetron reactive sputtering for the production of solar cell quality thin films of CdS/$Cu_2S$ for large-scale terrestrial photovoltaic energy conversion. The reactive sputtering process is being investigated at Telic Corporation. The coating and device characterization is being done at the Lockheed Palo Alto Research Laboratory (Contract No. XJ-9-8033-1).[1]

## 1.2 Previous Work

The program is a continuation of work which was begun in October 1977 as a subcontract to Lockheed under DOE Contract EG-77-C-03-1459.[2] During that work an apparatus capable of fabricating all-sputter-deposited solar cells was assembled by mounting four cylindrical-post magnetron sputtering sources of the type shown in Fig. 1 in a small vacuum chamber (0.38m ID) which was available for dedication to the program. The apparatus is shown schematically in Fig. 2. Photovoltaic cells were prepared on glass substrates by dc sputtering. One sputtering source was used to deposit the rear electrode. Niobium was used for most of the work. A second source was used to deposit CdS or $Cd_xZn_{1-x}S$ by sputtering from a Cd or a Cd/Zn alloy target in an Ar-$H_2S$ working gas. A third source was used to deposit the $Cu_2S$ layer by sputtering Cu in an Ar-$H_2S$ mixture. The fourth magnetron served as an auxiliary source for doping by co-deposition and/or for depositing a layer of modified composition at the rear electrode to assure an ohmic contact.

The following observations were made during the course of the first year of work.[2]

1) A tendency for cathode arcing was observed to occur at high current densities during the CdS or $Cd_xZn_{1-x}S$ deposition, particularly after sustained periods of dc operation in working gases containing a relatively high partial pressure of $H_2S$. The cause was tentatively identified as a form of unipolar arc[3] resulting from charge accumulation at insulating deposits on the cathode surface. The use of rf power eliminated the arcing. However, dc was used throughout most of the work.

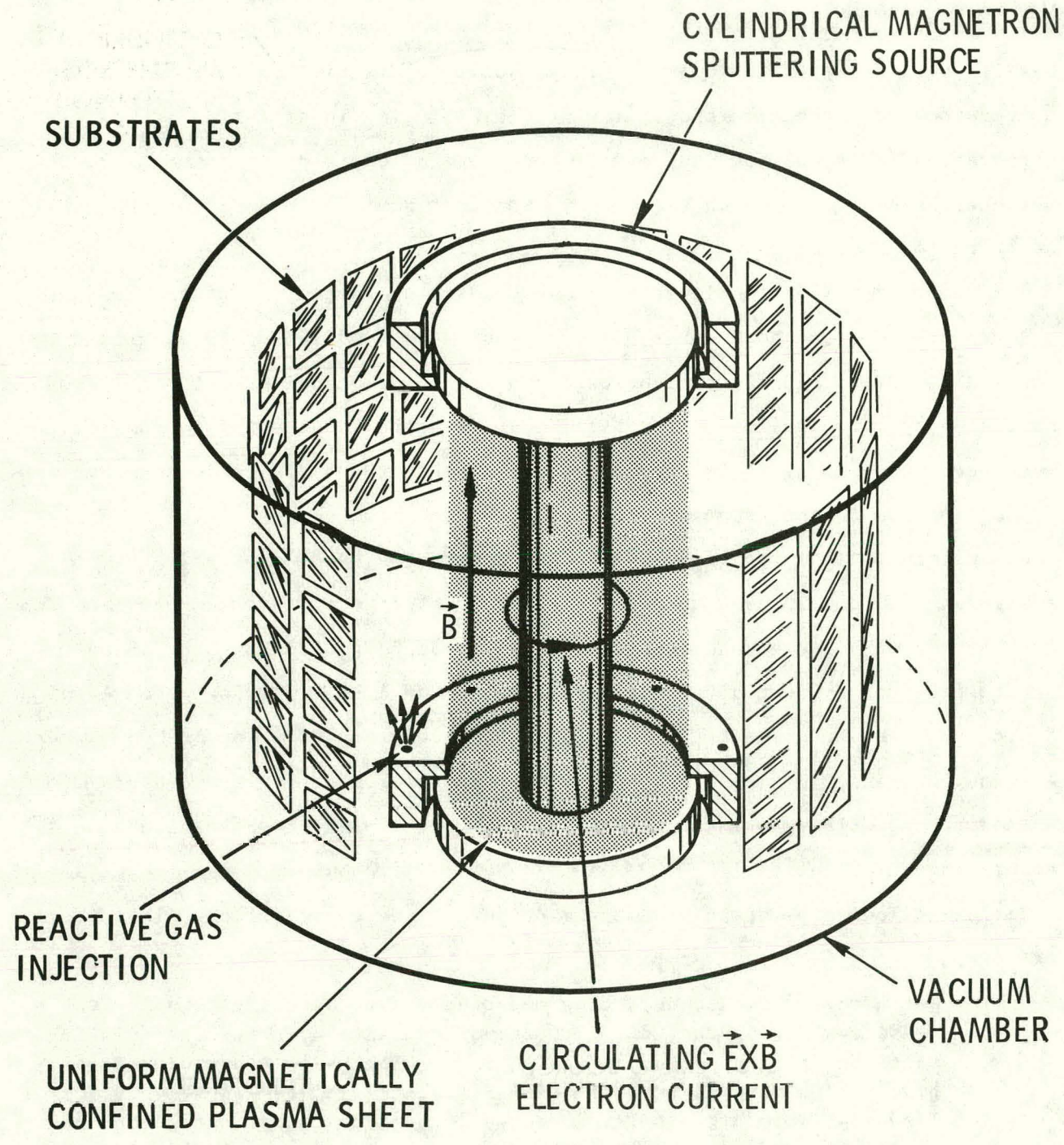



FIG. 1 Schematic illustration of cylindrical magnetron sputtering source.

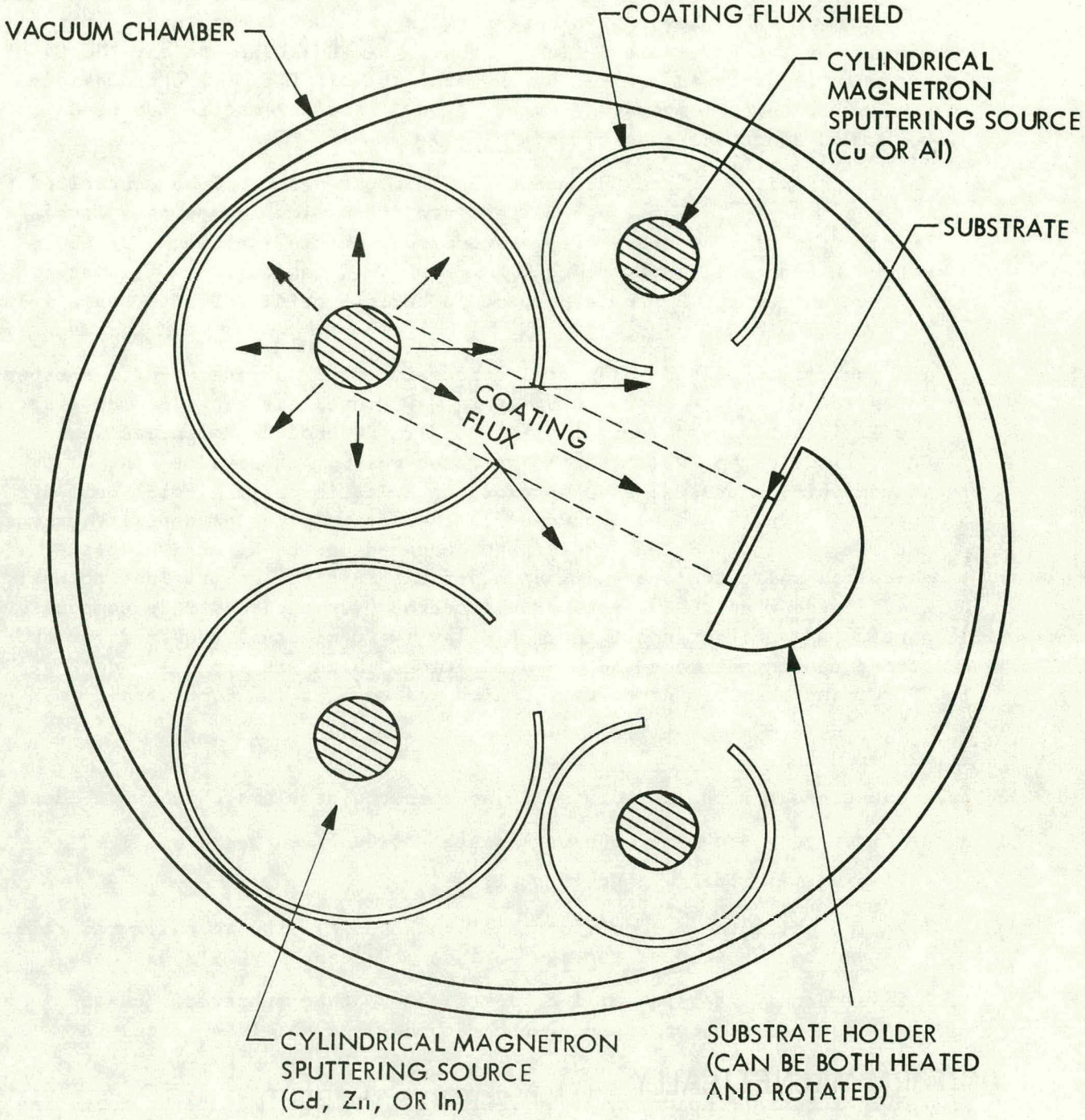



FIG. 2 Schematic diagram of multi-source deposition apparatus assembled during first year's program.

2) At the substrate temperatures of interest for the CdS and $Cd_xZn_{1-x}S$ deposition (>200°C), re-evaporation was found to limit the CdS accumulation rate to the extent to which the Cd could interact with the S flux and form CdS. At low $H_2S$ injection rates, the CdS accumulation is rate-limited by the available S flux. At high $H_2S$ injection rates, the CdS accumulation rate is limited by the available Cd flux. The process is similar to three-temperature evaporation.[4] Stoichiometric CdS tends to be formed under all conditions.

3) The resistivity of both CdS and $Cd_xZn_{1-x}S$ coatings could be controlled by indium doping. The range of required doping levels was established by co-deposition studies. It was concluded that a 2 atomic percent In concentration could provide $Cd_{0.9}Zn_{0.1}S$ with a resistivity of about 30 Ω-cm and that 0.3 atomic percent In could provide CdS with resistivity of about 1 Ω-cm.

4) All-sputter-deposited solar cell structures were fabricated with sputter-deposited $Cd_{0.9}Zn_{0.1}S$ and $Cu_xS$ layers. Photovoltaic behavior was observed, but efficiencies were very low (~0.03%). Several deficiencies were identified in the experimental apparatus which made precise control over the deposition process and therefore optimization of the solar cell structures difficult. These included (1) the accumulation of deposits on the cathode shields and the release from these deposits of active species which can shift the operating point of the reactive sputtering process; and (2) the requirement for better control over the substrate temperature, particularly with respect to time delay (~20 minutes) required for substrate cooling between the CdS deposition, which was typically done at 250-300°C, and the $Cu_xS$ deposition, which was done at 150°C or less.

## 1.3 Work Statement

The present program was formulated to address the problems which were identified in the first year program. The work statement is given below.

TASK 1: DEPOSITION PROCESS DEVELOPMENT

1.1 The shielding around individual cathodes will be reconfigured to reduce the area of foreign surfaces adjacent to the substrates.

1.2 A vacuum interlock will be installed so that substrates can be inserted without exposing the cathodes and shield surfaces to the atmosphere.

1.3 A substrate holder will be fabricated for the multicathode coating apparatus that incorporates provision for heating and for rapid cooling of the substrates.

1.4 An investigation will be performed of the use of rf power for producing (Cd,Zn)S coatings by reactive sputtering from a metal target to determine if high sputtering rates can be achieved in the absence of arcing.

TASK 2: (Cd,Zn)S, CdS AND $Cu_2S$ DEPOSITION

2.1 An investigation will be performed of the relationship between Cd-Zn target doping level and the resultant electrical resistivity in $Cd_{1-x}Zn_xS$ coatings deposited by cylindrical magnetron reactive sputtering. The course of this investigation will be based on coating characterization studies made at Lockheed.

2.2 An investigation of resistivity control in (Cd,Zn)S and CdS films by off-stoichiometric deposition, annealing, post-deposition heat treatment in different ambient conditions, and Cu diffusion will be performed. A key decision will be made after 6 months as to the most desirable method of controlling the resistivity of these films. The course of this investigation will be based on coating characterization studies made at Lockheed.

2.3 The investigation will continue on the optimum method of depositing $Cu_2S$ film. The course of this investigation will be based on coating characterization studies made at Lockheed.

TASK 3: DEVICE-MATERIAL PARAMETER OPTIMIZATION

3.1 Multilayer solar cell structures will be deposited onto glass substrates during all stages of material and device development. The course of this investigation will be based on solar cell characterization studies made at Lockheed.

## 2. DEPOSITION PROCESS DEVELOPMENT (TASK 1)

### 2.1 Apparatus Modifications

Task 1 required that the deposition apparatus be modified. The specific objectives of the modifications were to:

1) Reconfigure cathode shielding to reduce the shield surface area adjacent to the sputtering sources and the substrates (Task 1.1).

2) Install a vacuum interlock so that substrates can be inserted without exposing the cathode and shield surfaces to the atmosphere (Task 1.2).

3) Redesign the substrate holder to permit rapid cooling of the substrates between the CdS and the $Cu_2S$ depositions (Task 1.3).

The formulation of Task 1.1 is based on the fact that vacuum chamber and shield surfaces can interfere with the reactive sputtering process in the following ways.

1) By absorbing atmospheric gases (particularly, water vapor) when they are exposed to the atmosphere during substrate loading, and the release of these species when they are placed under vacuum.
2) By acting as catalytic surfaces for reactions between the sputtered flux and the working gas.
3) By releasing volatile reactive species from accumulated deposits, particularly under the influence of heating.

All of these effects are exacerbated by the accumulation of thick coating deposits. Such deposits are often porous in nature (because of changing deposition conditions) and therefore present large surface areas for the absorption and reaction of gases. The close proximity of the circular shields shown in Fig. 2 to the magnetron sources causes these deposits to be particularly thick (1 mm thick deposits were routinely removed during the first year program.) Occasionally these deposits break loose from the shields during exposure to the atmosphere (probably because of stress formation during oxidation), and dump debris onto the cathode surface.

Therefore it was concluded that the modified design should significantly increase the distance between the sputtering sources and the shields. It was also concluded that provisions should be made for cooling the shields so that the release of volatile reactive species due to shield heating could be suppressed. The vacuum interlock was also expected to help in reducing the effects due to the absorption of atmospheric gases.

In evaluating the requirements for the apparatus modification, it became immediately apparent that the coating chamber used during the first program was too small to permit the expanded shielding and the interlock to be installed. Once it was decided that a larger chamber should be fabricated, a number of design options became possible. Therefore the apparatus modification was delayed

in order to explore several of these possibilities in detail. For example, the possibility of an extensive modification, that would have changed the basic configuration of the apparatus and made it more like a production coating system, was examined in some detail, but concluded to be inappropriate for the present program. The design that was finally selected is very similar in its basic features to the one which was used during the first program. It is shown schematically in Fig. 3. Because of the design delays cited above, the modified apparatus was not placed into operation until the fourth quarter of the program. However, the apparatus was tested in the fourth quarter and found to function properly.

The modification involved fabricating and mounting a larger vacuum chamber (0.64m ID) and magnetic field coil system on the same pumping stand that was used for the previous program. The new vacuum chamber is shown in Fig. 4. The basic design of the vacuum chamber and magnetic coil system are shown schematically in Fig. 5. The magnetic field coils are located in the annular space between a nonmagnetic (Type 304) stainless steel vacuum chamber wall and a carbon steel outer cylinder. The chamber top and bottom plates are also fabricated from carbon steel. Thus the field coils are enclosed within a shell of magnetic material which is made thick enough so that it is not saturated by the magnetic flux. Magnetic field lines pass through the chamber and then return via the shunt path in the steel as indicated in Fig. 5. With this configuration a magnetic field that is uniform in magnitude and direction can be produced within the vacuum enclosure by the short solenoidal coil system. Such a field is required in the chamber for operating the cylindrical-post magnetron sputtering sources. The coil system is connected electrically as three coil sets, so that the currents can be independently controlled. This adjustment permits the effects of perturbations, such as the holes in the top plate where the cathodes are inserted, to be compensated for. Magnetic probe measurements at the cathode mounting positions verified that the magnetic field strength and uniformity were adequate for reliable operation in cylindrical-post magnetron sputtering sources.

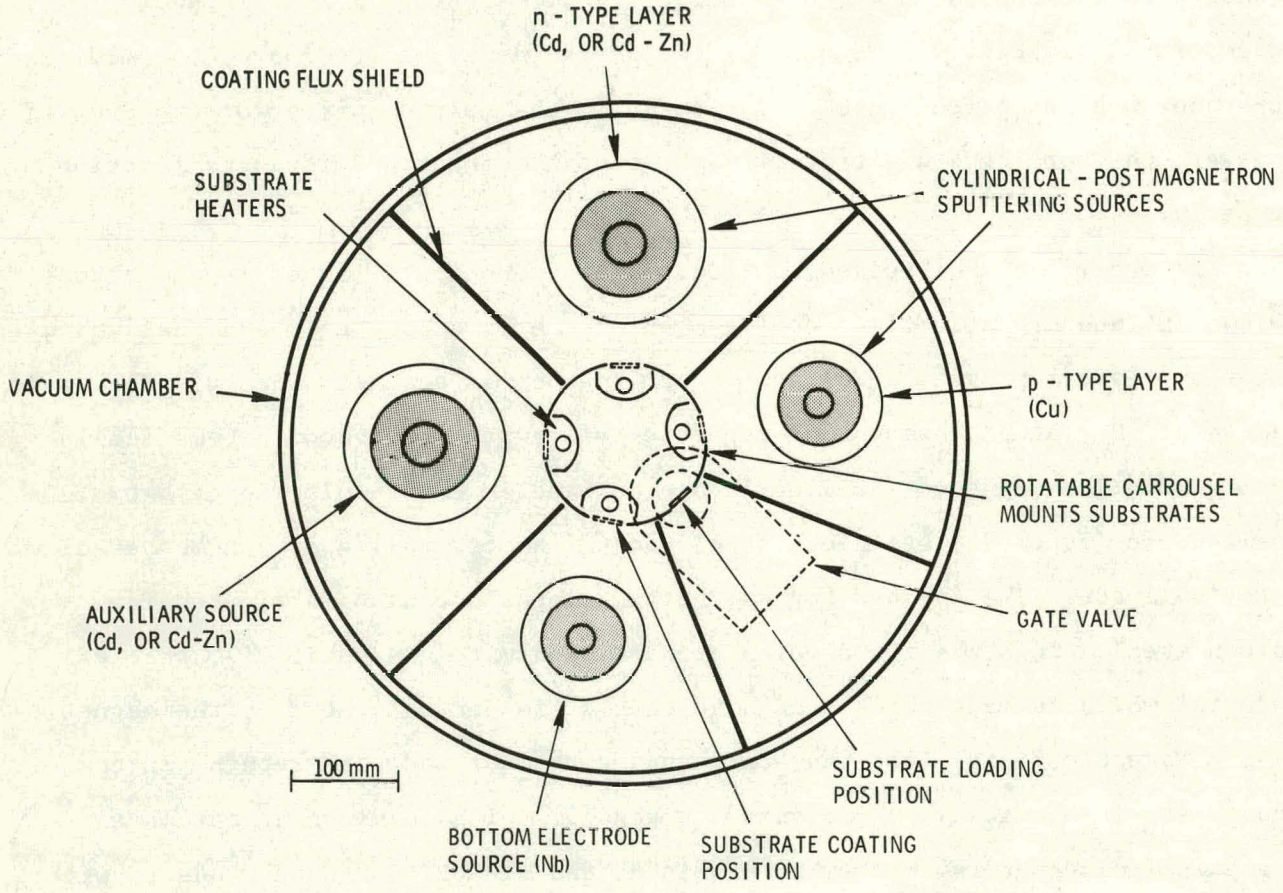



FIG. 3 Schematic illustration of modified multi-source deposition apparatus assembled during present program.

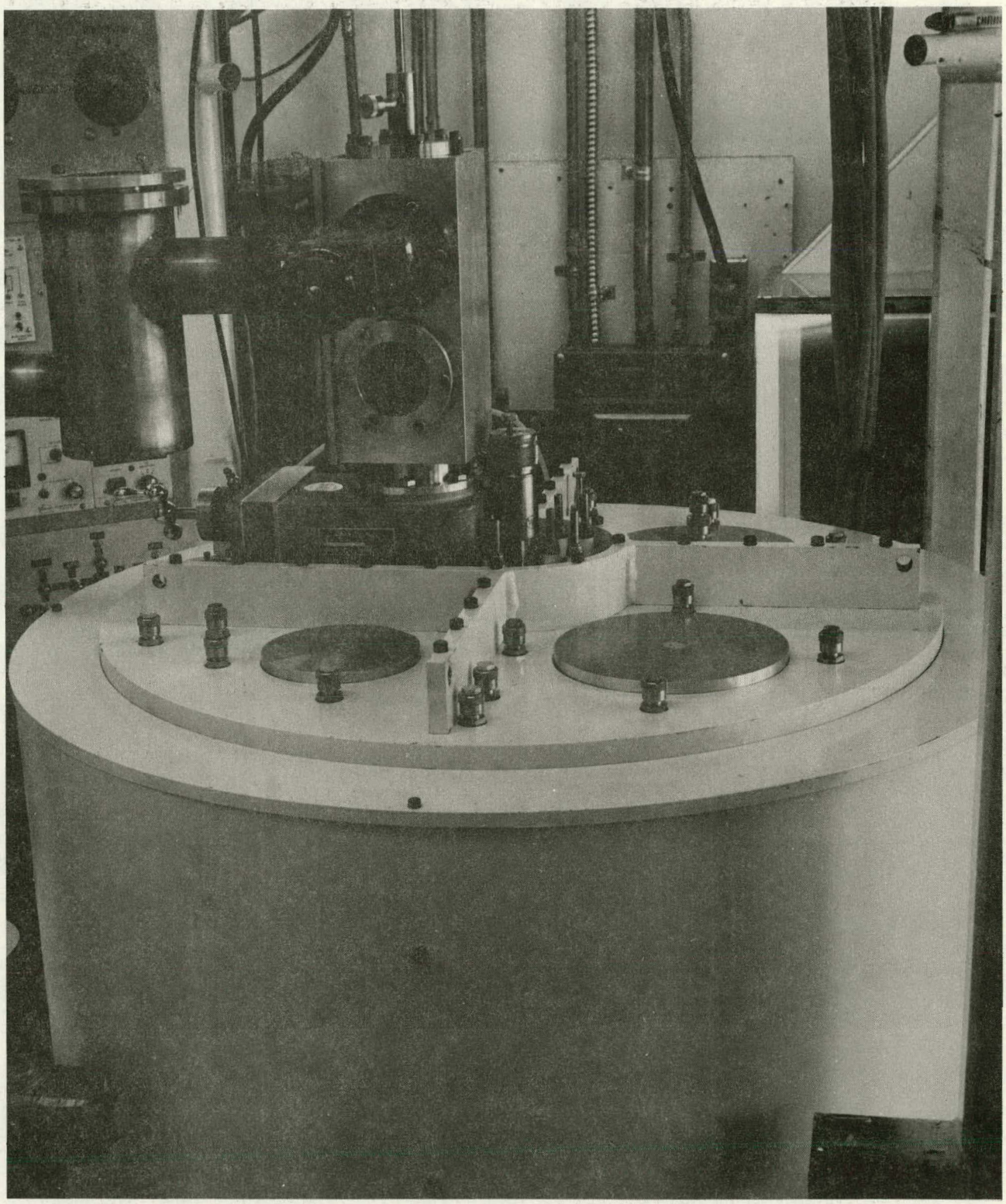


FIG. 4 Photograph showing modified deposition apparatus. The vacuum interlock can be seen at the left.

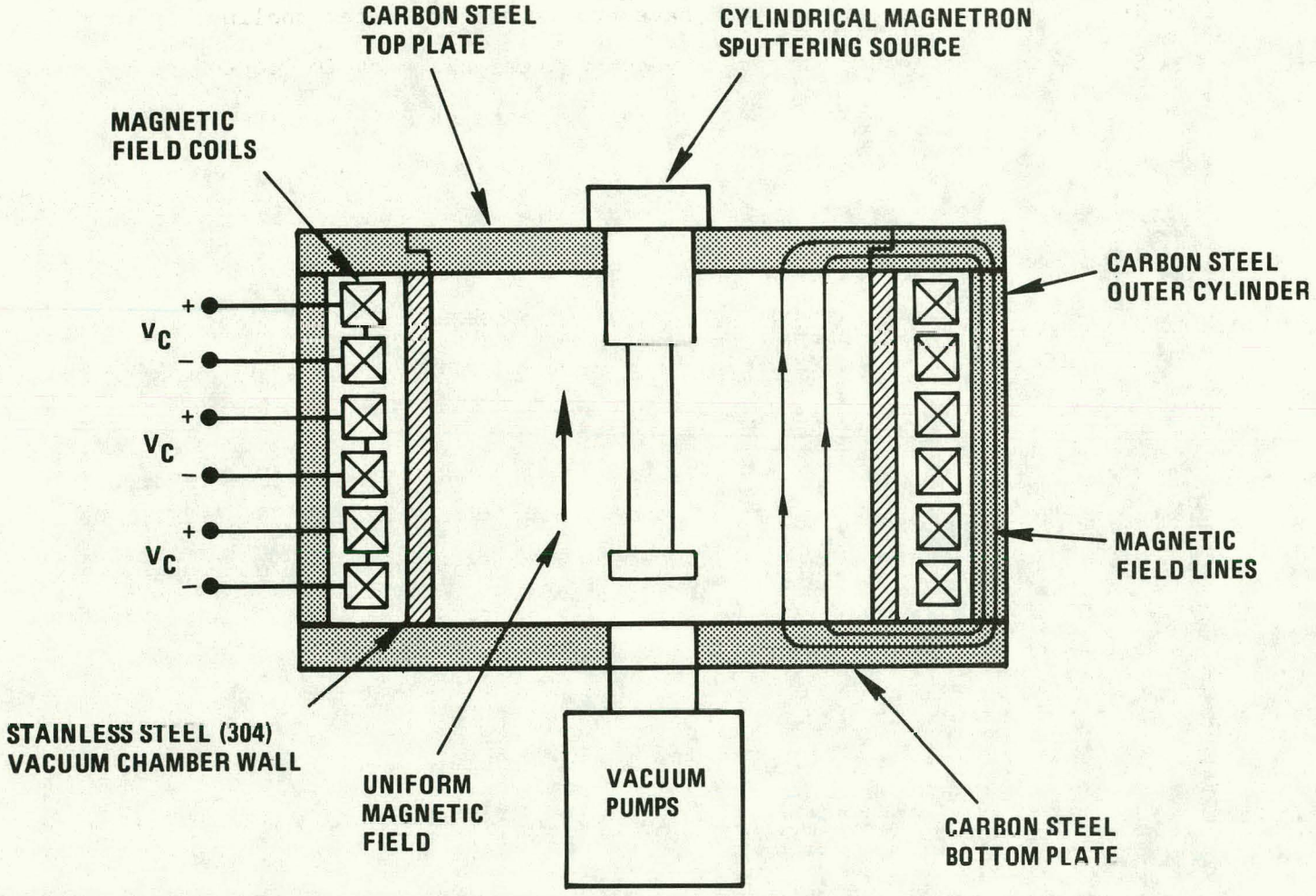



FIG. 5 Schematic illustration of chamber magnetic field coil system.

A series of shields partition the coating chamber into four compartments, within which the individual magnetron sputtering sources are located, as shown in Fig. 3. The shields are located much farther from the sputtering sources than in the previous apparatus, and have provisions for water cooling.

Substrates are loaded through a vacuum interlock which is located on the top of the chamber. The substrates are placed into a stainless steel frame of low thermal mass. The frame is designed to mount five 25 mm x 25 mm x 1.2 mm glass substrates. Typically only the lower three substrate positions are used because of deposition uniformity considerations with the cathode lengths which are currently being used. The frame is passed through a door in the interlock chamber and attached to the end of a loading rod. After the interlock chamber is evacuated, the rod is used to lower the substrate frame through a 2-inch gate valve and onto the carrousel-type mounting frame shown in Fig. 3. The loading procedure is shown schematically in Fig. 6. The carrousel frame permits the substrates to be rotated and passed into the four different coating positions. Fixed substrate heaters are located behind the carrousel at each of the coating positions. The carrousel has a low thermal mass, so that the substrates can be quickly cooled by rotating them away from a substrate heater to a cooling position. The cooling time is determined primarily by the thermal capacity of the glass substrates. Typical cooling times between CdS deposition at 250°C and $Cu_2S$ deposition at 150°C are about 3 minutes. The equivalent cooling times for the old apparatus were in the range from 13 to 20 minutes.

Dummy glass substrates with imbedded chromel-alumel thermocouples are mounted on the carrousel, adjacent to the deposition substrates, in holders identical to the ones used for the deposition substrates. These thermocouples are calibrated against similar thermocouple-containing-plates, which were placed at the deposition positions during heater tests. These calibrations were made for various combinations of emittances on the substrate and reference surfaces and are used to estimate the substrate temperatures during deposition. See discussion in

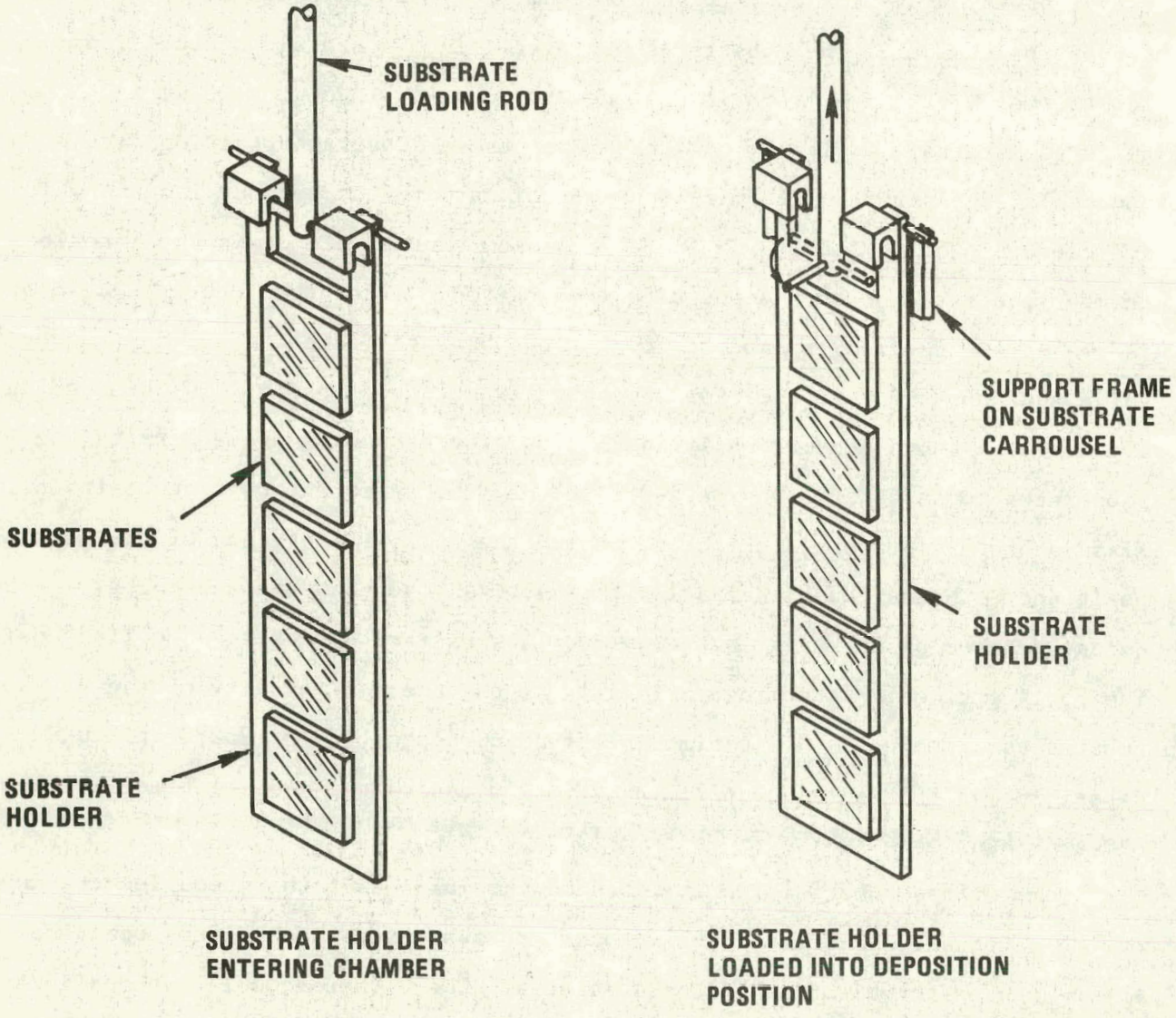



FIG. 6 Schematic illustration of substrate loading procedure.

Section 3.1. (This is the same procedure that was used with the previous apparatus). The carrousel and substrate holder are shown in Fig. 7 as viewed from the position of a sputtering source. The lower two substrate positions mount the plates which contain the reference thermocouples.

2.2 Cathode Arcing

During the first year of the program a tendency for cathode arcing was encountered when Cd was sputtered using $H_2S$ or Ar-$H_2S$ mixtures at high current densities or high partial pressures of $H_2S$ (see Section 1.2). The arcs have tentatively been identified as a form of unipolar arc[3] resulting from charge accumulation at insulating deposits on the cathode. Accordingly, rf sputtering is expected to reduce this tendency because the polarity reversal reduces the charge accumulation on the deposits. Preliminary experiments during the first year program verified this conclusion. Additional experiments were conducted during the present program to further examine the use of rf reactive sputtering (see Section 2.3).

Observations on the present program indicate that the arcing problem is not so severe as had been previously thought. At the substrate temperatures being used (200 to 300°C), no correlation has been seen between the occurrence of arcing during dc reactive sputtering of CdS and the properties of the resulting coatings. The only observed effect is loss of precise control over deposition rate (coating thickness) because of the cessation of sputtering during an arc.

The possibility of virtually arc-free, dc reactive sputtering has also been established. CdS and Cd(Zn)S coatings of the desired thickness (3000 to 6000 nm) have been deposited with less than one(non-sustaining)arc per hour (the occurrence of arcs is monitored with a recorder) both with and without the interlock system. These observations permit several possible causes for the insulating deposits to be excluded. In particular, the occurrence of severe arcing has been found not to correlate with: (1) the vacuum chamber having been open to the atmosphere for an extended period of time prior to the run in question; (2)

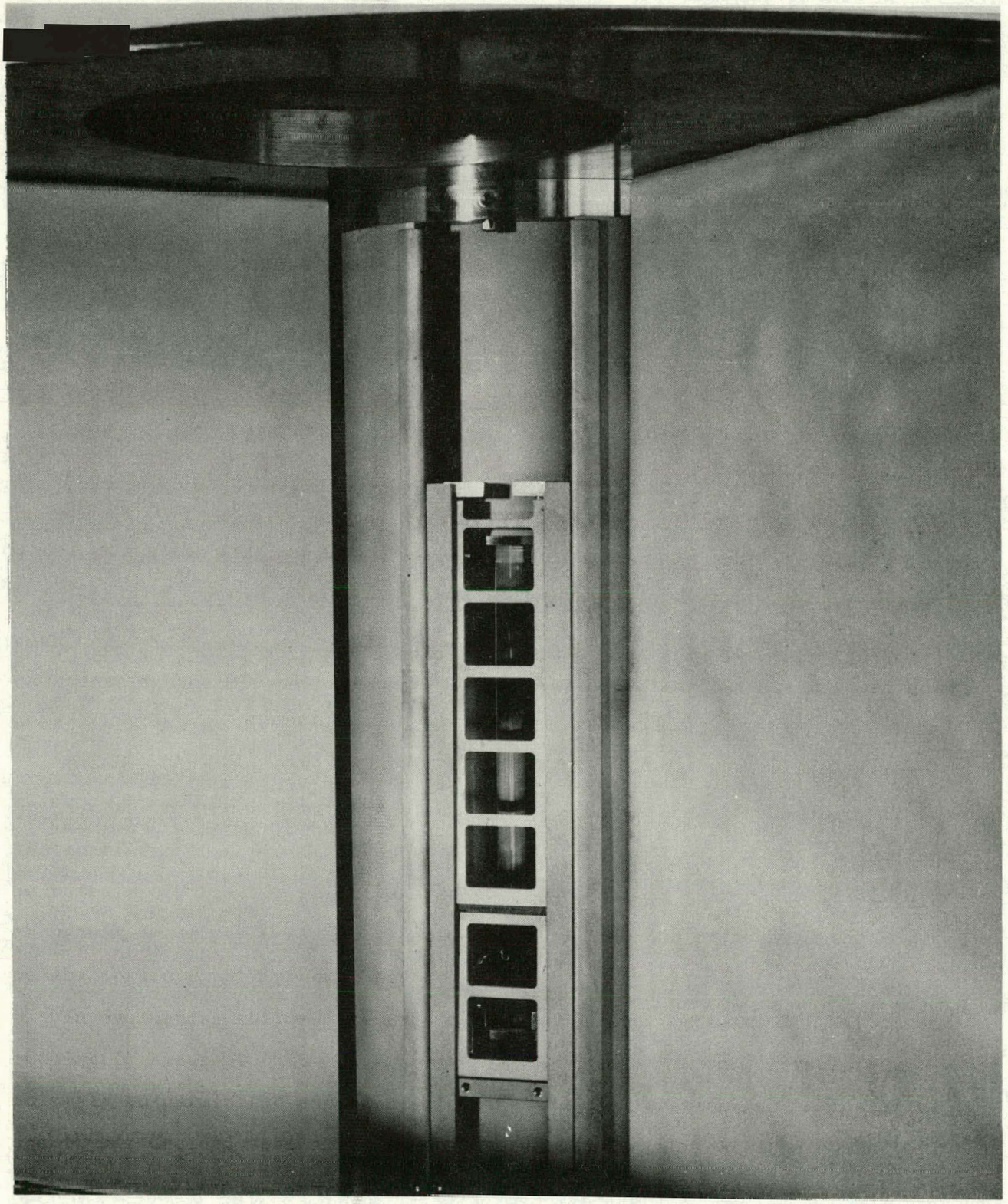


FIG. 7 Photograph with chamber lid raised showing carrousel type substrate holder.

the number of deposition runs following a change in the experimental configuration, including shield cleaning, at least for sequences involving as many as ten runs; nor (3) the presence of chips, flakes, or other debris on the anode and on the cathode end flanges (see Fig. 1).

In addition, the following has been observed.

1) A cathode which has drifted into a state of severe arcing can be renewed and passed into a condition of smooth operation by simply operating for a short period (several minutes) in pure Ar. Presumably this Ar operation sputters the offending deposits from the cathode surface. During the present program experiments have been conducted in which the $H_2S$ injection has been periodically ceased in an attempt to promote the formation of nonstoichmetric CdS deposits (see Section 3.4). Preliminary observations indicate that typical operating conditions selected to control the resistivity are also effective in reducing the frequency of arcing.

2) Evidence has been found which indicates that the Cd vacancy level must be controlled in order for the doping to be effective in an In doped CdS deposit (see Section 3.3). Thus it is necessary to carefully control the $H_2S$ injection rate at levels which also turn out to be favorable with respect to reducing the occurrence of arcing.

3) The modified apparatus with the vacuum interlock was placed into service during the fourth quarter. Therefore the experience with this device is limited in comparison with that which has been obtained with the old apparatus. However, the observations thusfar indicate that arcing is less frequent with the modified apparatus.

Because of the above considerations, the rf sputtering experiments described in the following section were carried out only in sufficient detail to identify the usefulness of the approach as a viable future alternative. Dc power is desired when it can be used. Accordingly, a new dc power supply with an improved arc suppression circuit was designed and constructed on an independent Telic-sponsored project. This power supply has been placed into operation and has proven effective in largely eliminating the occurrence of sustaining arcs.

## 2.3 Investigation of rf Reactive Sputtering (Task 1.4)

The purpose of this task was to examine some of the considerations which are important in applying rf power to cylindrical-post magnetron sputtering sources for the purpose of minimizing arcing during CdS reactive-sputtering, as discussed in the preceding section.

In rf sputtering the electrodes are capacitively coupled to the plasma. A self-bias that is negative relative to the plasma potential develops on any surface that is capacitively coupled to a glow discharge.[5] Consequently, both electrodes in an rf discharge develop a significant negative potential relative to the plasma potential throughout most of the rf cycle and are therefore subject to sputtering.

Two approaches are used in conventional sputtering sources to avoid unwanted sputtering. The so-called "double ended" approach makes both electrodes identical sputtering targets. The "single ended" approach makes use of the fact that the voltage drop in each of the electrode plasma sheaths depends on the current density and sheath capacitances and therefore on the electrode areas in contact with the plasma. An approximate analysis predicts that the ratio of these sheath-voltage-drops varies inversely with the electrode area ratio raised to the fourth power.[6] Accordingly, in the single ended case, the counter or non-target electrode is made large enough so that the sheath voltage drop is less than the sputtering threshold.

In the present case we require that the same cylindrical-post magnetron that was used for the dc reactive sputtering work also be used for the rf studies. This dictates a single ended design. The requirements for the counter-electrode are:

1) That it have an area which is larger than that of the sputtering target.
2) That it make contact with the magnetron plasma so that the required current can be drawn.
3) That it operate without inducing a large voltage drop. This requires that it have an effective electrode shape that is also compatible with the magnetic field applied to the magnetron.

CdS rf reactive sputtering experiments were conducted with both the circular cathode shields (Fig. 2) and the chamber walls serving along with the normal dc anodes (Fig. 1) as the counter electrodes. The arrangements are shown schematically in Fig. 8. The working gas was Ar-$H_2S$ injected under the same general range of

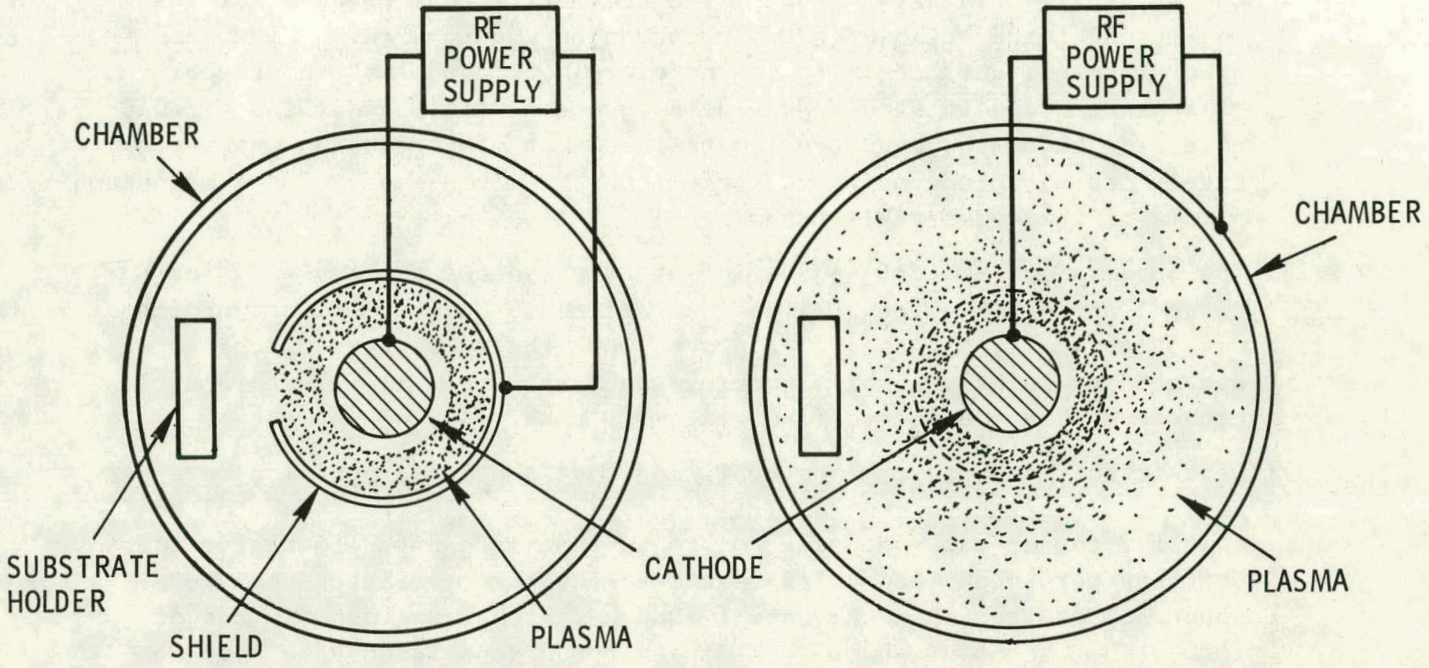



FIG. 8 Schematic illustration of experimental arrangement used in rf sputtering experiments.

conditions that was used in the dc experiments. The following observations were made.

1) The circular cathode shields formed an efficient counter electrode from an electrical point of view. The apparatus operated effectively with the plasma confined primarily within the shielded cavity as indicated in Fig. 8A. However, this configuration is obviously unacceptable as a production coating source, since most of the sputtered flux is blocked by the shield. When the shields were removed, the chamber walls and other surfaces within the chamber were forced to serve as the counter-electrode. The axial magnetic field offered a strong impedance to the radial electron motion from the magnetron plasma to these surfaces. Consequently a discharge glow filled the entire chamber, as indicated in Fig. 8B, with brighter glows apparent on the substrate holder and other internal surfaces. It is therefore concluded that an effective rf apparatus design should provide a counter-electrode surface of suitable size below the magnetron source, so that electrons can pass relatively freeely along magnetic field lines from the edges of the magnetron plasma to the counter-electrode.

2) The observation that rf sputtering greatly reduced the tendency for cathode arcing (Section 2.2) was reconfirmed. However, mirror arcing was observed, even with the rf power, when the sputtering discharge was operated at relatively high working gas pressures ( >10 mTorr) and cathode current densities ( >10 mA/cm$^2$ - rms).

3) Deposition rate measurements confirmed that the CdS deposition rate per unit of discharge current for rf reactive sputtering is identical to that for the dc case when the rms rf current is equated to the dc current. Coatings were deposited by rf reactive sputtering at rates that were about 50% greater than the rate ($\sim$0.5 nm/s) that was used in the dc work. The use of rf power should permit the deposition rate used in previous work to be approximately doubled for the apparatus (pumping system) presently being used. (When arcs are eliminated, the limitation on deposition rate becomes the ability of the system pumps to remove the hydrogen that is liberated by the reactive sputtering according to the reaction $Cd+H_2S \rightarrow CdS+H_2$.)

The rf reactive sputtering work was not pursued beyond the work described above because of the encouraging results which were obtained using dc power as the program progressed (see Section 2.2), and because the major thrust of the program is to demonstrate all-sputter-deposited solar cells with high efficiencies and not to achieve high deposition rates per se.

## 3. CdS, $Cd_xZn_{1-x}S$, AND $Cu_2S$ DEPOSITION (TASK 2)

### 3.1 Effect of Substrate Emittance

The glass substrates are heated by 500W tubular quartz heating lamps which are mounted in reflector assemblies located behind the substrate mounting carrousel, as shown in Fig. 3. The distance from the lamps to the rear of the substrates is about 3 cm. A similar configuration with a single lamp was used in the apparatus shown in Fig. 2. The substrate temperatures are implied from the temperature which is measured by using a thermocouple embedded in an identical glass plate mounted below the deposition substrates, as indicated schematically in Fig. 9. (See discussion in Section 2.1). Calibration data were generated with glass substrates containing embedded thermocouples located at the deposition positions as well. Tests conducted over the temperature range from 200°C to 350°C showed that the maximum variation in substrate temperature between the three deposition positions in the modified apparatus was about ± 2%, and that the average substrate temperature at these deposition positions was about 10% higher than the temperature at the calibration position when all the substrates had identical surfaces.

The temperature of a substrate is determined by the rate at which lamp energy is delivered to its rear surface and absorbed, and the rate of radiation losses from both the front and rear surfaces. Glass has a high absorptance for infrared radiation. We measured a room temperature total hemispherical emittance of 0.90 (consistent with handbook values) for the Corning 7059 glass plates, using an International Technology Ambient Emissometer. We therefore assume that virtually all of incident radiation energy from the lamp is absorbed in the glass, or at least that the net glass absorption is not sensitive to the presence of a reflecting coating on the glass front surface. Accordingly, one can write the following relationship between the equilibrated substrate temperatures, $T_1$ and $T_2$, and the average front and back surface emittances, $\langle \epsilon_1 \rangle$ and $\langle \epsilon_2 \rangle$, for two substrates absorbing a common radiant flux from the lamp. $T_o$ is the background temperature in the chamber.

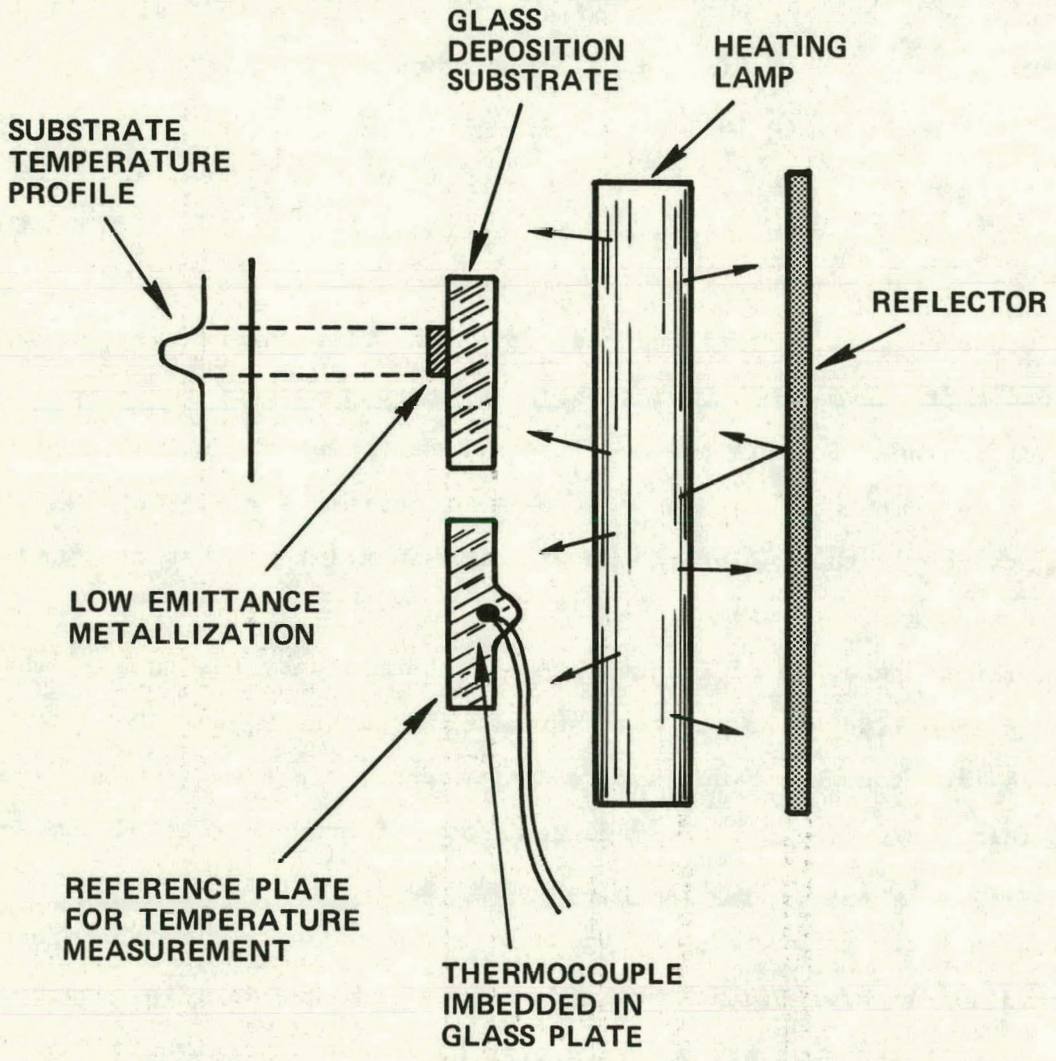



FIG. 9 Schematic illustration of substrate heating arrangement.

$$\frac{T_1^4 - T_o^4}{T_2^4 - T_o^4} = \frac{\langle \epsilon_2 \rangle}{\langle \epsilon_1 \rangle} \qquad (1)$$

Equation 1 shows that a substrate with a low emittance metallization on the front surface (low average $\epsilon$) will equilibrate at a higher temperature than will the glass by itself.

Equation (1) has significant consequences for the deposition of multi-layer coatings onto radiation-heated substrates in general, and for the calibration procedure in particular. This is illustrated by the following observations.

1) The lamp current was adjusted to provide a temperature of 300°C on an unmetallized glass substrate with an embedded thermocouple. A 150 nm thick Nb coating was then deposited onto one surface of the glass while the lamp current remained constant, and the temperature was monitored. The glass temperature increased to 360°C. This temperature increase is consistent with predictions made using Eq (1) and the emittance of sputtered Nb which was measured and found to be 0.14 for a 100 nm thick layer on the Corning 7059 plates.

2) The calibration factor relating the average temperature of the deposition substrates and the temperature of the reference substrate was shown to be independent of whether the substrates were all uncoated glass or were all coated with Nb. The uncoated glass substrate temperature implied by a glass reference substrate with no Nb coating will be referred to in subsequent discussions as the "glass calibration temperature." When the deposition substrates were Nb coated and the reference substrate was uncoated, the calibration factor increased from 1.10 to 1.40, consistent with Eq (1).

3) When Nb metallized substrates with embedded thermocouples were overcoated with a 1000 nm layer of reactively sputtered CdS at substrate temperatures in the 200°C to 400°C range, the substrates were observed to decrease in temperature by an amount (typically 5 to 20°C) which is consistent with Eq (1) and with measured emittance values for Nb overcoated with CdS. In particular, the CdS coatings were found to have a relatively small infrared absorptance. Thus when a 500 nm CdS coating was deposited onto a sputter deposited Nb metallization layer, the emittance measured with the Ambient Emissometer increased only from 0.14 to 0.18. Similarly, when a 500 nm CdS layer was deposited directly onto a glass substrate, the measured emittance decreased only from 0.90 to 0.80.

The above observations show that, although the CdS coatings exert a minimal influence on the emittance and therefore the temperature of radiation heated substrates, large perturbations can be induced by the metallization layers. Furthermore, because of the relatively low thermal conductivity of glass, large temperature variations can occur across the surface of a glass substrate that has localized regions of metallization such as predeposited electrodes. Two examples of this behavior were observed during the project.

During a study of the electrical properties of sputter deposited CdS and (Cd,Zn)S, coatings were deposited onto glass substrates having pre-deposited Nb electrodes in a geometry designed to facilitate van der Pauw measurements (see Fig. 10). It was found that the thickness, structure, and surface topography of the CdS deposited over the Nb was different from that of the CdS deposited over the glass.[7] It is believed that these observations were a consequence of local differences in surface temperature. Of particular importance was the discovery that the electrical properties of CdS deposited onto uncoated glass at a glass-calibration substrate temperature of 300°C was significantly different from the properties of CdS deposited onto Nb-coated glass substrates. Indium contacts were pressed onto the top surface of a CdS coating which had been deposited over both the Nb-metallized diagnostic electrodes and the unmetallized regions of a glass substrate, as shown in Fig. 10.[8] Contacts over the glass (positions A and B in Fig. 10) yielded ohmic behavior when connected to each other or to the Nb diagnostic electrodes. However, In contacts located over the Nb (positions C and D) were blocking in one polarity. The effect was observed for CdS, with and without an In underlayer, and for $Cd_{0.9}Zn_{0.1}S$ deposited from a cathode doped with 2 atomic percent In. When the glass-calibration substrate temperature was reduced to 250°C, the In contacts were ohmic, independent of whether the underlying CdS was deposited over glass or over a Nb metallization. These observations, which suggest that an electrically active species may have been passing from the Nb metallization into the CdS at high substrate temperatures and influencing the surface,[8] were made during the first quarter of the program.[7]

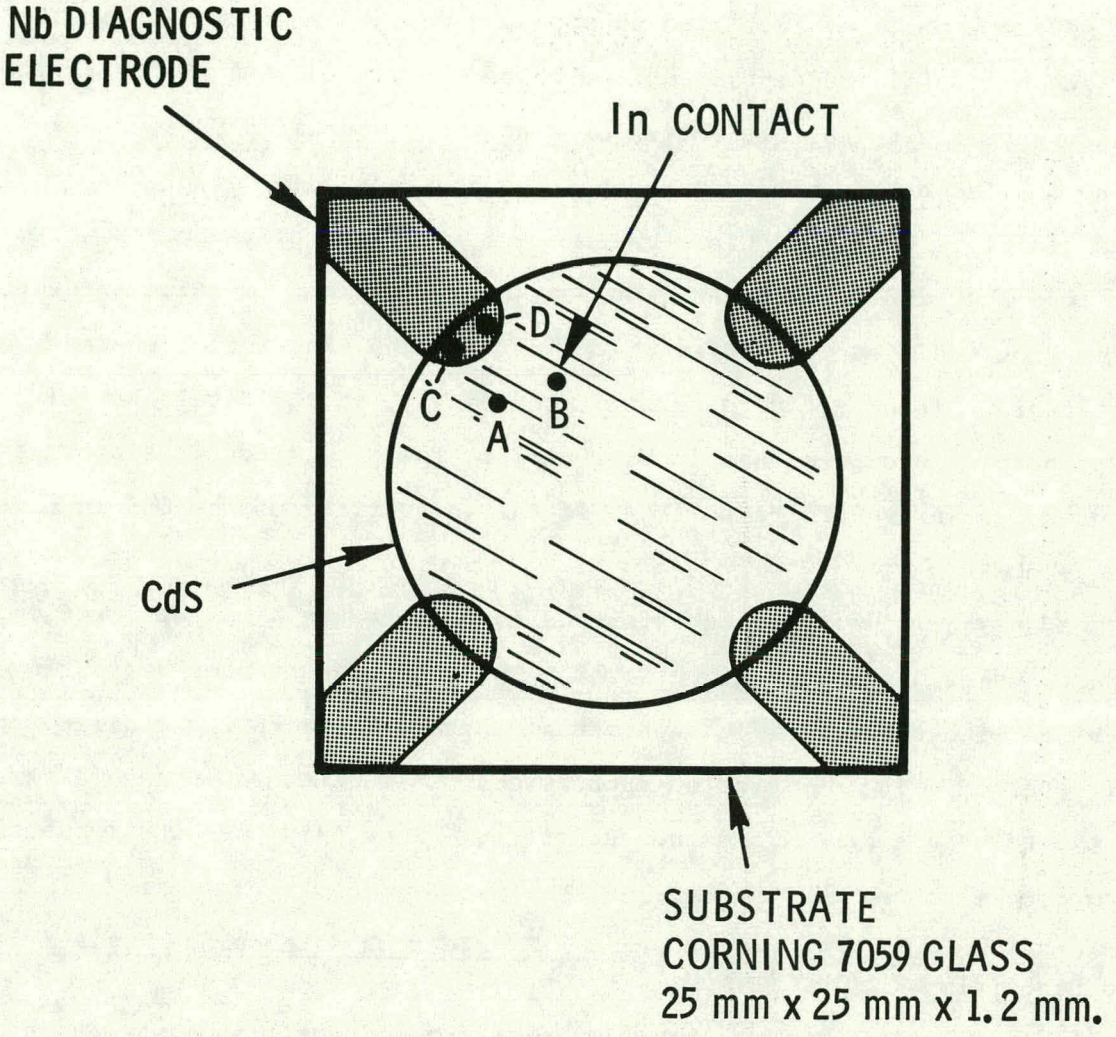



FIG. 10 Diagnostic electrode configuration used for measuring resistivity of CdS and $Cu_xS$ coatings.

Therefore the glass-calibration substrate temperature used in cell fabrication was reduced from the 300°C value which had been used previously to a value of 250°C (actual surface temperature of about 300°C for substrate with Nb rear electrode). See Section 4.1.

The second example of localized substrate temperature gradients relates to the functionability of pre-deposited electrodes. Early studies of the effect of In doping on the electrical properties of reactively sputtered CdS were made by depositing the CdS coatings onto pre-deposited Nb electrodes having the configuration shown in Fig. 10.[7,9,10] Glass-calibration substrate temperatures were, in general, less than 250°C. However, subsequent examinations revealed evidence of a region having modified properties at the edge of the electrodes, where a temperature gradient is expected to exist. Accordingly, in the data taken with the modified apparatus and presented in this report, the Nb diagnostic electrodes were deposited at near-room temperature on the top surface of the CdS in a second pumpdown.

In the subsequent discussion reference is made to the glass calibration temperature, and estimates are given for the true temperature when discussing data obtained with the unmodified apparatus. Data taken with the modified apparatus were obtained using calibration factors that include the emittance differences between the reference plates and the substrates. Thus only the actual substrate temperatures are quoted for these cases.

### 3.2 Effect of Substrate Temperature and $H_2S$ Injection Rate on CdS Resistivity and Deposition Rate.

Sputtering is characterized by relatively large deposition areas, as compared to evaporation, but the deposition rates are lower. CdS reactive sputtering studies during the first year of the program revealed that the relatively low sputtering deposition rates make it difficult to control the coating resistivity by the same off-stoichiometry method that is used in evaporation.[2] At the substrate temperatures of interest for depositing coatings with reasonable crystallographic perfection (>200°C), the CdS accumulation rate is limited by re-evaporation. In the case of deposition by evaporation, the flux leaving the source is

rich in Cd, and coatings deposited at low temperatures (<150°C) are dark in appearance and highly conducting. As the substrate temperature is increased, the excess Cd content is reduced by re-evaporation and the coating resistivity increases. In depositing solar cell quality CdS by evaporation, a substrate temperature of typically about 230°C is used to provide coatings with resistivities in the 1 to 3 Ω-cm range.[11] The substrate temperature must be controlled carefully. Slight increases in temperature result in large increases in resistivity.

In the reactive sputtering case, the arrival flux is low enough so that re-evaporation tends to limit the CdS accumulation rate to the extent to which the Cd can interact with the sulfur flux and form near stoichiometric CdS. Thus the reactive sputtering process was found to be similar to "three temperature" evaporation.[2] This is shown by the data in Figs. 11 and 12, which were obtained during shakedown tests of the modified apparatus. The cathode current density was ~4 mA/cm$^2$. The deposition rates were determined from interferometric measurements of the thickness of coatings about 500 nm thick using a Sloan Angstrometer--Tolansky method.[12] The reduction in deposition rate with increasing substrate temperature at a fixed $H_2S$ injection rate is shown in Fig. 11. The dependence of the deposition rate on the $H_2S$ injection rate at a fixed substrate temperature is shown in Fig. 12. At high $H_2S$ injection rates (A in Fig. 12) the deposition rate is limited by the available Cd flux. At low injections rates (B) the sulfur flux is rate limiting. An increase or decrease in substrate temperature shifts the entire curve downward or upward according to the type of relationship shown in Fig. 11.

The coating material which survives re-evaporation and accumulates, tends to approach to relatively stoichiometric composition and therefore to exhibit a relatively high resistivity.[2] Figure 13 shows the resistivity versus substrate temperature for CdS coatings deposited using a 99.9999% Cd target with no attempt to obtain an off-stoichiometric state. The coatings were approximately 200 nm thick and were deposited using the unmodified apparatus shown in Fig. 2 at a

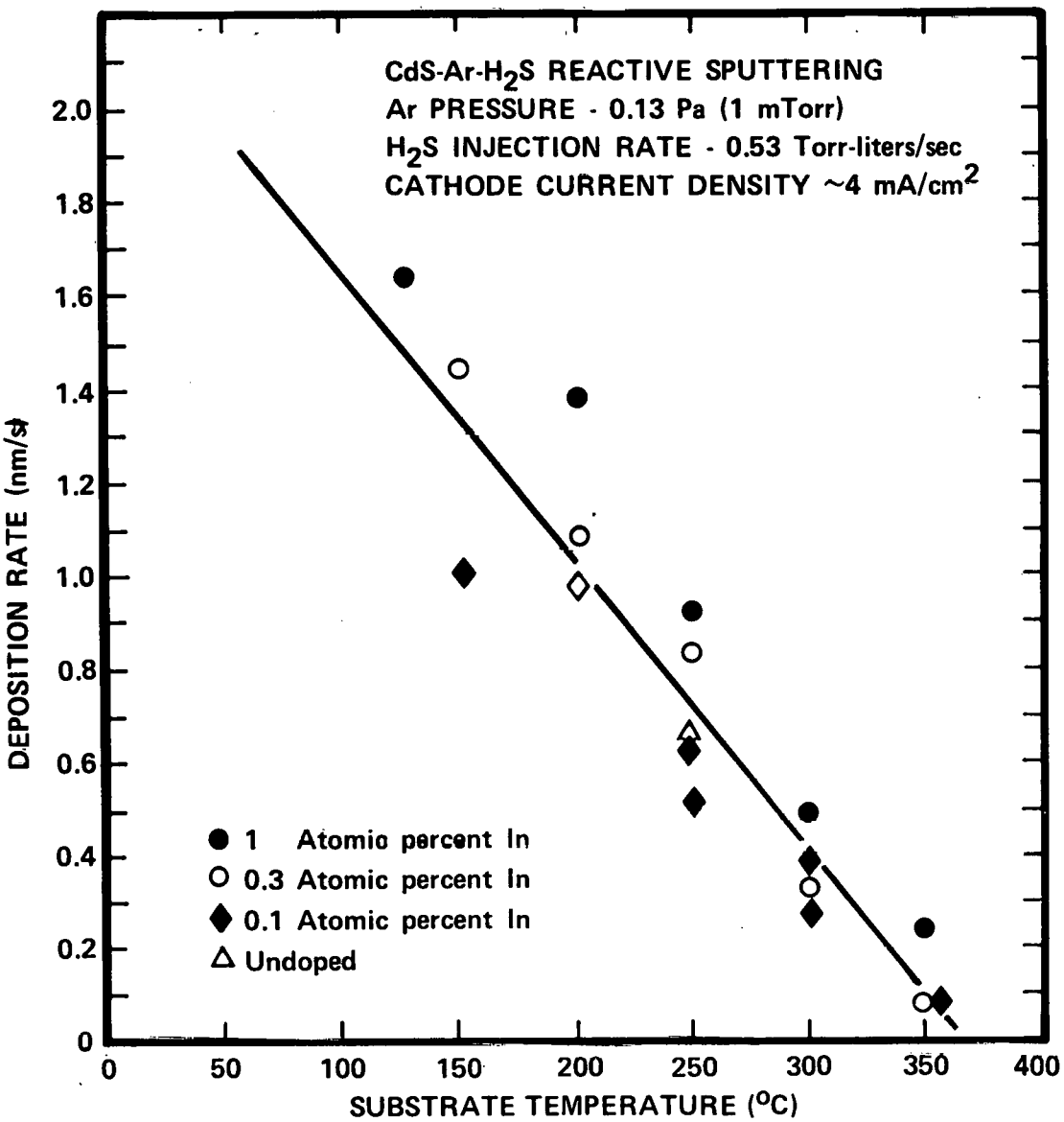



FIG. 11 Dependence of CdS deposition rate on substrate temperature at fixed $H_2S$ injection rate in the modified apparatus.

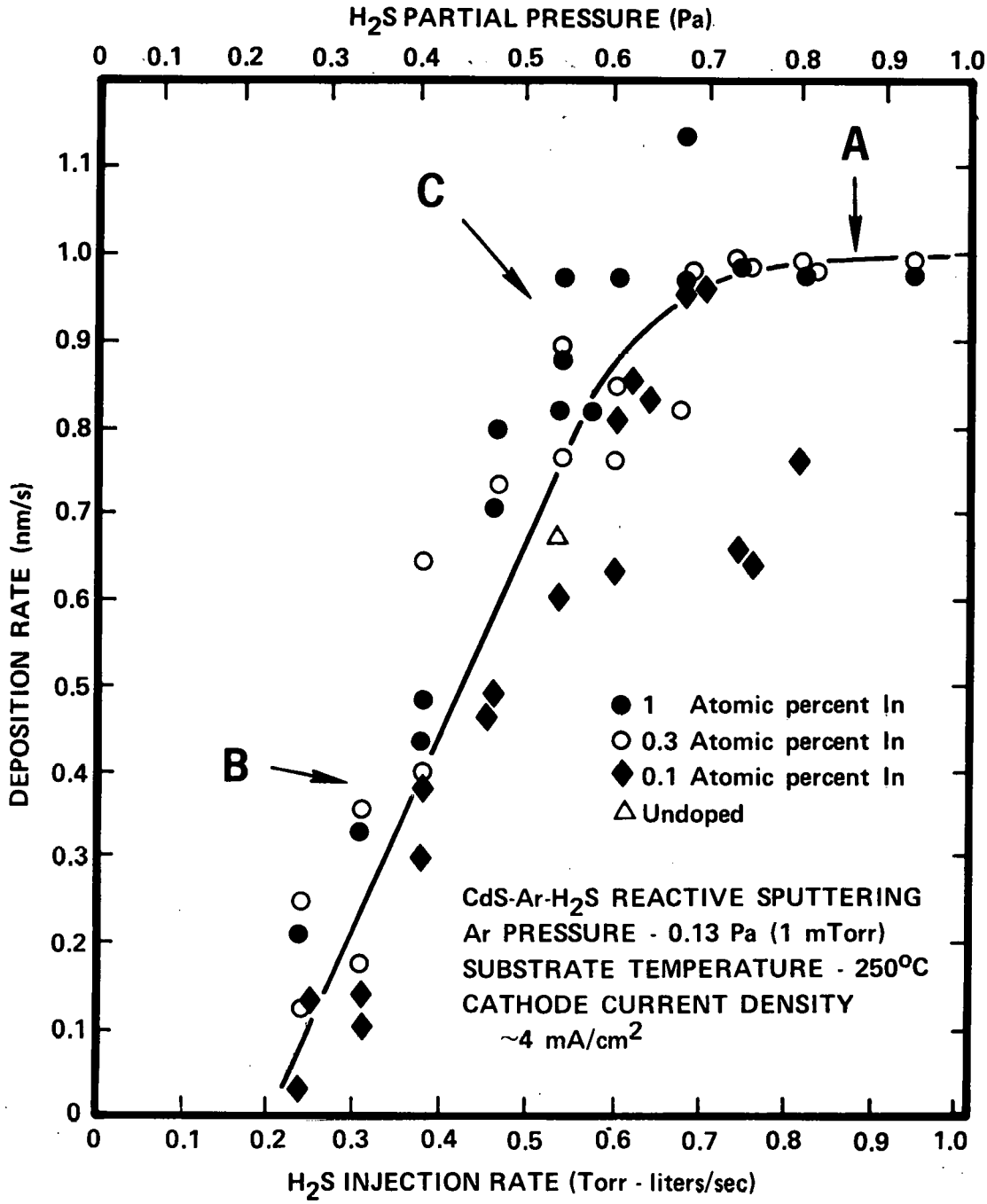



FIG. 12 Dependence of CdS deposition rate on $H_2S$ injection rate at fixed substrate temperature in the modified apparatus.

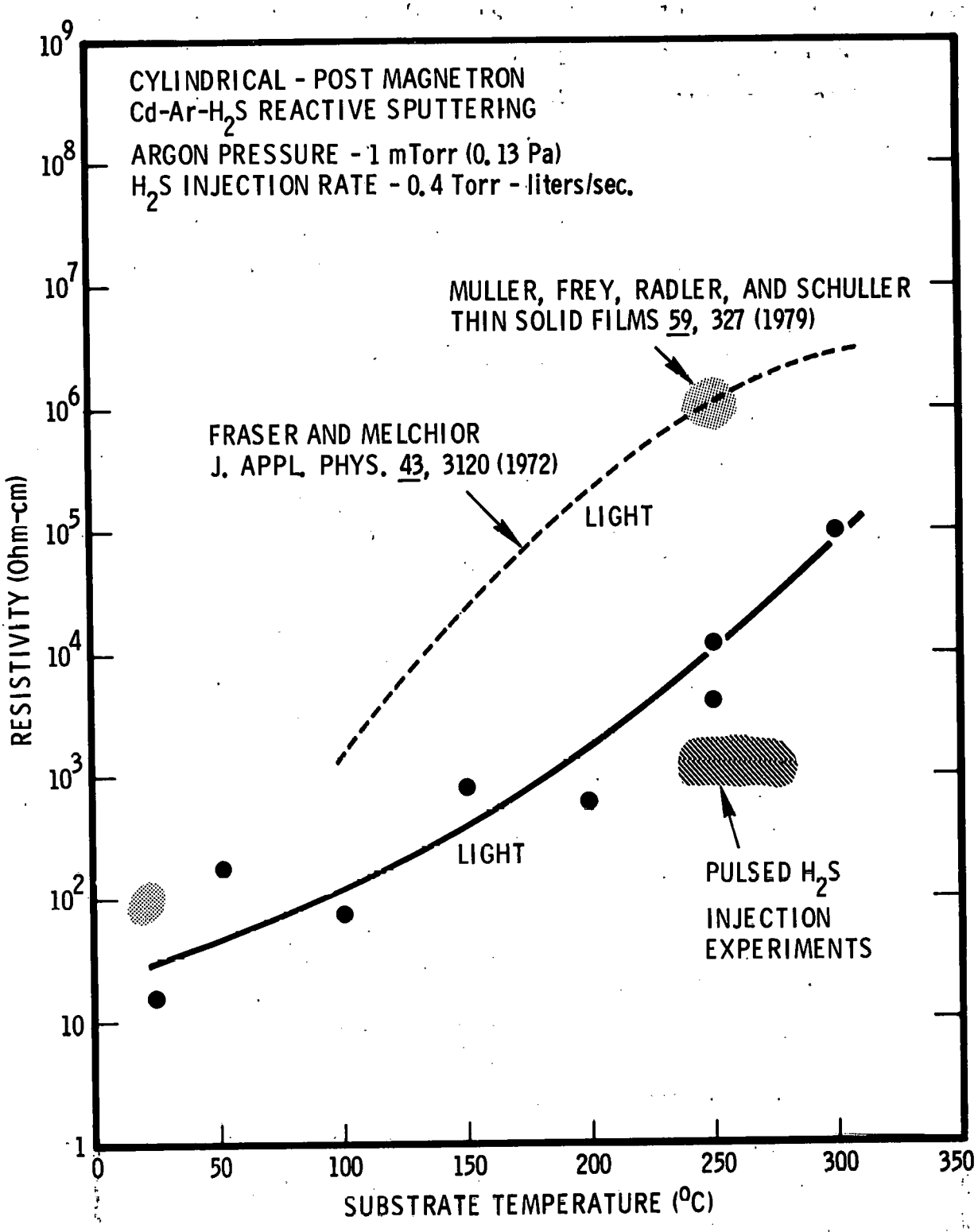



FIG. 13 Resistivity versus substrate temperature for sputtered undoped CdS coatings.

cathode current density of ~4 mA/cm$^2$. The $H_2S$ injection rate corresponded approximately to the knee of the curve (point C) in Fig.12. The resistivity measurements were made by depositing the coatings onto glass substrates having pre-deposited Nb diagnostic electrodes in the configuration shown in Fig. 10. The coatings were highly photoconductive, undergoing order-of-magnitude increases in resistivity in the dark. The data in Fig. 13 were obtained under laboratory fluorescent lighting. Data reported by Fraser and Melchior,[13] for coatings deposited by sputtering from a CdS target in an Ar-$H_2S$ mixture and measured under a microscope lamp, are also shown, along with similar data obtained by Muller et al.[14] At low substrate temperatures (~50°C) all the data are in approximate agreement (resistivity 10 to $10^2$ Ω-cm). However, the resistivities of the reactive sputtered coatings exhibit a less dramatic rise with temperature than do the resistivities of other coatings shown.

The top curve in Fig. 14 shows the resistivity versus $H_2S$ injection rate for undoped CdS coatings deposited at a substrate temperature of 250°C. The coatings were approximately 500 nm thick and were deposited onto glass substrates using the modified apparatus shown in Fig. 3. Niobium diagnostic electrodes for making the resistivity measurements were deposited onto the top surface of the CdS coatings in a separate deposition operation. It is seen that starving the deposition flux for $H_2S$ does indeed reduce the resistivity, but that this reduction is not adequate to provide the resistivities of a few hundred Ω-cm or less that are desired for fabricating thin film solar cells.

Thus it was concluded from data obtained during the first year, and reconfirmed by additional and more detailed data obtained during the present program, that special deposition procedures would be required to provide the desired resistivity control. The development of these procedures was a major part of Task 2 in the present program.

3.3 Resistivity Control by Indium Doping (Task 2.1)

The objective of this task was to determine the relationship between the Cd-Zn target doping level and the resultant electrical resistivity in $Cd_{1-x}Zn_xS$

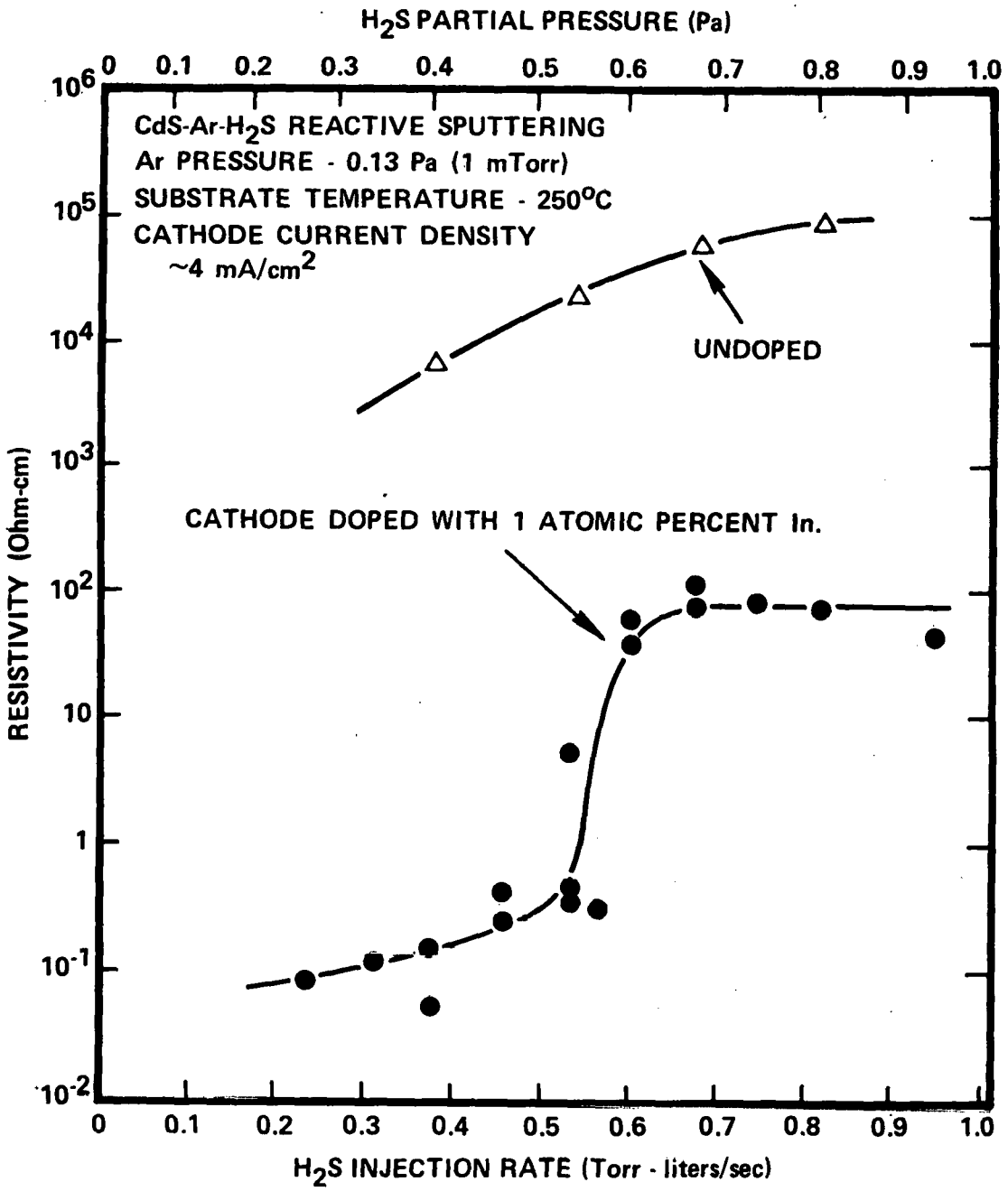



FIG. 14 Resistivity versus $H_2S$ injection rate for reactively sputtered CdS coatings.

coatings deposited by cylindrical magnetron reactive sputtering. CdS rather than (Cd,Zn)S was selected for this work because of the greater amount of available data on the performance of undoped evaporated CdS solar cells, and because of the need for comparing performance between the doped sputtered cells and undoped cells in order to identify any deleterious effects on cell performance which might result from the In doping.

Two methods were used to implement the In doping in the present program:

1) Sputtering from an In doped Cd target in an $H_2S$-Ar working gas.
2) Diffusion of In into a reactive sputtered CdS layer by depositing the CdS over an In coated substrate.

General doping level requirements were established during the first year by co-sputtering from Cd and In targets.[2] These results are summarized in Fig. 15. Note that a substrate temperature of 300°C was used in this early work. Based on the results given in Fig. 15, Cd targets were obtained from Cominco American (Spokane, Washington) with overall purity levels of 99.9999% and In doping levels of 0.1, 0.3 and 1.0 atomic percent.

Figures 14, 16, and 17 show the resistivity versus $H_2S$ injection rate for coatings deposited from the three different doped cathodes onto substrates maintained at 250°C. The coatings were deposited onto glass substrates using the modified apparatus with the vacuum interlock. The cathode current density was $\sim 4$ mA/cm$^2$. Niobium diagnostic electrodes were deposited onto the top surface of the CdS coatings in a separate deposition operation. The doping is seen to rapidly increase in effectiveness as the $H_2S$ injection rate is reduced sufficiently to pass into the range (B in Fig. 12) where the $H_2S$ flux, and not the Cd flux, is rate-limiting in the deposition process. Microprobe measurements for the 1 at. percent In case confirmed that the high resistivity coatings deposited at large $H_2S$ injection rates did indeed contain the 1 at. percent of In. The high resistivity doped coatings were photosensitive. The data in the figure were taken in laboratory fluorescent lighting. The low resistivity doped coatings were slightly photosensitive, undergoing resistivity increases of about 30% in the dark.

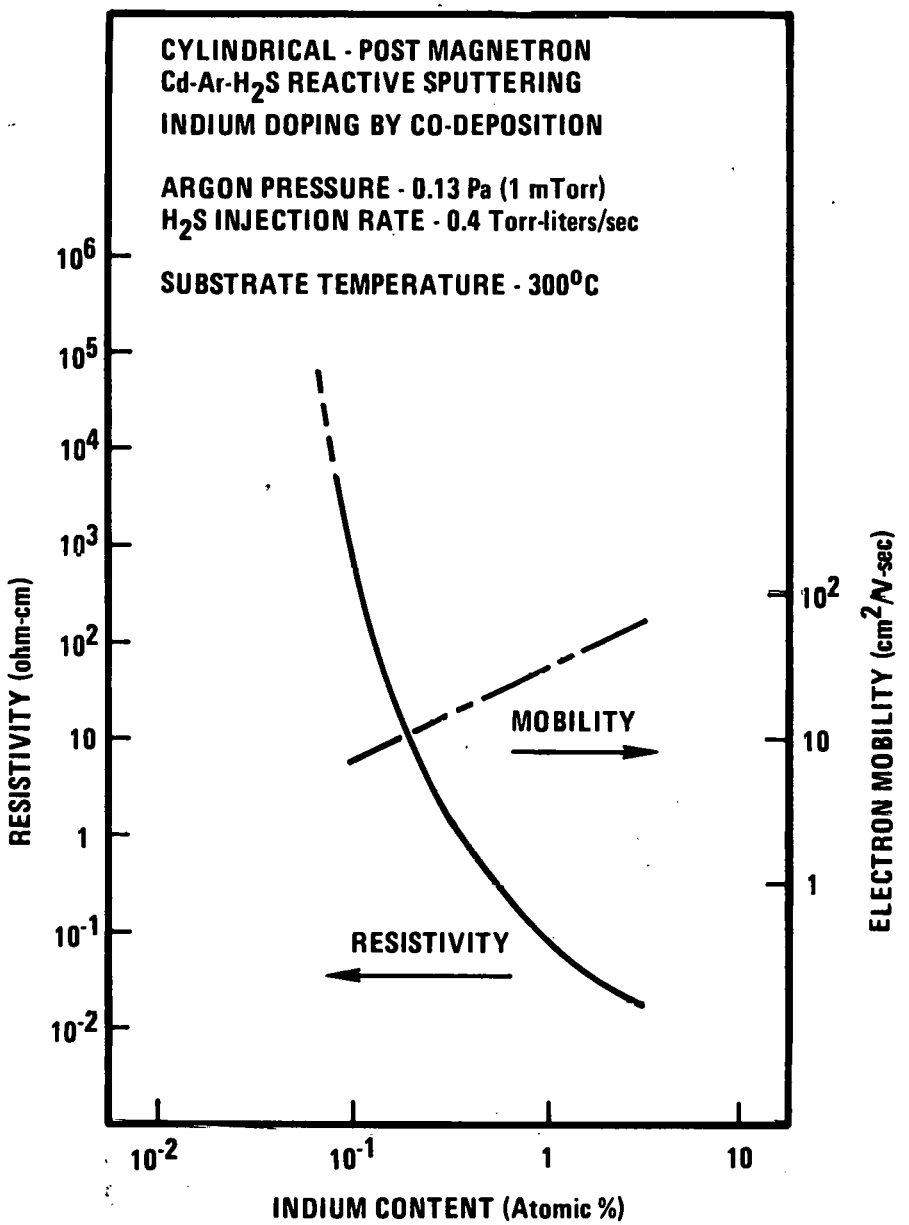



FIG. 15 Resistivity of reactively sputtered CdS versus indium content. Data from Ref. 2

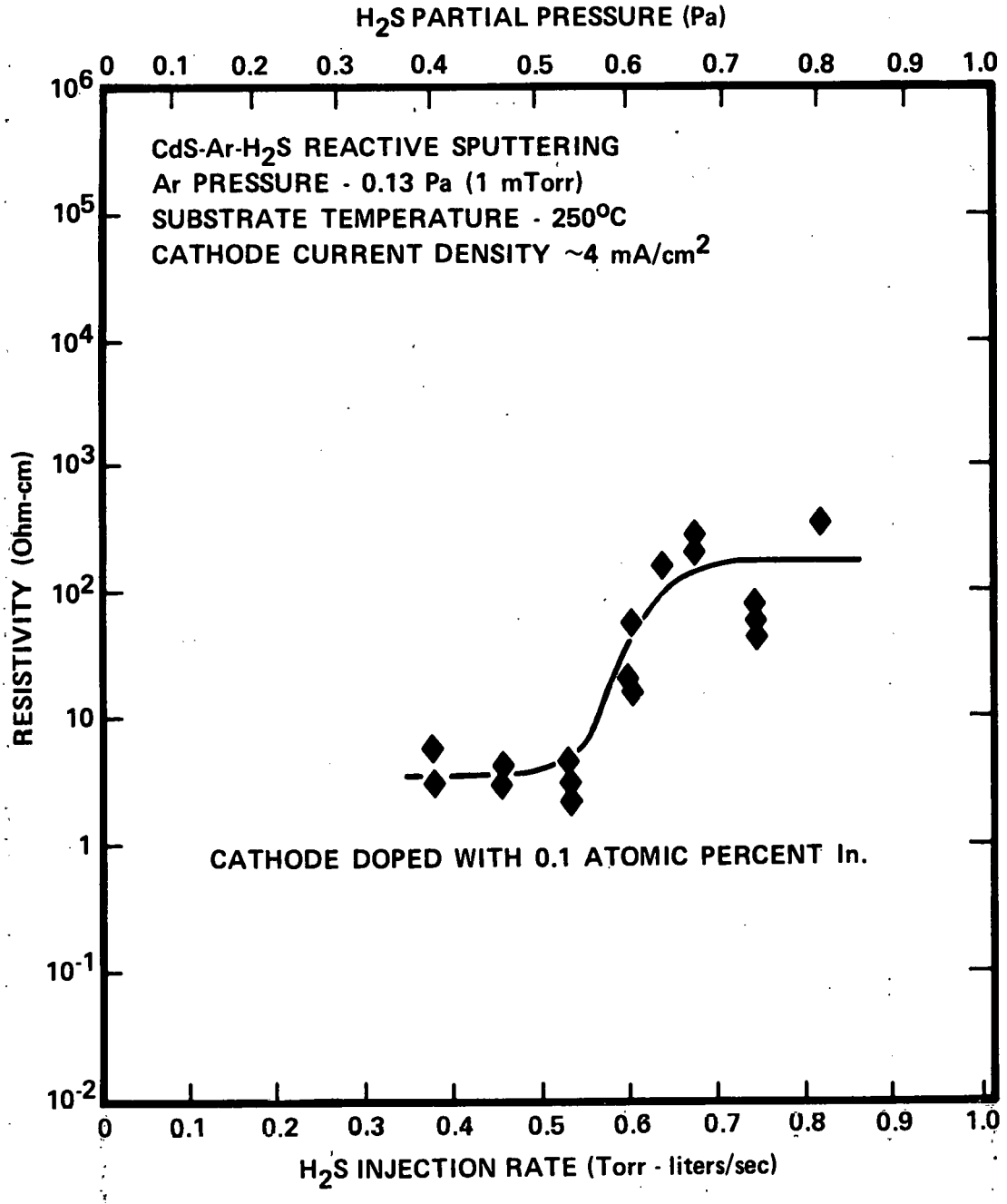
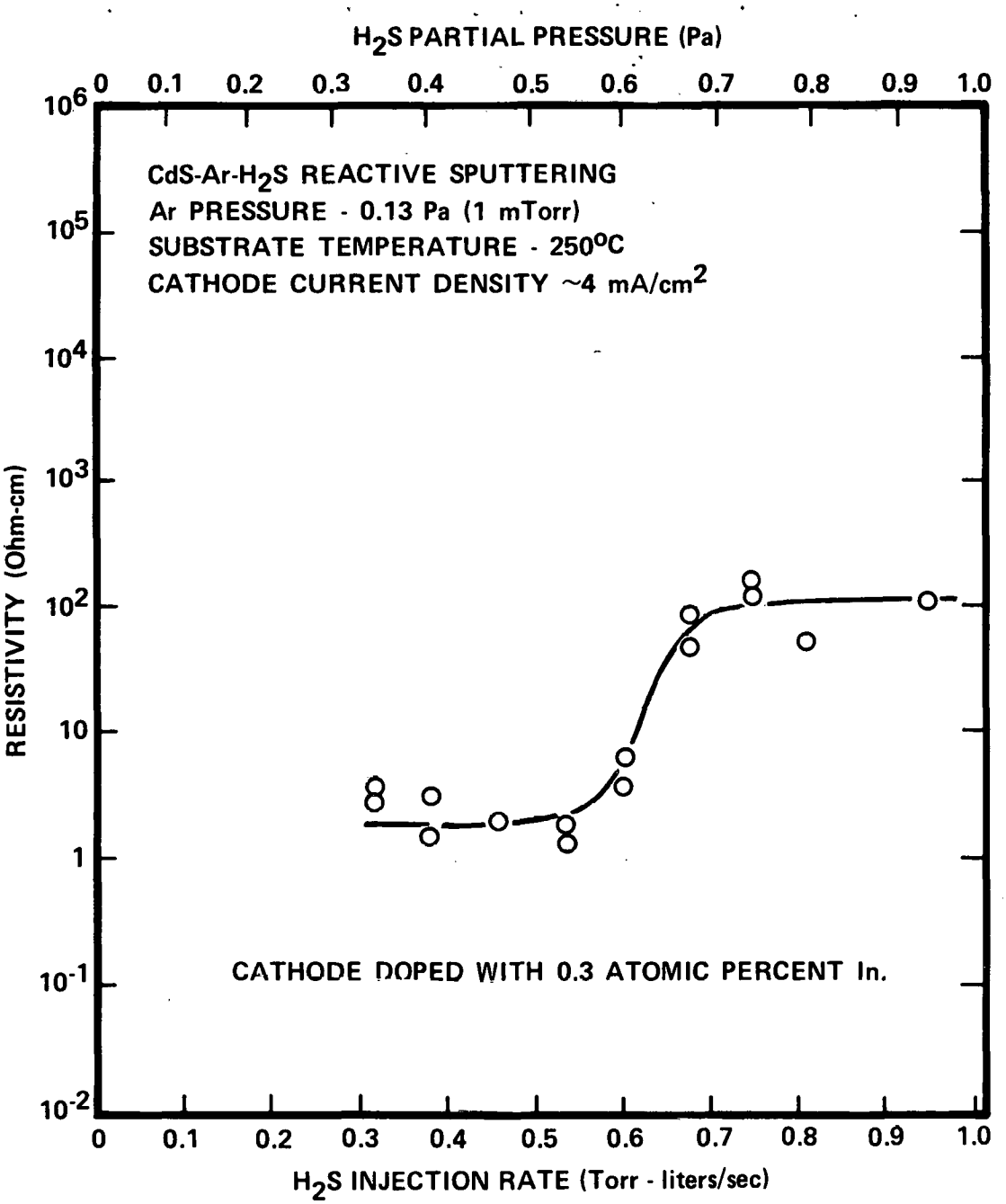



FIG. 16 Resistivity versus $H_2S$ injection rate for CdS coatings reactively sputtered from target containing 0.1 atomic percent indium.




FIC. 17 Resistivity versus $H_2S$ injection rate for CdS coatings reactively sputtered from target containing 0.3 atomic percent indium.

The strong dependence of the doping efficiency on the $Cd/H_2S$ flux is believed to be due to the compensating effect of Cd vacancies. The probability for self compensation is relatively high for large band-gap materials such as the highly ionic II-VI semiconductors.[16] Thus, in order to obtain a high conductivity in both undoped and doped CdS, it is necessary that the Cd vacancy level be minimized.[17] Equilibrium calculations indicate,[1,18] and numerous experimental observations have confirmed, that a high Cd vapor pressure over CdS crystal minimizes Cd vacancy formation and enhances the effectiveness of In doping. Approximate calculations based on reasonable acceptor ionization energies predict that compensation by doubly ionized Cd vacancies should be a major effect for the partial pressures of Cd and $S_2$ that are accessible in sputtering.[1] Woodbury prepared doped CdS samples by diffusing In into the crystals.[19] The In levels ranged from about $10^{17}$ $cm^{-3}$ to $10^{20}$ $cm^{-3}$. The carrier concentrations were found to be much lower than the doping levels (e.g., doping level of $10^{20}$ $cm^{-3}$ yielded carrier concentration of $8x10^{17}$ $cm^{-3}$), unless the samples were fired in saturated Cd vapor at 800°C for a few hours. With this extreme type of treatment a 1:1 correspondence was obtained between the In content, as determined spectroscopically, and the room temperature carrier concentration, for carrier concentrations ranging from $10^{20}$ $cm^{-3}$ down to the donor impurity level of about $10^{17}$ $cm^{-3}$. In more recent work[20] a CdS single crystal was doped by pressing measured amounts of high purity In metal into the surface and annealing at 855°C for 430 hours in an evacuated tube containing metallic Cd. Electrical measurements indicated that less than 3% of the estimated $3.7x10^{18}$ $cm^{-3}$ In impurity atoms caused an electron to be provided to the conduction band.

Figure 18 shows the resistivity versus substrate temperature for CdS coatings deposited by reactive sputtering from the targets doped with 0.1, 0.03 and 1.0 atomic percent of In. The coatings were about 500 nm thick and were deposited using the modified apparatus shown in Fig. 3. The data for coatings doped with 1 atomic percent In are compared with similar data obtained with the unmodified apparatus and seen to be consistent. The coatings were deposited at a cathode current density of about 4 $mA/cm^2$ and an $H_2S$ injection rate (0.53 Torr-liters/sec)

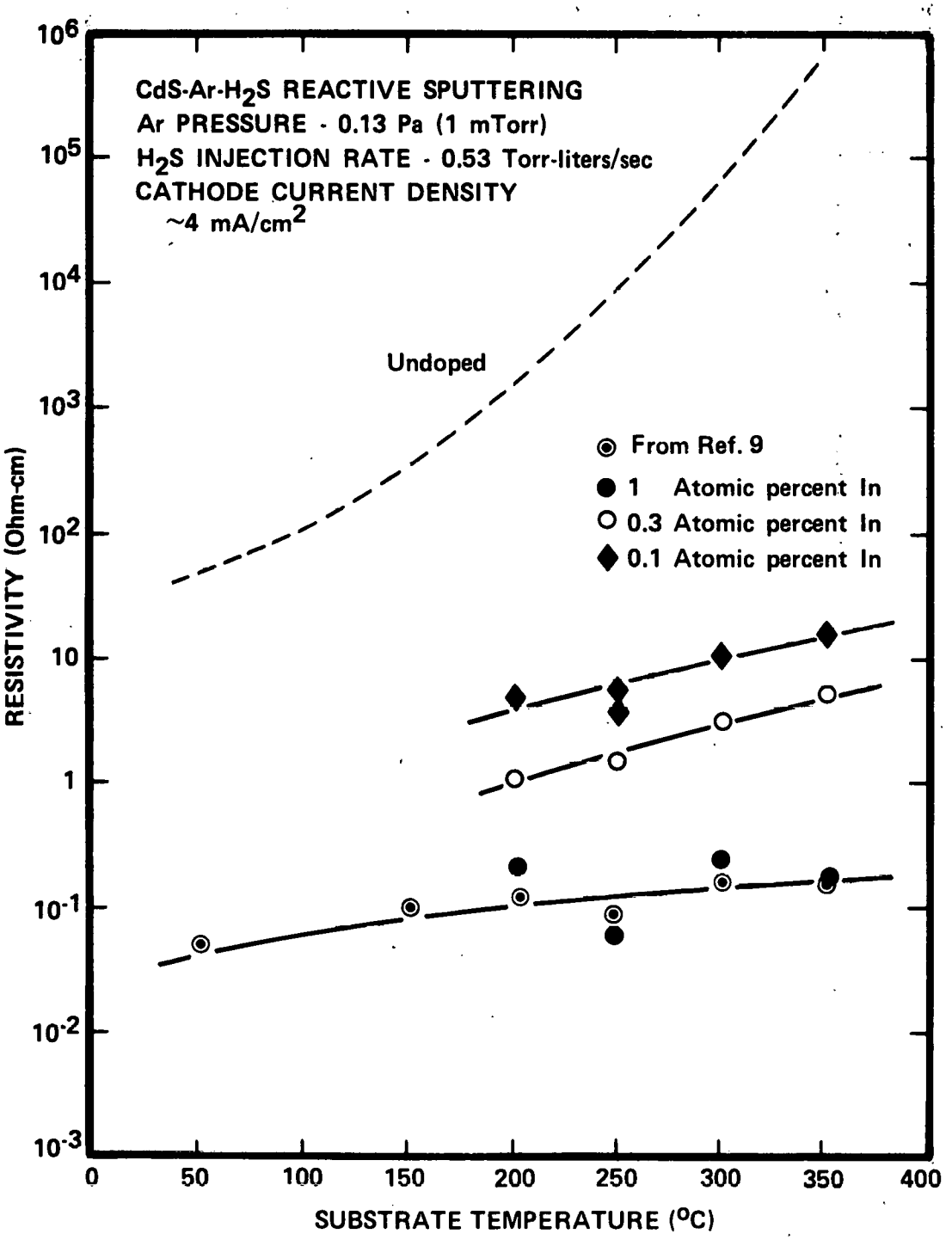



FIG. 18 Resistivity versus substrate temperature for CdS coatings reactively sputtered from indium doped targets.

which permits effective use of the In dopant (see Figs. 16, 17, and 18) without too great a loss in deposition rate (see Fig. 12). The resistivity values at In contents of 0.3 and 1 atomic percent are consistent with the data shown in Fig. 15. The new resistivities at 0.1 atomic percent are lower than previously reported values,[2,10] probably because of the use of a more optimum $H_2S$ injection rate.

Van der Pauw measurements were made on the 1 atomic percent doped coatings at Lockheed. These measurements yielded electron mobilities of about 10 $cm^2/V\text{-}sec$ and carrier concentrations of about $7x10^{18}$ $cm^{-3}$. This implies that about 3.5% of the In atoms contributed electrons to the conduction band, a conclusion which is consistent with results reported for single crystals.[20]

Figure 19 shows the CdS film resistivity as a function of substrate temperature for coatings doped by the third method--diffusion of In from an In-coated substrate. The coatings were about 5000 nm thick and were deposited using the unmodified apparatus shown in Fig. 2. The target was a 99.9999% Cd cathode. The coatings were deposited over a 50 nm thick layer of In. If this In were to be uniformly distributed within the CdS, it would correspond to a doping level of 2 atomic percent. The method is seen to be reasonably effective in producing doping levels in a desirable range (10 to 100 $\Omega$-cm) over the substrate temperature range of interest. Van der Pauw measurements at Lockheed yielded mobilities of about 25 $cm^2/V\text{-}sec$, with carrier concentrations in the range from $3 \times 10^{15}$ $cm^{-3}$ to $5 \times 10^{16}$ $cm^{-3}$.

3.4 Resistivity Control by Off-Stoichiometry (Task 2.2)

Two approaches were examined to achieve resistivity control by off-stoichiometry.

1) Pulsed $H_2S$ gas injection
2) Post-deposition heat treatment

From an equilibrium point of view the density of Cd atoms absorbed on the surface of a growing CdS coating, and thus the Cd content within the coating, are related to the Cd partial pressure over the surface. In the pulsed gas

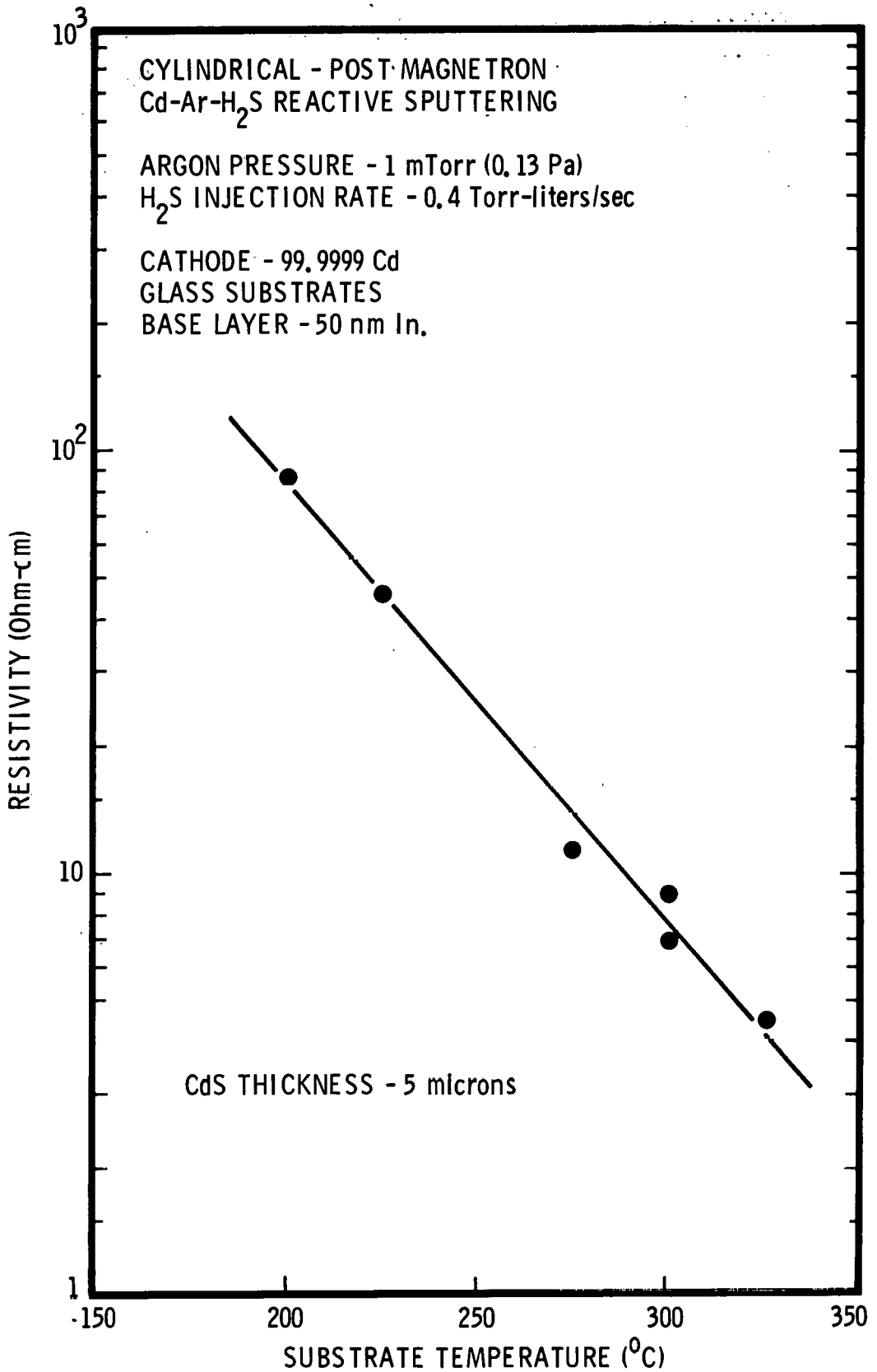



FIG. 19 Resistivity versus substrate temperature for CdS coatings doped by diffusion from pre-deposited In layer.

injection approach, the $H_2S$ injection is periodically terminated, thereby permitting the cathode to periodically deliver a high Cd flux to the surface of the growing CdS coating. This flux will largely re-evaporate but will cause the time-averaged Cd adatom surface density to be larger than it would be under steady state $H_2S$ injection. Studies of the Cd accumulation and re-evaporation on heated CdS coated surfaces were made through in situ resistivity measurements.[9] Order of magnitude reductions in resistivity have been achieved for coatings deposited in the 250°C to 300°C temperature range using the pulsed $H_2S$ injection method.[9] The data are indicated by the shaded region in Fig. 13. Solar-illuminated resistivities of $10^2\,\Omega$-cm and electron mobilities of 20 $cm^2$/V-sec have been measured for these coatings. The results of the pulsed deposition studies are promising. However, the resistivities still need to be reduced by a factor of three or more. Another point requiring attention is the observation that the resistivities of the pulse-deposited coatings increased significantly when the coatings were heat treated in $H_2$ at 350°C. Nevertheless, the highest all-sputtered cell efficiencies achieved to date have been for devices fabricated with undoped CdS layers deposited using the pulsed $H_2S$ gas injection. See Section 4.1. The efficacy of the pulsed $H_2S$ injection rate was further illustrated by the observation that low resistivity In-doped (1 at. percent In) coatings were obtained with pulsed injection at average $H_2S$ injection rates that would yield high resistivity coatings under steady state conditions. Pulsed injection with doped or undoped cathodes can also reduce the occurrence of arcing.

Various groups have reported success in reducing the resistivity of CdS coatings by post-deposition heating in $H_2$.[21,22] In our work heat treatment for 30 min at temperatures of 250°C and 350°C in an atmospheric pressure mixture of 15% $H_2$ - 85% $N_2$ did not significantly change the resistivity of the sputtered coatings. Attempts to heat-treat the samples in $H_2$ plasma discharges at moderate temperatures (~350°C) were unsuccessful in producing significant reductions in coating resistivity without causing coating damage.[10] Future work will examine higher annealing temperatures and the effects of annealing in a Cd vapor flux.

3.5 $Cu_2S$ Deposition Studies (Task 2.3)

A detailed study of the influence of the $H_2S$ injection rate, and to some extent the substrate temperature, for $Cu_xS$ coatings deposited onto glass substrates was conducted during the previous program.[2,23] It was determined that two types of copper sulfide coatings could be formed, depending on the deposition conditions. One material, which formed primarily on substrates at 130°C, exhibited a resistivity of about $10^2\ \Omega$-cm and a relatively high density of Cu nodules (several thousand nm in size) on the surface. X-ray diffraction indicated that the material was primarily chalcocite, with a small djurleite content which increased with increased $H_2S$ injection rate. The Cu nodule density decreased with increasing $H_2S$ injection rate. The second material, which formed primarily on low temperature (35°C) substrates, exhibited a resistivity of about $10^{-2}\ \Omega$-cm, and a much lower density of nodules which virtually disappeared with increasing $H_2S$ injection rate. X-ray diffraction showed this material to be a mixture of chalcocite and djurleite, becoming primarily djurleite with increasing injection rate. The absorption coefficients of the high resistivity material, and the low resistivity material deposited at low $H_2S$ injection rates, were found to be in excellent agreement with those previously reported for chalcocite.[23]

Additional studies during the present program have confirmed that the same basic relationship between the $Cu_xS$ coating properties and the $H_2S$ injection rate and substrate temperature applies also for coatings deposited onto CdS. The data are summarized in Fig. 20. High substrate temperatures (135°C and 150°C have been explored) promote formation of the high resistivity material, while low temperatures at high $H_2S$ injection rates generally produce the low resistivity copper sulfide. As a general rule, the high resistivity material possessed a relatively high density ($5 \times 10^6/cm^2$) of the Cu surface modules.[9] An important observation was that the Cu nodules under a Au contact grid electrode did not result in a cell short.

The data given in Fig. 20 were obtained before the apparatus modification discribed in Section 2 was completed. Evidence was seen to indicate that the

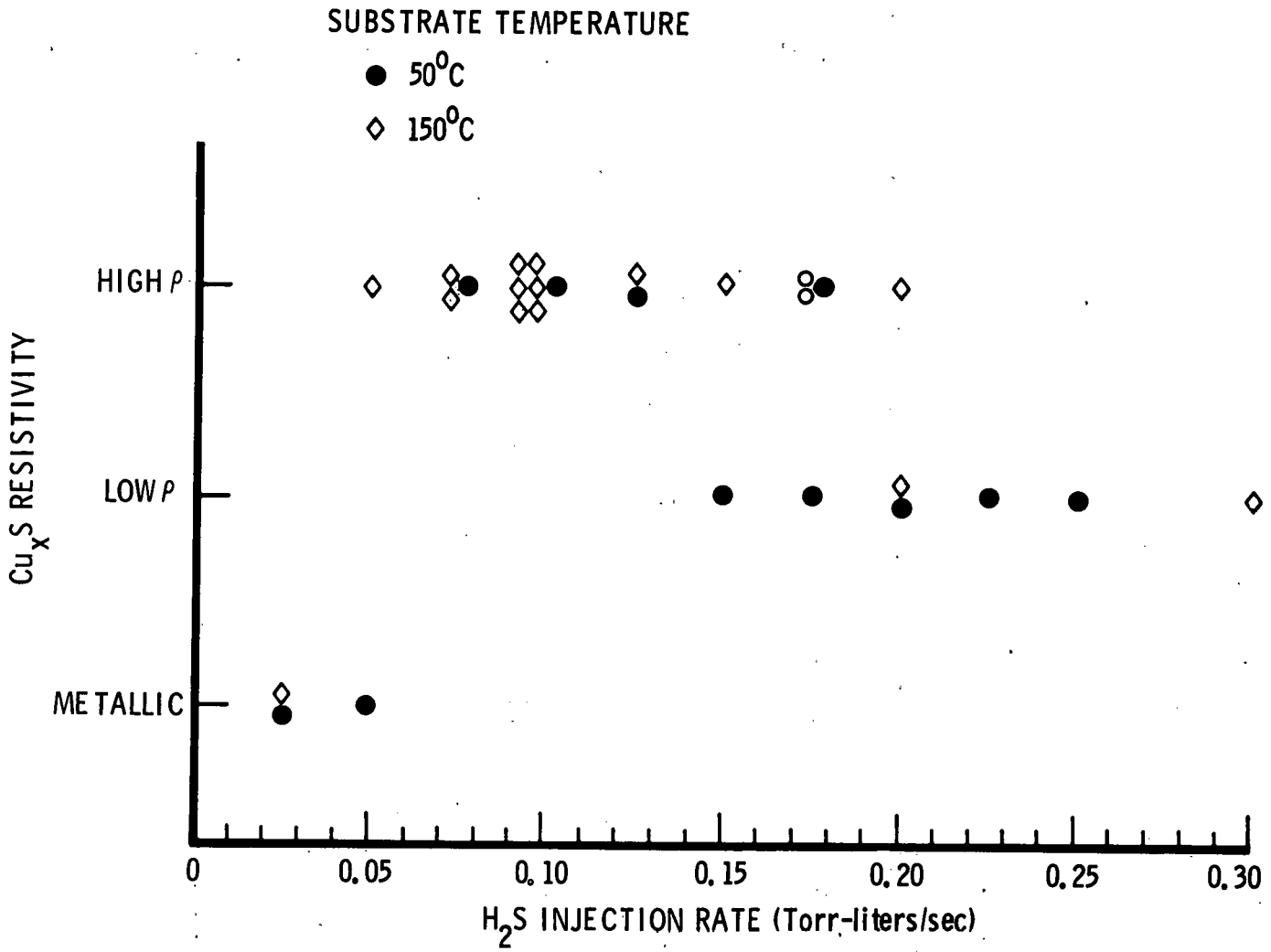



FIG. 20 Schematic representation of dependence of resistivity of $H_2S$ injection rate for $Cu_xS$ coatings deposited onto CdS during present program.

accumulation of coating material on shield walls introduced a memory of previous deposition conditions and therefore compromised the reproducibility. (See discussion of role of shield surfaces on reactive sputtering in Section 2.1.) Performance data on the reactive sputtering of copper sulfide with the modified apparatus are now being accumulated.

## 4. DEVICE-MATERIAL PARAMETER OPTIMIZATION (TASK 3)

### 4.1 Cell Fabrication

Glass plates (Corning 7059), 25 mm x 25 mm x 1.2 mm, are used as substrates. The cells fabricated during the previous program and during the first quarter of the present program were of the general form shown in Fig. 21. A Nb rear electrode 100 nm thick was deposited onto the glass substrates in a separate pumpdown. These precoated substrates were then stored and used as required in the multi-source deposition chamber shown in Fig. 2. A set of three substrates was coated at one time. Predeposition pumping was typically to a pressure of $10^{-4}$ to $10^{-3}$ Pa ($7 \times 10^{-7}$ to $7 \times 10^{-6}$ Torr). In most cases the CdS or $Cd_xZn_{1-x}S$ layers were 3000 to 5000 nm thick, and were deposited at a glass calibration temperature of 300°C (substrate temperature ~350°C) over an In layer about 50 nm thick. The In layer was used to assure an ohmic contact to the Nb electrode. The substrates were then allowed to cool in $H_2S$ to 150°C (required about 20 min), and the $Cu_xS$ layer was deposited. Finally a top Au electrode was applied in a separate chamber. Antireflective top layers have not been used thusfar.

Table I summarizes the performance of selected cells fabricated during the course of the program. Cell #274 is representative of the best heterojunction devices fabricated during the previous program. The devices were characterized by particularly low short circuit currents and fill factors. Cell #274 had a 3000 nm CdS layer deposited at about 350°C. The layer was doped by co-deposition from an In source that is estimated to have produced an In content of about 0.3 atomic percent and a resistivity of about 3 Ω-cm. The low short circuit current in these cells was due in part to the top electrode, which was a small circular

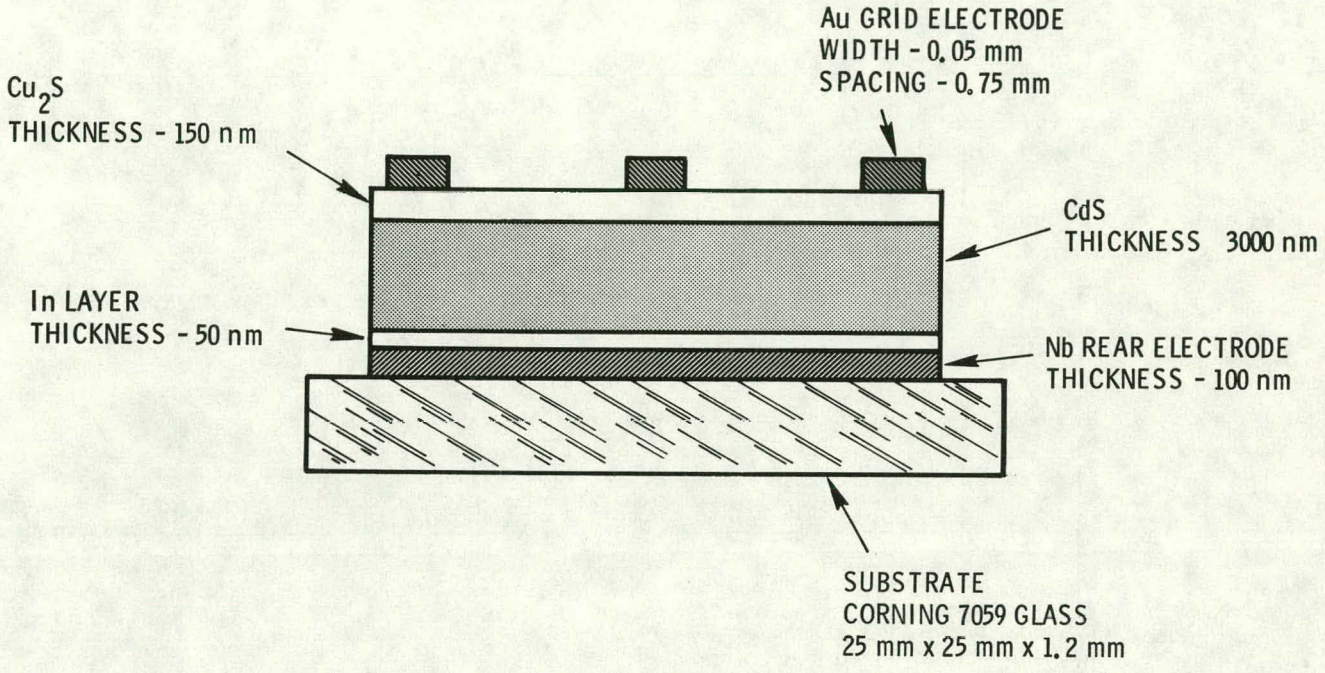



FIG. 21 General configuration of sputter-deposited solar cells fabricated during the first quarter of the program.

TABLE I

PERFORMANCE OF SELECTED SOLAR CELLS

| Cell Number | $J_{sc}$(mA/cm$^2$) | $V_{oc}$(V) | FF | (%) | Insulation | Comment |
|---|---|---|---|---|---|---|
| 274 | 0.19 | 0.3 | 0.28 | 0.03% | 53 mW/cm$^2$ | CdS cell fabricated on previous program. |
| 401 | 3.0 | 0.35 | 0.37 | 0.4% | 94 mW/cm$^2$ | In-doped (CdZn)S |
| 653 | 3.5 | 0.43 | 0.41 | 0.6% | 107 mW/cm$^2$ | Undoped CdS pulsed gas injection. |
| 917 | 2.5 | 0.32 | ~0.3 | ~0.25% | 107 mW/cm$^2$ | Composited CdS structure (see Fig. 23) |
| 967 | 6.9 | 0.40 | 0.43 | 1.2% | 107 mW/cm$^2$ | Hybrid cells sputtered CdS. Dry CuCl-$Cu_2S$ |

Au pad rather than a grid array.

Cell #401 is representative of the best cells fabricated during the first quarter of the present program. This cell has a 4500 nm thick In doped Cd(Zn)S layer which was deposited at about 350°C (calibration temperature of 300°C) by reactive sputtering from a Cd target containing 10 atomic percent Zn and 2 atomic percent In. The 150 nm thick $Cu_2S$ layer was deposited at 150°C as described above. Cells in this group had Au grids consisting of 1000 nm thick lines, 0.05 mm wide, spaced on 0.75 mm centers (see Fig. 21) which were sputter-deposited using a mechanical mask. The short circuit current is seen to be significantly improved over the cells fabricated during the first year.

During studies of the CdS deposition process (see Section 3.1) it was discovered that when a metallized glass substrate, is heated to ~ 250-300°C at the deposition station, the actual temperature is about 50°C greater than the calibration temperature for a glass substrate. The difference results from the reduced emittance of the metallized surface. Evidence was also seen which indicated that a substrate temperature of 350°C (calibration temperature of 300°C) results in the passage of an electrically active impurity from the Nb into the (Cd,Zn)S. Therefore in subsequent cell fabrication the glass calibration temperature for the CdS deposition was reduced to 250°C (substrate temperature 300 C). When this was done it was found that the In layer shown in Fig. 21 was no longer required to provide an ohmic contact to the Nb rear electrode. Therefore use of the In layer was discontinued.

About the end of the first quarter, it was decided that CdS rather than (Cd,Zn)S cells would be fabricated for the remainder of the program. This was done because a great deal more data are available on the fabrication and performance of solar cells with evaporated CdS than with (Cd,Zn)S. These data form a useful basis for comparison in optimizing the performance of the all-sputter-deposited cells.

Cell #653 is representative of several cells that were fabricated midway through the program. The CdS layers were nominally about 4000 nm thick and were

deposited at a substrate temperature of about 300°C (calibration temperature of 250°C) using the pulsed gas injection method discussed in Section 3.4. No In base layer was used over the Nb rear electrode. The $Cu_xS$ layers were deposited at a substrate temperature of 150°C. These cells have provided the best performance achieved thusfar for all-sputter deposited cells. The as-deposited cells exhibited short circuit currents of about 1 mA/cm$^2$ and open circuit voltages of about 0.27V under a solar simulator at an incident power of 107 mw/cm$^2$. Annealing in $H_2$ at 200°C for 2 minutes raised the open circuit voltage to about 0.43V and the short circuit current to about 3 mA/cm$^2$. The IV characteristic for cell #653, which had a efficiency of about 0.6%, is shown in Fig. 22. Additional annealing for 2 min at 200°C caused a drop in short circuit current to about 2.5 mA/cm$^2$.

A few cells with In-doped CdS layers having In concentrations of from 0.1 to 1 atomic percent were fabricated. Deposition temperatures were in the range from 250°C to 300°C. In the 1% In case the as-deposited cells did not exhibit a barrier, probably because of electron tunneling, since the depletion layer thickness is estimated to have been of the order of 10 nm for the high conductivity CdS (see Fig. 18). Annealing in $H_2$ at 200°C did not develop the barrier. The cells doped with 0.1% In exhibited excellent as-deposited diode characteristics with open circuit voltages of about 0.1V.[1] However, annealing for two 60 min segments at 150°C in an $H_2$-Ar atmosphere did not improve the photovoltaic performance.

Cell #917 is representative of cells which were fabricated with the composite CdS structure shown in Fig. 23. The composite layers were formed by sputtering in sequence from doped (1 at. percent In) and undoped cathodes. The thickness of the undoped region adjacent to the junction was varied between 100 and 500 nm thick. The highly doped material ($\sim$0.1 $\Omega$-cm) extended from this region to the rear electrode. The substrate temperature during CdS deposition was 300°C (glass calibration temperature of 250°C). The reactively sputtered $Cu_2S$ layers were about 150 nm thick. They were deposited at a substrate temperature of 150°C.

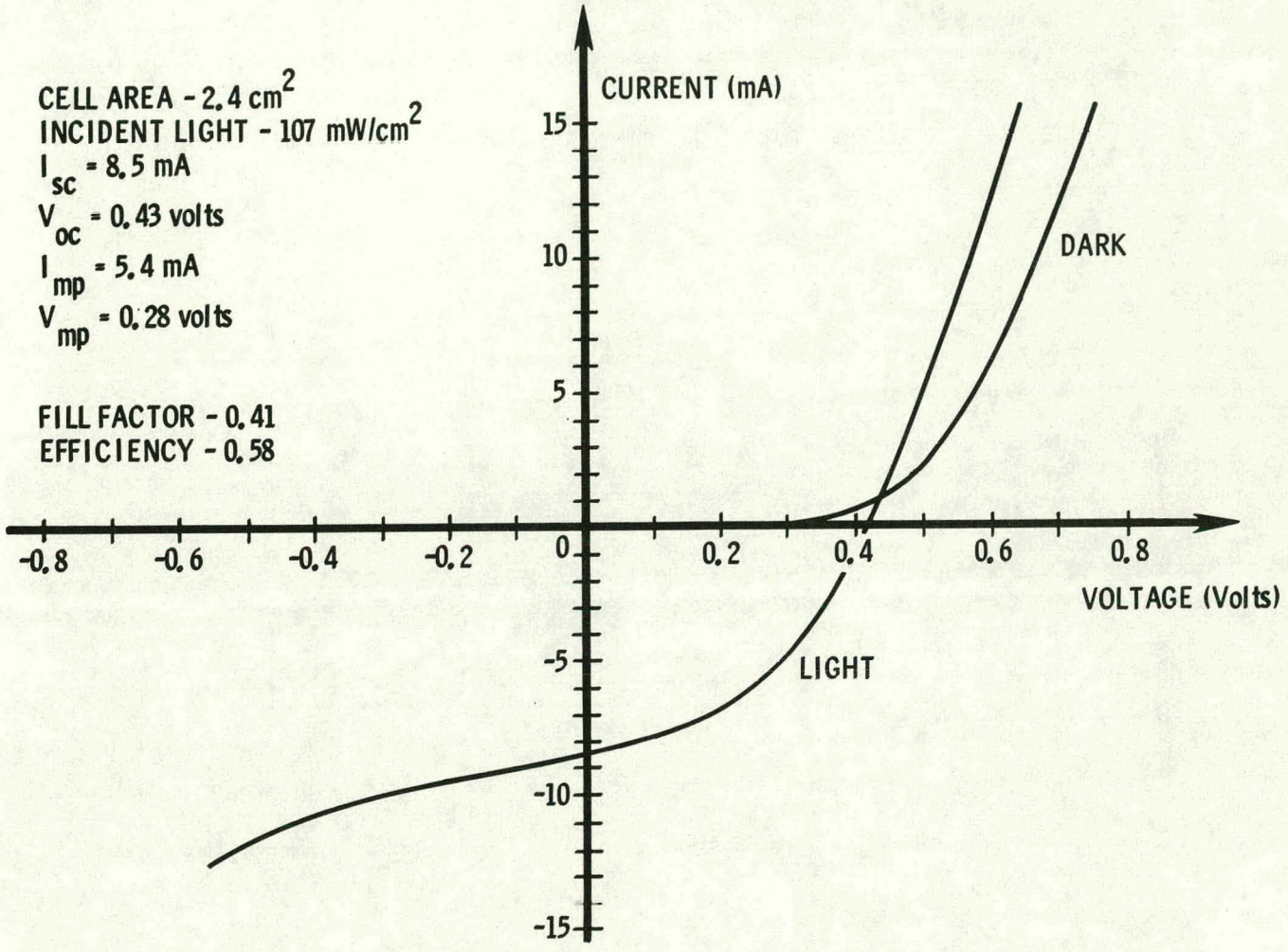



FIG. 22 Current-voltage characteristic for best all-sputter-deposited cell which was fabricated during present program.

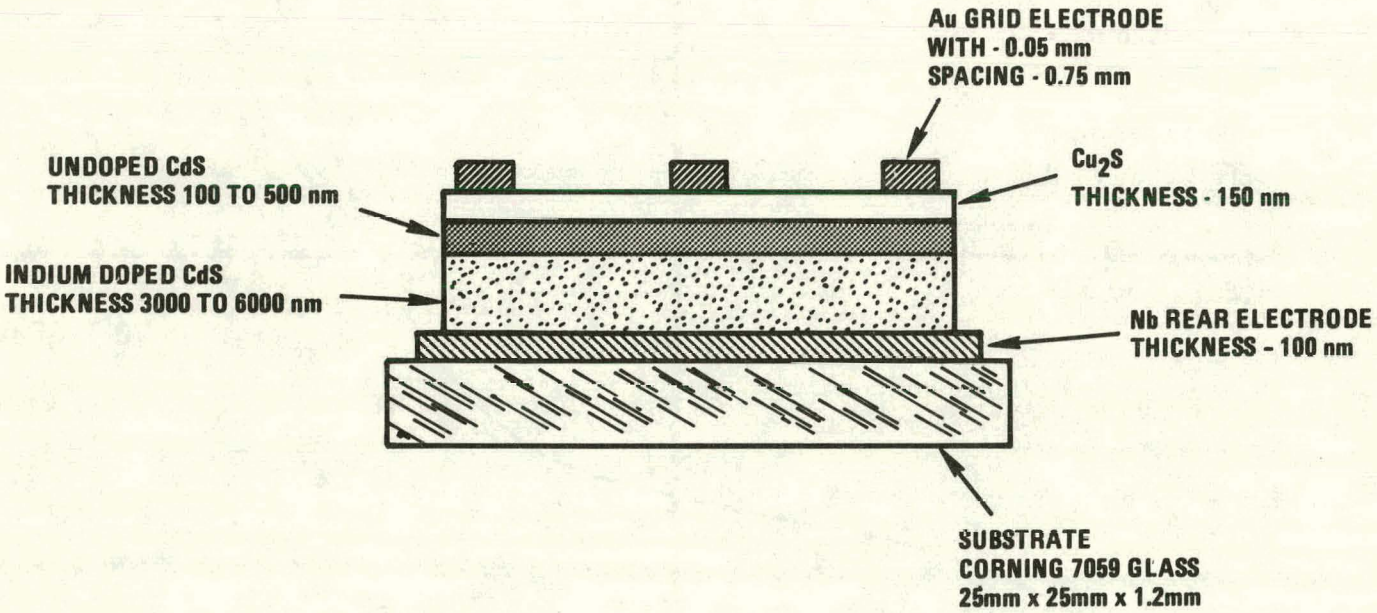



FIG. 23 General configuration of sputter-deposited cells with composite CdS layer.

The doping profiles of the composite CdS layers were investigated at Lockheed using capacitance-voltage measurements.[24] The measurements show carrier concentrations of about $5 \times 10^{-13}$ $cm^3$ in the undoped regions and verify a large increase in carrier concentration ($\sim 10^{17}$ $cm^{-3}$) at distances below the junction that are consistent with the deposition thicknesses for the undoped layers. The cells were slightly photovoltaic in their as-deposited state ($V_{oc} \sim 0.05V$). Annealing the cells for three 60-min periods at 175°C in $H_2$ raised the open circuit voltage and short circuit current, in the case of cell #917, to 0.32V with a short circuit current to 2.5 $mA/cm^2$ as indicated in Table I.

A series of relatively thick (5000 to 11000 nm) reactively sputtered CdS coatings were deposited onto Nb-coated glass and sent to the Institute of Energy Conversion (IEC) at the University of Delaware, where $Cu_2S$ layers were applied by both the wet and dry CuCl processes. The objective was to obtain an improved understanding of the differences between the evaporated and sputtered CdS layers. The CdS coatings were deposited from undoped Cd targets and from targets doped with 0.1 atomic percent of In. The cells to be given the wet process were heated for 30 sec in boiling $H_20$ and then textured by immersion in a 25% (by volume) HCl solution at 60°C for from 5 to 10 sec. (The texturing of the cell doped with 0.1 atomic percent In was terminated after 5 sec because of a severe reaction with the HCl solution.) Following texturing the cells were processed for 10 sec in the standard IEC CuCl "wet process" bath that is used for evaporated cells.[25] The dry $Cu_2S$ layers were formed by evaporating enough CuCl to react to an approximate $Cu_2S$ thickness of 250 nm. The reaction to form $Cu_2S$ from the CuCl was accomplished by placing the sample in flowing $H_2$-Ar gas at 70°C for 5 minutes. After cooling in this atmosphere, the samples were removed and the $CuCl_2$ rinsed off using de-ionized water. Finally the samples were dried in an $H_2$-Ar flow.

The completed heterojunctions were then returned to Telic where Au grid electrodes of the type shown in Fig. 21 were applied. Finally the cells were sent to Lockheed for testing and heat treatment.

The wet processed cells all exhibited a high conductance from the grid lines through to the Nb rear electrodes, although some photovoltaic response was recorded. The dry processed cells exhibited good as-deposited diode characteristics.[1] The dry processed cells with the 0.1% In-doped CdS exhibited a low open circuit voltage (~0.1V) which did not improve significantly on heat treatment at 150°C in $N_2$-$H_2$. This result is similar to that which was observed for all-sputter-deposited cells with 0.1% In doped CdS as described previously. Cell #967 in Table I is representative of the hybrid cells with the dry processed $Cu_2S$ on the undoped CdS. The CdS layer for this cell was about 5000 nm thick. It was deposited at 300°C (calibration temperature of 250°C). The as-deposited open circuit voltage was ~0.32V. However, after 60 min of annealing in $H_2$-Ar at 150 C, the open circuit voltage and short circuit current increased significantly. When several grid lines that covered regions of compromised performance were removed, the remaining area (2.8 $cm^2$) yielded an open circuit voltage of 0.40V and a short circuit current of ~7 $mA/cm^2$. This hybrid cell is the most efficient device fabricated during the program (>1%). The low fill factor is believed to be due to the relatively high resistivity of the CdS, which was deposited with no particular attempt to control its resistivity.

Several cells with the composite structure shown in Fig. 23 were fabricated as part of the shakedown on the modified deposition apparatus. These cells were deposited with a reduced In content (0.1 rather than 1 atomic percent) in the doped CdS "back-up" layer. The as-deposited cells yielded open circuit voltages of about 0.2V and single-grid short circuit currents of about 0.1 mA. Subsequent heat treatments at 150°C did not improve the photovoltaic performance.[1]

4.2 Cell Fabrication Techniques.

At the beginning of the program a problem of shorting due to pin holes was encountered on the Au gridded cells. Improved handling and storage of the pre-metallized substrates was found to greatly reduce this problem.[7] By the midpoint of the program the fabrication techniques had improved to the point where it was common to have no grid-to-rear-electrode shorts among the 31 grid lines.[26]

Cell fabrication with the modified apparatus (Fig. 3) is just beginning. When this apparatus is used, the Nb rear electrodes are deposited in-situ as part of the cell deposition process. This procedure reduces the substrate handling prior to depositing the semiconducting layers and should further reduce the frequency of flaws in the cells.

The mechanical deposition masks are held in close contact to the substrates, using the magnetic hold-down method shown in Fig. 24. Additional work is required to improve the mask contact and therefore the width of the grid lines. The thickness of the glass reduces the magnetic field strength at the mask plane to the point where the magnetic force has difficulty in overcoming forces generated in the mechanical mask by cold working.

4.3 Analysis of Cell Performance

Table II summarizes the performance of one of the best all-sputter-deposited cells prepared on the present program with that for a high performance planar CdS cell fabricated at the Institute of Energy Conversion.[27] The IEC cell should probably be considered as a "nearly planar" cell, since a slight etch of the CdS was used prior to the deposition of the $Cu_2S$ by CuCl evaporation and ion exchange reaction. The estimated optimum performance of a truly planar cell is also shown for comparison. This estimate is based on: (1) top grid electrode system with 90% transmission, (2) $Cu_2S$ layer thickness of 150 nm, (3) Mulder's single crystal $Cu_2S$ optical data,[28] (4) zero recombination on the $Cu_2S$ front surface, (5) total reflection at the Nb rear electrode, (6) a $Cu_2S$ minority carrier diffusion length of 100 nm, (7) a fill factor of 0.8 (arbitrarily selected) and (8) an open circuit voltage of 0.54V (assumed). See Fig. 36 of Ref. 2.

The difference between the short circuit currents in the IEC cell and the idealized planar cell is believed to be indicative of the light trapping which occurs in the IEC cell because of the slight surface texture which is built into these cells. The sputtered cells have a very planar structure because of the smooth glass starting substrate and the absence of an etch sequence between the CdS and $Cu_2S$ depositions. This is apparent in the intense CdS and $Cu_2S$ interferenc

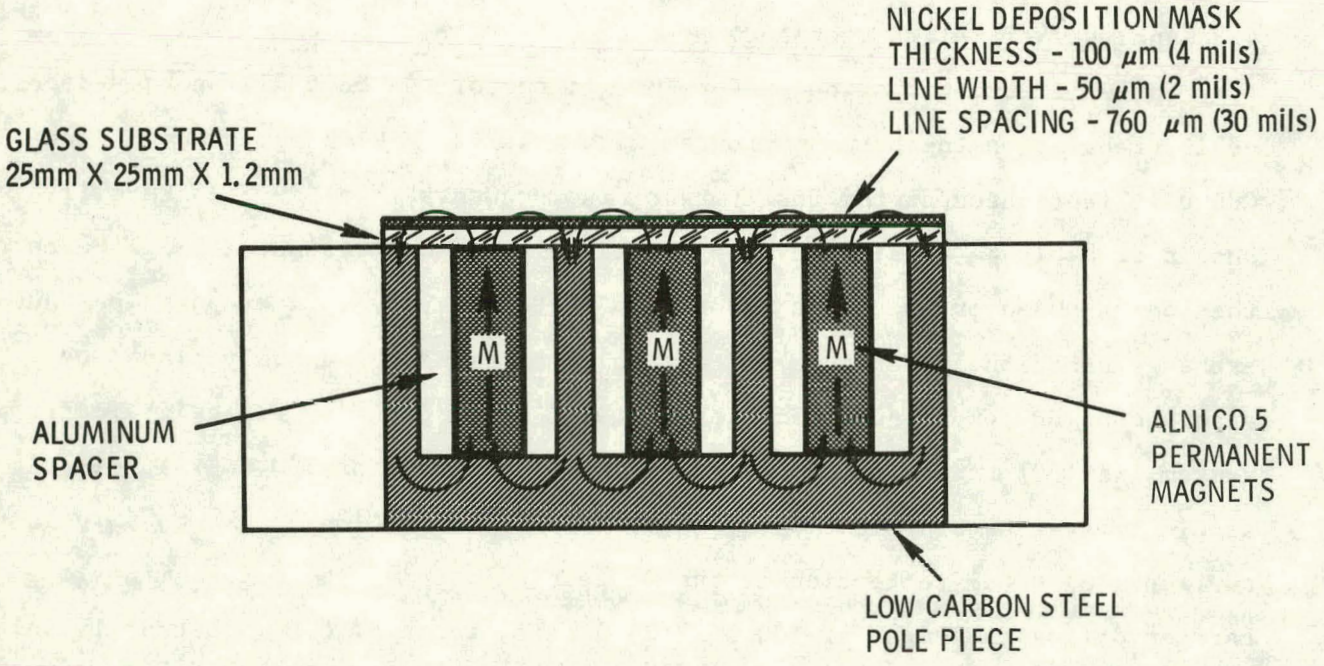



FIG. 24 Magnetic hold-down configuration used for mechanical deposition masks.

TABLE II

COMPARATIVE PERFORMANCE OF SELECTED SOLAR CELLS

| Cell | $J_{sc}$* ($mA/cm^2$) | $V_{oc}$ (V) | FF | $\eta$ (%) |
|---|---|---|---|---|
| Cell deposited using pulsed $H_2S$ injection method cell 653 | 3.5 | 0.43 | 0.41 | 0.58 |
| Institute of Energy Conversion planar cell with evaporated CdS. $Cu_2S$ deposited by dry process after slight each. (From Ref. 27) | 21 | 0.54 | 0.72 | 8 |
| Estimated optimum performance for planar cell with $L_n$ = 100 nm. (See Ref. 1) | 15.5 | 0.54 | 0.8 | 6.5 |

* Based on illumination intensity of 100 $mA/cm^2$.

pattern which has been observed in the sputter-deposited cells.[29] Therefore an assessment of the performance of the sputter-deposited cells can probably best be made by comparing their performance with that of the idealized planar cell. Picking $J_{sc} \sim 3$ mA/cm$^2$, $V_{oc} \sim 0.4$V, and FF $\sim 0.4$ as being representative of the best sputtered cells, we conclude that:

$J_{sc}$ for sputtered cell is $\sim 20\%$ of planar cell goal,

$V_{oc}$ for sputtered cell is $\sim 75\%$ of planar cell goal,

FF for sputtered cell is $\sim 50\%$ of planar cell goal.

Cells with sputtered CdS and CuCl dry processed $Cu_2S$ yielded $J_{sc} \sim 7$ mA/m$^2$. Nevertheless, it is clear that the primary problem with the sputter-deposited cells is the low $J_{sc}$. The second most serious problem is the low fill factor.

There are three factors that can cause a low $J_{sc}$:

1) Failure to absorb radiation and produce photocarriers because of a low absorptivity in the $Cu_2S$.
2) Failure of the photocarriers to reach the junction because of a high front surface recombination velocity or a low minority carrier diffusion length in the $Cu_2S$.
3) Failure of the photocarriers to pass over the p/n junction because of interface recombination.

Measurements of the short circuit current spectral response for a cell (#824), with the configuration of cell #917 and a short circuit current of 3.7 mA/cm$^2$, indicate that all of the photocurrent is generated within the $Cu_xS$ layer.[29] This is consistent with previous work[23] which showed that the absorption characteristics of $Cu_2S$ layers deposited using cylindrical magnetrons are equivalent to those reported for chalcocite, and with that of other workers who have fabricated cells with efficiencies of several percent using sputter deposited $Cu_2S$ layers on single crystal and evaporated CdS.[30,31] These observations imply that the problem is at the p/n junction. Neglecting shunt currents, one can write

$$J_{sc} \sim J_L \quad \eta_c \qquad (2)$$

where $J_L$ is the light-generated current reaching the junction from the $Cu_2S$ and $\eta_c$ is the junction collection efficiency.[32] If we use a $J_{sc}$ of 3 mA/cm$^2$ for the sputter-deposited cells, and assume that the $J_L \sim 15$ mA/cm$^2$ (ideal planar cell), we obtain $\eta_c \sim 0.2$ from Eq (2). Collection efficiencies for high performance evaporated cells are about 0.95. The $J_L$ for the sputter-deposited cells is undoubtedly a little less than 15 mA/cm$^2$. However, the indications are that the primary problem with the sputter-deposited cells is the low junction collection efficiency, which is perhaps about 0.25.

According to the theory of field-aided collection,[32] one has

$$\eta_c = \frac{E_o}{S_I/\mu + E_o} \quad , \tag{3}$$

where $S_I$ is the interface recombination velocity for interface states created by the $Cu_2S$/CdS lattice mismatch, $\mu$ is the electron mobility in CdS, and $E_o$ is the electric field strength at the junction.

For a uniform doping level the junction field is given by

$$E_o = \frac{2(V_D - V)}{W} \quad , \tag{4}$$

where $V_D$ is the diffusion potential, V is the external junction voltage, and W is the depletion layer width. The depletion layer width can be written as

$$W = \left[\frac{2\,\epsilon\epsilon_o(V_D - V)}{q\,N_D^*}\right]^{1/2} \quad , \tag{5}$$

where q is the electronic charge, $\epsilon_o$ is the dielectric constant of free space, $\epsilon$ is the relative dielectric constant of CdS ($\sim 10$), and $N_D^*$ is the effective donor dopant density (assumed uniform).

The low values of $\eta_c$ for the sputtered cells imply that $E_o << S_I/\mu$. When Eqs (2) through (5) are combined, one obtains the following relationship, in the limit of $E_o << S_I/\mu$, for the case of a small and negative bias V.

$$J = J_L \frac{\mu}{S_I} \left( \frac{2_q N_D V_D}{\epsilon \epsilon_o} \right)^{1/2} \left( 1 - \frac{V}{V_D} \right)^{1/2} \qquad (6)$$

The $J^2$ vs V dependence implied by Eq (6) has been confirmed for cells 653 and 917 in the low and negative bias regime.[29] These measurements therefore support the conclusions that most of the photocurrent reaches the junction and that $E_o << S_I/\mu$.

A more complete picture of the electric field at the junction, and its influence on the short circuit current, is provided by capacitance-versus-voltage studies made at the Institute of Energy Conversion on cells with evaporated CdS layers and at Lockheed on the sputter-deposited cells.[29] Table III compares depletion layer widths deduced from these capacitance measurements for cells in their as-fabricated state, after heat treatment and during subsequent exposure to solar illumination. The as-deposited depletion layer thicknesses for the evaporated cells are consistent with predictions made using Eq (5) and measured donor densities. The sputtered cell data are for cells with the composite structure shown in Fig. 23, The depletion layer implied by the capacitance measurements corresponds, as would be expected, to the width of the undoped layer and therefore confirms the control which was maintained during the deposition, as reported in Section 4.1. During heat treatment the depletion layer widths increased in both cases and, in the sputtering case, extended to about the thickness of the cell. The significant observation is that under solar illumination the depletion layer width in the evaporated cells decreased by approximately an order of magnitude, while in the sputtered cells the decrease was much less.

Using W = 200 nm and $V_D$ = 0.8V for the evaporated cells yields $E_o = 8 \times 10^4$ V/cm. Recent estimates for high performance evaporated cells place $S_I/\mu$ in the range from $1.3 \times 10^3$ to $4.5 \times 10^3$ V/cm.[33] Using Eq (3) and $S_I/\mu = 3 \times 10^3$ V/cm, we obtain $\eta_c = 0.96$ for the evaporated cells. The $I^2$ vs V plots indicate that the diffusion potentials for the sputtered cells are a little less than 0.8V.[29] Using $V_D$ = 0.5V and W = 3000 nm for the sputtered cell yields $E_o = 3.3 \times 10^3$ V/cm.

TABLE III

DEPLETION LAYER WIDTHS

| | Evaporated CdS<br>Wet process $Cu_2S$<br>Inst. Energy Conv. | Sputtered CdS<br>Sputtered $Cu_2S$<br>Telic/Lockheed* |
|---|---|---|
| As deposited | ~100 nm | ~500 nm |
| After heat treatment | ~10000 nm | ~5200 nm |
| Under solar illumination | ~170 nm | ~3000 nm |

* Cell with composite structure shown in Fig. 23.

This electric field, along with $\eta_c \sim 0.25$, implies that $S_I \sim 1.3 \times 10^4$ V/cm, a value that is three to four times larger than the values for the evaporated cells. The higher $S_I/\mu$ in the sputtered cell may be due to a greater degree of disorder on the surface of the sputtered CdS (no etch is used to place the junction within the CdS).

The above analysis can be summarized as follows:

1) The major reason for the poor efficiency of the sputter-deposited cells is a poor junction collection efficiency, which results from a low electric field and an elevated $S_I/\mu$.

2) A major difference between the cells fabricated using evaporated CdS and those fabricated thusfar by sputtering at Telic is that the depletion layer width in the sputtered cells does not decrease significantly under solar illumination.

The low electric field is particularly important. The dependence of $\eta_c$ on $E_o$ and $S_I/\mu$ is shown in Fig. 25. The range of $S_I/\mu$ observed for evaporated cells is indicated by the shading. Note that if the electric field in the sputtered cells were increased to a value comparable to the evaporated cells ($E_o = 8 \times 10^4$ V/cm), then $\eta_c$ for the sputtered cells would be about 0.9, with no improvement in $S_I/\mu$.

The generally accepted model for junction formation in the evaporated cells is that the heat treatment causes Cu acceptors to diffuse into the CdS junction region. The compensating effect of these acceptors causes the space charge region to increase in width. However, under illumination the space charge region shrinks by an order of magnitude because of trapping of photogenerated holes by the Cu acceptors.[32]

The explanation for the failure of the depletion layer width to decrease under illumination in the sputter-deposited cells may be related to an enhanced Cu diffusion into CdS when In doping is present. Enhanced diffusion of In and Cd into CdS containing In has been measured.[18,34,35] The usual explanation is that charge neutrality requires that one Cd vacancy be present in the crystal lattice for every two In atoms, and that these vacancies promote those diffusion processes which occur via a vacancy mechanism. The copper diffusion into CdS

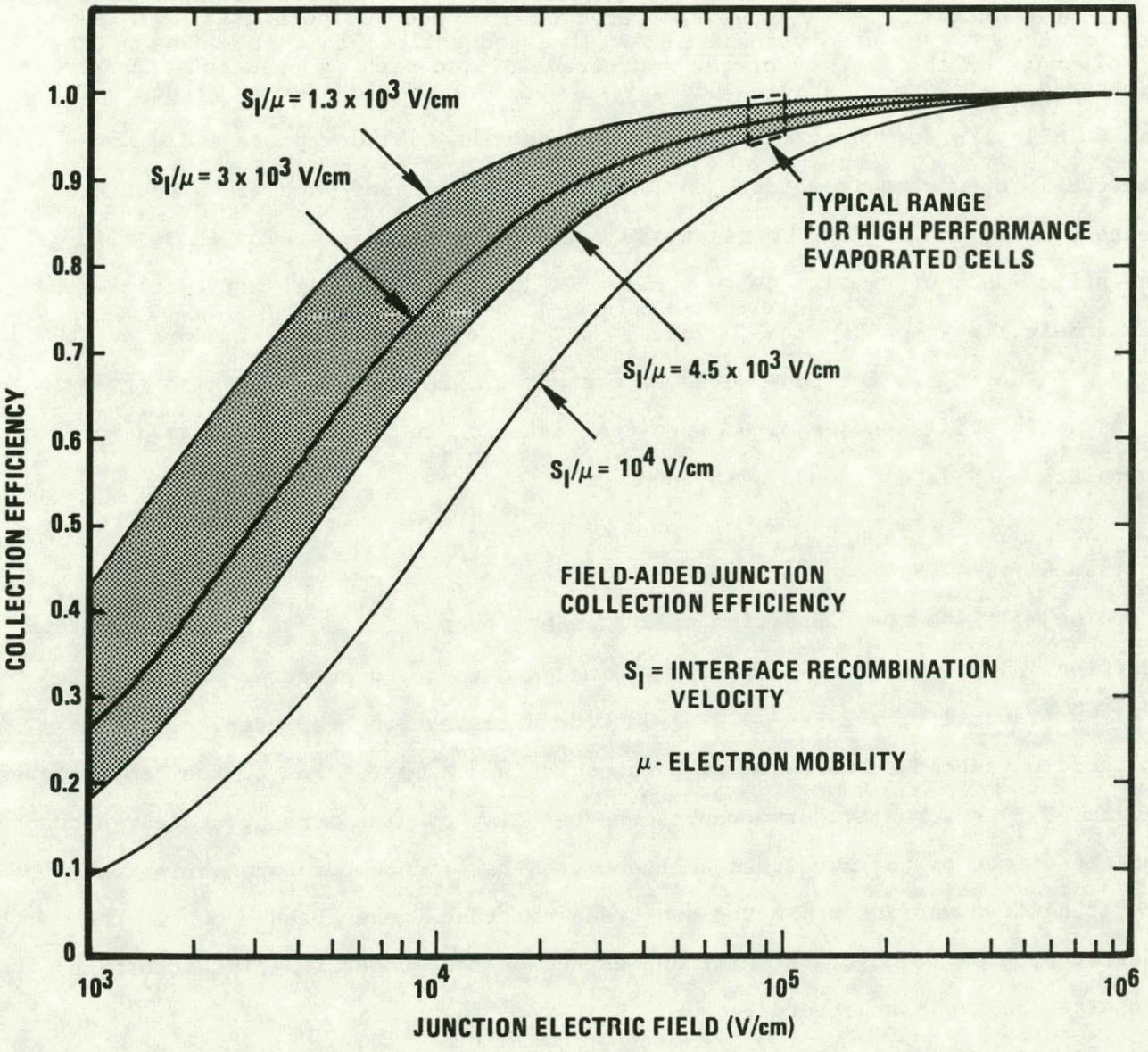



FIG. 25 Dependence of $\eta_c$ on $E_o$ for various values of $S_I/\mu$. Range of $S_I/\mu$ observed for evaporated cells[33] are indicated by the shaded region.

is expected to proceed by a vacancy mechanism. Therefore, for a given heat treatment, it is possible that much more Cu passes into the In-doped sputtered coatings than passes into the undoped evaporated cells. Different heat treatment procedures are undoubtedly required for In-doped cells. Thus it was seen that sputter-deposited cells having CdS layers with 0.1 atomic percent In doping and $Cu_2S$ layers formed by either sputtering or the CuCl dry process did not improve in open circuit voltage and short circuit current when given heat treatments of from one to four hours at 150°C in a $H_2$-Ar atmosphere. See Section 4.1. The performance of similar cells without In doping improved significantly when given heat treatments typical of those used for evaporated cells. However, the use of In doping is not considered to present a fundamental problem in itself. Cells having efficiencies of 6% were fabricated on the Clevite program using evaporated CdS layers doped with In.[36]

## 5. SUMMARY STATUS

The multi-source deposition apparatus has been modified to provide a vacuum interlock, improved inter-source shielding, and improved substrate heating and cooling (Tasks 1.1, 1.2, and 1.3). Shakedown tests have been completed. The calibration procedure which relates the substrate temperatures to the temperatures indicated by reference thermocouples has been improved to more accurately account for the effect of the substrate emittance. Substrate temperature variations, resulting from variations in the substrate emittance, have been shown in the present program to have a significant effect on the properties of CdS coatings deposited on these substrates.

The vacuum interlock will significantly increase the frequency with which heterojunctions can be fabricated in support of future research. Thus an auxiliary sputter coating chamber has been assembled using parts from the old multi-source deposition system. The auxiliary chamber will be committed to the program for use in depositing grid electrodes and anti-reflective coatings.

An investigation of cylindrical-post magnetron rf reactive sputtering has reconfirmed that the use of rf power effectively reduces the occurrence of cathode arcing (Task 1.4). However, dc reactive sputtering work during the past year indicates that the arcing problem is not so severe as had been thought. A new dc power supply with an improved arc suppression circuit has been placed into operation. It is anticipated that future work will be done using dc power.

CdS resistivity control by In doping has been investigated using both diffusion from pre-deposited In layers and reactive sputtering from In-doped Cd sputtering targets (Task 2.1). The use of In-doped targets shows particular promise. However, the $H_2S$ injection rate must be carefully controlled to minimize the level of Cd vacancies. When this is done, the fraction of In donors which contribute electrons to the conduction band is similar to that which has been reported for CdS single crystals. Thus resistivities in the desired 5 to 10 $\Omega$-cm range can be achieved with doping levels of about 0.1 atomic percent In.

CdS resistivity control by off-stoichiometry has been achieved using a cyclic reactive sputtering process where the $H_2S$ injection rate is periodically switched on and off. Resistivities of about $10^3$ $\Omega$-cm under laboratory lighting and about $10^2$ $\Omega$-cm under solar illumination have been achieved using this method. These resistivities are within a range which makes the CdS suitable for use in cells which incorporate thin CdS layers (1000-2000 nm).

Progress has been made toward improving the procedures for depositing $Cu_2S$ by reactive sputtering (Task 2.3). It has definitely been established that the $Cu_xS$ layers deposited onto CdS exhibit the same property-deposition condition relationships that were previously observed for $Cu_xS$ coatings deposited onto glass substrates. The $Cu_xS$ deposition process is vulnerable to process drifts, because the deposition time is short compared to the typical times required to condition cathode and deposition surfaces. The modified apparatus should be particularly useful in permitting improved control over the $Cu_xS$ deposition process.

The efficiencies of all-sputter-deposited photovoltaic devices have been

improved from less than 0.1% to about 0.6% during the present contract period (Task 3). Considerable progress has been made in improving the general techniques of cell fabrication. Most cells presently being fabricated are photovoltaic in their as-deposited state. The number of pinhole flaws which are present in Au gridded cells has been greatly reduced, and it is not uncommon to now form cells with zero flaws among the 31 grid lines. In general, the highest efficiencies have been achieved with cells having CdS layers deposited with off-stoichiometry rather than In doping as a means of resistivity control, although an efficiency of 0.4% was obtained with a (CdZn)S cell (10%Zn) which was doped with 2 atomic percent of In. Open circuit voltages are typically 0.35 to 0.43V (see Table I). The primary deficiency of the sputter-deposited cells is a low short circuit current (values are typically about 3 $mA/cm^2$). The second most serious problem is a low fill factor (values are typically about 0.4). The cause of the low short circuit current appears to be due primarily to a low junction collection efficiency.

Future work will concentrate on increasing the electric field in the vicinity of the junction. This will be done using techniques such as the formation of composited cells which control the doping profile by placing a thin undoped Cd(Zn)S layer at the junction and a thicker In doped CdS layer at the rear of the cell. Specialized heat treatments both before and after junction formation will also be examined. The differences between the all-sputter-deposited cells and the more conventional evaporated cells will be investigated by fabricating hybrid cells. Thus cells will be fabricated which combine sputtered CdS with $Cu_2S$ layers formed by the wet or dry CuCl process. Other hybrid cells will incorporate sputtered $Cu_2S$ with evaporated CdS layers. In preliminary work short circuit currents of $\sim$7 $mA/cm^2$ and efficiencies of over 1% have been achieved by hybrid cells which combine an undoped sputtered CdS layer with $Cu_2S$ layers formed by the CuCl dry process.

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