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Digital SLIFER Recorder, Model A

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ABSTRACT

This manual describes the design, operation, and performance characteristics of the Digital SLIFER Recorder used by Sandia Laboratories to record the SLIFER data from underground nuclear tests.

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DIGITAL SLIFER RECORDER, MODEL A

1. Introduction

The Digital SLIFER Recorder (DSR) is an instrument that records a time-varying frequency signal in the range from 700 kHz to 1500 kHz with an amplitude greater than 200 mV. This signal is referenced to an input fiducial marker, and recording is initiated by an increase in the frequency of the signal. The primary purpose of this instrument is to record data from the SLIFER system.*

The DSR records 512 samples after the record trigger signal, with a sample interval of 50 μ s (for a total recording time of 25.55 ms). The measurement essentially uses a 20-cycle period-averaging counter technique.

Figure 1-1 shows a front view of the DSR, and Figure 1-2 shows the corresponding rear view. Figures 1-3 and 1-4 are top and bottom views, respectively, of the DSR with the covers removed. Figure 1-5 shows a simplified block diagram of the DSR.

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* Bass, et al, SLIFER Measurement for Explosive Yield, SAND76-0007, Sandia Laboratories, Albuquerque, NM, April 1976.

Figure 1-1. Digital SLIFER Recorder--Front View

Figure 1-2. Digital SLIFER Recorder--Rear View

Figure 1-3. Digital SLIFER Recorder--Top View

Figure 1-4. Digital SLIFER Recorder--Bottom View

Figure 1-5. Block Diagram of the Digital SLIFER Recorder

2. Physical Description

2.1 Overall Dimensions

Overall dimensions for the Digital SLIFER Recorder are as listed below:

Front Panel:

Height	5.25 in. (13.3 cm)
Width	19 in. (48.3 cm)

Chassis:

Height	5.25 in. (13.3 cm)
Width	17.25 in. (43.8 cm)
Depth	12.625 in. (32.1 cm)

Weight:

15 lb (6.8 kg)

2.2 Front Panel Controls, Connectors, and Readouts

Figure 1-1 shows a front view of the DSR, displaying the control switches, connector jacks, and digital readouts. A brief description of each of these features follows:

POWER Switch -- This switch applies 28 V to the TEST-SHOT switch and to the remote closures.

POWER Indicator -- This indicator lights whenever the unit is ON, whether for test purposes or for remote recording.

TEST-SHOT ENABLE Switch -- In the TEST position, this switch allows power to be applied to all of the circuits, independent of remote closures. This position is used for readout of recorded data and for bench work (recording and reading).

In the SHOT ENABLE position, the only way in which power can be applied to internal circuits is for the POWER ON remote closure to be engaged. This position is used only for remote recording of data.

PRINT/READ-RECORD Switch -- In the PRINT/READ position, the prerecorded data can be printed or else read visually. In the RECORD position, the unit accepts and records data.

SHOT ENABLE Indicator -- This (green) light indicates that the unit is ready to accept remote closures. For this indication, the following conditions must be met:

- a. The battery switch for memory power (internal to the chassis) must be in the ON position.
- b. The POWER switch must be ON.
- c. The TEST-SHOT ENABLE switch must be in the SHOT ENABLE position.
- d. The PRINT/READ-RECORD switch must be in the RECORD position.
- e. 28-V power must be supplied to the unit.

CURRENT ADJUST Potentiometer and Jacks -- When the unit is being used to apply power to the SLIFER oscillator, the potentiometer and jacks are used in the following manner: To adjust the current to the oscillator, the unit must be ON, and a suitable ammeter (100-mA range) must be plugged into the jacks, with the common lead to the black and the positive lead to the red jack. Then with the oscillator connected to the signal input connector, adjust the potentiometer for the desired current (60 mA) to the oscillator. After the current has been adjusted, remove the ammeter and short the two jacks by means of the shorting plug. If the unit is not supplying power to a SLIFER oscillator but is being used to record data, this shorting plug must be removed!

FIDU Connector -- This connector (in parallel with the connector on the rear panel) is used for a fiducial or start pulse to be used as a timing reference.

SIGNAL Connector -- This connector (in parallel with the connector on the rear panel) is used to bring in the signal that is to be recorded.

ADDRESS Readout -- This display reads the address of data in the memory.

PERIOD-NSEC Readout -- This display reads the period of the frequency of the source signal.

The three switches labeled READ ADDRESS, USEC, and 50 USEC are used to time-reference the fiducial signal to an internally generated trigger and to the data stored in the memory.

READ ADDRESS Switch -- This switch produces the memory address when the unit has internally generated a trigger.

USEC Switch -- This switch produces the time (in μ s) between the leading edge of the fiducial pulse and the leading edge of the first 50- μ s pulse occurring after the fiducial pulse.

50-USEC Switch -- This switch produces the number of 50- μ s pulses occurring between the fiducial pulse and the internal trigger.

The fiducial input can be synchronized to within $\pm 1 \mu$ s of the data stored in the memory.

Unlabeled switch -- This switch (S14), which is recessed from the front panel, is used to enable the DATA ENABLE switch on the front panel. This is a data safeguard to prevent losing data on recovery by inadvertently engaging the DATA ENABLE switch while power is being applied to the unit.

DATA ENABLE Switch -- This switch is used in conjunction with the aforementioned switch (S14) to enable the unit (i.e., to begin storing data in the RECORD mode) without using the remote closures.

MANUAL TRIGGER Switch -- This switch simulates an internally generated start trigger.

The three switches labeled RESET, MANUAL STEP-FAST STEP, and AUTO STOP-AUTO PRINT/READ are used in conjunction with the PRINT/READ-RECORD switch to read or print the recorded data.

RESET Switch -- When this switch is engaged, the address counter is reset to 000.

AUTO STOP-AUTO PRINT/READ Switch -- With this switch in the AUTO STOP position, the address counter advances only by means of the MANUAL STEP switch, advancing one count each time the switch is engaged. With this switch in the AUTO PRINT/READ position, the address counter advances automatically, approximately 2.5 counts per second or 10 counts per second, depending upon the position of the PRINT SPEED switch (S9) on the rear of the chassis. These switch positions also drive the digital printer at the corresponding speeds.

For a fast visual scan of data (without printing), place the AUTO STOP-AUTO PRINT/READ switch in the AUTO PRINT/READ position and engage and hold the MANUAL STEP-FAST STEP switch. In this mode of operation, the address counter advances approximately 160 counts per second.

2.3 Rear Panel Controls and Connectors

Figure 1-2 shows a rear view of the DSR, displaying the control switches and connector jacks. A brief description of each of these features follows:

PRINT SPEED Switch -- This switch controls the speed of the data output, either FAST (10 prints per second) or SLOW (2.5 prints per second).

DATA OUT Connector -- The data output connector (J5) pin connections are as shown in Table 2-I.

FIDU IN Connector -- This connector (in parallel with the connector on the front panel) is used for a fiducial or start pulse which is utilized to time-reference the data that are to be stored.

SIGNAL IN Connector -- This connector (in parallel with the connector on the front panel) is used to bring in the signal that is to be recorded.

REMOTE CLOSURE Connector -- A closure between the pins shown in Table 2-II performs the functions shown.

DC PWR IN Connector -- This connector is used to couple the recorder with the DC power needed for operation (+ on pin B, - on pin A).

SIGNAL OUT Connector -- This connector produces a 0- to 5-V square wave at the frequency of the signal input and at 1-k Ω impedance.

MONITOR Connector -- This connector produces a 0- to 5-V DC signal to monitor that the power is on and that the recorder has been enabled.

TABLE 2-I
Printer Connections

DSR (Connector Type LJT06-19-32P)	Function	HP 5055A (Connector Type Amphenol 57-30500)
A	Data	1
B		2
C		26
D		27
E		3
F		4
G		28
H		29
J		5
K		6
L		30
M		31
N		7
P++		8
R*		32
S+		33
g	+ inhibit	22
j	+ print	23
h	+ 5 volt	25
R*	Ground	50
T	Memory	13
U		14
V		38
W		39
X		15
Y		16
Z		40
a		41
b		17
c		18
d	Address	42
e		43
f		19
P++		20
R*		44
S+		45

++ Jumper in connector

* Jumper in connector

+ Jumper in connector

TABLE 2-II

Remote Closures
(Connector Type LJTOO-13-98S)

	<u>Function</u>
F	ENABLE
G	
H	POWER ON
K	
B	POWER OFF
D	

2.4 Internal Controls

Battery -- The memory battery must be fully charged in order to maintain data in the memory.

Battery Switch -- This switch determines the supply of voltage to the memory. In the ON position, power is from the internal battery. In the OFF position, power is from the 5-V DC-DC converter that also supplies all of the other 5-V power.

Internal Trigger Set -- Socket E4-04 is used to set the number of consecutive decreases of the signal period required to produce the internal record trigger. It is programmable from 1-15 with the following weights:

pins 2-13	"1"
pins 3-12	"2"
pins 4-11	"4"
pins 5-10	"8"

These weights are additive when activated by shorts between the appropriate pins.

Fiducial Input Amplitude -- Resistor Rh on the printed circuit board at the rear of the chassis adjusts the threshold required to activate the fiducial input signal circuitry.

3. Operating Instructions

3.1 Remote Recording

To operate in this mode, proceed as follows:

- a. Connect a 28-V source to the recorder.
- b. Switch POWER to ON.
- c. Switch TEST-SHOT ENABLE to SHOT ENABLE.
- d. Switch PRINT/READ-RECORD to RECORD.
- e. Switch AUTO STOP-AUTO PRINT/READ to AUTO STOP.
- f. The memory battery switch (internal) must also be ON.

With the switches in these settings and with 28 V applied, the SHOT ENABLE (green) light should be on. If this light is not on, determine the problem; do not use the recorder.

3.2 Remote Recording Simulation Using Test Box

To operate in this mode, proceed as follows:

- a. Connect the test box remote closure cable to the REMOTE CLOSURES jack (J2) of the DSR. Connect the TRIGGER from the test box to the FIDU IN jack (J3) of the DSR. Connect SIGNAL OUT from the test box to the SIGNAL IN jack (J4) of the DSR.
- b. Turn the test box power ON.
- c. Press the POWER ON remote closure on the test box. DSR power should come on (as indicated by readouts lighting up, etc).
- d. Press the ENABLE remote closure on the test box. The DSR should start recording the period of the signal from the test box.
- e. Press the TRIGGER push-button switch on the test box. This simulates a fiducial pulse and also changes the frequency, causing the DSR to record data and power down.

Before a simulation using the test box or a frequency generator, always remove the shorting plug on the front panel. The RESET switch on the test box must be pressed to repeat steps (c) through (e) for another simulation.

3.3 Data Readout

To operate in this mode, proceed as follows:

- a. Switch TEST-SHOT ENABLE to TEST.
- b. Switch PRINT/READ-RECORD to PRINT/READ.
- c. In order to print the data, connect a Hewlett Packard Model No. 5055A digital recorder to the DATA OUT connector (J5) and place the PRINT SPEED switch (S9) on the rear of the chassis in the FAST position. Turn the DSR power ON. Press the RESET switch to verify that the address reads 000. Turn the HP digital printer power ON and place the HP OPERATE/STANDBY switch in the OPERATE position.

Press the 50 USEC push-button switch and hold it while pressing the RESET switch twice. The last two digits of the period readout represent the number of 50- μ s pulses. Repeat the previous step using the USEC push-button switch and the RESET switch. Repeat again using the ADDRESS switch and the RESET switch.

- d. To read data out, press RESET and then place the AUTO STOP-AUTO PRINT/READ switch in the AUTO PRINT/READ position. After the entire memory has been printed, place the OPERATE/STANDBY switch on the HP printer in the STANDBY position and the AUTO STOP-AUTO PRINT/READ switch in the AUTO STOP position.

3.4 Test Operation

To operate the unit on a bench, connect a 28-V power source to the recorder. To record, place the TEST-SHOT ENABLE switch in the TEST position and the PRINT/READ-RECORD switch in the RECORD position.

Press the unlabeled, recessed switch (S14). This enables the DATA ENABLE switch on the front panel. Then press the DATA ENABLE switch. The DSR should now be recording the input signal. The DSR will stop recording either upon a change in the input frequency or upon pressing the MANUAL TRIGGER. Power will remain on. Data may be read out as described in Section 3.3.

4. Performance Characteristics

Input Power: 28±4 V DC, 600 mA

Input Signals:

Power On: Relay closure

Power Off: Relay closure

Enable: Relay closure

Signal: 700-1500 kHz, 0.2-10 V peak-peak, 50-Ω input impedance

Fiducial: Pulse, >200 ns wide, 0.2-10 V peak, 50-Ω input impedance

Sample Rate: 50 μs

Triggering: Self-triggering on input data. An internal trigger is generated upon recording a consecutive number of decreases (from 0 to 15) in the period readings taken at 250-μs intervals.

Storage: 1024 samples total (512 after internal record trigger, 512 before internal record trigger)

Resolution: ±1 ns on the period of the input signal

Time Reference: Fiducial input to address reading in memory, given by
time = [50 (50 USEC reading -1) + USEC reading + 5] μs;
Accuracy is ±1 μs.

Time Correction: For the time to the center of the sample window (20-cycle gate), add 13.5 x (period reading), or approximately 15 μs; accurate to ±1 μs.

Printer Output:

Rate: 2.5 or 10 prints per second

Logic: 1-2-4-8 BCD, positive logic, TTL levels

Output Drive: 2 TTL loads

Operational Environmental Limits:

Temperature: -40 to +125°C

Humidity: 93% noncondensing

Shock: 30 g, 50-ms half-sine, 3-axis, both directions

Pressures: 10,000 feet altitude

Nonoperational Environmental Limits:

Storage: -65 to +150°C

Shock: 30 g, 50-ms half-sine, 3-axis, both directions

Pressures: 50,000 feet altitude

5. Circuit Description

5.1 Fiducial Input Circuit

The fiducial input circuit consists of J3, J6, and the amplifier Ab.

The fiducial pulse inputs the circuit through either J3 (on the front panel) or J6 (on the back panel). The pulse is AC-coupled to amplifier Ab through capacitor Ca. The amplifier is protected from a high-amplitude pulse by the transient protector CRA, which shunts any transient larger than approximately 8 V.

The amplifier is biased by the resistor network Rh, Rj, Rk, Rl, and Rm, so that, by adjusting Rh, an input threshold from approximately 120 mV to 10 V can be set.

The amplifier output pulse is pulled up to +5 V through resistor R22.

5.2 Signal Input Circuit

The signal input circuit consists of J4, J7, the multistage filter, the amplifier Aa, and the pulse-shaping network E1-03A.

The SLIFER oscillator output arrives at either J4 (on the front panel) or J7 (on the back panel). This signal (from 700 kHz to 1500 kHz) is AC-coupled to the high-pass filter (see Figure 5-1) by capacitor Ce. The output of the filter is AC-coupled to amplifier Aa through capacitor Cf. The amplifier input is biased by the voltage divider circuit consisting of Rb, Rc, Rd, Re, and Rf so that the amplifier is held in an off state until a signal greater than approximately 10 mV appears at pin 4.

The positive output of the amplifier is pulled to +5 V through resistor Rl.

E1-03A takes the pulses from Aa, reshapes them to square pulses, and outputs the squared pulses to the Signal Out driver D1-05A and to the 20-count gate circuit.

Figure 5-1. SLIFER Input Filter (3 Section)

5.3 20-Cycle Gate Generating Circuit

The 20-cycle gate is generated by the circuit consisting of the integrated circuits C1-04; E1-01A and B; E1-02A and B; E1-03B, C and D; and E2-05C.

The signal input pulse train from E1-03A (see Figure 5-2) starts the counter C1-04A, assuming the clock input (pin 1) is low. The counter output, Q3, is a divide-by-8 output and, along with the input pulse train, enables the gate E1-01B. The output of E1-01B is inverted by E1-02B and sets the 20-cycle gate flip-flop (E1-03B and E1-03C) high.

C1-04A output Q4 and C1-04B output Q1, along with the input pulse train, enable gate E1-01A. The output of E1-01A is inverted by E1-02A and resets the 20-cycle gate flip-flop (E1-03B and E1-03C).

The clock input (C1-04A pin 1) is controlled by C1-04A output Q4 and C1-04B output Q1. When both are high, E1-03D goes low and E2-05C goes high, thereby stopping the counter. A reset pulse returns Q1 and Q4 to low, once again enabling C1-04A to begin counting another 20-cycle gate.

Figure 5-2. Timing Diagram 20-Count Gate Generator Circuit.

5.4 Period Counter

The period counter circuit consists of integrated circuits E2-05A, D5-03C and D, E2-06, E3-06, and D3-02.

E2-05A is a gate that allows the 50-MHz oscillator pulses to pass through during the time the 20-cycle gate is high (see Figure 5-3).

D5-03C resets the period counter when the 20-cycle gate generator circuit is reset or when a $\overline{WE}$ pulse and a 20-cycle gate appear simultaneously.

E2-06, E3-06, and D3-02 are counters that count the 50-MHz pulses and give a BCD output. This BCD output is the period of the incoming frequency (in nanoseconds) and is written into memory by a $\overline{WE}$ command (see Figure 5-3).

Figure 5-3. Timing Diagram Period Counter/ $\overline{CS}$ / $\overline{WE}$

5.5 Internally Generated Timing

Internal timing has the 50-MHz oscillator as the heart of the system. The 50-MHz oscillator is divided down to 20 kHz at output QD on E3-01 by the divide-by-2500 circuit consisting of E2-01, E2-02, E2-03, and E3-01.

A combination of E3-01 outputs QA, QB, QC, and QD generate the $\overline{WE}$ pulse, the $\overline{CS}$ pulse, the comparator circuit clock, and the internal trigger circuit clock.

The $\overline{CS}$ command, which loads an address to memory on the falling edge of the pulse, is generated by D4-03A. It occurs when QA is high, QB is low, and QC is high (see Figure 5-3).

The $\overline{WE}$ command writes the output of the period counter to memory on the trailing edge of the pulse. This pulse is generated by D3-03B and occurs when QA is low, QB is low, QC is low, and QD is high (see Figure 5-3). F3-02C is a gate that allows the $\overline{WE}$ pulse to write on memory only after the DSR is ENABLED and before the stop record counter (C3-02) reaches 512 counts.

The clock for the comparator circuit storage flip-flops (C3-03 and C3-04) is generated by E3-02B. This clock occurs every 250 μ s and is generated when E3-01 output QA is high, QB is high, QC is low, and E3-03 output QD is high.

The internal record trigger generator clock is generated by E3-02A when E3-01 output QA is high, QB is low, QC is low, QD is low, and E3-03 output QD is high. This clock occurs every 250 μ s.

The QD output of E3-01 is also the 20-kHz timing for the gate counter reset (C1-03A), for the period counter reset (C1-03A), for counter C3-02, and for the address select counter C3-05.

5.6 Externally Initiated Timing

The externally initiated timing starts with commands remotely generated while in a SHOT mode or manually generated by front panel switch settings while in a TEST mode.

5.6.1 SHOT Mode -- A POWER ON closure between pins H and K of J2 latches relay K1, turning on the 5-V power supply PS1. An ENABLE closure between pins F and G of J2 latches relay K2, enabling the recorder as follows.

When K2 is energized, pin 10 of the relay goes low, setting the enable flip-flop (D3-04C and D) high at pin 10 and low at pin 11. When the pulse at pin 11 goes low, it triggers C1-01B and also enables the $\overline{WE}$ gate F3-02C. The pulse out of C1-01B latches F4-01 pin 1 high, latches F4-01 pin 2 high, and resets F4-01 pin 10 low.

When F4-01 pin 1 goes high, the following occur:

- a. the fiducial gate E2-05B is enabled;
- b. the microsecond counter F4-05 is held in a reset state;
- c. the 50- μ s counter F4-04 is held in a reset state.

When F4-01 pin 2 goes high, the following occur:

- a. the address counter reset gate D5-04B is enabled;
- b. the stop record counter C3-02 is held in a reset state, disabling the counter;
- c. C1-03B is enabled, allowing the 20-kHz pulses to pass.

A fiducial pulse out of the Fiducial Input circuit passes through the fiducial gate E2-05B, resets F4-01 pin 1 low, and sets F4-01 pin 9 high. When F4-01 pin 1 goes low, it disables the fiducial gate E2-05B and also removes the resets from the microsecond counter F4-05 and from the 50- μ s counter F4-04.

When F4-01 pin 9 goes high, it enables the microsecond counter F4-05. F4-05 in turn counts a 1-MHz clock until the next 20-kHz pulse from C1-03B resets F4-01 pin 9 low, disabling F4-05.

A trigger pulse out of C1-01A, generated either by a manual trigger (S4) which sets flip-flop D3-04B pin 4 low or by a pulse sent from the internal trigger generator C4-02, sets F4-01 pin 2 low and D4-04B pin 4 high.

When F4-01 pin 2 goes low, the following occur:

- a. C1-03B becomes disabled, stopping the 20-kHz pulses;
- b. The address counter reset gate (D5-04B) is disabled, allowing the address at which the trigger occurred to be stored in the address counters F4-02 and F4-03;
- c. the reset is removed from the stop record counter C3-01.

When the reset is removed from C3-01, this counter starts to count at a 20-kHz rate. After 512 counts (approximately 25.6 ms), pin 14 (Q10 output) goes high. This high, along with D4-04B pin 4 high, enables gate D4-04D, turning on transistor Q1. This in turn resets relays K1 and K2, turning off power to the DSR.

5.6.2 TEST Mode -- In the TEST mode, remote closures are not necessary to operate the DSR. Placing S3 in the TEST mode turns on the 5-V power supply PS1. The DSR is then enabled by depressing front panel switch S5. The enable sequence of events is almost the same as in the SHOT mode; however, the power does not shut off as in the SHOT mode, and switch S14 must be depressed (enabling gate D5-05A) before the unit may be ENABLED again.

5.7 Internal Record Trigger Circuit

The internal record trigger circuit consists of integrated circuits C3-03, C3-04, C4-02, C4-03, C4-04, C4-05, and the programmer network E4-03 and E4-04.

C3-03 and C3-04 are storage flip-flops used to delay the data monitored from memory. This delay is accomplished by means of the 250- μ s clock described in Section 5.5. These delayed data are then compared with the present data by integrated circuits C4-03, C4-04, and C4-05. Anytime the delayed data are greater than the present data, a high level will be sent from C4-03 pin 13 to C4-02 pin 9. This high level at pin 9 enables C4-02 to count at the rate of the internal record trigger

generator clock (250 μ s) described in section 5.5. When C4-02 counts to 15, a pulse will be sent out of C4-02 pin 15 to C1-01A pin 4. This pulse is the internal record trigger. A low at C4-02 pin 9 reloads the initial count which is set by jumpers on E4-04.

5.8 Trigger Address Location Counter

The address of the data at the time when the trigger occurred is generated by the counters F4-02 and F4-03.

When the DSR is enabled, F4-02 and F4-03 start counting at a 20-kHz rate (see Figure 5-4). The same command enables the reset gate D5-04B. The memory address generator, C3-05, resets F4-02 and F4-03 through the gate D5-04B every 1024 counts. This insures that these two address generators (C3-05 and the combination of F4-02 and F4-03) are sending out the same addresses simultaneously.

When a trigger occurs, the reset gate D5-04B is disabled and, at the same time, the 20-kHz clock pulses are stopped. This address is stored until the unit is either reenabled or the battery (BT1) power is removed.

To read out this address stored in F4-02 and F4-03, the READ ADDRESS switch (S11) on the front panel is depressed, enabling buffers F3-03, F3-04, and F3-05. These buffers take the address stored in F4-02 and F4-03 and output it to the readout drivers for visual display at the front panel or for printout from J5 on the back panel.

Figure 5-4. Timing Diagram Address/50 μ s Counters

5.9 50-Microsecond Counter

The time between the fiducial arrival and the generation of the internal record trigger is counted in 50- μ s intervals by integrated circuit F4-04.

When the DSR is enabled, the counter F4-04 is placed in a reset state by the high level from F4-01 pin 1. Fiducial arrival sets F4-01 pin 1 low, removing the reset from F4-04. F4-04 then counts at a 20-kHz rate until the internal record trigger is generated, which shuts off the 20-kHz pulse train from C1-03B (see Figure 5-4). This count is stored in F4-04 until the unit is reenabled or the battery (BT1) power is removed.

To read out this count, the READ 50 USEC switch (S13) on the front panel is depressed, enabling buffers F3-05 and F3-06. These buffers take the count stored in F4-04 and output it to the read out drivers for visual display at the front panel or for printout from J5 on the back panel.

5.10 Microsecond Counter

The time between the fiducial arrival and the first 20-kHz pulse sent by C1-03B is counted in 1- μ s intervals by F4-05.

When the DSR is enabled, the counter is held in a reset state when F4-01 pin 1 is at a high level. The fiducial arrival sets F4-01 pin 1 low, removing the reset on F4-05, and also sets F4-01 pin 9 high, enabling F4-05 (see Figure 5-4). F4-05 then counts the 1-MHz pulses from E2-02 until the first 20-kHz pulse from C1-03B sets F4-01 pin 9 low, disabling counter F4-05. This count is stored in F4-05 until the unit is either reenabled or the battery (BT1) power is removed.

To read out this count, the READ USEC switch (S12) on the front panel is depressed, enabling the buffers F3-06 and F4-06. These buffers take the count stored in F4-05 and output it to the readout drivers for visual display at the front panel or for printout from J5 on the back panel.

5.11 Memory

The memory consists of thirteen 1024x1-bit random access memory (RAM) integrated circuits. Each memory chip has 10 address inputs, a data input, a data output, a $\overline{CS}$ input, and a $\overline{WE}$ input.

The addresses are generated in the RECORD mode by C3-05 as it counts the 20-kHz pulses from the QD output of E3-01. C3-05 counts up to 1024, resets itself, and starts again. In the PRINT mode, the addresses are generated by C2-04. The buffers (C1-06, C2-06, and C3-06) select which address to present to the memory chips, depending on which mode the DSR is in.

The addresses are loaded into memory on the negative edge of the $\overline{CS}$ pulse. The $\overline{CS}$ pulse is generated by D4-03A in the RECORD mode (Section 5.5) and by C2-02A in the PRINT mode (Section 5.12).

The data present at the data input are loaded into the selected address on the negative edge of the $\overline{WE}$ pulse. The $\overline{WE}$ pulse is generated by D3-03B in the RECORD mode (Section 5.5) and is disabled in the PRINT mode.

The memory integrated circuits will retain their memory after DSR shutoff as long as the battery (BT1) power is present.

The data stored in the memory integrated circuits are sent to the readout drivers for visual display at the front panel or for printout from J5 on the back panel. The data present at the output (pin 7) are the contents of the address currently in the address register.

5.12 Print Mode

In the PRINT mode, the sequence of events is dictated primarily by the 20-kHz pulses from the QD output of E3-01.

When the PRINT/READ-RECORD switch (S2) on the front panel is placed in the PRINT/READ position, the 20-kHz pulses start the counters C1-02 and D2-05A, provided that the gate E1-01C has been enabled by the front panel switch S6 being in the AUTO PRINT position. These counters take the 20-kHz pulses and count them down to 9.76 pulses per second at the Q12 output of C1-02 and 2.44 pulses per second at the Q output of D2-05A.

The Q8 output of C1-02 counts at a rate of approximately 160 pulses per second. This output is used strictly as an advance of memory for a visual readout and is not to be used for printout (Section 2.2). The print rate is selected by the setting of back panel switch S9. These pulses (2.44 per second or 9.76 per second) clock the address counter C2-04, trigger the $\overline{CS}$ generator C2-02A, trigger the print command generator C2-01, and clock the readout address counters C1-05 and C2-05. After 1024 of these pulses, C2-04 resets the system through C2-02B.

The print command may be given manually using the front panel switch S7, provided that the front panel switch S6 is in the AUTO STOP position. Depressing S7 sets flip-flop D5-05D pin 10 low, which triggers C3-01B. The pulse out of C3-01B activates the print system in the same way as do the 9.76-per-second or the 2.44-per-second pulses.

The reset command may also be sent manually by depressing the front panel switch S8. This triggers the reset generator C2-02B in the same way as does the 1024-count pulse from C2-04.

APPENDIX A
Parts List and Drawings

[illegible]

DWG CLASSIFICATION LEVEL

UNCLASSIFIED

NOTES: PROCUREMENT INFORMATION

1. DRAWING OR PART NUMBERS LISTED PARENTHETICALLY AS REFERENCE IN THE DESCRIPTION COLUMN ARE FOR INTERNAL STOCK AND PROCUREMENT PURPOSES AT SANDIA.
2. PROCURE ITEMS LISTED BY COMMERCIAL PART NUMBER IN THE 'DESIGN AGENCY NO.' COLUMN AS MANUFACTURED BY THE SOURCE LISTED OR AS DEFINED ON THE REFERENCED SANDIA DRAWING WHEN LISTED, OR A COMMERCIAL EQUIVALENT WHEN A SANDIA DRAWING IS NOT LISTED.
3. PLASTIC SHEET, ITEM 1, MAY BE PURCHASED FROM REGAL PLASTICS, ALBUQUERQUE; STANDARD COLOR 2423 (TRANSPARENT).
4. TO BE SUPPLIED BY SANDIA LABORATORIES, ORGANIZATION 1123.

ASSEMBLY INFORMATION

7. FOR SPECIFIC PROCESSING, MANUFACTURING ASSEMBLY REQUIREMENTS NOT OTHERWISE COVERED ON THE DRAWING, SEE 173125.
8. USE THE SUFFIX SPECIFIED OR ANY HIGHER OF 7-DIGIT STANDARD(S), S3 OR 400000 SERIES SPECIFICATION(S).
9. FOR EXPLANATION OF DIMENSIONS, TOLERANCES AND SYMBOLIZATION, SEE 9900000.
10. COMPONENTS NOT IDENTIFIED BY ITEM NUMBERS ON THE ASSEMBLY ARE LOCATED IN THE LIST OF MATERIAL BY REFERENCE DESIGNATIONS.
11. USE THIS DIMENSION FOR PRINT INSPECTION MEASUREMENT ONLY. DO NOT USE PRINTS MORE THAN .100 INCH OUT-OF-SCALE FOR DRILLING TEMPLATES.
12. ORIENT COMPONENTS IN POSITIONS SHOWN.
13. ASSEMBLY HARDWARE IS SUPPLIED WITH PART(S).

DWG CLASSIFICATION LEVEL

UNCLASSIFIED

SIZE

A

CODE IDENT NO.

14213

DWG NUMBER

T41063

ISSUE

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SCALE

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DWG CLASSIFICATION LEVEL
UNCLASSIFIED

ASSEMBLY INFORMATION (CONTINUED)

14. DO NOT MARK DESIGNATIONS APPEARING IN BRACKETS AND DIMENSIONS APPEARING WITHIN OUTLINE OF VIEWS ON THE UNIT.
16. ENGRAVE $.125 \pm .030$ INCH CONDENSED CHARACTERS, GROOVE WIDTH $.020$ TO $.030$ INCHES, GROOVE DEPTH $.020$ INCH MINIMUM, WHITE FILLER, ITEM 49. LOCATE APPROXIMATELY AS SHOWN.
17. ENGRAVE LINES AND $.190 \pm .030$ INCH CHARACTERS, GROOVE WIDTH $.020$ TO $.030$ INCHES, GROOVE DEPTH $.020$ INCH MINIMUM, WHITE FILLER, ITEM 49. LOCATE APPROXIMATELY AS SHOWN.
18. ENGRAVE $.100 \pm .020$ INCH CONDENSED CHARACTERS, GROOVE WIDTH $.015$ TO $.020$ INCHES, GROOVE DEPTH $.020$ INCH MINIMUM, WHITE FILLER, ITEM 49. LOCATE APPROXIMATELY AS SHOWN.
19. MARK (WITH COVER COAT) REFERENCE DESIGNATIONS, FUNCTIONS, PART NUMBER AND SERIAL NUMBER; $.120$ INCH CHARACTERS, CONTRASTING COLOR. LOCATE APPROXIMATELY AS SHOWN.
20. REFERENCE DESIGNATIONS APPEARING WITHIN A DOTTED RECTANGLE ARE TO BE MARKED ON OPPOSITE SIDE.
21. ANODIZE PER 9904102, DYE BLACK.
22. MOUNT COMPONENTS SO THAT ALL VALUES OR PART NUMBERS MAY BE EASILY READ, PREFERABLY IN THE SAME DIRECTION.
23. FABRICATE PER 9928009-02, USING TIN-LEAD PLATING; USE CM AND DL-T43184
24. FABRICATE PER 9928009-02, USING TIN-LEAD PLATING; USE CM AND DL-T43153.

DWG CLASSIFICATION LEVEL

UNCLASSIFIED

SIZE

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DWG NUMBER

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ISSUE

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SCALE

SHEET

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DWG CLASSIFICATION LEVEL

UNCLASSIFIED

WIRING INFORMATION

- 25. ALL SOLDERLESS WRAPPED ELECTRICAL CONNECTIONS SHALL BE PER SANDIA FURNISHED SPECIFICATION.
- 26. ALL WIRE SHALL BE ITEM 52, UNLESS OTHERWISE SPECIFIED.
- 27. UNLESS OTHERWISE SPECIFIED, ALL WIRE WRAP HOOK-UP WIRE SHALL BE SIZE 30, ITEM 51.
- 28. ALL SHIELDED WIRE SHALL BE ITEM 57, UNLESS OTHERWISE SPECIFIED.
- 29. ALL WIRES TERMINATING AT COMPONENTS HAVING SCREW TYPE TERMINALS SHALL BE EQUIPPED WITH PREINSULATED LUG TERMINALS. TERMINAL SIZE TO BE DETERMINED BY THE SCREW TERMINAL AND THE WIRE SIZE. USE SHAKE PROOF WASHERS.
- 30. CLAMP WIRE HARNESSSES AS SHOWN. CLAMP SIZES ARE TO BE DETERMINED AT ASSEMBLY BY THE SUPPLIER
- 31. LACE ALL WIRES INTO A HARNESS USING TAPE, ITEM 54, UNLESS OTHERWISE SPECIFIED.
- 32. LOCATE COMPONENTS APPROXIMATELY IN LINE BETWEEN THEIR TERMINATION POINTS.
- 33. DASH-DOT LINE SHOWN ON AY-T41063 INDICATES PATH OF WIRES TO BE FOLLOWED WHEN UNIT IS WIRED.
- 34. ITEM 26 TO BE CUT IN HALF TO MAKE CONNECTOR ONE END OTHER END OPEN.

DWG CLASSIFICATION LEVEL

UNCLASSIFIED

SIZE

A

CODE IDENT NO.

14213

DWG NUMBER

T41063

ISSUE

C

SCALE

SHEET

4

OF

14

AR DENOTES AS REQD NA DENOTES DOCUMENTS				ARS DENOTES AS REQD PER ASSY EM DENOTES EXPENSE MATERIAL ALT DENOTES ALTERNATE PM DENOTES PROCESS MATERIAL		DWG CLASSIFICATION LEVEL UNCLASSIFIED				
QUANTITY REQUIRED				DESIGN AGENCY NO.	DESCRIPTION	NOTE	SHEET ZONE	ITEM		
			NA	AY-T41063-000	ASSEMBLY, DIGITAL SLIFER RECORDER, MOD A					
			NA	CK-T41063-000	SCHEMATIC, DIGITAL SLIFER RECORDER, MOD A					
			NA	CM-T43153-000	CIRCUIT MASTER, READOUT BOARD, RECORDER	4				
			NA	CM-T83184-000	CIRCUIT MASTER SIGNAL/FIDU INPUT CIRCUIT	4				
			NA	SS323207-000	SOLDERLESS WRAPPED ELECTRICAL CONNECTIONS	25				
			NA	173126	GENERAL SPECIFICATIONS FOR ACCEPTANCE EQUIPMENT	7				
			NA	9900000	GENERAL REQUIREMENTS AND DRAWING INTERPRETATIONS	8,9				
			NA	9928009	FABRICATION, PRINTED WIRING BOARD					
			NA	9904102	ANODIZING ALUMINUM	21				
103			1		PLASTIC SHEET, LUCITE, RUBY RED, .125 THK	3	2/A3		1	
104			1		ALUMINUM SHEET, 2024-T4, .06 THK		2/A7		2	
			2		ALUMINUM BAR, 6061-T6, 1/4 SQUARE		3/G7		3	
			1		ALUMINUM BAR, 6061-T6, 1/4 SQUARE		3/F8		4	
			1		ALUMINUM BAR, 6061-T6, 1/4 X 3/8		3/F6		5	
			1		ALUMINUM FLAT, 6061-T6, 1/4 X 3/4		3/F7		6	
			1		ALUMINUM PLATE, 6061-T6, 1/4 THK		3/D3		7	
			1		ALUMINUM SHEET, 6061-T6 1/8 THK		4/C5		8	
			1		ALUMINUM SHEET, 5052-H22 1/16 THK		4/D3		9	
			1		RECORDER READOUT BOARD ASSEMBLY		3/A3		10	
			1		SIGNAL/FIDU INPUT CIRCUIT BOARD ASSEMBLY		3/A6		11	
105			1	DL-T43153-000	PRINTED CIRCUIT CARD, RECORDER READOUT		3/A3		12	
106			1	DL-T43184-000	PRINTED CIRCUIT CARD, SIGNAL/FIDU INPUT CIRCUIT		3/A7		13	
107			1	-	SUB-CHASSIS FRAME (ASSEMBLY OF ITEMS 3,4,5 & 6)		3/C6		14	
108			1		POWER SUPPLY AND RELAY BOARD		3/C3		15	
			1		BATTERY BOARD ASSEMBLY		4/A5		16	
109			1		RETAINER, BATTERY		4/A3		17	
43			1	170926-00	PLATE, IDENTIFICATION				18	
44			1	VIP170512-43-PX	DRAWER, ELECTRICAL EQUIPMENT, ZERO MFG CO.	13			19	
45			12	6012-1-A-BA	GUARD, SWITCH, BLACK, VEMALINE PRODUCTS CO. (872836)	1			20	
46			22	1558-2	TERMINAL STUD, DOUBLE TURRET, CAMBRIDGE THERMIONIC				21	
47			2	2371	SPACER, SLEEVE, 4-40X3/8 LG, HERMAN SMITH INC. (607136)				22	
48			6	2372	SPACER, SLEEVE, 4-40X1/2 LG, HERMAN SMITH INC. (607137)				23	
102			1	3030	SHORTING LINK, BINDING POST POMONA ELECTRONICS				24	
49			2	16TD012	PLUG ASS'Y, 16 PIN, 12 IN. LG, CONN EACH END STAND LOGIC				25	
50			3	16TD030	PLUG ASS'Y, 16 PIN, 30 IN. LG, CONN EACH END STAND LOGIC	34			26	
51			1	14TS015	PLUG ASS'Y, 14 PIN, 15 IN. LG, CONN ONE END STAND LOGIC				27	
110			1	8136-652P2	CLIP, JUMPER, AUGAT				28	
52			2	516-AG10D	DIP SOCKET, 16 CONTACT, AUGAT				29	
53			2	514-AG10D	DIP SOCKET, 14 CONTACT, AUGAT				30	

CONTRACT ITEM NO. REF. UNCLASSIFIED				DWG CLASSIFICATION LEVEL UNCLASSIFIED	SIZE A	CODE IDENT NO. 14213	DWG NUMBER T41063
ISSUE	IC						SHEET 5 OF 14

AR DENOTES AS REQ NA DENOTES DOCUMENTS				ARS DENOTES AS REQ PER ASSY EM DENOTES EXPENSE MATERIAL ALT DENOTES ALTERNATE PM DENOTES PROCESS MATERIAL		DWG CLASSIFICATION LEVEL UNCLASSIFIED				
QUANTITY REQUIRED				DESIGN AGENCY NO.		DESCRIPTION		NOTE	SHEET ZONE	ITEM
										31
										32
111			1			ALUMINUM, BAR 1/2 DIA 6061-T6			4/A7	33
										34
										35
										36
										37
										38
112			2	FHA-440-12		STAKED STUD 4-40 UNC X 3/4 LG TEM				39
			6			ROLL, PIN 3/32 DIA X 1/2 LG				40
										41
										42
			1	AN931-A4-7		GROMMET, RUBBER 1/4 I.D. 5/8 O.D. (611014)				43
										44
			ARS			HARDWARE, MOUNTING, PER 173126				45
										46
										47
										48
			ARS			FILLER, ENGRAVERS ENAMEL, HIGH GLOSS WHITE NEW HERMES ENGRAVING MACHINE CO.				49
			ARS			SOLVENT, ENGRAVERS ENAMEL CLEANER NEW HERMES ENGRAVING MACHINE CO.				50
			ARS			WIRE, "KYNAR" INSULATED, SIZE 30, BLUE (631580)				51
			ARS	MIL-W-16878		WIRE INSULATED, SIZE 22 WHITE, TYPE E				52
										53
			ARS	MIL-T-713		LACING TAPE NYLON WAXED, TYPE P, CLASS 2				54
			ARS	RNF-100		TUBING HEAT, SHRINKABLE, FLEXIBLE, POLYOLEFIN				55
			ARS	QQ-S-571		SOLDER, SN 60, FORM W. TYPE R OR RMA, COND. P2				56
			ARS	RG-196A/U		CABLE, COAXIAL (631518)				57
										58
										59
										60
										61
										62
										63
										64
										65
										66
										67

CONTRACT ITEM NO. REF.				DWG CLASSIFICATION LEVEL UNCLASSIFIED		SIZE A	CODE IDENT NO. 14213	DWG NUMBER T41063
ISSUE	C						SHEET 6 OF 14	

AR DENOTES AS REQD NA DENOTES DOCUMENTS				ARS DENOTES AS REQD PER ASSY EM DENOTES EXPENSE MATERIAL ALT DENOTES ALTERNATE PM DENOTES PROCESS MATERIAL		DWG CLASSIFICATION LEVEL UNCLASSIFIED				
QUANTITY REQUIRED				DESIGN AGENCY NO.		DESCRIPTION		NOTE	SHEET ZONE	ITEM
54			1	05-KGR		CASH KLUGE CARD STANDARD LOGIC		2/E6	B	
55			2	16-24H		CASH CARD WITH DIP SOCKETS STANDARD LOGIC	2/E5	2/E1	C, F	
56			1	46-23H		CASH CARD WITH DIP SOCKETS STANDARD LOGIC		2/E4	D	
57			1	16-24-14H		CASH CARD WITH DIP SOCKETS STANDARD LOGIC		2/E3	E	
58			5	MC14528AL		INTEGRATED CIRCUIT, DUAL RETRIGGERABLE/RESETTABLE MCNOSTABLE MULTIVIBRATOR, MOTOROLA			C1-01 C1-03 C2-01 C2-02 C3-01	
59			4	MC14040AL		INTEGRATED CIRCUIT, 12-BIT BINARY COUNTER MOTOROLA			C1-02 C2-04 C3-02 C3-05	
60			1	MC14520AL		INTEGRATED CIRCUIT, DUAL BINARY UP COUNTER MOTOROLA			C1-04	
61			7	MC14518AL		INTEGRATED CIRCUIT, DUAL BCD UP COUNTER MOTOROLA			C1-05 C2-05 D3-02 F4-02 F4-03 F4-04 F4-05	
CONTRACT ITEM NO. REF.						DWG CLASSIFICATION LEVEL UNCLASSIFIED		SIZE	CODE IDENT NO. 14213	DWG NUMBER T41063
ISSUE	C							SHEET	7	OF 14

AR DENOTES AS REQD NA DENOTES DOCUMENTS				ARS DENOTES AS REQD PER ASSY EM DENOTES EXPENSE MATERIAL ALT DENOTES ALTERNATE PM DENOTES PROCESS MATERIAL		DWG CLASSIFICATION LEVEL UNCLASSIFIED					
QUANTITY REQUIRED				DESIGN AGENCY NO.		DESCRIPTION		NOTE	SHEET ZONE	ITEM	
62		3	MC14519AL			INTEGRATED CIRCUIT, 4-BIT AND/OR SELECTOR, MOTOROLA				C1-06 C2-06 C3-06	
63		2	CD4042AE			INTEGRATED CIRCUIT, HEX BUFFER, INVERTING, RCA				C2-03 C4-06	
64		1	MC14002AL			INTEGRATED CIRCUIT, DUAL 4-INPUT NOR GATE, MOTOROLA				D3-03	
65		1	MC14013AL			INTEGRATED CIRCUIT, DUAL TYPE D FLIP FLOP, MOTOROLA				D2-05	
66		6	MC14011AL			INTEGRATED CIRCUIT, QUAD 2-INPUT NAND GATE, MOTOROLA				D3-04 D4-04 D5-03 D5-04 D5-05 F3-02	
67		1	MC14025AL			INTEGRATED CIRCUIT, TRIPLE 3-INPUT NOR GATE, MOTOROLA				D4-03	
68		1	MC14001AL			INTEGRATED CIRCUIT, QUAD 2-INPUT NOR GATE, MOTOROLA				D4-05	
CONTRACT ITEM NO. REF.				DWG CLASSIFICATION LEVEL UNCLASSIFIED		SIZE	CODE IDENT NO. 14213	DWG NUMBER T41063			
ISSUE	C							SHEET	8	OF 14	

AR DENOTES AS REQD NA DENOTES DOCUMENTS				ARS DENOTES AS REQD PER ASSY EM DENOTES EXPENSE MATERIAL ALT DENOTES ALTERNATE PM DENOTES PROCESS MATERIAL		DWG CLASSIFICATION LEVEL UNCLASSIFIED				
QUANTITY REQUIRED				DESIGN AGENCY NO.	DESCRIPTION	NOTE	SHEET ZONE	ITEM		
69		2	HD1-54C174		INTEGRATED CIRCUIT, HEX D FLIP-FLOP MONOLITHIC COMPLEMENTARY MOS(CMOS), HARRIS SEMICONDUCTOR			C3-03 C3-04		
70		1	HD1-54C161		INTEGRATED CIRCUIT, BINARY COUNTER WITH ASYNCHRONOUS CLEAR, HARRIS SEMICONDUCTOR			C4-02		
71		3	HD1-54C85		INTEGRATED CIRCUIT, 4-BIT MAGNITUDE COMPARATOR HARRIS SEMICONDUCTOR			C4-03 C4-04 C4-05		
72		6	MM54C902		INTEGRATED CIRCUIT, HEX LEVEL TRANSLATOR/BUFFER NATIONAL SEMICONDUCTOR			D1-03 D1-04 D2-03 D2-04 D3-05 D1-05		
73		2	916C223X5PE		INTEGRATED CIRCUIT, RESISTOR PACK, 15 EACH 22K SPRAGUE ELEC. CO.			D4-01 D4-02		
74		1	SN54LS11J		INTEGRATED CIRCUIT, TRIPLE 3-INPUT POSITIVE AND GATES, TEXAS INSTRUMENTS			E1-01		
75		1	SN5428J		INTEGRATED CIRCUIT, QUADRUPLE 2-INPUT POSITIVE NOR BUFFERS, TEXAS INSTRUMENTS			E1-02		
76		1	SN54LS00J		INTEGRATED CIRCUIT, QUADRUPLE 2-INPUT POSITIVE NAND GATES, TEXAS INSTRUMENTS			E1-03		
CONTRACT ITEM NO. REF.				DWG CLASSIFICATION LEVEL UNCLASSIFIED		SIZE	CODE IDENT NO.	DWG NUMBER		
ISSUE C							14213	T41063		
								SHEET 9 OF 14		

AR DENOTES AS REQD NA DENOTES DOCUMENTS				ARS DENOTES AS REQD PER ASSY EM DENOTES EXPENSE MATERIAL ALT DENOTES ALTERNATE PM DENOTES PROCESS MATERIAL		DWG CLASSIFICATION LEVEL UNCLASSIFIED				
QUANTITY REQUIRED				DESIGN AGENCY NO.		DESCRIPTION		NOTE	SHEET ZONE	ITEM
77		+1	4	SN54LS196J		INTEGRATED CIRCUIT, 50 MHZ PRESETTABLE DECADE COUNTER, TEXAS INSTRUMENTS			E2-01 E2-02	
									E3-01 E3-06 E3-03	
113			1	MM54C08		INTEGRATED CIRCUIT, QUAD 2-INPUT AND GATE NATIONAL SEMICONDUCTOR			E3-02	
78			1	SN54S00J		INTEGRATED CIRCUIT, QUAD 2-INPUT NAND GATE, TEXAS INSTRUMENTS			E2-05	
79			2	SN54196J		INTEGRATED CIRCUIT, 50 MHZ PRESETTABLE DECADE COUNTER, TEXAS INSTRUMENTS			E2-03 E2-06	
80			1	C0238-A2		INTEGRATED CIRCUIT, 50 MHZ CLOCK OSCILLATOR, VECTRON LABORATORIES, INC.			E2-04	
81			2	914C502X2PD		INTEGRATED CIRCUIT, RESISTOR PACK 12 EACH 5K SPRAGUE ELEC ELEC.			E3-05 E4-03	
82			13	1M6508A-M-DE		INTEGRATED CIRCUIT, 1024 BIT READ ACCESS MEMORY, INTERSIL, INC.			F1-01 THRU F3-01	
83 4			1	CD4043AD		INTEGRATED CIRCUIT, COS/MOS QUAD 3-STATE R/S LATCH, TCA			F4-01	
15 16										
84			5	340097DM		INTEGRATED CIRCUIT, 3-STATE HEX NON-INVERTING AND INVERTING BUFFER, FAIRCHILD			F3-03 F3-04 F3-05 F3-06 F4-06	
CONTRACT ITEM NO. REF.						DWG CLASSIFICATION LEVEL UNCLASSIFIED		SIZE	CODE IDENT NO. 14213	DWG NUMBER T41063
ISSUE IC								SHEET	10	OF 14

AR DENOTES AS REQD NA DENOTES DOCUMENTS				ARS DENOTES AS REQD PER ASSY EM DENOTES EXPENSE MATERIAL ALT DENOTES ALTERNATE PM DENOTES PROCESS MATERIAL		DWG CLASSIFICATION LEVEL UNCLASSIFIED					
QUANTITY REQUIRED				DESIGN AGENCY NO.		DESCRIPTION		NOTE	SHEET ZONE	ITEM	
1			2	CMP-01Y		INTEGRATED CIRCUIT COMPARATOR PRECISION MONOLITHICS INC.			Aa, Ab		
2			1	EP610		BATTERY, 6V, 1AH, ELPOWER CORP.			BT1		
3			1	2143-0		BINDING POST, DOUBLE POMONA ELECTRONICS			E1		
4			3	CK05BX221K		CAP., FIXED, CERAMIC, 220PF $\pm 10\%$, 200WVDC (633185)			C4 C12, C13		
5			2	150D226X005052		CAP., FIXED, ELECT., 22UF $\pm 20\%$, 50WVDC SPRAGUE			C14 C15		
6			4	CK05BX101K		CAP., FIXED, CERAMIC, 100PF $\pm 10\%$, 200WVDC (633183)			C2, C3 C7, C11		
7			4	150D225X9015A2		CAP., FIXED, ELECT. 2.2 UF $\pm 20\%$, 15WVDC SPRAGUE ELEC CO.			C5, C8 C10, C16		
8			1	CK05BX102K		CAP., FIXED, CERAMIC .001UF $\pm 10\%$, 200WVDC (633189)			C6		
9		+1	3	CK06BX103K		CAP., FIXED, CERAMIC, .01UF $\pm 10\%$, 200WVDC (633234)			Cb, Cc Cd C1		
10			3	CK06CW472M		CAP., FIXED, CERAMIC, .0047UF $\pm 20\%$, 200WVDC (603773)			Ch, Cj Ck		
11			3	VK30BX104M		CAP., FIXED, CERAMIC, .1UF $\pm 20\%$, 200WVDC (603782)			Ca, Ce Cf		
12			1	150D224X0035A2		CAP., FIXED, ELECT., .22UF $\pm 20\%$, 35VDW (603636)			Cm		
13			1	IN914		SEMICONDUCTOR DEVICE, DIODE, SWITCHING (839085)			CR1		
14			1	GHV-13		SEMICONDUCTOR DEVICE, GENERAL SEMICONDUCTOR			CRa		
15			1	5082-4655		DIODE LIGHT EMITTING RED, HEWLETT-PACKARD			DS1		
16			1	CF3-GT-1762		LAMP, INCANDESCENT, GREEN, 28V, ELDEMA CORP (613345)			DS2		
17			8	5082-7340		INDICATOR, DIGITAL, HEXADECIMAL, HEWLETT-PACKARD			DS3A THRU DS4D		
CONTRACT ITEM NO. REF. DWG CLASSIFICATION LEVEL UNCLASSIFIED SIZE CODE IDENT NO. 14213 DWG NUMBER T41063											
ISSUE C SHEET 11 OF 14											

AR DENOTES AS REQD NA DENOTES DOCUMENTS				ARS DENOTES AS REQD PER ASSY EM DENOTES EXPENSE MATERIAL ALT DENOTES ALTERNATE PM DENOTES PROCESS MATERIAL		DWG CLASSIFICATION LEVEL UNCLASSIFIED				
QUANTITY REQUIRED				DESIGN AGENCY NO.		DESCRIPTION		NOTE	SHEET ZONE	ITEM
18,19			1	AN3102A-16	CONN, RECP, ELEC.	(609029)8(609132)			J1	
20				LJT00-13-98S	BENDIX, SA1438-10	(358315)			J2	
21		+2	4	UG-2904/U	RF	(818367)			J3, J4 J6, J7 J8, J9	
22			1	LJT00-19-32S	CONN, RECP, ELEC BENDIX, SA1438-3	(358188)			J5	
23			2	SL11D	RELAY, ARMATURE, LATCHING, POTTER-BRUMFIELD	(837664)			K1, K2	
24			1	9250-105	COIL, INDUCTORS, 1000UH, J.W. MILLER				La	
25			3	9250-393	COIL, INDUCTORS, 39UH, J.W. MILLER				Lb, Lc Ld	
26			1	9591-102	POWER SUPPLY, 5V, 1.2 AMP, TECHNETICS, INC.				PS1	
27			1	9591-106	POWER SUPPLY, 30V, .2 AMP, TECHNETICS, INC.				PS2	
28			1	2N2222A	TRANSISTOR, LOW POWER, SILICON NPN (6338C1)				Q1	
29			1	224S-1-201M	RESISTOR, VARIABLE, PANEL MOUNT, 200 OHM $\pm 5\%$ 1 W BOURNS TRIMPOT DIV. (875355-00)				R23	
30			6	RLR05C102GM	RESISTOR, FIXED, FILM, 1 K $\pm 2\%$, 1/8 W, (44005-292)				R1, R20 R22, R26	
31			2	RLR05C562GM	5.6 K $\pm 2\%$, 1/8 W (440005-328)				R27, R29 R2, R3	
32			2	RLR05C103GM	10 K $\pm 2\%$, 1/8 W (440005-340)				R4, R14	
33			2	RLR05C512GM	5.1 K $\pm 2\%$, 1/8 W (440005-326)				R5, R25	
34			7	RLR05C104GM	100 K $\pm 2\%$, 1/8 W (440005-388)				R6, R7 R10, R11 R15, R16 R24	
35			1	RLR05C152GM	RESISTOR, FIXED, FILM, 1.5 K $\pm 2\%$, 1/8 W (440005-300)				R8	
			1	RLR05C101GM	RESISTOR, FIXED, FILM, 100 OHM $\pm 2\%$, 1/8W (44005-244)				R30	
CONTRACT ITEM NO. REF.						DWG CLASSIFICATION LEVEL UNCLASSIFIED		SIZE	CODE IDENT NO.	DWG NUMBER
ISSUE E									14213	T41063
								SHEET 12 OF 14		

AR DENOTES AS REQD NA DENOTES DOCUMENTS				ARS DENOTES AS REQD PER ASSY EM DENOTES EXPENSE MATERIAL ALT DENOTES ALTERNATE PM DENOTES PROCESS MATERIAL				DWG CLASSIFICATION LEVEL UNCLASSIFIED						
QUANTITY REQUIRED				DESIGN AGENCY NO.				DESCRIPTION				NOTE	SHEET ZONE	ITEM
36			4	RLR05C513GM	RESISTOR, FIXED, FILM, 51 K $\pm 2\%$, 1/8 W (440005-374)							R9, R12 R13, R28		
37			1	RNC65H287OFS	287 OHM $\pm 1\%$, 1/4 W (440004-432)							R17		
38		+1	3	RLR05C223GM	22 K $\pm 2\%$, 1/8 W (440005-356)							R18 R19 R21 R31		
39			1	RLR32C330GP	36 OHMS $\pm 2\%$, 1W (440002-222)							Ra		
40			2	RNC65H1002FS	10 K $\pm 1\%$, 1/4 W (440004-580)							Rb, Rd		
41			2	RNC65H2052FS	20.5 K $\pm 1\%$, 1/4 W (440004-610)							Rk, Rj		
42			6	RCR05G510JS	51 OHMS $\pm 5\%$, 1/8 W (440020-165)							Rn, Rp Rq, Rr Rs, Rt		
85			2	RNC65H1003FS	100 K $\pm 1\%$, 1/4 W (440004-676)							Re, Rf		
86			1	RNC65H4022FS	40.2 K $\pm 1\%$, 1/4 W (440004-638)							Rm		
87			1	RNC65H1872FS	18.7 K $\pm 1\%$, 1/4 W (440004-606)							Rl		
88			2	RNC65H51R1FS	RESISTOR, FIXED, FILM 51.1 OHM $\pm 1\%$, 1/4 W (440004-360)							Rc, Rv		
89			1	56PR20K T1	RESISTOR VARIABLE 20K $\pm 5\%$ 1 W, HELITRIM (871488)							Rh		
114			1	933	SWITCH, PUSH, MINIATURE, SPDT - BUTTON TYPE(626486) BLACK, SWITCHCRAFT							S14		
90, 93			3	8837K4	SWITCH, TOGGLE, 2PDT, ON-NONE-ON, MS25307-232(856349) CUTLER-HAMMER							S1, S9, S6		
91			2	8838K4	SWITCH, TOGGLE, 4PDT, ON-NONE-ON (858444) CUTLER-HAMMER							S2, S3		
92			7	2PB299-T2	SWITCH, PUSH BUTTON, HONEYWELL MICROSWITCH DIV(870609)							S4, S5 S7, S8 S11, S12 S13 S10		
94			1	8869K4	SWITCH, TOGGLE, MINIATURE, 2PDT, ON-NONE-ON (874457) MS90311-231, CUTLER HAMMER									
CONTRACT ITEM NO. REF.								DWG CLASSIFICATION LEVEL UNCLASSIFIED		SIZE	CODE IDENT NO.	DWG NUMBER		
ISSUE								UNCLASSIFIED		14213	T41063			
E										SHEET	13	OF	14	

DESIGN AGENCY CONTROL NO.		ISSUE		REVISIONS		PREPARED BY		DATE		CHKR		ENGR	
DL-T43153-000		A		D. KEENER 9652		D. FOGEL 1123						1/17/76	
		B		DS4D WAS DS4B, ADDED		B & S 2 PLCS		9-15-76				1/14/76	
				D. KEENER 9652		D. FOGEL 1123							

- RED - CIRCUITRY NEAR SIDE
- BLUE - CIRCUITRY FAR SIDE
- BROWN - CIRCUITRY BOTH SIDES
- TERMINAL SIZES ARE (COLOR CODE SIZES REQ'D IN TABLE AND ON LAYOUT).
- ALL LINE WIDTHS ARE .002, .005, .010, .015, .020, .025, .040, .050, .100, .125, .150 (CIRCLE SIZE).
- MINIMUM CLEARANCE BETWEEN CIRCUITS AND CIRCUITRY AND EDGE OF THE BOARD IS .010 (CIRCLE SIZE).
- LOCATE IDENTIFICATION INFORMATION AS SHOWN.
- SUPPLIER WILL BE FURNISHED DUPLICATE REPRODUCTION OF MASTER DRAWING CM-T43153 FOR PLATE MAKING PURPOSE.
- MATERIAL: PLASTIC SHEET, LAMINATED, 2 OZ. COPPER CLAD BOTH SIDES, GLASS BASE, EPOXY RESIN, FLAME RETARDANT, .062 THK (FL-GF OR GH-062-C-2/2, m11-P-13949)(531 236)
- FABRICATE PRINTED-WIRING ASSEMBLY PER 9928009, USING TIN-LEAD PLATING.
- SEE T41063 AND AY-T41063 FOR COMPONENT VALUE AND ASSEMBLY INFORMATION.

TERMINAL SIZE	HOLE DIA	HOLE DIA	HOLE DIA
.040	⊕	⊕	⊕
.050	⊕	⊕	⊕
.062	⊕ .027/.033	⊕	⊕
.075	⊕	⊕	⊕
.086	⊕	⊕	⊕
.100	⊕	⊕	⊕
.125	⊕	⊕	⊕
.150	⊕	⊕	⊕
.175	⊕ .096/.102	⊕	⊕

AGENCY APPROVALS			SHEET		TITLE	
ORG	DATE	APPROVALS	ISSUE	INDEX	LAYOUT, READOUT BOARD, RECORDER	
PART CLASSIFICATION					SIZE CODE IDENT. NO. DWG NUMBER	
UNCLASSIFIED					D 14213 DL-T43153	
					SCALE 4/1 SHEET 1 OF 1	

NOTES

1. PIN NUMBER OF CONNECTOR PLUG D3-01.
2. PIN NUMBER OF CONNECTOR PLUG E4-01.

3. JUMPED WIRE BETWEEN PANEL/CHASSIS MOUNTED COMPONENTS AND WIRE-BOUND BOARDS. TERMINAL DESIGNATIONS SHOWN IN PARENTHESES. (1) INDICATE COMPLETE UNTESTED LOGIC CIRCUIT. UNTESTED INPUT TERMINALS OF

4. DON'T LOGIC CIRCUITS ARE CONNECTED TO POWER AND/OR GROUND TO ENHANCE RELIABILITY. THESE TERMINALS ARE SHOWN IN THE 'CONNECTED' COLUMN.
5. SOLDER TERMINAL ON SIGNAL/INPUT CIRCUIT BOARD.
6. SOLDER TERMINAL ON RECORDER BOARD OUT BOARD.

REF. DESIG.	IC TYPE	UNTESTED TERMINALS	TESTED
A	D. KEENE 9652	7, 9	10
B	S. MOETHEN 1123	7, 9, 10, 11, 12, 13, 14, 15	16
C	D. KEENE 9652	7, 9	10
D	S. MOETHEN 1123	7, 9, 10, 11, 12, 13, 14, 15	16
E	D. KEENE 9652	7, 9	10
F	S. MOETHEN 1123	7, 9, 10, 11, 12, 13, 14, 15	16

SOCKET BOARD C

REF. DESIG.	IC TYPE	UNTESTED TERMINALS	TESTED
C1-01	MC1558AL	7, 9	10
C1-02	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
C1-03	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
C1-04	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
C1-05	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
C1-06	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
C1-07	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
C1-08	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
C1-09	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
C1-10	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
C1-11	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
C1-12	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
C1-13	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
C1-14	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
C1-15	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
C1-16	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
C1-17	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
C1-18	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
C1-19	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
C1-20	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16

SOCKET BOARD D

REF. DESIG.	IC TYPE	UNTESTED TERMINALS	TESTED
D1-01	MC1558AL	7, 9	10
D1-02	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
D1-03	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
D1-04	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
D1-05	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
D1-06	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
D1-07	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
D1-08	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
D1-09	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
D1-10	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
D1-11	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
D1-12	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
D1-13	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
D1-14	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
D1-15	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
D1-16	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
D1-17	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
D1-18	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
D1-19	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
D1-20	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16

SOCKET BOARD E

REF. DESIG.	IC TYPE	UNTESTED TERMINALS	TESTED
E1-01	MC1558AL	7, 9	10
E1-02	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
E1-03	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
E1-04	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
E1-05	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
E1-06	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
E1-07	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
E1-08	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
E1-09	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
E1-10	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
E1-11	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
E1-12	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
E1-13	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
E1-14	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
E1-15	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
E1-16	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
E1-17	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
E1-18	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
E1-19	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
E1-20	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16

SOCKET BOARD F

REF. DESIG.	IC TYPE	UNTESTED TERMINALS	TESTED
F1-01	MC1558AL	7, 9	10
F1-02	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F1-03	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F1-04	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F1-05	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F1-06	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F1-07	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F1-08	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F1-09	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F1-10	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F1-11	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F1-12	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F1-13	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F1-14	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F1-15	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F1-16	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F1-17	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F1-18	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F1-19	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F1-20	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16

REF. DESIG.	IC TYPE	UNTESTED TERMINALS	TESTED
F2-01	MC1558AL	7, 9	10
F2-02	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F2-03	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F2-04	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F2-05	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F2-06	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F2-07	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F2-08	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F2-09	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F2-10	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F2-11	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F2-12	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F2-13	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F2-14	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F2-15	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F2-16	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F2-17	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F2-18	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F2-19	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16
F2-20	MC1558AL	7, 9, 10, 11, 12, 13, 14, 15	16

DWG. NO. CK-T41063 E SHEET 2 OF 3

DESIGN AGENCY		REVISIONS		0131957	
PART NO.	ISSUE	DESCRIPTION	PREPARED BY	DATE	CHKR
DL-T43184-000	A	D. KEENER 9652 J. LOUKOTA 1123			
	B	.400 TERMINAL SIZE WAS .300, +28V WAS 28V R _h , R _p , R _g , R _r , R _s & R _t WERE .033/.039 DIA HOLE D. KEENER 9652 J. LOUKOTA 1123			
	C	DWG NO. WAS T83184 D. KEENER 9652 J. LOUKOTA 1123		10-4-76	

9. SUPPLIER WILL BE FURNISHED DUPLICATE REPRODUCTION OF MASTER DRAWING CM-T83184 FOR PLATE MAKING PURPOSE.
10. MATERIAL: PLASTIC SHEET, LAMINATED, 2 OZ. COPPER CLAD BOTH SIDES, GLASS BASE, EPOXY RESIN, FLAME RETARDANT, .062 THK (FL-GF OR GH-062-C-2/2, MIL-P-13949) (531 236)
11. FABRICATE PRINTED-WIRING ASSEMBLY PER 9928009, USING TIN-LEAD PLATING.
12. SEE T41063 AND AY-T41063 FOR COMPONENT VALUE AND ASSEMBLY INFORMATION.

1. RED - CIRCUITRY NEAR SIDE
2. BLUE - CIRCUITRY FAR SIDE
3. BROWN - CIRCUITRY BOTH SIDES
4. TERMINAL SIZES ARE (COLOR CODE SIZES REQ'D IN TABLE AND ON LAYOUT).

TERMINAL SIZE	HOLE DIA	HOLE DIA	HOLE DIA
.040	⊕	⊕	⊕
.050	⊕	⊕	⊕
.062	⊕ .027/.033	⊕	⊕
.075	⊕	⊕	⊕
.086	⊕	⊕	⊕
.100	⊕ .033/.039	⊕ .025/.030	⊕
.125	⊕ .043/.048	⊕	⊕
.150	⊕	⊕	⊕
.175	⊕ .096/.102	⊕	⊕
.460	⊕ .152/.160		

5. ALL LINE WIDTHS ARE .002, .005, .010, .015, .020, .025, .040, .050, .100, .125, .150 (CIRCLE SIZE).
6. MINIMUM CLEARANCE BETWEEN CIRCUITS AND CIRCUITRY AND EDGE OF THE BOARD IS .010, .015, .020, .025, .030, .040, .050, OTHER (CIRCLE SIZE).
7. LOCATE IDENTIFICATION INFORMATION AS SHOWN.

B. GROUND PLANE FAR SIDE.

AGENCY APPROVALS			SHEET		TITLE	
ORG	DATE	APPROVALS	ISSUE	C	LAYOUT, SIGNAL/ FIDU INPUT CIRCUIT	
					UNCLASSIFIED	
					UNCLASSIFIED	
					SIZE	CODE IDENT. NO.
					D 14213	DL-T43184
					SCALE	2/1
					SHEET	OF

STATION NAME		STATION NO.		STATION NAME		STATION NO.	
STATION NAME		STATION NO.		STATION NAME		STATION NO.	
AK-741063 000	N	G. WORTHEN	1123				
		D. KREMER	9658				
	B	G. WORTHEN	1123				1/2
		D. KREMER	9658				
	C	ADDED PART STEP TO					
		57, D. KREMER	9658				
		G. WORTHEN	1123				
	D	ADDED REF F-30					
		D. KREMER	9658				
		G. WORTHEN	1123				1/2
	E	D. KREMER	9658				
		G. WORTHEN	1123				

HOLE TABLE			
ITEM	DEVELOP	IN	OUT
A	300	308	11
B	125	130	11
C	375	383	9
D	147	152	42
E	180	200	1
F	750	780	1
G	240	260	2
H			
J	106	108	1
K	113	116	1
L			
M			
N			
P			
R			
S			

CHANGES TO TEMPLATE VIEWS
MUST BE MADE TO SCALE

TITLE			
ASSEMBLY, DIGITAL SLIFER RECORDER, MOD A			
SIZ	CODE	IDENT NO	CARD NUMBER
E	14213		AY-T41C23
SCALE	1	1	OF

SOLDER C5 LEAD TO BOTH
B1-10 AND B1-8 BEFORE
TRIMMING TO LENGTH

SOLDER E25 LEAD TO BOTH
B1-35 AND B1-34 BEFORE
TRIMMING TO LENGTH

"HOUSE" CARD

"20 SOLID
BUS" WIRES

B

C

D

E

F

WIRE-WRAP PRINTED CIRCUIT CARDS COMPONENT ASSEMBLY

ITEM 1
SCALE 1/1
FRONT PANEL TO BE MATCH
MARKED AND LABELLED EXCEPT
AS SHOWN FROM ITEM 2

DATE	FILE	REV	BY
11/14/73	AY-14063	1	1
UNCLASSIFIED			

ITEM 16
SCALE 1/1
BATTERY BOARD
ASSEMBLY

REVISION	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50
UNCLASSIFIED																																																		
E114213 AY-141063																																																		
SCALE NOTED																																																		

APPENDIX B
Data Sheets

CD4043AD

The RCA-CD4043A types are quad cross-coupled 3-state COS/MOS NOR latches. Each latch has a separate Q output and individual SET and RESET inputs. The Q outputs are controlled by a common ENABLE input. A logic "1" or high on the ENABLE input connects the latch states to the Q outputs. A logic "0" or low on the ENABLE input disconnects the latch states from the Q outputs, resulting in an open circuit condition on the Q outputs. The open circuit feature allows common busing of the outputs. The logic operation of the latches is summarized in the truth table.

The CD4043A types are supplied in 16-lead hermetic dual-in-line ceramic packages (D, F, Y suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in-chip form (H suffix).

Features

- 3-Level outputs with common output ENABLE
- Separate SET and RESET inputs for each latch
- Quiescent current specified to 15V
- Maximum input leakage of 1 μ A at 15V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

S	R	E	Q
X	X	0	OC*
0	0	1	NC+
1	0	1	1
0	1	1	0
1	1	1	Δ

* Open Circuit

+ No Change

Δ Dominated by S = 1 Input

CD4043A Functional Diagram

CD4049AD

Hex Buffers

The CD4049AD hex inverter/buffers are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS devices find primary use where low power dissipation and/or high noise immunity is desired. These devices provide logic-level conversion using only one supply voltage, V_{CC} . The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage for logic-level conversions. Two TTL/DTL loads can be driven when the devices are used as CMOS-to-TTL/DTL converters ($V_{CC} = 5.0\text{ V}$, $V_{OL} \leq 0.4\text{ V}$, $I_{OL} \geq 3.2\text{ mA}$). Note that pin 16 is not connected internally on these devices; consequently, connections to this terminal will not affect circuit operation.

- Direct Drive of Two TTL/DTL Loads
- High Source and Sink Currents
- High-to-Low or Low-to-High Level Converter
- Quiescent Power Dissipation = 5 nW/package typical
- Single-Supply, Pin-for-Pin Replacements for Types MC14009

Maximum Ratings (Voltages Referenced to V_{SS} , Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{CC}	+18 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	+18 to -0.5	Vdc
DC Current per Input Pin	I_{in}	10	mAdc
DC Current per Output Pin	I_{out}	45	mAdc
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Logic Diagram

NC = Pin 16
 V_{SS} = Pin 8
 V_{CC} = Pin 1

CMP-01Y

Absolute Maximum Ratings

Total Supply Voltage, V+ to V-	35V
Output to Ground	-5V to +32V
Output to Negative Supply Voltage	50V
Ground to Negative Supply Voltage	30V
Positive Supply Voltage to Ground	30V
Positive Supply Voltage to Offset Null	0 to 2V
Power Dissipation (See Note)	500 mW
Differential Input Voltage	±11V
Input Voltage ($V_S = \pm 15V$)	±15V
Output Sink Current (Continuous Operation)	75mA
Operating Temperature Range	-55 to +125°C.
Storage Temperature Range	-65 to 150°C
Lead Temperature (Soldering, 60 s)	300°C
Output Short Circuit Duration - to ground	Indefinite
to V+	1 min.

Note: Maximum package power dissipation vs. ambient temperature.

Maximum Ambient Temperature for Rating = 100°C

Derate Above Maximum Ambient Temperature = 10.0 mW/°C.

Pin Connections (Top View)

14-Pin DIP

C0238-A2

Features: Consumes space of only one 14-pin DIP 0.35 in. high

Frequency: 3 MHz thru 100 MHz

Output: Drives 10 TTL loads (above 50 MHz drive capability decreases: at 100 MHz drives 2 Schottky TTL loads). Logic "0": 0.4V max, sink 16 ma. Logic "1": 2.4V min, source 2 ma. Symmetry: 50/50 $\pm$ 15% (improved symmetry available on some models).

Input Voltage: 5 VDC $\pm$ 5%

Input Current: 15-80 ma; current drain depends upon frequency - it is typically 15-20 ma in 4-20 MHz range.

Tuning Option Available: No

Accuracy (Maximum error at 25°C): C0-238A: $\pm$ 0.005%

Stability-Standard (See below for options): 0°C to +70°C: $\pm$ 0.0025%. +20°C to +30°C: $\pm$ 0.0005%.

Stability-Options Available: 1; 2 (to 70 MHz); 3 (above 6 MHz); 5 (above 4 MHz); 6; and 8.

Definition of Stability Options: 1 = -55 to +85°C: $\pm$ 0.005%. 2 = -55 to +125°C: $\pm$ 0.005%. 3 = 0 to +50°C: $\pm$ 0.0003%. 5 = 0 to +50°C: $\pm$ 0.0005%. 6 = 0 to +50°C: $\pm$ 0.001%. 8 = 0 to +70°C: $\pm$ 0.01% (includes initial accuracy)

Size/Weight: 0.5 x 0.8 x 0.35 in., 1/8 oz. (12.7 x 20.3 x 8.9 mm, 3 g)

Mounting:

Note: Pins 4 and 8 may be externally tied together.

HD1-54C85

General Description

The HD1-54C85 is a four-bit magnitude comparator which will perform comparison of straight binary or BCD codes. The circuit consists of eight comparing inputs (A0, A1, A2, A3, B0, B1, B2, B3), three cascading inputs (A>B, A<B and A=B), and three outputs (A>B, A<B and A=B). This device compares two four-bit words (A and B) and determines whether they are "greater than," "less than," or "equal to" each other by a high level on the appropriate output. For words greater than four-bits, units can be cascaded by connecting the outputs (A>B, A<B, and A=B) of the least-significant stage to the cascade inputs (A>B, A<B and A=B) of the next-significant stage. In addition the least significant stage must have a high level voltage ($V_{IN(1)}$) applied to the A=B input and low level voltages ($V_{IN(0)}$) applied to A>B and A<B inputs.

Features

- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45 V_{CC} typ
- Low power TTL compatibility fan out of 2 driving 74L
- Expandable to 'N' stages
- Applicable to binary or BCD

Logic Diagram

General Description

These (synchronous presettable up) counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They feature an internal carry lookahead for fast counting schemes and for cascading packages without additional gating.

A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the C161 is asynchronous and a low level at the clear input sets all four outputs low regardless of the state of the clock.

Counting is enabled when both count enable inputs are high. Input T is also fed forward to enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low.

Features

- High noise margin
  - High noise immunity
  - Tenth power TTL compatible
  - Wide supply voltage range
  - Internal look-ahead for fast counting schemes
  - Carry output for N-bit cascading
  - Load control line
  - Synchronously programmable
- 1V guaranteed
0.45 V_{CC} typ
drives 2 LPTTL loads
3V to 15V

Connection Diagram

Logic Diagram

Top View

General Description

The HD1-54C174 hex D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. All have a direct clear input. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clear is independent of clock and accomplished by a low level at the clear input. All inputs are protected by diodes to V_{cc} and GND.

Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{cc} typ
- Guaranteed noise margin 1.0V
- Low power TTL compatibility fan out of 2 driving 74L

Logic Diagram

Connection Diagram

Top View

Truth Table

Inputs			Output
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q

General Description

The IM6508's are high-speed, low-power, silicon gate CMOS 1024-bit static RAM's organized 1024 words by 1 bit. In all static states these RAM's exhibit the microwatt power requirements typical of CMOS. Inputs and three-state output are TTL compatible. The basic part operates at 4 to 7 volts with a 5V, 25°C access time of 350 ns and supply current of 100 μ A. Faster access times and lower supply currents are offered in a DASH-1 version. Higher operating voltages are offered in an "A" version. Data retention is guaranteed to 3 volts on all parts.

Write Enable and Chip Select functions are active in the low state. These functions are specified for easy interface to common I/O data busses. On-chip address registers (clocked by the falling edge of CS_1) can often improve system performance and reduce package count.

These devices are ideally suited for memory systems requiring low operating power, high performance or non-volatility (battery backup).

Features

- Low Power Operation
- Excellent Speed Operation
- TTL or CMOS Compatible on Inputs and Outputs
- 4V-11V V_{CC} Operation
- Static Operation
- On-Chip Address Register

Connection Diagram

Pin 1 is designated either by a dot or a notch.

MC14001AL

Quad 2-Input "NOR" Gate

The MC14001 quad 2-Input NOR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 10 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation - Positive or Negative
- High Fanout >50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4001A

Maximum Ratings (Voltages Referenced to V_{SS} , Pin 7)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+18 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Logic Diagram
Positive Logic

V_{DD} = Pin 14

V_{SS} = Pin 7

$$3 = 1 + 2$$

MC14002AL

Dual 4-Input "NOR" Gate

The MC14002 dual 4-input NOR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 10 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation - Positive or Negative
- High Fanout >50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Pin-for-Pin Replacement for CD4002A.

Maximum Ratings (Voltages Referenced to V_{SS} , Pin 7)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+18 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Logic Diagram
Positive Logic

V_{DD} = Pin 14
 V_{SS} = Pin 7

MC14011AL

Quad 2-Input "NAND" Gate

The MC14011 quad 2-input NAND gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 10 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation - Positive or Negative
- High Fanout - >50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Symmetrical Output Resistance - 750 ohms typical

Maximum Ratings (Voltages Referenced to V_{SS} , Pin 7)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+18 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Logic Diagram
Positive Logic

V_{DD} = Pin 14

V_{SS} = Pin 7

$$3 = \overline{1 \cdot 2}$$

MC14013AL

Dual Type D Flip-Flop

The MC14013 dual type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data (D), Direct Set (S), Direct Reset (R), and Clock (C) inputs and complementary outputs (Q and $\bar{Q}$). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Static Operation
- Quiescent Power Dissipation = 25 nW/ package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation
- Toggle Rate = 10 MHz
- Logic Edge-Clocked Flip-Flop Design - Logic state is retained indefinitely with clock level either high or low, information is transferred to the output only on the positive-going edge of the clock pulse.
- Pin-for-Pin Replacement for CD4013A

Maximum Ratings (Voltages Referenced to V_{SS} , Pin 7)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+18 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Truth Table

Clock*	Inputs			Outputs	
	Data	Reset	Set	Q	$\bar{Q}$
	0	0	0	0	1
	1	0	0	1	0
	X	0	0	Q	$\bar{Q}$
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	.	.

X = Don't Care

* = Level Change

. = Invalid Condition

Block Diagram

MC14025AL

Triple 3-Input "NOR" Gate

The MC14025 triple 3-input NOR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Power Dissipation = 10 nW/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation - Positive or Negative
- High Fanout - >50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Symmetrical Output Resistance - 750 ohms typical
- Pin-for-Pin Replacement for CD4025A

Maximum Ratings (Voltages Referenced to V_{SS} , Pin 7)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+18 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Logic Diagram
(Positive Logic)

MC14040AL

12-Bit Binary Counter

The MC14040 12-stage binary counter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. This part is designed with an input wave shaping circuit and 12 stages of ripple-carry binary counter. The device advances the count on the negative-going edge of the clock pulse. Applications include time delay circuits, counter controls, and frequency-driving circuits.

- Fully Static Operation
- Quiescent Power Dissipation = 50 nW/package typical at $V_{DD} = 5.0\text{ V}$
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance = 5.0 pF typical
- All 12 Buffered Outputs Available
- Common Reset Line
- 13 MHz Typical Counting Rate at $V_{DD} = 15\text{ V}$
- Pin-for-Pin Replacement for CD4040A

Maximum Ratings (Voltages Referenced to V_{SS} , Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+18 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Truth Table

Clock	Reset	Output State
	0	No Change
	0	Advance to Next State
X	1	All Outputs are Low

X = Don't Care

Logic Diagram

MC14519AL

4-Bit and/or Selector or Quad 2-Channel Data Selector or Quad Exclusive "NOR" Gate

The MC14519 is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

This device exemplifies the design versatility of MCMOS logic structure. This part provides three functions in one package: a 4-bit AND/OR Selector, a Quad 2-channel Data Selector, or a Quad Exclusive NOR Gate.

- Quiescent Power Dissipation = 100 nW/ package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation - Positive or Negative
- High Fanout >50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout
- Plug-In Replacement for CD4019 in Most Applications

Truth Table

Control Inputs		Output
A	B	Z_n
0	0	0
0	1	Y_n
1	0	X_n
1	1	$X_n \oplus Y_n$

Note: $X_n \oplus Y_n$ means X_n
(Exclusive-NOR) Y_n

V_{DD} = Pin 16
 V_{SS} = Pin 8

MC14520AL
MC14518AL

Dual Up Counters

The MC14518 dual BCD counter and the MC14520 dual binary counter are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4-stage counters. The counter stages are type D flip-flops, with interchangeable Clock and Enable lines for incrementing on either the positive-going or negative-going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518 will count out of all undefined stages within two clock periods. These complementary MOS up counters find primary use in multi-stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

- Quiescent Power Dissipation = 1.0 μ W/package typical
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Low Input Capacitance = 5.0 pF typical
- Internally Synchronous for High Internal and External Speeds
- Logic Edge-Clocked Design - Incremented on Positive Transition of Clock or Negative Transition on Enable
- 6.0 MHz Counting Rate

Maximum Ratings (Voltages Referenced to V_{SS} , Pin 8)

Truth Table

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+18 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain Per Pin	I	10	mAdc
Operating Temperature Range	T_A	-55 to +125	$^{\circ}$ C
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}$ C

Clock	Enable	Reset	Action
	1	0	Increment Counter
0		0	Increment Counter
	X	0	No Change
X		0	No Change
	0	0	No Change
1		0	No Change
X	X	1	Q0 thru Q3 - 0

Block Diagram

X = Don't Care

MC14528AL

Dual Monostable Multivibrator

The MC14528 provides the function of a dual, retriggerable, resettable, monostable multivibrator. This device may be triggered from either edge of an input pulse and will produce an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components C_X and R_X .

- Separate Reset Available
- Low Quiescent Power Dissipation - 25 nW at 5.0 Vdc
- Diode Protection on All Inputs
- Triggerable from Leading or Trailing Edge Pulse

Maximum Ratings (Voltages Referenced to V_{SS} , Pin 8)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+18 to -0.5	Vdc
Input Voltage, All Inputs	V_{in}	V_{DD} to -0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

Block Diagram

MM54C08

Quad 2-Input and Gate

General Description

Employing complementary MOS (CMOS) transistors to achieve wide power supply operating range, low power consumption, and high noise margin, these gates provide basic functions used in the implementation of digital integrated circuit systems. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No dc power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45 V_{CC} typ
- Low power TTL compatibility fan out of 2 driving 74L
- Low power consumption 10 nW/package typ

Connection Diagrams

Top View

Truth Tables

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Level
L = Low Level

MM54C902

Hex Non-Inverting TTL Buffer

General Description

These hex buffers employ complementary MOS to achieve wide supply operating range, low power consumption, and high noise immunity. These buffers provide direct interface from PMOS into CMOS or TTL and direct interface from CMOS to TTL or CMOS operating at a reduced V_{cc} supply.

Features

- Wide supply voltage range   3.0V to 15V
- Guaranteed noise margin   1.0V
- High noise immunity   0.45 V_{cc} typ
- TTL compatibility   fan out of 2 driving standard TTL

Top View

SN54LS00J

Quad 2-Input NAND Gate

Guaranteed Operating Ranges

Supply Voltage			Temperature
Min	Typ	Max	
4.5 V	5.0 V	5.5 V	-55 to 125°C

SN54LS11J

Triple 3-Input and Gate

Guaranteed Operating Ranges

Supply Voltage			Temperature
Min	Typ	Max	
4.5 V	5.0 V	5.5 V	-55 to 125°C

Dual-In-Line

- Performs BCD, Bi-Quinary, or Binary Counting
- Fully Programmable
- Fully Independent Clear Input
- Input Clamping Diodes Simplify System Design
- Output Q_A Maintains Full Fan-out Capability in Addition to Driving Clock-2 Input

Guaranteed		Typical Power Dissipation
Count	Frequency	
Clock 1	Clock 2	
0-30 MHz	0-15 MHz	60 mW

Description

These high-speed monolithic counters consist of four d-c coupled, master-slave flip-flops which are internally interconnected to provide a divide-by-two and a divide-by-five counter. These four counters are fully programmable (that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs). The outputs will change to agree with the data inputs independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which, when taken low, sets all outputs low regardless of the states of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low but will remain unchanged when the count/load is high and the clock inputs are inactive.

All inputs are diode-clamped to minimize transmission-line effects and simplify system design. These circuits are compatible with most TTL and DTL logic families. Typical power dissipation is 60 milliwatts. Circuits are characterized for operation over the full military temperature range of -55 to 125°C.

SN54S00J

Quadruple 2-Input NAND Gates

Typical Propagation Time . . . 3 ns at $C_L = 15$ pF

Typical Power Dissipation . . . 19 mW per Gate at 50% Duty Cycle

Recommended Operating Conditions

	<u>Min</u>	<u>Nom</u>	<u>Max</u>	<u>Unit</u>
Supply voltage, V_{CC}	4.5	5	5.5	V
Normalized fan-out from each output, N	{ High logic level			20
	{ Low logic level			10
Operating free-air temperature, T_A	-55		125	°C

Dual-In-Line

Positive Logic: $Y = \overline{AB}$

SN5428J

Quadruple 2-Input Positive-NOR Buffers

positive logic: $Y = \overline{A+B}$

Dual-In-Line

- Performs BCD, Bi-Quinary, or Binary Counting
- Fully Programmable
- Fully Independent Clear Input
- Guaranteed to Count at Input Frequencies from 0 to 50 MHz
- Input Clamping Diodes Simplify System Design

Description

These high-speed monolithic counters consist of four d-c coupled, master-slave flip-flops which are internally interconnected to provide a divide-by-two and a divide-by-five counter. These four counters are fully programmable (that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs). The outputs will change to agree with the data inputs independent of the state of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low but will remain unchanged when the count/load is high and the clock inputs are inactive.

These high-speed counters will accept count frequencies of 0 to 50 megahertz at the clock-1 input and 0 to 25 megahertz at the clock-2 input. During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which, when taken low, sets all outputs low regardless of the states of the clocks.

All inputs are diode-clamped to minimize transmission-line effects and simplify system design. These circuits are compatible with most TTL and DTL logic families. Typical power dissipation is 240 milliwatts. Circuits are characterized for operation over the full military temperature range of -55 to 125°C.

914C502X2PD

- Designed for use in signal and data processing applications where repetitive resistance values and patterns are required.
- Cut package count, reduce equipment size, minimize costs.
- Up to 28 metal-film resistors on ceramic base.
- High packaging density - fewer components to stock, handle, inspect, install.
- Standard resistance tolerance, $\pm 2\%$.
- Typical temp. coefficient, with 250 ppm/ $^{\circ}\text{C}$. Tracking between resistors, ± 50 ppm/ $^{\circ}\text{C}$.
- Type 914C has dual in-line packages compatible with ICs. Continuous power dissipation at 25 C is 3W and 3.5W, respectively. Derating is linear to $+150$ C.
- For data on Type 914C, see Bulletin 7042.

916C223XSPE

- Designed for use in signal and data processing applications where repetitive resistance values and patterns are required.
- Cut package count, reduce equipment size, minimize costs.
- Up to 28 metal-film resistors on ceramic base.
- High packaging density - fewer components to stock, handle, inspect, install.
- Standard resistance tolerance, $\pm 2\%$.
- Typical temp. coefficient, with 250 ppm/ $^{\circ}\text{C}$. Tracking between resistors, ± 50 ppm/ $^{\circ}\text{C}$.
- Type 916C has dual-in-line packages compatible with ICs. Continuous power dissipation at 25 C is 3W and 3.5W respectively. Derating is linear to +150 C.
- For data on Type 916C, see Bulletin 7042.

3-State Hex Non-Inverting Buffers

Description

These CMOS buffers provide high current output capability suitable for driving high capacitance loads. The 340097 is a Non-Inverting CMOS Buffer with 3-state outputs. The 3-state outputs of each device are controlled by two Enable Inputs ($\overline{EO}_4$, $\overline{EO}_2$). A HIGH on Enable Input $\overline{EO}_4$ causes the Outputs of four of the six buffer elements to assume a high impedance or OFF state, regardless of other input conditions, and a HIGH on Enable Input $\overline{EO}_2$ causes the Outputs of the remaining two buffer elements to assume a high impedance or OFF state, regardless of other input conditions.

- 3-State Outputs
- TTL Compatible - Fan Out of One TTL Load
- Active Low Enable Inputs

Pin Names

1A-6A	Buffer Inputs
$\overline{EO}_4$, $\overline{EO}_2$	Enable Inputs (Active LOW)
1X-6X	Buffer Outputs (Active HIGH)

Connection Diagram
DIP (Top View)

340097 Logic Diagram

V_{DD} = Pin 16

V_{SS} = Pin 8

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