PROGRAMMABLE MULTI-TIMER FOR TRU WASTE ANALYSIS APPLICATIONS*

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Summary

A programmable, multiple-function timing module has been developed for use in transuranic (TRU) waste analysis applications at the Idaho National Engineering Laboratory. The Programmable Multi-Timer (PRMT) is an expanded version of a module originally built for accelerator-based active photon interrogation experiments[1,2]. During the course of the experiments, it became obvious that a more versatile timer was needed to meet several unforeseen requirements. The PRMT was designed to meet the new requirements and to serve as a general-purpose timing module for other applications.

For photon interrogation, two independent timing gates (T1 and T2) of variable width and delay are required. The gates are used to seperate induced prompt and delayed photofission neutrons that occur after an accelerator injection pulse. The T1/T2 circuits are triggered ON by the application of an externally applied trigger pulse from the accelerator. The T1 and T2 gating pulses are generated at the end of user-programmed delays after the trigger pulse. In addition to the external trigger capability, the PRMT has been designed to trigger the T1/T2 circuits from a variable, internal, periodic source. Delay times and pulse widths are variable from Ø to 999 X 10^7 microseconds.

A 24-hour time-of-day (TOD) clock has been included in the PRMT. The PRMT has the capability of generating two independent timing gates based on time-of day requirements. Two variable general-purpose reference frequency outputs are also available from the TOD clock.

User-selected operating parameters for the T1/T2 circuits, trigger selection, the TOD clock and gates, and the reference frequencies are loaded in memory in the PRMT. Memory includes data latches and a random access memory (RAM).

A print mode circuit permits hard-copy output from the RAM to a strip printer or TTY via a standard ORTEC printing loop.

In addition to its use in photon interrogation, the PRMT is being used as a controller for neutron multiplication experiments. In conjunction with various special-purpose modules, data for neutron time correlated distributions can be obtained.

The PRMT is regularly used as a gate and/or trigger controller for external equipment such as oscilloscopes, pulse height analyzers, etc.

OPERATION

The PRMT is operated from the front panel via two sets of thumbwheel switches, two pushbutton switches, and two toggle switches. A two digit thumbwheel switch selects 1 of 16 function addresses. Data is selected by a four-digit thumbwheel switch. With the address and data selected, depression of the STORE pushbutton will load the data into the appropriate address in a 16 X 16 RAM. The RAM function addresses are listed in Table 1. For certain function addresses, the data is also loaded into data latches. Immediately after the data is loaded to the RAM, that memory location is automatically read and the contents displayed in a six-digit LED display. Four digits of data and a two-digit memory address are displayed, except for the time-of-day location that displays hours, minutes, and seconds in a continuously updating mode. At any time, except during a PRINT cycle, the contents of any memory location may be displayed by selecting a function address and depressing the DISPLAY pushbutton switch. For display, the data switches are ignored.

Two toggle switches complete the front-panel controls. Timing gates activated by the time-of-day clock may be delayed up to three days. There are two sets of time-of-day gates. A toggle switch selects #1 or #2 for delay programming. The second toggle switch selects the polarity of input data to a coincidence circuit. The output of the circuit is a function of the T1 gate and input data.

SYSTEM DESCRIPTION

Physical

The PRMT is built into a standard triple-width Nuclear Instrumentation Module (NIM). Input and output signal connections to the module are made through 24 BNC cable connectors on the front panel. The control cable to connect the module into the print mode loop mates with a miniature D-type connector mounted on the rear panel.

Internally, the circuit components are mounted on two wire-wrap cards. Connections between the two cards and the components on the front panel are made through plug-in ribbon-cable connectors. Logic devices are primarily Low-Power-Schottky TTL types.

Functional

The primary clock for the PRMT is a crystal controlled oscillator circuit operating at 10 MHz. The oscillator drives two counter circuits to generate pulses for the programmed timing gates. The clock and counters are shown in the simplified block diagram of Figure 3. A continuously driven, seven-decade real time clock (RTC) counter is used to generate time-of-day information. The second counter is an eight-decade, triggered circuit to determine elapsed time after a selected trigger event. The outputs of all decades of both counters are available, through programming, for rate information.

Triggered Clock Circuits. These circuits generate two independent, variable width gating pulses (T1 and T2) that occur some variable delay after a trigger event. See Figure 3. The trigger may be internally or externally generated. Trigger selection and internal repetition rate are programmed from the front panel to RAM address Ø7. Internal trigger selection is made by a "Ø" in the trigger select digit. See Table 1. A "1" selects an external trigger. The internal

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TABLE 1

FUNCTION ADDRESSES

Address	Input	Display	Function
00-04	XXXX	XXXX0Y	General information channels. 0Y is Address.
05	HHMM	HHMMSS	Time-of-day in hours, minutes, and seconds.
06	--N_2N_1	--$N_2N_1$06	Reference frequency repetition rates.
07	ABCD	ABCD07	A: Trigger Select B,C: RTC Delays. D: Internal Trigger Repetition Rate.
08	$M_2M_1M_0N$	$M_2M_1M_0$N08	TI Start Time = $M_2M_1M_0 \times 10^N$ microseconds.
09-11	Same as 08 Except Display Address		TI Stop Time, T2 Start Time, T2 Stop Time.
12	HHMM	HHMM12	RTC1 Start Time Given as Time-Of-day
13-15	Same as 12 Except Display Address		RTC1 Stop Time, RTC2 Start Time, RTC2 Stop Time

trigger repetition rate is given as 10^D microseconds, where D=0 to 7.

Delays are programmed as start times in microseconds after a trigger event. Pulse widths are determined from start time to a stop time. The stop time is also programmed in microseconds after the trigger event. The T1 and T2 start and stop times are programmed from the front panel to RAM addresses 08-11. See Table 1. The times are given as $M_2M_1M_0 \times 10^N$ microseconds, where $M_2M_1M_0$=000 to 999, and N=0 to 7. Programmed start and stop times stored in latches are compared to elapsed times in counters to generate control pulses to set and clear output latches. In addition to the gating pulses, each of the T1 and T2 circuits generates a delay pulse that is active during the delay time, a short start pulse at the beginning of the gating pulse, and a short stop pulse at the end. Typical control and output pulses are shown in Figure 1.
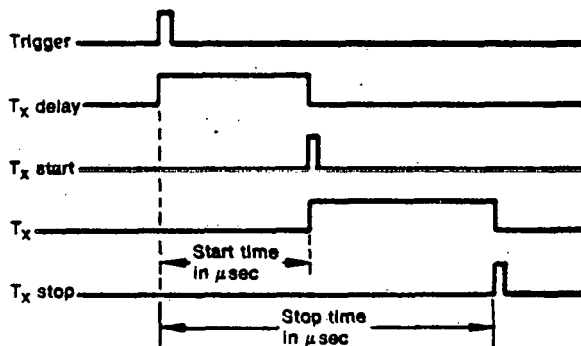

Figure 1. Typical Pulses for T1 and T2.

Time-of-day Clock Circuits. A 24-hour time-of-day (TOD) clock has been built into the PRMT. The TOD clock is shown in the simplified block diagram of Figure 4. The preset for the clock is accomplished from the front panel to RAM address 05 by selecting the appropriate function address, setting the time-of-day in hours and minutes in the data thumbwheel switches, and depressing the STORE pushbutton. The STORE loads the time to RAM and presets the clock. At preset, the seconds timer is cleared to zero. Once every minute, the time-of-day in RAM is automatically updated. The

time may be displayed by selecting the appropriate function address, and pressing the DISPLAY pushbutton. Time is displayed in HRS-MINS-SECS and is automatically updated every second.

Two sets of timing gates (RTC1 and RTC2) may be generated from the TOD clock. Start and stop times for the gates are programmed as a time-of-day in hours and minutes and loaded in the RAM. Programmed start and stop times from RAM are compared to the TOD clock once every minute. Comparator outputs are fed to latches to generate the timing gates. Delays up to three days may be programmed for both sets of timing gates. The RTC delays are programmed to the PRMT via the RAM address 07. See Table 1. The B and C digits of the input data word are the start and stop delays respectively. Delays of 0, 1, 2 and 3 days are determined by input digits 1, 2, 4 and 8. A front-panel toggle switch selects RTC1 or RTC2 for delay programming. Input delay data is loaded to latches. For each gating pulse, short start and stop pulses are generated. Typical pulses are shown in Figure 2.
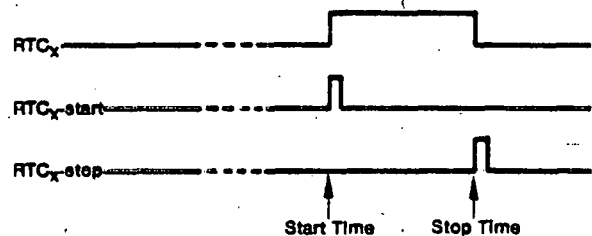

Figure 2. Typical pulses for RTC1 and RTC2.

Print Interface. The PRMT module has been designed to be connected in a standard ORTEC printing system. A simplified block diagram is shown in Figure 4. The printer used in this system is an ORTEC Model 777A Line Printer. The PRMT can be inserted at any position within the loop. The PRMT data fed to the printer is sixteen channels of four BCD digits each. The data comes from the RAM within the PRMT. The purpose of the printing capability is to obtain a hard-copy output of the PRMT operating parameters along with accumulated data from external counters, timers, et al. The 16 output channels include several channels for general information (not used internally) and may be programmed as

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the operator sees fit. Possible information may be date, run number, etc. See Table 1.

Memory Addressing. Address generation for the RAM originates from three sources. (1) In Figure 3, BCD data from the user-controlled function address switches is converted to binary and fed to a data selector in Figure 4 as a function address. (2) Once each minute, the TOD clock triggers the MEMORY CONTROL circuits in Figure 4. The MEMORY CONTROL outputs feed a binary counter in Figure 4 that automatically generates five memory addresses to update the TOD in memory, and to output data for the RTC gating pulse comparators. (3) During a PRINT cycle, the PRINT CONTROL circuits in Figure 4 generate memory addresses 0-15 to output data to the external printer. One of the address sources (1), (2), or (3) is fed to the RAM through data selectors shown in Figure 4.

Reference Frequencies. Three independently programmable periodic pulse trains are generated in the PRMT module, and are available at BNC connectors on the front panel. Two of the outputs are generated as outputs only, and are not used internally. These are the Reference Frequencies #1 and #2. The third pulse train is used primarily as an internal trigger for the Triggered Clock Circuits and is available as an incidental output. If either internal or external triggering is used for the Triggered Clock Circuits, the internal trigger may be programmed for a selected rate, and is available as an output at the "Internal Trigger" output BNC. The reference frequencies are programmed from the front panel via RAM address 06. See Table 1. Reference frequency repetition rates are given as 10^N microseconds, where $N=0$ to 7. Programming is accomplished by selecting the appropriate function address on the two-digit address thumbwheel switches, setting the required repetition rates on the data switches, and depressing the STORE pushbutton switch. The data is loaded to RAM and data latches.

Miscellaneous. The PRMT contains a data coincidence circuit that is a function of the T1 gate and data. The output of the circuit is a coincidence gate to enable a pulse height analyzer during T1 time. The circuit is designed to hold the coincidence gate off if the leading edge of the T1 gate attempts to go HI at the same time a data pulse is being input to the analyzer. The gate goes HI after the data pulse goes LO. This prevents the analyzer from trying to process distorted data pulses. A toggle switch is available to select positive or negative logic data pulses.

A TRIGGER DELAY input is available to disable the Triggered Clock Circuits without removing the applied trigger. This allows some automatic data acquisition capability.

CONCLUSION

The programmable multi-timer now in use at the Idaho National Engineering Laboratory has been developed primarily for a series of experiments concerned with TRU waste analysis. The nature of these requirements has resulted in a flexible timing module that meets all the requirements, and can also serve as a general-purpose timing unit.

The present module has been designed using low-power Schottky TTL devices. Consideration was given to a microprocessor-based unit, but the requirement for handling four or more values simultaneously at a one microsecond repetition rate precluded the use of standard microprocessors.

The input/output (I/O) interface circuits have been designed for use with an existing hard-copy device, an ORTEC Model 777A Line Printer. Future versions of the timer will have to be interfaced to computers for processing. Appropriate I/O interface circuits will be designed.
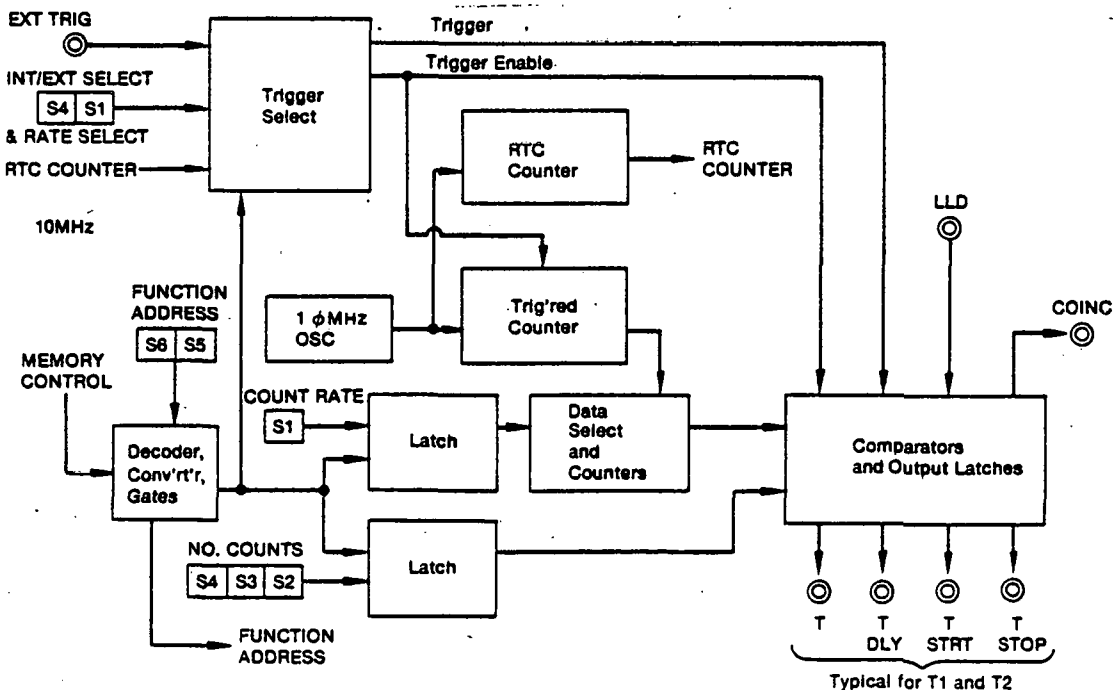

Figure 3. OSC/Counters; Trigger Select; T1/T2

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REFERENCES

1. E. B. Nieschmidt, et al, An accelerator Based Transuranic Waste Assay System, Bulletin of the American Nuclear Society, Volume 25, Number 7, September 1980.

2. R. S. Lawrence, et al, An Electronics System For Transuranic Waste Assays, IEEE Transactions on Nuclear Science, Volume NS-28, Number 1, February 1981.
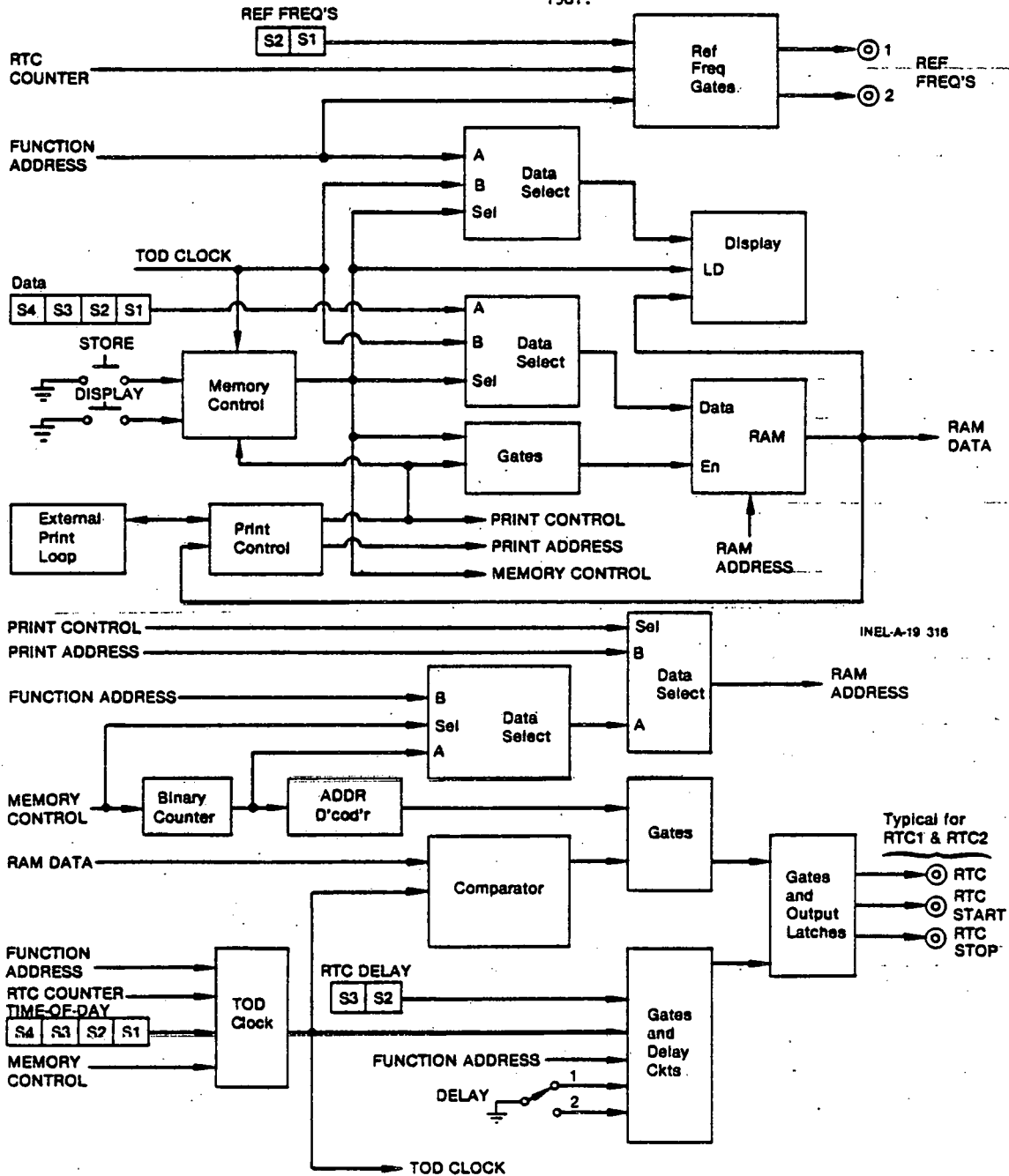
Figure 4. RAM, Print, TOD Clock, RTC1, RTC2, Display.   INEL-A-19 307

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