400
2-28-78

44.1880

COO-4081-2

MASTER

DEVELOPMENT OF PASSIVE ELECTRONIC COMPONENTS FOR INSTRUMENTATION OF IMPROVED GEOTHERMAL LOGGING TOOLS AND COMPONENTS

Annual Progress Report

By
L. S. Raymond
D. J. Hamilton
W. J. Kerwin

October 20, 1977

Work Performed Under Contract No. EY-76-S-02-4081

Solid State Engineering Laboratory
College of Engineering
University of Arizona
Tucson, Arizona

U. S. DEPARTMENT OF ENERGY
Geothermal Energy

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency Thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

NOTICE

This report was prepared as an account of work sponsored by the United States Government. Neither the United States nor the United States Department of Energy, nor any of their employees, nor any of their contractors, subcontractors, or their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness or usefulness of any information, apparatus, product or process disclosed, or represents that its use would not infringe privately owned rights.

This report has been reproduced directly from the best available copy.

Available from the National Technical Information Service, U. S. Department of Commerce, Springfield, Virginia 22161.

Price: Paper Copy \$4.50
Microfiche \$3.00

DEVELOPMENT OF PASSIVE ELECTRONIC COMPONENTS
FOR INSTRUMENTATION OF IMPROVED GEOTHERMAL
LOGGING TOOLS AND COMPONENTS

DOE Contract No. EY-76-S-02-4081

Annual Progress Report
TO

UNITED STATES DEPARTMENT OF ENERGY
Division of Geothermal Energy

20 October 1977

Report No. COO/4081-2

UA Reference No.: 76-EE-65

NOTICE
This report was prepared as an account of work sponsored by the United States Government. Neither the United States nor the United States Department of Energy, nor any of their employees, nor any of their contractors, subcontractors, or their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness or usefulness of any information, apparatus, product or process disclosed, or represents that its use would not infringe privately owned rights.

Principal Investigator: L. S. Raymond

Co-Investigators: D. J. Hamilton
W. J. Kerwin

Solid State Engineering Laboratory
Department of Electrical Engineering
College of Engineering
The University of Arizona
Tucson, Arizona 85721

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

ABSTRACT

Instrumentation of geothermal wells requires development of electronic circuits for well-logging tools; such circuits must be able to withstand environmental conditions much more severe than are encountered by conventional or military electronics. Short term objectives for well-logging instrumentation are circuits which can operate at temperatures in the range 275°C to 350°C; the medium term goal is operation up to 500°C, and the long term goal is to achieve operation at 1000°C.

It is apparent that useful electronic circuits will require the combination of both passive components and active devices. This means that the components developed in this project must be compatible with active devices both in fabrication processing and in circuit performance. Active devices under development in other projects include MOS silicon devices for short term temperatures and integrated thermionic devices for medium and long term temperatures. In order to meet the compatibility requirements, the basic technology which has been selected in this project is the chemical vapor deposition (CVD) of metal interconnections, resistor material, dielectric material and passivating material. It is to be emphasized that this is a thin-film, not thick-film, technology which is compatible with the processing methods used in fabricating either semiconductor or integrated thermionic devices, and produces components which are electrically compatible with those devices. The investigation in this project is primarily directed toward tungsten metallization, tungsten-silicon resistors, and silicon nitride dielectric and passivation.

INTRODUCTION

Instrumentation of geothermal wells requires development of electronic circuits for well-logging tools; such circuits must be able to withstand environmental conditions much more severe than are encountered by conventional or military electronics. Short term objectives for well-logging instrumentation are circuits which can operate at temperatures in the range 275°C to 350°C; the medium term goal is operation up to 500°C, and the long term goal is to achieve operation at 1000°C.

The two-year project discussed in this report is generally directed toward the development of passive components for electronic circuits for geothermal well-logging tools; specifically, this involves resistors, capacitors, metallization and passivation.

It is apparent that useful electronic circuits will require the combination of both passive components and active devices. This means that the components developed in this project must be compatible with active devices both in fabrication processing and in circuit performance. Active devices under development in other projects include MOS silicon devices for short term temperatures and integrated thermionic devices for medium and long term temperatures. In order to meet the compatibility requirements, the basic technology which has been selected in this project is the chemical vapor deposition (CVD) of metal interconnections, resistor material, dielectric material and passivating material. It is to be emphasized that this is a thin-film, not thick-film, technology which is compatible with the processing methods used in fabricating either semiconductor or integrated thermionic devices, and produces components which are electrically compatible with those

devices. The investigation in this project is primarily directed toward tungsten metallization, tungsten-silicon resistors, and silicon nitride dielectric and passivation. Figure 1 shows schematically how CVD layers of these thin-film materials can be deposited to form an integrated passive-component structure. Since CVD can be done at temperatures in the range 500°C to 1200°C, the resulting components are capable of operating at least at short and medium term temperatures, and possibly at long term temperatures.

The devices investigated in this project will be deposited on their own substrate, either sapphire or oxidized silicon. Since they are compatible with both semiconductor and integrated thermionic devices, future development (beyond the scope of this two-year project) would see them deposited on the same substrate as these devices, probably as the final steps in the fabrication process. The result would then be a monolithic integrated functional electronic block containing both active and passive components.

Project Goals

In general, the goals for the first year of this project included development of the processes required; for the second year they include optimization of the processes, integration, and life-testing of components. The last half of the second year will also include technology transfer. For the first year, the major tasks established for the project were process preparation, reactor modification, substrate evaluation, tungsten deposition, tungsten-silicon deposition, and silicon nitride deposition.

Results

Although the next section of this report deals with the technical details of the project, the important results are summarized briefly here to set the stage for the technical discussion.

Fig. 1 Cross-sectional View of a Thin Film Resistor, Capacitor, Interconnects and Passivation

Process Preparation: All the necessary reactions for CVD tungsten, tungsten-silicon, and silicon nitride were worked out. Arrangements were also made to complement some of the CVD reactions by sputtering and by thermal evaporation techniques.

Reactor Modifications: All necessary reactor modifications, including elaborate safety precautions were completed and by the end of December, 1976, the first CVD processing was under way.

Substrate Evaluation: Both sapphire and oxidized silicon wafers were used, with successful deposition in both cases.

Tungsten Deposition: Tungsten films of 1250 Angstrom thickness have been deposited by CVD; these films have a resistivity of 7.8×10^{-6} ohm-cm, about 40% higher than bulk tungsten. Temperature coefficients of resistance (TCR) as low as 1090 parts per million per degree C (ppm/°C) from 25°C to 550°C have been obtained. Interconnect patterns of the CVD tungsten have also been delineated by photolithography techniques.

Tungsten-Silicon: Tungsten-silicon resistors have been deposited by CVD and delineated by photolithography. A typical value of sheet resistance is 200 ohms per square, and a typical TCR is 50 ppm/°C, although a TCR as low as 6 ppm/°C has been obtained. The resistors perform from 25°C to 500°C with these values of TCR.

Silicon Nitride: Silicon nitride has been deposited by CVD and used as the dielectric material for capacitors. Thicknesses from 900 - 5140 Angstroms have been deposited with corresponding capacitances of 849 - 148 pF/mm².

Temperature coefficient of capacitance was -70 ppm/ $^{\circ}$ C. Leakage resistivity is a nonlinear function of both temperature and average electric field; a typical value is 10^{11} ohm-cm at 300° C and 10^6 volts/cm. Capacitor patterns have been delineated by photolithography.

TECHNICAL RESULTS

The program tasks are divided into the following major headings:

1. Process Preparation
2. Reactor Modifications
3. Material Development
4. Component Development
5. Process Optimization
6. Component Testing
7. Technology Transfer.

These tasks will be covered in detail in this section; however, Tasks #3 and #4 will be covered together since the material parameters are evaluated in terms of component characteristics and performance.

Process Preparation

The success of fabricating high temperature passive components depends on the materials used in the various components as well as the method of deposition. Both the materials and the method of deposition used for the high temperature components are significant departures from those used in commercial thin-film components.

Chemical vapor deposition (CVD) was chosen over the standard methods of sputtering or thermal evaporation for a number of reasons. Chemical vapor deposition is a high temperature process, and allows the materials to be

deposited at temperatures which exceed the component operating temperatures. Greater control over the process variables can be realized and material properties can be readily modified.

The general deposition process (CVD) is shown in Fig. 2 where the substrates are placed on a graphite susceptor. The susceptor is then loaded into a quartz reaction chamber and heated inductively by the RF coil that is placed around the outside of the quartz tube. A carrier gas such as hydrogen or helium is introduced into the reaction tube where it replaces all of the atmospheric gases. The susceptor is then heated until the correct deposition temperature is reached, typically 500°C to over 1000°C. One or more reactant gases are then added to the flow stream of the carrier gas. Upon reaching the heated substrate surface the gases react on the surface depositing the desired thin film of material and rejecting the by-products of the reaction back into the gas stream.

In general, the flowrate of the carrier gas is 100 to 10,000 times greater than the flowrates of the other gases. The carrier gas serves to provide correct gas environment for the reaction and also to keep the gas velocity at a reasonable rate through the reactor.

The materials selected for use in the components must be high temperature materials and stable in themselves in order to fabricate stable compounds. Film thicknesses range from 0.01 μm to >1.0 μm . The initial materials used in fabricating the resistors, capacitors, interconnects, and passivation are:

1. Tungsten

2. Tungsten-Silicon

3. Silicon Nitride

Fig. 2 General Deposition System for Chemical Vapor Deposition

The reactant gases, along with a carrier gas, are introduced into a quartz reaction chamber where they react on the heated substrate surfaces to form the desired materials.

These materials are formed by the following reactions:

Tungsten

Carrier Gas: H_2

Tungsten-Silicon

Carrier Gas: H_2 or H_2 and He

Silicon Nitride

Carrier Gas: H_2 or He

Reactor Modifications

The modified chemical vapor deposition reactor is shown in Fig. 3. The modifications were completed in December, 1976. Figure 4 is an identification of the various control panels and sections of the reactor.

The reactor was designed to be extremely flexible in terms of the process parameters and the materials that can be deposited.

The gas control panel has a total of ten rotometer type flowmeters for use with the carrier gases as well as the reactant gases. The controls for the tungsten hexafluoride (WF_6) and silane (SiH_4) are separated from the main controls for safety reasons. The flowrates of both WF_6 and SiH_4 are measured with electronic mass flowmeters. The flowrates are displayed on the front panel.

The main reaction tube is nominally 4" in diameter and the graphite susceptor is 2-1/2" x 6" which allows us to process two 2" diameter substrates at a time. The temperature range of the reactor is 400°C to >1200°C.

Fig. 3 Front View of the Modified Chemical Vapor Deposition Reactor

Fig. 4 Outline of the Controls on the Modified CVD Reactor

The majority of the reactor modifications in one way or another resulted from the use of WF_6 in the system. The reactions using WF_6 are carried out at pressures less than 200 torr. The reaction chamber and all associated lines must operate at pressures of 1×10^{-4} torr without leaking. Tungsten hexafluoride gas is extremely corrosive and toxic. The source and gas controls for the system are designed with a minimum of internal volume and only acceptable materials come into intimate contact with the gas for any extended period of time.

The major components of the system are shown in Fig. 5. The carrier along with the various reactant gases are injected into the main reaction chamber where they pass over the RF heated graphite susceptor. The carrier gas, unspent reactant gases, and by-product gases are pumped out of the main reaction chamber. The gas then enters a secondary reaction chamber which is designed with a large high temperature surface area to insure that all of the WF_6 has been reacted. The gas is cooled and passed through a large column of potassium hydroxide to remove hydrofluoric gas, which is a by-product of the reaction of WF_6 and H_2 . The final stage is a vacuum pump that provides system vacuum and exhausts the remaining gases out of the building.

Initial deposition runs using the modified reactor were made during the first part of January 1977. The reactor performed exceedingly well and has provided us with a very versatile system for growing the materials needed during this program.

Materials and Component Development

The fabrication of thin-film components requires the sequential deposition of several thin-film layers depending on the circuit and components to be fabricated. After the deposition of each layer, the substrate is removed

Fig. 5 Major Internal System Components in the Modified Reactor

from the reactor and a pattern is delineated into the deposited thin film by transferring a photographic image into a layer of photoresist. The film is then chemically etched.

All of the materials used in the components must be compatible with each other at elevated temperatures, 750°C to 950°C. The diffusion of one layer into another over a long period of time at high operating temperatures is also very undesirable for high stability components. The materials originally selected for this work have the required compatibilities.

The materials are typically characterized by their electrical parameters, so the following section will cover the materials and the component together.

Substrates: The substrate on which the thin films are deposited serves strictly as a mechanical support. The substrate must be inert to the deposited materials and the high temperature deposition conditions. Another important parameter is the polish of the substrate since scratches and surface deviations could lead to component instability and failure.

The two substrates used to date are oxidized silicon wafers, the same type as used in standard integrated circuits, and polished sapphire wafers. Deposition on both substrates has been successful with no apparent difference. The current component development work is carried out using oxidized silicon wafers due to the ease of handling, size and cost.

Future work will include high temperature component testing on both types of substrates as well as on polished quartz substrates.

Tungsten Metallization and Interconnects: Tungsten was developed as the metallization layer for capacitor plates and the interconnects between

components. The conductivity was measured by delineating the test pattern shown in Fig. 6 in the tungsten layers. The test configuration is shown in Fig. 7.

For convenient analysis, modeling, and understanding the properties of the deposited tungsten, the tungsten interconnect can be considered as a low value resistor. The tungsten interconnects can also be considered as a limiting case for the W-Si resistors in which the silicon concentration is reduced to zero. This is important since the characteristics of the tungsten metallization predictably follow our assumptions and theory for developing high temperature resistors using grain growth control.

The deposition parameters that provided the initial results were carried out at pressures of ~ 55 torr with a tungsten hexafluoride, WF_6 , flowrate of 2.5 cc/min in a carrier gas of hydrogen.

The films were uniform and specular after a minimum of parameter adjustment. The deposition temperature was 750°C . The initial conductivity measured was 7.76×10^{-6} ohm-cm on a sample 1250A thick. The bulk value given for tungsten is 5.5×10^{-6} ohm-cm. The measured value is about 40% higher than the bulk value; however, for a film thickness of only $0.1250 \mu\text{m}$, this is a very reasonable value.

Additional tungsten depositions were made in order to verify the repeatability of the tungsten and to determine the temperature coefficient of resistance of tungsten. The first series of depositions were made using tungsten hexafluoride in a carrier gas of hydrogen along with a secondary carrier gas of helium to improve the uniformity of the deposition. The helium was added strictly as an inert carrier gas; however, it produced a significant increase in the resistivity of the tungsten. The temperature

Fig. 6 Resistivity Test Pattern Used to Determine the Resistivity of CVD Deposited Tungsten

Fig. 7 Test Arrangement for Measuring the Resistivity of Tungsten

coefficient of the material was also modified by the utilization of helium. The second series of depositions were run with hydrogen as the only carrier gas. The total flowrate and reactor pressure were held constant for both groups.

The resistivity of the samples grown in the presence of helium ranged from 9.9×10^{-6} to 42×10^{-6} Ω -cm with the majority of the samples having a resistivity 3 to 8 times the bulk resistivity of tungsten. The temperature coefficients of resistance of bulk tungsten is ~ 4700 ppm/ $^{\circ}\text{C}$. The TCR of the samples grown in the presence of helium ranged from 1,090 to 2977 ppm/ $^{\circ}\text{C}$ and the samples grown in hydrogen only ranged from 2320 to 2781 ppm/ $^{\circ}\text{C}$. It was also noted that the sample with a resistivity of 42×10^{-6} Ω -cm also had the lowest temperature coefficient of 1090 ppm/ $^{\circ}\text{C}$.

The lower temperature coefficients can be attributed to the grain size. The bulk resistivity of tungsten would be measured on a high purity tungsten sample with a relatively large grain size. The grain size of the films is severely limited by the thickness of the film which accounts for the higher resistivities. The grain size is also varied by the deposition parameters. The utilization of helium reduces the grain size; however, this has not been analytically verified. This same phenomenon has been observed with the growth of silicon in helium in one of our previous programs. The temperature of the deposition also affects the grain size; the higher the deposition temperature, the larger the grain size will tend to be. This is demonstrated by the fact that the lowest resistivity measured, 6.47×10^{-6} , was grown in hydrogen at a temperature of 880°C . Figure 8 shows several Resistance versus Temperature plots for tungsten grown under different conditions.

Fig. 8 Resistivity of Tungsten as a Function of the Deposition Carrier Gas

Tungsten will be utilized in the high temperature passive circuits as capacitor plates and to interconnect the various components. A very simple model of the interconnect along with a W-Si resistor is shown in Fig. 9. In this model we can consider the interconnect as a second resistor in series with the tungsten-silicon resistor. The temperature dependence of the interconnect resistance must be taken into account when designing precision network functions in which the temperature dependence on the desired resistor is critical. The interconnect can be so designed so that it has minimal affect on the total circuit operation.

Tungsten-Silicon Resistors: The basic material is grown from two gases, tungsten hexafluoride and silane. The basic reaction is

The W-Si material should be considered as a family of materials as opposed to a single compound. This is the reason for writing it as W-Si (tungsten-silicon) and not as a standard compound. The composition is variable over the complete range from 0 - 100% of either tungsten or silicon. As noted in the previous section, a resistor composed completely of tungsten (the interconnects) represents a limiting case in the W-Si family of materials.

The very large range of material composition along with being able to control the deposition parameters somewhat independently is what gives the tremendous advantage in using CVD to produce the high temperature materials. The processing variables are much more readily available to the designer than with either sputtering or thermal evaporation. However, with a large range of controllable variables we have an equally large task of

$$R_{Total} = R_I + R_{W-Si}$$

Fig. 9 Equivalent Circuit for a Resistor and Its Interconnects

The equivalent TCR would be calculated using the total resistance change of the interconnect and the W-Si resistor.

Fig. 10 Resistor Test Pattern Used to Delineate Test Resistors in Tungsten Silicon Thin Films

sorting out their interdependence and how they affect the device parameters.

Not all of the materials developed in the material studies will be used, but these studies are necessary in order to complete our understanding of the materials, and to provide direction in developing materials that will eventually be used in various ways in the design of geothermal instrumentation.

A matrix approach is used in mapping out the deposition parameters and the material characteristics of the tungsten-silicon family of materials.

The initial deposition conditions were as follows:

Deposition Temperature: 750°C to 780°C;

Pressure: 5.5 torr;

Approximately a one-to-one gas concentration ratio
of WF_6 to SiH_4 .

The tungsten-silicon film was delineated with the resistor test pattern shown in Fig. 10. The temperature coefficient of resistance, TCR, was less than 100 ppm for all of the films grown under these conditions. The Resistance versus Temperature curves for three resistors are shown in Fig. 11.

The best temperature coefficient was +6.1 ppm/°C. Both positive and negative TCR's were produced along with near zero TCR's.

We expanded the matrix of deposition parameters to the following set:

Pressure: 5.2 torr

Deposition Time: 6.0 min

WF_6 : 3 cc/min

SiH_4 : 3 cc/min

Carrier Gas: H_2 and He

Temperature: 700, 750, 800, 850, 900°C

Fig. 11 Resistance versus Temperature for Three Tungsten-Silicon Resistors. Temperature Range of Measurement: 25 to 550°C.

The deposition rate of the material varied slightly, but was in the 1,000 to 1,100 Å/min range. Wafers were run in the reactor two at a time. Following the deposition of the resistive material, they were measured with a four-point probe and then processed into resistors.

The reactant gases, WF_6 and SiH_4 , were injected into the carrier gas stream at a ratio of 1:1; however, we know that this is no guarantee that the ratio in the deposited material will be in a ratio of 1:1. From our data it was evident that there was a concentration gradient across the two wafers; the rear wafer has a higher concentration of silicon than the front one.

From a physical point of view the silane molecule has a mass of approximately 1/10 that of the tungsten hexafluoride and as a result was more mobile in the gas stream. As the gas flows across the wafers, the gas stream becomes slightly depleted of the reactant gases; since the silane was more mobile in the gas stream, it was replaced at a faster rate. The resistivities of the material on the rear wafers were higher and the TCR's lower than the front wafers.

The TCR's for this series of runs varied from +268 ppm/°C to +72 ppm/°C, except for the wafers run at 900°C. It should also be noted that the Resistance versus Temperature curves for all of the resistors were straight lines and have constant TCR's over the entire measurement range of 25°C to 550°C. The material had a very high silicon concentration, and the resulting Resistance versus Temperature curve was logarithmic. The sheet resistance at room temperature was on the order of $10^8 \Omega/\square$. A resistor in which the silicon concentration approaches 100% represents the other limiting case.

The resistivity of the material to date is in the 1000 to 2300×10^{-6} ohm-cm range. Future work will be directed toward expanding the W-Si materials in the direction of higher resistivity with controllable low TCR's.

Silicon Nitride Capacitors: High temperature capacitors were formed using CVD deposited tungsten as the plate material and CVD deposited silicon nitride as the dielectric. The capacitance, C , of a capacitor is given by

$$C = \epsilon_r \epsilon_o \frac{A}{d}$$

where ϵ_r is the relative dielectric constant, $\epsilon_o = 8.85 \times 10^{-12}$ F/m, A is the plate area, and d is the dielectric thickness.

The relative dielectric constant, ϵ_r , is a parameter of the dielectric material and is also dependent on the method of deposition. The measured relative dielectric constant is 8.6 for silicon nitride grown in a carrier gas of helium at 750°C . Figure 12 shows the capacitance as a function of temperature for three separate thicknesses. The temperature coefficient of capacitance is in a small range around -70 ppm/ $^\circ\text{C}$. The test area of the capacitors is 1.0 mm^2 . There was no problem with pin holes or defects in the dielectric material. The capacitors were not cycled above 350°C due to the rapid oxidation of unpassivated tungsten above 400°C .

A series of capacitors was run using hydrogen as the carrier gas; the results were extremely poor. The capacitors were very leaky, and there was a significant amount of mobile charge in the dielectric. All work on silicon nitride using hydrogen as the gas stream has been discontinued.

Two major areas of concern in the design and use of high temperature capacitors are the leakage current and the dielectric breakdown voltage.

Fig. 12 Capacitance versus Temperature Curves for Three High Temperature Capacitors.

It is possible to have leakage currents through the capacitors of the same order of magnitude as the signal or larger. The leakage could affect the biasing of active devices or degrade the circuit function of a passive network.

We can model the capacitor by the following circuit:

where C is an ideal capacitor and R is the resistance through the dielectric between the two plates. A typical plot of the leakage current density and the applied voltage at constant temperatures is shown in Fig. 13. The conductivity of the silicon nitride is dependent on the temperature, the applied field, and the dielectric thickness. Figure 14 illustrates the affect of these parameters on the conductivity of Si_3N_4 .

The analytical expression for the current density is

$$j = j_0(d,T) [\exp(8V)-1] .$$

The β term is independent of temperature, but it is dependent on the dielectric thickness and processing. For comparison we also show in Fig. 14 a curve representing the values of σ as a function of temperature taken from Introduction to Ceramics by W. D. Kingery. Kingery did not provide further information on the dielectric thickness, applied field, or on the method of material preparation. It should be noted that our data does follow the general shape of the Kingery curve. The dependents of σ on the applied field is also illustrated by the shift in the curve for low field and high field

Fig. 13 Capacitor Leakage Current as a Function of Applied Voltage and Temperature

Dielectric: Si_3N_4

Thickness: 5140A

WDW - 52A

Fig. 14 Conductivity versus Inverse Temperature of the Silicon Nitride Dielectric Layer

conditions. For low field conditions and a relatively thick dielectric layer, the conductivity of the dielectric is less than the values given by Kingery.

In Fig. 15 we have plotted the $j_o(d,T)$ for the very low field case where V approaches zero volts. At higher temperature, $T > 500^\circ\text{K}$, the curve appears to match the equation

$$j_o = A \exp(-E/KT)$$

where E is calculated from the slope of the high temperature region of the conductivity curve, and

$$E = 1.14 \text{ eV.}$$

Then for high temperatures our current density equation has the form

$$j = g(d) \exp(-1.14/KT) [\exp(\beta V) - 1]$$

where $g(d)$ and β are dependent only on the dielectric thickness and processing conditions. For the low temperature region, $T < 500^\circ\text{K}$, it appears that the temperature dependence of the equation could be approximated by a factor of $\exp(\alpha T)$ instead of $\exp[-E/KT]$.

We do not fully understand the field dependence of the conductivity; however, it should be noted that our capacitors must be capable of operating with several hundred volts applied which means that they are operating at extremely high field conditions, typically 1×10^6 to 1×10^7 volts/cm.

The equation for the resistance, R , of a capacitor is

$$R = \frac{d}{A\sigma}$$

Fig. 15 Current Density, j , as a Function of Inverse Temperature as the Applied Field Approaches Zero

Passivation: The passivation layer is the final layer of material over the passive components which protects the devices from oxidation at high temperature in an oxidizing environment. Sputtered silicon dioxide is presently being used with good results. It is compatible with the materials used in the devices and has successfully worked as a passivation layer.

Future efforts will be directed at using CVD silicon dioxide and CVD silicon nitride as passivation layers.

Alternate Dielectrics: Any dielectric chosen for high temperature capacitors must be viewed in the following terms:

1. relative dielectric constant,
2. high temperature conductivity,
3. breakdown voltage, and
4. compatibility with the rest of the components and processing.

There are a number of dielectrics that have conductivities lower than that of silicon nitride at high temperature; however, the relative dielectric constants are typically lower than the value for silicon nitride.

Boron nitride has a relative dielectric constant of ~5 which is less than the 8.6 for silicon nitride. The conductivity, however, is approximately five orders of magnitude lower than that of silicon nitride at 500°C. The high temperature data for boron nitride are limited and are probably dependent on the means of deposition. Boron nitride at this point appears to be the best alternate dielectric.

Boron nitride can be deposited by CVD using diborane and ammonia.

The material will be tested in much the same manner at the Si_3N_4 . The reactor is currently ready for the experimental work with boron nitride.

Bonding: A major area of concern in using the high temperature passive components is in connecting the devices to external circuits such as amplifiers, oscillators, transducers, or additional passive components. The bonding techniques must be compatible with the current passive components as well as with the proposed active devices.

The bonding pads and wire will be platinum. A platinum sputtering target has been purchased and received. It will be used to deposit the platinum bonding pads to the components and lead package. The platinum will adhere to the metallization through contact windows etched in the passivation layer. The platinum will not be affected by high temperature operation in an oxidizing atmosphere.

Wire bonding will be accomplished by using an ultrasonic wire bonder to bond 25 μm (0.001 in.) platinum wire. A parallel gap bonder and two hand-held spot welders have also been purchased in order to bond heavier gauge wire and leads.

The bonding equipment is shown in Fig. 16.

Process Optimization, Component Testing, and Technology Transfer: Tasks #5, #6, and #7 will be accomplished in the second year's work and have not received any significant amount of attention during the first year of research.

GENERAL SUMMARY

In the first year of research on high temperature passive components it has been established that the use of chemical vapor deposition and the selected materials together form a viable approach to the design and

Fig. 16 Ultrasonic Wire Bonder and Parallel Gap Bonder

fabrication of high temperature passive components. More work is yet required in expanding and optimizing the processes, but basic ground work is now firmly set.

Table I summarizes the current passive component parameters. The values in Table I are not meant to indicate limiting boundaries on the process but instead indicate the limits of the current processes as they now exist.

In the second year of research, the majority of the current areas will be expanded and optimized. Attention will be directed toward the total integration of the passive components into a functioning network which will demonstrate the capability of the total processing sequence and will include bonding development.

Process monitoring and materials analysis will be used to optimize components and processes; this should lead to a systematic fabrication routine for the passive components.

A new data acquisition system has been ordered and will be used extensively in component testing. The system will be capable of handling a large number of measurements and the data reduction needed to determine the long term characteristics of the components; it also has the required accuracy to measure long term component drift and the tracking of temperature coefficients.

Technology transfer workshops will be held during the year in order to transfer information about the high temperature components to prospective end users and to possible manufacturing concerns. Through these workshops we also hope to gain additional insight into the current instrumentation problems and component requirements.

Table I Summary of Current Passive Component Parameters

Component	Material	Resistivity ρ (Ω -cm)	Relative Dielectric Constant	Sheet Resistance $\Omega/\square$	Temperature Coefficient ppm/ $^{\circ}$ C
Resistors	Tungsten-Silicon [W-Si]	1000 to 2300 $\times 10^{-6}$	--	50 - 500	$< \pm 100$
Capacitors	Silicon Nitride [Si ₃ N ₄]	See Fig. 14	8.6	--	~ -70
Interconnects	Tungsten [W]	7×10^{-6}	--	0.1 - 2.0	2900 (Lower TCR with high ρ .)
Passivation	Silicon Dioxide sputtered [SiO ₂]	$\sim 10^8$ at 500 $^{\circ}$ C (Worst case)	3.9	--	--

PROGRAM MODIFICATIONS

Table II is an updated Program Development and Milestone chart reflecting minor program changes and new milestone dates for a number of areas.

A brief description of the milestones for the second year follows.

Tungsten-Silicon: (1 February 1978) Develop increased material resistivity with low temperature coefficient of resistance.

Dielectric, Si₃N₄: (1 January 1978) Analysis and characterization of silicon nitride as a dielectric.

Alternate Dielectric: (1 April 1978) Analysis and characterization of boron nitride as a dielectric.

Substrates: (1 February 1978) Determine characteristics of oxidized silicon wafers, sapphire, and quartz as substrates for passive components.

Resistors: (1 February 1978) Evaluations of the initial phase of resistor development and characteristics.

Capacitors: (1 January 1978) Evaluate capacitors using silicon nitride as the dielectric.

(1 April 1978) Evaluate capacitors using boron nitride as the dielectric.

Passivation: (1 July 1978) Develop CVD deposited SiO₂ and Si₃N₄ as passivation layers.

Table II

PROGRAM DEVELOPMENT AND MILESTONES

Integration: (1 August 1978) Demonstration of Networks composed of multiple passive components.

Bonding: (1 February 1978) Develop bonding techniques for high temperature circuits using platinum.

Process Monitoring: (1 July 1978) Develop in-process optical monitoring for resistor and capacitor fabrication.

Process Analysis: (1 July 1978) Analysis of CVD deposited materials.

Optimization: (1 September 1978) Optimize deposition processes for the fabrication of integrated passive networks.

Fabrication Technology: (1 September 1978) Summarize the fabrication techniques developed under this program.

Life/Temperature Testing: (1 April 1978) Initial results from long term high temperature testing of components. This work will continue throughout the rest of the program.

Temperature Limitation: (1 May 1978) Determine the upper temperature limitations of the current materials.

Temperature/Power: (1 May 1978) Determine power limitations of resistors at high temperatures.

Cycling: (1 January 1978) Evaluate effects of temperature cycling of component stability.

Data Acquisition System: (1 December 1978) Install and program for component testing and evaluation.

Technology Transfer: (April 1978) Hold a short workshop on high temperature passive components to exchange information concerning the current status of the technology and to acquire fresh input to the needs of the industry.

(August 1978) Hold one or more additional workshops.