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Solutions to Heavy Ion Induced Avalanche Burnout in Power Devices*

Solutions au claquage par avalanche causé par des ions lourds dans les composants de puissance

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Abstract--**Reviews of normal breakdown and current induced avalanche breakdown mechanisms in silicon power transistors are presented. We show the applicability of the current induced avalanche model to heavy ion induced burnouts and present solutions to current induced avalanche in silicon power semiconductors.**

Resume: **L'article présente un examen des mécanismes de défaillance normale et de claquage par avalanche causé par une surintensité dans les transistors de puissance au silicium. Démonstration de l'applicabilité du modèle de chaquage par avalanche causé par une surintensité aux claquages causés par des ions lourds, et proposition de solutions au problème du claquage par avalanche causé par une surintensité dans les semi-conducteurs de puissance au silicium.**

INTRODUCTION

Silicon power devices fall into two broad categories, bipolar and field effect. Transistors using both of these technologies are often used in satellite applications for power conversion. The present trend is toward integrating power transistors and control electronics on the same chip. In this case, it is the power portion of the chip that is most susceptible to burnout failures, because of it's high voltage operation. Hence, it is important to understand the operational limitations of power transistors when exposed to intense heavy ion and/or dose-rate environments.

We first review normal avalanche breakdown modes in bipolar structures and show how these mechanisms apply to power metal-oxide-semiconductor field-effect-transistors (MOSFETs). We next review the high current induced avalanche mechanism stimulated by a high dose-rate irradiation and then discuss how this mechanism applies to heavy ion induced burnout in silicon power devices. Finally, we propose solutions for current induced avalanche burnout, concentrating on techniques that reduce current injection for high emitter doping concentrations.

NORMAL BREAKDOWN MODES IN BIPOLAR SEMICONDUCTOR JUNCTIONS

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Collector to base, open emitter breakdown voltage (BV_{CBO}). As the electric field in the collector base depletion region of a bipolar transistor is increased, a point is reached where the velocity of electrons in the conduction band exceeds their thermal velocity and they become "hot" carriers [1]. When hot electrons collide with atoms in the silicon lattice, they can transfer enough energy to valence band electrons to promote them to the conduction band, thus creating electron/hole pairs. Although many of the generated electrons and holes recombine, some of these charge carriers drift across the depletion region. For an npn transistor, holes are injected into the base and electrons into the collector. Because electrons are injected into n-type material and holes into p-type, this is an injection of majority carriers.

As the intensity of the electric field increases, impact generated carriers multiply and the overall avalanche multiplication factor (M) approaches infinity.

When this happens, the junction is in avalanche breakdown. BV_{CBO} must not be exceeded in normal operation.

Collector to emitter, open base breakdown voltage (BV_{CEO}). Avalanche multiplication in the collector base junction produces majority carrier injection into the transistor base region. This occurs at electric field levels less than where M becomes infinite. If the base region of the transistor is open (or at least connected to the emitter via a high impedance), the majority carrier injection can forward bias the emitter base junction and produce minority carrier injection from the emitter. When the injected minority charge carriers reach the depletion region, they produce additional carriers via impact ionization and more majority carrier injection which again increases the forward bias on the emitter base junction. This regenerative feedback mechanism can produce a breakdown mode at electric field levels well below those required for BV_{CBO}.

Reducing the value of resistance (R) between the base and emitter leads requires higher currents to maintain a given b-e junction bias and hence the minority carrier injection level. When R is reduced to 0, the b-e junction can not turn on (ignoring base spreading resistance) and the transistor can only break down at the higher BV_{CBO}. Therefore, BV_{CER} (collector to emitter breakdown voltage with the base connected to the emitter with resistance R) avalanche is depend-

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ent on R and varies from BV_{CEO} (high R or open) to $\approx BV_{CBO}$ (R=0).

Thermal second breakdown. Once a junction enters breakdown from whatever mechanism, filamentary current conduction occurs. The filaments are often referred to as microplasmas and are very stable. An increase in avalanche current increases the filament diameter thus maintaining an almost constant current density. This condition is stable as long as the local temperature, in the vicinity of the filament, does not increase. If the local temperature increases, thermally generated carriers increase the current density and the temperature rises further. This is a regenerative process and the junction will eventually fail because the silicon temperature is raised above the eutectic point of silicon/aluminum or the melting point of silicon (1412 °C). This mechanism, referred to as second breakdown, is destructive [2].

Applicability of bipolar breakdown mechanisms to power MOSFETs. At first, one might question the relationship of the foregoing bipolar phenomena with power MOSFETs. However, inspection of the structure of a power MOSFET demonstrates the existence of a parallel parasitic bipolar transistor. Fig. 1a shows a schematic cross section of a n-channel double diffused power MOSFET (DMOS), the most popular type. Following the vertical line shown in this figure, a n^+,p,n,n^+ structure exists with the diffusion profile similar to a power bipolar transistor (emitter on top). An approximate equivalent circuit is shown in Fig. 1b. Although the base and emitter are connected at the surface of the device, some resistance (R_{SHUNT}) exists from the source contact to the region of the base under the source diffusion.

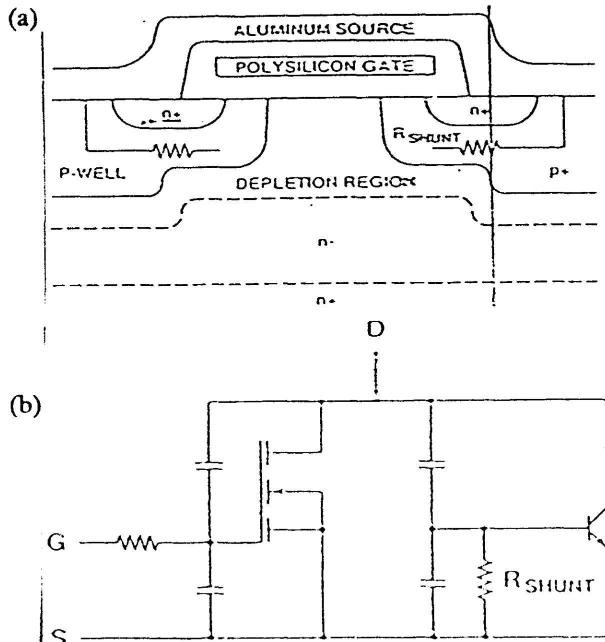


Fig. 1. (a) Schematic diagram of a power MOSFET transistor, and (b) the approximate equivalent circuit.

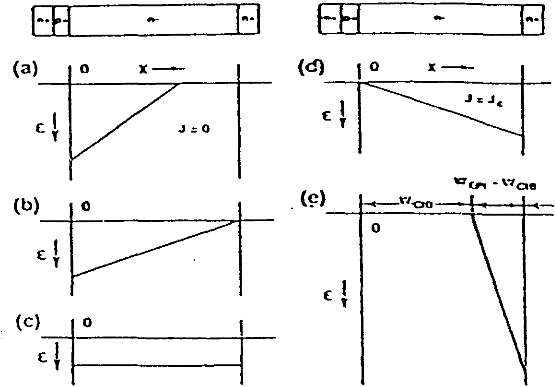


Fig. 2. Epitaxial layer electric field profiles at increasing areal current densities, (a) through (e).

It is this resistance that accounts for the lower voltage BV_{CER} breakdown mode.

CURRENT INDUCED AVALANCHE (CIA)

The model for current induced avalanche [3] is an extension of the base pushout model in epitaxial structures. Fig. 2a through 2e shows the electric field profiles in a one-sided abrupt junction for increasing areal current density, J. As J increases from 0 (Fig. 2a) to J_c(fig. 2e), the depletion layer first expands to the n-n+ boundary, then becomes uniform across the epitaxial layer (Fig. 2c), and finally inverts (Fig. 2d). (J_c is the current density where the peak electric field shifts from the p-n boundary to the n-n+ boundary.) It should be remembered that the applied voltage is the integral of the electric field and hence is a constant. J_c is given by [4],

$$J_c = q\, v_s\, [\, N_n + (2\epsilon V_{CB})/(qW_n^2)], \qquad (1)$$

where q = 1.6 x 10^{-19} C, v_s is the saturated limited velocity $\approx 10^7$ cm/s for electrons, N_n is the ionized carrier concentration in the epitaxial layer, ϵ is the product of the relative dielectric constant in silicon (11.9) and vacuum permittivity (8.85 x 10^{-14} F/cm), V_{CB} is the applied junction voltage, and W_n is the epitaxial layer thickness. As the current density increases above J_c, the base region expands into the epitaxial layer. The expanded base is referred to a current induced base (W_{CIB}) and is given by,

$$W_{CIB} = W_n[\, 1 - (\{J_c - qv_sN_n\}/\{J_h - qv_sN_n\})^{\frac{1}{2}}], \qquad (2)$$

where J_h is the high current density and is greater than J_c.

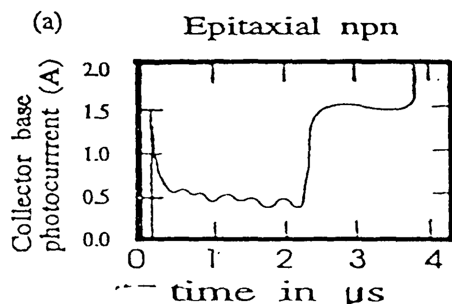
As W_{CIB} expands into W_n, the electric field must become larger. This is shown in Fig. 2(e). Eventually, the peak electric field can reach an intensity that sustains avalanche multiplication and results in majority carrier injection into

the base region. Once the injection occurs, the emitter base junction becomes forward biased, minority carriers are injected and diffuse to the shifted depletion region undergoing additional avalanche multiplication and more injection. Once this regenerative mechanism is initiated, there is no way to shut it off and the device eventually enters second breakdown and fails.

The initiating mechanism is the high current density, either locally produced by a heavy ion or caused by a more uniform ionizing irradiation at high dose rates. The high current density shifts the depletion region from the p,n junction to the n,n^+ junction and the effective base pushes into the epitaxial layer. The depletion region cannot expand into the n+ region because it is highly doped. (This is why current induced avalanche occurs only in epitaxial structures.) The depletion region narrows, the peak electric field increases, and avalanche occurs. When the avalanche current turns on the emitter base junction, a regenerative feedback condition is established and the device burns out.

Current induced avalanche can occur in both bipolar transistors and power DMOS devices and has the following features:

1. it occurs in devices built on epitaxial substrates (therefore it includes most,if not all power devices);



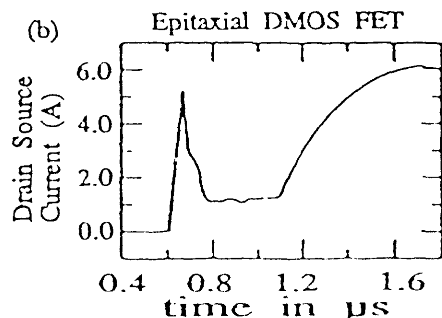


Fig. 3. CIA Responses for bipolar (a) and power MOSFET (b) devices.

2. it occurs at high areal current densities (note, it is the areal current density and not the total current that is important);

3. it can occur at bias levels <u>well below</u> BV_{CEO} and BV_{CBO}; and

4. it usually does not occur in p-channel or pnp transistors because of the lower hole ionization coefficient.

Fig. 3 shows CIA burnout responses measured for both bipolar and DMOS transistors [3] and lists the applied bias (V_{CB}) and the measured breakdown voltages. As can be seen from this figure, the burnout responses of the two devices are almost identical indicating that the same burnout mechanism is responsible. For the bipolar case, burnout occurred with a collector base bias of BV_{CIA} = 32 V while the measured BV_{CEO} = 53 V and BV_{CBO} = 77 V. For the power DMOS burnout occurred at a drain source voltage of BV_{CIA} = 40 V while BV_{DS} = 220 V. (It is not possible to measure BV_{CEO} for power DMOS.) Additional power DMOS burnout data have demonstrated the following:

1. BV_{CIA} can range from 1/2 to 1/15 of BV_{DS},

2. BV_{CIA} will not occur below a minimum dose-rate exposure level regardless of how high V_{DS} is (up to a maximum of BV_{DS}, and

3. BV_{CIA} is not reduced at dose-rate exposure levels greater than the minimum threshold.

Once a threshold dose rate and voltage are reached, the device will burn out. It is the dose-rate exposure level that establishes the areal current density of the device and that is why the dose-rate thresholds were about the same for different devices.

Single event stimulated current induced avalanche. Current induced avalanche can be stimulated by the intense charge deposition of a heavy ion traversing an epitaxial device [5]. In the case of heavy ion current induced avalanche, it is not the average areal current density but a localized areal current density that triggers the failure. A minimum ion linear-energy transfer (LET) is required to trigger burnout rather than a minimum dose rate. Unfortunately, the current signature for ion induced burnouts cannot be compared directly with dose rate burnout signatures because they look quite different [6].

The main difference between a heavy ion and dose-rate induced failure is the volume of semiconductor material affected. Ion induced burnouts show localized burn spots

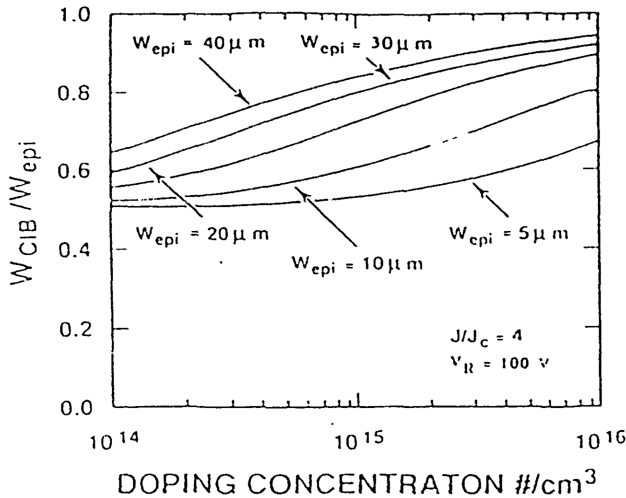


Fig. 4. Plot of W_{CIB}/W_{EPI} versus epilayer doping concentration and thicknesses between 5 $\mu$and 40 μm.

while dose-rate induced burnouts tend to destroy the entire chip. Both are triggered by high current densities (one localized and the other uniform) and both can occur at V_{DS} bias much less than BV_{CEO}. Other investigators have stated that heavy ion induced failures can occur only with bias levels in excess of the BV_{CEO} of the parasitic bipolar [5]. However, we disagree with this limitation. First, experimental bipolar dose-rate data shows CIA burnout at bias levels below BV_{CEO} (see Fig. 3), and second, recent bipolar heavy ion induced burnout data shows CIA occurring at bias levels below BV_{CEO} [7].

SOLUTIONS

In an attempt to mitigate the CIA problem and achieve some degree of operational margin, one may be tempted to use devices with higher voltage breakdown ratings. However, experimental data [3] show that higher voltage devices do not increase margin and typically exhibit CIA breakdown at smaller fractions of their rated breakdown, e.g., 500 V devices burn out at 0.2 BV and 100 V devices burn out at 0.75 BV. To understand this behavior, we can substitute (1) into (2) and solve for the background doping concentration. Fig. 4 is a plot of this function for a ratio of J_h/J_c = 4 and V_R = 100 V. The 5 curves are for increasing epitaxial layer thicknesses ranging from 5 μm to 40 μm. If the 10^{15}/cm^3 doping level is examined, it can be seen that the current induced decrease in depletion layer thickness is $\approx$50% for a 5 μm layer and $\approx$88% for a 40 μm layer.

Therefore, thicker epitaxial layers have larger fractional current induced reductions in epitaxial layer thickness and a larger fractional decrease in CIA threshold voltage.

To eliminate CIA burnout in power devices, it is necessary to eliminate the coupling between CIA and current injection in the transistor by either reducing CIA or reducing transistor current injection.

Eliminating CIA. CIA can be reduced or eliminated in several ways:

1. Eliminate the epitaxial layer (the n^- layer on top of the n^+ shown in Fig.1 thereby eliminating the quasi junction where the electrical field peaks. This has the disadvantage of increasing on resistance (R_{DS}(on)) in DMOS or the bipolar saturation voltage (V_{CE}(sat)), especially for high voltage devices.

2. Because holes have a lower ionization coefficient than electrons [1], CIA is virtually eliminated in p-channel and pnp transistors. The disadvantage of these devices is increased R_{DS}(on) or V_{CE}(sat) because of the lower hole mobility.

3. A graded transition in doping level between the epitaxial and substrate layers increases the length of silicon over which the voltage is dropped--reducing the electric field. The disadvantages of this technique are that it increases processing complexity and is not very effective since the peak electric field can be reduced no more than a factor of 2.

4. Use current limiting (inductance, resistance, or both) to prevent a simultaneous high current, high-voltage condition. This limits the device to the normal safe operating area. The main disadvantage of this technique is that is not very effective for heavy ion induced CIA burnout because the high current density is localized and involves a small portion of the entire chip. Therefore, a very high impedance is required and can interfere with normal circuit operation.

Minimizing current injection. Current injection from the emitter into the base can be minimized in two ways. First, by reducing the parasitic base to emitter resistance, larger collector base junction avalanche currents are required to forward bias the emitter base junction. Second, minimizing the emitter injection efficiency reduces the charge transport for a given emitter base bias level. Fortunately, these effects are somewhat coupled so that reducing the resistance also can reduce the injection efficiency.

It can be shown that the gain of a bipolar transistor (when the gain is dominated by the emitter injection efficiency) is given by

$$\beta = D_n Q_E / D_p Q_B \qquad (3)$$

where D_n and D_p are the average diffusion coefficients for electrons and holes, and Q_E and Q_B are the total ionized doping impurities in the emitter and base regions [8]. In addition, at high doping levels ($N_D > \approx 2 \times 10^{19}$) the effective ionized impurity concentration is reduced [9]. A plot of the effective impurity concentration for various emitter depths is shown in Fig. 5. As can be seen from this figure, the effective Q_E (the area under the curve) is reduced because of the high doping concentration near the surface. From (3) it is clear that this reduces the gain and hence emitter injection. Additional gain reduction is achieved by using a very shallow diffusion.

Eliminating current injection. To prevent parasitic transistor turnon, the base-emitter junction bias must be kept low as current flow into the base increases. It can be shown [2] that the effective parasitic bipolar current gain, with a resistive base shunt (R_S) is given by

$$\alpha_s = \alpha/(1 + I_s/I_b) \tag{4}$$

where I_s is the current through the shunt resistance (see Fig. 1), I_E is the current through the emitter junction, α is the common base current gain of the transistor(which is dominated by the emitter injection efficiency [2]) and α_s is the effective current gain of the transistor. As can be seen from this equation, the more current shunted by the resistor and/or the smaller α, the lower the effective current gain of the device, and hence, the injection. The key to eliminating current injection is to maximize the ratio of I_R/I_E and/or

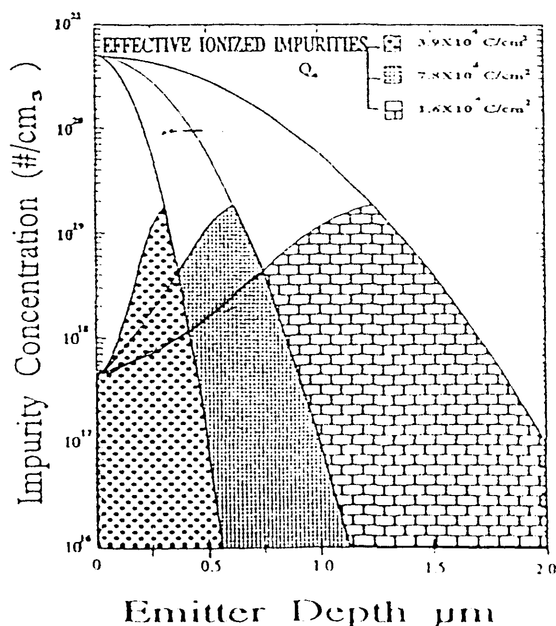


Fig. 5. Plot of a Gaussian emitter profile with emitter depths of 0.5 μm, 1.0 μm, and 1.5 μm, and (2) and the effective profile (shaded areas).

minimize α (and therefore β). All the solutions reducing current injection also minimize the value of the shunt resistance either directly or indirectly.

CONCLUSIONS

Solving the problem of CIA burnout in npn bipolar and n-channel DMOS devices is at best, difficult. We have discussed several techniques to harden these devices to the effects of heavy ion and dose-rate induced failure. The most effective techniques are those that minimize the emitter current injection by reducing the emitter injection efficiency or making the parasitic bipolar more difficult to turn on. However, we believe the simplest solution to the problem is to use pnp bipolar and p-channel DMOS devices. Speed and on-resistance penalties are less than a factor of three and one can use off-the-shelf components to solve the problem.

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