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CONTRACT REPORT

DEVELOPMENT OF FLIP CHIP TECHNIQUES
FOR CONSTRUCTING MONOLITHIC
MULTI-CHIP ARRAYS

Prepared by
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SANDIA LABORATORIES

OPERATED FOR THE U. S. ATOMIC ENERGY COMMISSION BY SANDIA CORPORATION

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DEVELOPMENT OF FLIP CHIP TECHNIQUES FOR
CONSTRUCTING MONOLITHIC MULTI-CHIP ARRAYS

Final Report

November 1967

Prepared by

F. W. Stork
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for

Sandia Corporation

under

Contract No. 57-1766

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A B S T R A C T

A five-bit binary counter module was developed utilizing standard purchased monolithic circuit chips mounted to a bumped substrate using flip-chip techniques.

Two-level metallization process was developed for both the monolithic circuits and the thin film substrate. RF-sputtered glass is used as the dielectric insulator.

The integrated circuit chips are ultrasonically bonded to the raised contact bumps on the alumina substrate and then reflow soldered for optimum bonding strength. A specially designed lead frame is also reflowed to the substrate to form external lead connection and package seal simultaneously, resulting in a completely "wireless" fabrication concept.

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DEVELOPMENT OF FLIP CHIP TECHNIQUES FOR CONSTRUCTING MONOLITHIC MULTI-CHIP ARRAYS

I. INTRODUCTION

The objective of this program was to develop flip chip techniques for fabricating arrays of monolithic circuit chips. Since monolithic circuits in flip chip format were not available in the industry, the key to this approach was the capability to convert standard monolithic circuits into flip chips.

The approach pursued was to provide electroformed silver bumps on the thin film substrate and to modify the aluminum metallization on the monolithic circuit chip for good attachment to the substrate bumps. The modification of the metallization consisted of increasing the thickness of the aluminum for stronger ultrasonic attachments and re-defining the aluminum pad layout in an optimum geometry for ease of alignment for flip chip attachment. In this manner standardized pad locations could be established so that small variations in different manufacturers layout patterns could be eliminated and a standard substrate bump layout utilized.

Development of the bumped substrate for attachment of the circuit chips led to the technique of simultaneous electroforming of raised bumps for attachment of the external leads as well as a raised picture frame bump around the perimeter of the substrate for sealing of the package lead frame. A two-level metallization system is utilized to provide thin film cross-overs and eliminates the need for bonded jumper wires to provide the necessary crossover connections.

The circuit array module developed on this program is a five-bit binary counter utilizing five Siliconix AO-3 shift register chips packaged in a .400 x .250 flat pack. (see Figure 1).

FIGURE 1. Schematic of Five-Bit Binary Counter

II. DEVICE FABRICATION

Initial experiments were conducted to determine if the existing aluminum bonding pads on standard monolithic circuit chips could be utilized for bonding directly to a bumped substrate. Based on these experiments, it was determined that it was not practical to use this approach due to two shortcomings:

1. The aluminum thickness on standard monolithic circuit chips was quite thin, approximately 6000 Å on the Siliconix AO-3 slices. This is insufficient thickness of aluminum to obtain a strong ultrasonic bond to a bumped substrate, the bump actually "wearing" right through the aluminum layer during the ultrasonic cycle. This resulted in the bump bearing against the silicon dioxide surface of the AO-3 chip with virtually no bond strength.
2. The center to center spacing between aluminum bonding pads in standard monolithic circuits is quite small, approximately 8 mils in the case of the AO-3 circuit chip. This presents a critical alignment step to insure perfect mating of the aluminum pad and the substrate bump, and for production would result in a lower assembly yield due to electrical shorts between contacts. In addition, various inter-connection runners are located as close as .5 mil to certain bonding pads making even greater the possibility of electrical shorts by a slight misalignment of the substrate bumps.

Therefore, it was determined that an aluminum re-metallization process would be desirable to overcome these shortcomings. The approach utilized consisted of the following procedure:

1. Purchase standard completely processed and tested slices of AO-3 monolithic circuits.
2. Deposit by RF sputtering a glass layer over the entire slice.

3. Open holes in the glass to expose those original aluminum pads which are to be used for the five bit counter array.
4. Evaporate a thick aluminum layer over the entire slice.
5. Mask and etch the aluminum to a layout with large pads and greater space between them.

A. Glass Passivation:

The RF sputtered layer of glass serves as a passivating layer to protect the entire circuit, especially the aluminum interconnection pattern, as well as provide insulation between the new pad layout and the original aluminum pattern. For this reason, it is important that this be a pin-hole-free layer of glass free from stresses. The glass chosen was Corning 1723 which has a very low content of sodium and has a thermal coefficient of expansion which matches very closely with silicon. It was experimentally determined that approximately 1.5 microns of glass was required to provide a pin-hole-free passivation layer.

Probably the most difficult problem in the circuit chip fabrication was the opening of contact holes in the sputtered glass layer. The glass can be etched with hydrofluoric acid but the acid also etches the aluminum pads when the glass is broken through.

Since the etch rate of aluminum in HF is many times faster than that of glass and the aluminum is so very thin, this process was not controllable. In most cases one or more pads were completely etched before the glass etch was completed in other contact areas. Therefore, a reversal masking process previously developed by Hughes Aircraft Company was utilized for this critical operation. The procedure is as follows:

- 1) Photoresist is applied to the wafer, masked, exposed and developed. The photoresist remains on the desired contact pads and as a grid work between the devices to provide dicing grooves. The photoresist layer should be 4 to 6 microns thick to ease the break-out operation.

- 2) A 15,000 Å layer of Corning 1723 glass is then RF sputtered onto the wafer.
- 3) The glass is opened in J-100 photoresist stripper with ultrasonic power applied to the beaker. In this operation the photoresist pops the glass off and is then removed. No additional treatment or mechanical action is necessary.

B. Second Level Metallization:

After the glass opening 25,000 Å of aluminum are evaporated onto the glass layer. The aluminum is sintered to the glass and to the original aluminum in the contact holes for optimum adherence. The 25,000 Å of aluminum were found to be necessary for a maximum strength of the ultrasonic bond. (see Section VI- 1). To ease the alignment and bonding operation of the AO-3 chips to the bumped substrate, the thick aluminum contact pads on top of the glass are extended from the original contact pads using standard photoresist masking techniques. (see Figure 2).

FIGURE 2.

Remetallized AO-3 Chip with Extended Contact Pads

The wafer is then diced and sorted and only those individual circuit chips are tested which were previously ascertained good by the semiconductor supplier. After testing the good chips are stored in nitrogen.

The ultrasonic bond of aluminum to the tin solder bump has proven to be unreliable. Most of the bonded chips failed in the mechanical shock tests and some even failed in storage. Since the phase diagram of aluminum - tin (see Figure 3) does not show any intermetallic compounds it is believed that the failures are caused by corrosion and oxidation. For instance, the oxides on the surfaces of the aluminum pads and the tin bumps may be broken through only in spots resulting in weak unreliable bonds.

This bond strength problem prompted the investigation of reflow soldering after ultrasonic attachment, in view of the fact that the phase diagram shows a true eutectic does exist. However, very little improvement in bond strength was obtained due to the reluctance of the solder to wet to the aluminum, again the problem is believed to be the oxide of aluminum.

FIGURE 3. Phase Diagram Al - Sn

Therefore, since Hughes Aircraft Company has had good experience in bonding tinned bumps to gold interconnections a process was developed for plating a solderable metal to the aluminum pads. After the thick aluminum pads are defined on top of the glass a layer of nickel followed by gold is electroless plated onto these pads. This readily permits reflow soldering of the tin bumps after ultrasonic attachment, resulting in a strong reliable bond.

III. SUBSTRATE FABRICATION

1. Substrate Material Selection:

The substrate for the flip chip wireless packaging approach must satisfy the following requirements:

- a) Contain all the interconnections between devices and from devices to external leads.
- b) Serve as the mounting base or platform for all circuit chips.
- c) Contain thin film crossovers, when required.
- d) Forms the bottom part of the package.

Three different materials were investigated, Corning Glass 7059; glazed Al Si Mag 614, and unglazed Al Si Mag 772.

Due to its superior mechanical and thermal properties as compared to glass or glazed alumina, the unglazed alumina Al Si Mag 772 was preferred.

- i) Unglazed alumina has improved thermal conductivity by a factor of two over glazed alumina.
- ii) The pull strength of ribbon leads soldered to thin films on unglazed alumina is 3 to 5 times higher compared to the same leads soldered to thin films on glazed alumina or on glass, (see Table I).

TABLE I

Lead No.	Glazed Al Si Mag 614	Unglazed Al Si Mag 772	Corning 7059 Glass
	1)	2)	1)
1	200 gr	700 gr	150 gr
2	250 "	1050 "	160 "
3	150 "	900 "	100 "
4	100 "	920 "	170 "
5	100 "	950 "	250 "
6	100 "	930 "	120 "
7	120 "	900 "	120 "

1) Lead breaks off when bent in vertical direction at angle of approximately 10° to 20°

2) Lead does not break off at bend angle of 90°.

2. Substrate Metallization:

Since the module contains no thin film resistors, a standard chrome-gold metallization process is used for the interconnections. The substrates are fabricated in a batch process on 1 x 3 inch slices, twenty-two at a time.

First a chromium layer is evaporated followed by a gold deposition in a single vacuum run. The chromium provides an excellent adherence to the alumina serving as an adhesive for the gold. The purpose of the gold is to provide electrical conductivity for the interconnections.

The slice is then masked with the interconnection mask, etched and masked again for electro-deposition of silver. Silver bumps are electroformed simultaneously for:

- a) The bump contacts for all the contact pads for the monolithic circuit chips.
- b) Large bump pads for attachment of the external leads.
- c) Picture-frame bump around the perimeter of the substrate for hermetic sealing of the lead frame.

(see Figure 4).

The silver plating is necessary for the tinning process. Without the silver the thin gold film would be dissolved in the tin solder bath. The bump structure is composed of a silver bump 4 mils in diameter and 1 mil high with a tin solder cap of approximately 0.5 mil in height. The solder alloy is quite soft and ductile which is advantageous in achieving ultrasonic bonds and provides a means for equalizing bump

FIGURE 4. 1" x 3" Slide with 22 Substrates, Diced Substrates

height differences when pressure is applied during the attachment. The silver bump is considerably harder than the solder alloy and does not deform during the ultrasonic attachment, essentially acting as a stand-off to insure clearance between chip and substrate.

3. Passivation and Crossovers:

After the substrate metallization a layer of Corning 1723 glass is deposited onto the substrate by RF sputtering. The purpose of the glass layer is:

- a) To provide the dielectric insulation for the thin film crossovers.
- b) To protect the gold interconnect pattern from completely dissolving into the solder bath when forming the solder caps.
- c) To protect the entire interconnect pattern from scratches and damage.

After the glass deposition the slice is masked with photoresist. The glass can be etched, with an HF solution, from the silver and the crossover contacts.

The crossover connections are made as follows:

Photoresist is applied to the slice, masked and developed. The photoresist covers the whole slice except the required L-shaped crossovers. In one vacuum run chrome-gold-chrome is then evaporated on the entire slice. Now the photoresist is stripped and only the crossovers remain (see Figure 5).

The slice is dipped in a tin solder bath to form solder caps on the bumps, the pads and the sealing frame. The top layer of chromium on the crossovers protects the gold in this operation.

The solder dip is a critical process. If the slice stays too long in the bath, much of the silver is dissolved by the tin, resulting

FIGURE 5. Thin Film Crossovers

in a wide-spread bump height tolerance. Bump height tolerances of $\pm .4$ mil were common. If the dip is too short, some bumps remain untouched from the solder.

Another approach which provides a small bump height tolerance is to electroplate tin solder. A layer of 15 microns of 60/40 tin solder is deposited onto the silver after the silver plating. The bump height tolerance can now be maintained within $\pm .1$ mil.

A disadvantage of the unglazed alumina is its relative rough surface of 8μ inches for thin film crossovers. It was found that crossovers with sufficient yield could be made on polished substrate surfaces with one micron RF sputtered glass as an insulator. The rough substrate surface requires at least 5 microns for a sufficient yield. The yields obtained from several RF sputtered glass thicknesses were as follows:

TABLE II

Thickness of RF Sputtered Glass	Yield
2.5 microns	10 %
5 microns	95 %
7 microns	99 % to 100 %

The average thickness of the RF sputtered glass on most slices was 5 to 6 microns. With five crossovers on each module the substrate yield obtained was 90 to 95%. The metallurgically finished slices are diamond sawed into individual substrates, followed by an inspection. They are then ready for the dice mounting.

IV. MODULE ASSEMBLY

1. Lead Frame Assembly:

The lead frame was designed to be mounted to the substrate by reflow soldering the sealing frame and the 14 external leads simultaneously. The .25 x .40 inch lead frame consists of a glass frame metallized on both sides with gold plated Kovar, which seals to the substrate and the lid. 14 gold plated Kovar ribbon leads serve as connectors between the thin film circuitry and the outside world. (see Figure 6).

In a fixture, (see Figure 7), the substrate is held on a heated vacuum chuck and aligned to the lead frame. The temperature is quickly raised above the melting point of the solder. The frame is then pressed to the substrate and the vacuum chuck is cooled down to approximately 40° C below the melting point of the solder.

This procedure was found to be very reliable since there were no rejects. Figure 8 shows a lead frame mounted to a substrate.

FIGURE 6. Lead Frame with Substrate and Lid

FIGURE 7. Jig Used for Lead Frame Mounting

FIGURE 8. Lead Frame Mounted on Substrate

2. Flip Chip Mounting:

The AO-3 chips metallized as described in Section II are mounted to the sub-assembled substrates with a Hughes Ultrasonic Flip Chip Bonder, Model 2906 (see Figure 9). The settings of the bonder are variable:

- a) The force with which the chip is clamped down to the bumps on the substrate.
- b) The ultrasonic power applied to the chip.
- c) The time duration at which the ultrasonic power is applied to the chip.

All of these settings must be determined experimentally and they depend on the number of bumps, the bump size and the material. The settings at which a sufficient bonding of the AO-3 chips is obtained are:

Clamping force -	500 to 600 grams
Ultrasonic power -	set dial to 6.0
Time -	set dial to 5.0 (approx.)

FIGURE 9. Hughes Aircraft Model 2906 Ultrasonic Flip Chip Mounter

Higher force and power squeezes the bumps too much and also may result in cracking of the chips. Because of the large extended pads on the chips alignment to the bumps is quite easy and allows a certain tolerance.

The chips with the nickel-gold plated pads have to be reflow soldered after they are attached by the flip chip bonder. The chips are heated to the melting point of the solder with a hot gas gun, one at a time. The substrate is heated to 150° C only, which is well below the melting point of the tin solder used to mount the lead frame. This time was determined empirically by shearing off the soldered chips. An inspection was then made with a microscope to see whether the bumps wetted the gold pads or not and how much the tin spread out. The tin solder wets the gold pads very easily in the reflow operation and requires a cycle time per chip of only 10 seconds. The short heating

cycle prevents the solder from dissolving the gold completely and also avoids the spreading of the tin solder over the entire pad. The wetted area of every single contact is only slightly larger than the bump diameter, resulting in very consistent bonding strength from chip to chip.

The reflow soldering process also makes repair of a completed module possible in case a chip should become malfunctional. The defective chip is heated with the hot gas gun until the solder melts and is then lifted and removed. A new chip can now be mounted and reflow soldered with the same process as described. It has been established that a one-time repair is always possible and a second repair can also be accomplished in some cases, depending on the amount of solder left on the bumps. Figure 10 shows sub-assembled package with the five AO-3 chips mounted.

This is an important feature of the solder bump since the defective chips can be merely lifted off the bumps after the solder melts without the necessity for fracturing its bond.

FIGURE 10. Assembled Five-Bit Binary Counter

3. Lid Mounting:

The gold-plated Kovar lid is mounted to the lead frame after the module is electrically pretested (see Section V). A standard process is used for sealing flat packs using a solder preform in a Dix Sealer. It is important that the bottom of the package is heat sunk very well, since the maximum allowed temperature inside the package is 150°C for keeping the lead frame and the chips at a safe level below the melting point of their solders. For identification purposes an identification dot, the type number and the serial number are printed on the sealed lid. (see Figure 11).

FIGURE 11. Symbolized Units

V. ELECTRICAL TESTING:

1. Chip Testing:

The AO-3 wafers are tested by the semiconductor supplier. Mal-functional devices are ink-marked so that no additional test is necessary prior to the glass deposition. See Figure 12.

After dicing and sorting, the devices without the ink marks are electrically tested. A schematic of the test set-ups are shown in Figure 13. The contact to the single pads is made by a multi-probe test station.

The chip is operated with a $V_{CC} = +5$ volts. Two voltmeters are connected to Q and $\bar{Q}$ to indicate either the low or the high state. 5 volt pulses applied to the input gate alternate the indications. There

FIGURE 12. Tested AO-3 Chips, As Purchased

AO-3 PROBE TEST SETUP.

FIGURE 13. Schematic of AO-3 Dice Test Set-Up

are no specification requirements but only the units within the following range were accepted:

Low state:	0.5 to 1.5 V
High state:	4.5 to 5.5 V

2. Testing of Completed Modules:

The assembled module is tested twice. A functional test is made before the packages are sealed to preserve the possibility for repair. The final electrical test is made after the package is sealed. The test procedure is similar to the single chip testing. Figure 14 shows a schematic of the module test set-up. Again, the module is operated at +5 volts. A pulse generator which delivers +5 volts pulses is connected to the input. With the voltmeters plugged in to the first stage, the conditions between the low and the high stage must change with every applied pulse. The meter indication should be .5 to 1.5 volts for the low state and 4.5 to 5.5 volts for the high state. With the voltmeters plugged into the second stage the condition must change with every second pulse. At the third stage every fourth pulse must change the conditions, at the fourth stage every eighth pulse and at the fifth stage every sixteenth pulse.

Figure 15 shows the pulses on a CRT in response to the clock pulses.

FIGURE 14. Schematic of Unit Test Set-Up

Functional Test of Five Bit Binary Counter

Module No. 1-001

FIGURE 15. CRT Photograph of Pulses, Stage 1 through 5

VI. MECHANICAL TESTING

1. Shear Tests:

The strength of the flip chip bonds were tested with a dynamometer by shearing the bonded chips off the substrate. Although this is a destructive test it is a practical method to judge the strength with which the chip was bonded to the substrate. A disadvantage of the flip chip technique is that a visual inspection of the bonds as with common methods is impossible. To prove whether all bumps make an ohmic contact with the contact leads, the bonded chip has to be tested electrically, but an ohmic contact does not necessarily mean that this contact provides the required mechanical strength.

Therefore, the shear strength of bonded chips was measured and the sheared-off contacts were inspected with a microscope. The measurement of the shear strength indicates the average bonding strength of the chip, and the visual inspection of the sheared contacts shows whether the bumps made contact in their full size, or in spots or whether one or more bumps did not make contact at all. One missing bump contact would not be indicated by the shear test alone since the indication tolerance is about $\pm 15\%$. It requires the electrical test to determine whether all bumps made an ohmic contact.

About 50 electrically rejected AO-3 chips, ultrasonically bonded and then reflow soldered, were sheared and inspected. The lowest observed values were 700 grams, the highest 1100 grams. A cross-section of a reflow soldered contact is shown in Figure 16.

If the bump height tolerance does not exceed ± 2.5 microns all nine bumps per chip will reflow solder and provide a reliable contact.

In the first phase of the contract it was tried to develop a non-soldered contact system. The silver/tin/lead bumps on the substrate were

FIGURE 16. Cross-Section of Reflow Soldered Bump

ultrasonically bonded to the aluminum leads on the chips. First the required aluminum thickness was studied, and as Figure 17 shows, about 25,000 Å aluminum are necessary to guarantee that the bumps do not wear through the aluminum. If the bumps punch through the aluminum and bear against the glass surface the shear strength is lowered, sometimes by a factor of two or more.

The silver-tin-lead to aluminum contact system, which cannot be reflow soldered provides a bonding strength high enough to withstand the required centrifuge test. However, during mechanical shock, storage and life tests, most modules failed due to open contacts.

2. Constant Acceleration:

The constant acceleration tests were carried out after MIL-STD-750 A, Method 2006 at 25,000 g's. None of the reflow soldered chip modules failed in this test. Since the mass of the chip is 10^{-3} gms the

Shear
Strength
gr.

SHEAR STRENGTH MEASUREMENTS ON BUMPED SUBSTRATES

Sample points represent average of 5 tests

FIGURE 17. Shear Strength vs Aluminum Thickness

25,000 g's acceleration force is equivalent to a shear strength of 25 gms. This is far below the minimum bonding strength obtained with the silver/tin/lead to aluminum system.

3. Shock Test:

This test is carried out after MIL-STD 750 A, Method 2016 at 300 g's, 1/2 sine wave, 3 milliseconds. Reflow soldered chips passed this test without failures. For the silver/tin/lead - aluminum system with ultrasonically attached chips only, this test resulted in open contacts or in most cases one or more chips came off the substrate. It appeared that no relationship existed between shear strength and ability to pass the shock test.

4. Temperature Cycling:

The silver/tin/lead - aluminum system was not tested in temperature cycling because of the failures in the shock tests. The reflow soldered chips passed the test, carried out after MIL-STD 750 A, Method 1051 without failures. Due to the silver/tin/lead-solder the maximum temperature of the unit must be limited to 150° C.

5. Leak Test:

The package consisting of substrate, lead frame and lid was tested after MIL-STD 202 C, Method 112. Based on this testing, the important question of whether the evaporated chrome/gold seals to the unglazed alumina or not can be answered in the affirmative. The measured leakage rate was below 4×10^{-8} cc/He/sec., but can only be attained when substrates and lead frames are properly selected. Most substrates and lead frames are more or less warped and it is difficult to fill the resulting gap with solder. When attempts were made to press the substrate and the lead frame together to close the gap, the glass of the lead frame cracked. The packaging yield depends on the flatness of the substrates and the lead frames. With flat parts this packaging concept is highly recommended.

VII. CONCLUSIONS AND RECOMMENDATIONS

The five bit binary counter described utilizes a flip chip lead frame packaging approach demonstrating the many features of this packaging concept:

1. Use of standard monolithic circuit chips modified for flip chip assembly.
2. Use of a bumped substrate for ultrasonic attachment of the chips which also serves as the bottom half of the package.
3. Use of a lead frame reflow soldered to the substrate to form external lead connections and package seal simultaneously.
4. Use of thin film crossovers.
5. Elimination of all wire bonds.
6. Improved thermal resistance since the circuit substrate is actually the base of the package, eliminating one thickness of material.
7. Lead frame packaging approach provides better utilization of the substrate area.
8. Simple assembly techniques required.
9. Circuit repairability by replacement of defective chips.

The bumps on the substrate approach was utilized in this program since it was considered impractical to deviate from aluminum metallization on the monolithic circuit slice, and electroformed bumps could not be formed directly onto aluminum metallization. However, during the latter part of the program it was recognized that the ultrasonic bond of the substrate bumps directly to the aluminum pads or the chips was not reliable enough to withstand all the necessary testing. Therefore, a process was developed to deposit a nickel and gold layer over the aluminum pads by electroless plating which enabled the ultrasonically bonded chips to be reflow soldered for increased bond strength. It now becomes apparent that a more desirable approach may be the bumps on chip approach since bumps can now be

formed onto the gold plating on the aluminum pads. This would eliminate the processing required for forming bumps on the substrate.

PROCESS FLOW OF FIVE-BIT BINARY COUNTER

<u>Item Number</u>	<u>Paragraph Number</u>	<u>Inspection</u>	<u>Process Title</u>
1	1.0		<u>AO-3 Remetallization</u>
2	1.1		Wafer Cleaning
3	1.2		Apply Photoresist
4	1.3		Contact Mask Alignment & Exposure
5	1.4		Photoresist Development
6	1.5	X	Photoresist Inspection
7	1.6		Glass Sputtering
8	1.7		Open Glass for Contact Windows
9	1.8	X	Inspection for Open Contact
10	1.9		Aluminum Evaporation
11	1.10		Apply Photoresist
12	1.11		Contact Pad Alignment & Exposure
13	1.12		Photoresist Develop
14	1.13	X	Photoresist Inspection
15	1.14		Aluminum Etching
16	1.15		Wafer Cleaning
17	1.16		Nickel and Gold Plating
18	1.17		Wafer Testing
19	1.18		Wafer Dicing
20	2.0		<u>Substrate Fabrication</u>
21	2.1		Substrate Clean-up
22	2.2		Chrome-Gold Evaporation

Process Flow of Five-Bit Binary Counter (continued)

<u>Item Number</u>	<u>Paragraph Number</u>	<u>Inspection</u>	<u>Process Title</u>
23	2.3		Apply Photoresist
24	2.4		Interconnect Masking & Exposure
25	2.5		Photoresist Develop
26	2.6	X	Photoresist Inspection
27	2.7		Interconnection Etching
28	2.8	X	Slice Inspection
29	2.9		Apply Photoresist
30	2.10		Align Bump Mask & Expose
31	2.11		Photoresist Develop
32	2.12		Bump Plating
33	2.13		Wafer Cleaning
34	2.14		Sputter Glass
35	2.15		Apply Photoresist
36	2.16		Glass Opening Mask Alignment & Exposure
37	2.17		Photoresist Develop
38	2.18		Glass Etch
39	2.19		Substrate Cleaning
40	2.20		Apply Photoresist
41	2.21		Crossover Mask Alignment & Exposure
42	2.22		Photoresist Develop
43	2.23		Cr/Au/Cr Evaporation
44	2.24		Substrate Cleaning
45	2.25	X	Inspection
46	2.26		Dicing
47	2.27	X	Testing
48	3.0		Assembly of the Five-Bit Binary Counter

Process Flow of Five-Bit Binary Counter (continued)

<u>Item Number</u>	<u>Paragraph Number</u>	<u>Inspection</u>	<u>Process Title</u>
49	3.1		Mount Lead Frame to Substrate
50	3.2		Substrate Cleaning
51	3.3		Ultrasonic Flip Chip Mounting
52	3.4		Reflow Solder AO-3 Chips
53	3.5		Test Module Electrically
54	3.6		Final Package Seal
55	3.7		Test Mechanically
56	3.8	X	Electrical Testing of Completed Unit

VIII. FABRICATION SPECIFICATIONS

The material, equipment and procedures necessary to manufacture the five stage binary counter will be described in this section. Solvents and acids are, "Electronic Grade".

1.0 AO-3 Remetallization

1.1 Wafer Cleaning:

A. Materials

1. Siliconix AO-3 wafer
2. TCE
3. Methanol
4. Dry nitrogen
5. Deionized water

B. Equipment

1. Hot plate
2. Beaker
3. Fixture (see Figure 25)

C. Procedure

1. Load wafer into fixture
2. Insert fixture containing wafer in hot TCE for 5 minutes.
3. Insert fixture containing wafer in hot methanol for 5 minutes.
4. Insert fixture containing wafer in hot D.I. water for 5 minutes.
5. Blow wafer with filtered nitrogen.
6. Store in Pyrex dish.

1.2 Apply Photoresist:

A. Materials

1. Photoresist (KPR/KPL) Viscosity as purchased from Kodak.
2. Dry nitrogen

B. Equipment

1. Photoresist spinner
2. Dust-free enclosure
3. Hypodermic needle

C. Procedure

1. Mix KPR and KPL (30% KPR and 70% KPL) and fill hypodermic syringe.
2. Mount wafer on vacuum chuck of spinner. Blow dry nitrogen over wafer. (Headway Model No. EC-100).
3. Apply KPR/KPL with hypodermic needle onto wafer, 5 drops and rotate wafer at 2000 rpm for 20 seconds.
4. Inspect for dust particles.
5. Store in dry nitrogen.

1.3 Contact Mask Alignment & Exposure:

A. Materials

1. Photoresist-coated wafer
2. Photomask (see Figure 18).

B. Equipment

1. Mask alignment exposure system, (Electroglass Model 500).
2. Tweezers

C. Procedure

1. Select proper mask and secure in mask fixture
2. Pick up coated wafer and place on alignment fixture
3. Place wafer under mask and align wafer to mask using the microscope. Align contact openings to center of aluminum pads on wafer.
4. Expose. Exposure time will be set by responsible Engineering personnel. Typical time is 13 seconds.
5. Remove wafer from exposure system, place in dish and send to be developed.

Wafer Glass Opening Mask

FIGURE 18. AO-3 Glass Opening Mask

1.4 Photoresist Development:

A. Materials

1. KPR developer
2. Denatured ethyl alcohol.

B. Equipment

1. Dust-free hood
2. Developing fixture
3. Pyrex tray
4. Timer
5. Filtered nitrogen

C. Procedure

1. Insert wafer in tray with KPR developer and immerse for two minutes.

2. Spray with alcohol for 5 seconds.
3. Blow dry with nitrogen
4. Place wafer in dish.

1.5 Photoresist Inspection

A. Material

1. Wafer with developed photoresist pattern.

B. Equipment

1. Metallurgical microscope (200X)
2. Tweezers

C. Procedure

1. Inspect wafers for the following photoresist defects:

Definition
Adherence
Alignment

2. Rejected wafers to be stripped and reprocessed.
3. Place wafer in dish and store in nitrogen.

1.6 Glass Sputtering:

A. Material

1. Wafers inspected with photoresist pattern.
2. Glass targets (Corning 1723) 5 inch diameter.
3. Argon

B. Equipment

1. Sputtering module with RF generator, Mathis SP-210.
Target to substrate distance ~ 1.5 inch. 13.56 MHz.
2. Control instruments for the control of temperature, vacuum, and argon gas pressure.

C. Procedure

1. Open vacuum chamber of sputterer.

2. Place wafers on substrate holder and place one half dummy wafer for the determination of the sputtered glass thickness in the center of the substrate holder.
3. Close vacuum chamber.
4. Pump down to 10^{-6} mm Hg.
5. Open needle valve and set argon gas pressure to 10 to 20 microns.
6. Start RF generator, increase power slowly to 200 W input power. Substrate temperature should not exceed 120°C . Sputtering time will be set by responsible engineering personnel. Typical time is 24 hours for two microns of glass.
7. When desired thickness of glass is reached, turn RF-generator off, close vacuum valves, flood vacuum chamber with dry nitrogen, pick up wafer and place in dish.
8. Angle-section the dummy wafer and determine the sputtered glass thickness. Required glass thickness: $2.0 \pm .5$ microns.

1.7 Open Glass for Contact Windows:

A. Material

1. Photoresist stripper J-100
2. Wafer with sputtered glass
3. Dry nitrogen
4. D.I. water

B. Equipment

1. Ultrasonic cleaning system
2. Beakers
3. Tweezers
4. Hot plate

C. Procedure

1. Heat concentrated J-100 in beaker up to 120°C .

2. Place wafer in beaker with hot J-100, soak for five minutes and place beaker in ultrasonic system.
3. Turn ultrasonic power ON, treat wafer for five minutes.
4. Rinse wafer in hot water, typical five minutes.
5. Rinse wafer in D.I. water, typical five minutes.
6. Blow wafer dry with nitrogen.
7. Place wafer in dish.

1.8 Inspection for Open Contact Windows:

A. Material

1. Wafer with contact windows opened.

B. Equipment

1. Metallurgical microscope (400X)
2. Tweezer

C. Procedure

1. Inspect wafer for the following defects:
 - Glass remaining in contact windows
 - Photoresist remaining in contact windows.
 - Aluminum on contact pads must be shiny, if any photoresist remains, repeat step 1.7.
2. Place inspected wafer in dish.

1.9 Aluminum Evaporation:

A. Material

1. Inspected wafer from step 1.8
2. Pure aluminum, 99.9%, A.D. Mackay, Inc.
3. Tungsten boat.

B. Equipment

1. Evaporator, NRC Model 3116
2. Angstrometer, Sloan Model M-100

C. Procedure

1. Mount wafer on substrate holder

2. Place clean aluminum in tungsten boat
3. Exhaust system to 1×10^{-6} torr.
4. Backfill vacuum chamber with argon and ion bombard
5. Exhaust system to 1×10^{-6} torr.
6. Evaporate aluminum to desired metal thickness
7. Close vacuum valves, open chamber and measure metal thickness on dummy slice with angstrometer, record on run sheet. Required aluminum thickness: $2.2 \pm .2$ microns.

1.10 Apply Photoresist:

A. Material

1. Wafer with aluminum
2. Photoresist.

B. Equipment

1. (see section 1.2)

C. Procedure

1. (see section 1.2)

1.11 Contact Pad Alignment & Exposure:

A. Material

1. Photoresist coated wafer
2. Photomask (see Figure 19).

B. Equipment

1. (see section 1.3)

C. Procedure

1. (see section 1.3)

Wafer Remetallizing Mask

FIGURE 19. AO-3 Extended Contact Pad Mask

1.12 Photoresist Develop:

A. Material

1. Exposed wafer
2. Photoresist developer

B. Equipment

1. (see section 1.4)
2. Oven

C. Procedure

1. (see section 1.4)
2. Bake wafer at 125° C for 15 minutes
3. Place wafer in dish.

1.13 Photoresist Inspection:

A. Material

1. Wafer with developed photoresist pattern

B. Equipment

1. Metallurgical microscope (200X)
2. Tweezer

C. Procedure

1. (see section 1.5)

1.14 Aluminum Etching:

A. Material

1. Inspected wafer
2. Sodium hydroxide solution, 10% concentration, 140° F temp.
3. Deionized water

B. Equipment

1. Acid sink
2. Beaker
3. Microscope
4. Fixture

C. Procedure

1. Place wafer in fixture and immerse in sodium hydroxide solution.
2. Etch wafer until all excess aluminum has been removed.
3. Remove wafer from etching solution and rinse in D.I. water.
4. Inspect wafer for remaining aluminum. If present repeat step 1 through 3.
5. Blow wafer dry with nitrogen.

1.15 Wafer Cleaning:

A. Material

1. Wafer with etched aluminum
2. J-100
3. Deionized water
4. Dry nitrogen

B. Equipment

1. Hot plate
2. Fixture
3. Beaker
4. Tweezer
5. Microscope

C. Procedure

1. Load fixture with wafer and insert in hot J-100, 10 mins. Temperature of J-100 must be 120° C.
2. Rinse wafer in D.I. water, 10 minutes.
3. Blow wafer dry with nitrogen.
4. Inspect under microscope. If necessary repeat steps 1 through 3.

1.16 Nickel and Gold Plating:

A. Material

1. Inspected wafer with etched aluminum pads.
2. Sodium hydroxide, 10%.
3. Deionized water.
4. Hydroflouric acid, 2%.
5. Nitric acid, concentrated.
6. Zincate: Sodium hydroxide 6.7 oz/gal; Zinc Oxide .67 oz/gal; Rochelle salt .67 oz/gal; Ferric Chloride .27 oz/gal, Sodium nitrate 13 oz/gal.
7. Shipley NL-61, as purchased.
8. Selrex electroless gold plating solution, Autronex-NL, as purchased.

B. Equipment

1. Hot plate
2. Ventilated hood with acid sink.
3. Beakers (pyrex and teflon).
4. Tweezers
5. Fixture
6. Furnace
7. Metallurgical microscope (200X).

C. Procedure

1. Dip wafer in sodium hydroxide for 5 seconds.
2. Rinse in running D.I. water, 2 minutes.
3. Dip wafer in HF solution for 5 seconds.
4. Rinse in running D.I. water for 2 minutes.
5. Dip wafer in zincate solution for 10 seconds.
6. Rinse in running D.I. water for 2 minutes.
7. Dip wafer in nitric acid, typically for 20 seconds.
8. Rinse in running D.I. water for 2 minutes.
9. Dip wafer in zincate solution for 15 seconds.
10. Rinse in D.I. water for 5 seconds.
11. Immerse in nickel plating solution for 2 minutes.
Required nickel thickness approximately 1 micron.
12. Rinse in running D.I. water for 2 minutes.
13. Immerse in gold plating solution for 30 minutes.
Required gold thickness approximately 1 micron.
14. Rinse in running D.I. water for 2 minutes.
15. Blow dry with nitrogen.
16. Diffuse nickel into aluminum in furnace at 300° C for 10 minutes in nitrogen atmosphere.
17. Inspect under microscope for complete plating of aluminum pads and blisters.

1.17 Wafer Testing:

A. Material

1. Wafer, nickel and gold plated.

B. Equipment

1. Special test fixture (see Figure 13).
2. Pulse generator (Data Pulse 106).
3. Multipoint probe assembly.
4. Voltmeter (0 -5 V).
5. Tweezer
6. Marking pen.
7. Power Supply (see Figure 13).

C. Procedure

1. Place on vacuum chuck.
2. Align and lower probe on die under test.
3. Define: Low State (1) .5 - 1.5 V
 High State (0) 4.5 - 5.5 V

	Q	$\bar{Q}$
I	0	1
II	1	0

4. Press reset button. Meters indicate the I condition.
5. Apply single pulse from generator and note that the conditions alternate.
6. Repeat 5.
7. Mark units not meeting the above requirements
8. Move to next unit and repeat procedure.

1.18 Wafer Dicing and Sorting:

A. Material

1. Tested wafers, malfunctional devices ink-marked.
2. Polyvinylchloride film

B. Equipment

1. Scriber
2. Roller
3. Tweezer

4. Dish
5. Microscope

C. Procedure

1. Place wafer on vacuum chuck of scribe
2. Scribe to required die size
3. Place wafer between pieces of PVC-film on a rubber pad and break into dice by rolling back side with roller.
4. Sort electrically good dice and inspect for scribing defects.
5. Store good dice in dish preserving lot identification.

2.0 Substrate Fabrication

2.1 Substrate Clean-up:

A. Material

1. Al Si base 772 slice 1 x 3 x .025 inch.
2. TCE
3. Methanol
4. Deionized water
5. Dry nitrogen
6. Solvent detergent, Amway Industrial Clean.

B. Equipment

1. Ultrasonic Cleaner
2. Hot plate
3. Fixture (see Figure 25)
4. Tweezer

C. Procedure

1. Clean substrates in detergent.
2. Load fixture with ceramic slices and insert in hot TCE.
3. Blow slices dry and insert in tray with methanol. Treat with ultrasonic.
4. Blow slices dry and insert in beaker with hot D.I. water. Treat with ultrasonic.

5. Rinse in D. I. water.
6. Blow dry with nitrogen and store in dish.

2.2 Chrome-Gold Evaporation:

A. Material

1. Powdered chromium
2. Gold wire
3. Cleaned ceramic slices

B. Equipment

1. Evaporator with controls for vacuum, temperature and film thickness, NRC Model 3116.

C. Procedure

1. Load substrate holder with ten ceramic slices
2. Load filaments with chromium and gold
3. Exhaust evaporator to 1×10^{-6} torr.
4. Backfill with argon to a pressure of 10 - 20 microns
5. Glow discharge and heat substrates to specified temperature.
6. Exhaust to 1×10^{-6} torr.
7. Evaporate chromium to desired film thickness, 100 Ω /sq.
8. Evaporate gold to desired film thickness, .08 Ω /sq.
9. Cool down to room temperature and unload evaporator.

2.3 Apply Photoresist:

A. Material

1. Photoresist (KTFR), mixed - 70% KTFR - 30% KTFR thinner. Viscosity as purchased from Kodak.

B. Equipment

1. Photoresist spinner
2. Dust-free hood
3. Fixtures
4. Hypodermic needle
5. Box filled with dry nitrogen

C. Procedure

1. Load spinner with one slice
2. Apply photoresist with hypodermic needle on slice
3. Spin for specified time
4. Store slice for 20 minutes in dry nitrogen

2.4 Interconnection Masking and Exposure:

A. Material

1. Photoresist coated slice
2. Photomask (see Figure 20).

B. Equipment

1. Mask alignment and exposure system

C. Procedure

1. Select proper mask and place in alignment system.
2. Insert slice under mask and align edges.
3. Expose for specified time.

FIGURE 20. Substrate Interconnect Mask

2.5 Photoresist Develop:

A. Material

1. Exposed slice
2. KMER developer
3. KTFR rinse
4. Dry nitrogen

B. Equipment

1. Ventilated hood
2. Tray
3. Fixture
4. Oven
5. Timer

C. Procedure

1. Soak slice for 2 minutes in KMER developer.
2. Rinse in KTFR rinse for 5 seconds.
3. Blow slice dry with nitrogen.
4. Bake at 125°C for 20 minutes.

2.6 Photoresist Inspection:

A. Material

1. Developed slice.

B. Equipment

1. Microscope

C. Procedure

1. Inspect photoresist for line definition and scratches.

2.7 Interconnection Etching:

A. Material

1. Aurostrip, concentration 60 grams/l.
2. Hydrochloric acid solution, 4 parts HCl - 1 part H₂O.
3. Deionized water.
4. J-100 concentrated.

B. Equipment

1. Hot plate
2. Hood with acid sink
3. Beakers
4. Slice holder.

C. Procedure

1. Load slice holder with slice.
2. Insert in beaker with Aurostrip (65°C) for specified time, typical 2 minutes.
3. Rinse in running water and inspect for residue gold. If necessary, repeat step 2.
4. Insert in HCl solution for specified time, typically 5 seconds.
5. Rinse in running water for 5 minutes and inspect for residue chromium. If necessary, repeat step 4.
6. Insert slice in J-100 (120°C) for 10 minutes.
7. Rinse in running water for 5 minutes.
8. Boil in deionized water for 10 minutes.
9. Rinse in deionized water for 5 minutes.
10. Blow dry with nitrogen.

2.8 Slice Inspection:

A. Materials

1. Etched slices

B. Equipment

1. Microscope

C. Procedure

1. Inspect for line definition, residual chromium between interconnection wiring and open lines.

2.9 Apply Photoresist:

A. Material

1. Slice with etched interconnections
2. Photoresist (KTFR) -mized solution 70% KTFR - 30% KTFR thinner.

B. Equipment

1. Photoresist spinner with speed control and timer
2. Fixtures
3. Hypodermic needle
4. Oven

C. Procedure

1. Place slice on spinner and set speed and time
2. Apply photoresist to slice
3. Spin at specified speed for 20 seconds
4. Dry photoresist 15 minutes at room temperature
5. Dry photoresist 15 minutes at 65° C.

2.10 Align Bump Mask and Expose:

A. Material

1. Slice coated with KTFR
2. Bump Mask (see Figure 21).

B. Equipment

1. Mask alignment and exposure system

C. Procedure

1. Select proper mask and place in alignment system
2. Insert slice under mask and align to each other
3. Expose for specified time.

2.11 Photoresist Develop:

A. Material

1. Exposed slice

FIGURE 21. Substrate Bump Mask

2. KMER developer
3. KTFR rinse
4. Dry nitrogen

B. Equipment

1. Ventilated hood
2. Tray
3. Fixture
4. Timer
5. Oven

C. Procedure

1. Soak slice for two minutes in KMER developer.
2. Rinse in KTFR rinse for 5 seconds.
3. Blow slice dry with nitrogen.
4. Bake at 125°C for 20 minutes.

FIGURE 22. Hot Gas Gun

2.12 Bump Plating:

A. Material

- 1 Silver-plating solution.
2. Tin-lead plating solution.
3. Deionized water.
4. Slice with developed KTFR pattern.

B. Equipment

1. Ventilated hood.
2. Plating bath for silver with power supply.
3. Plating bath for lead-tin with power supply.
4. Timer
5. Microscope

C. Procedure

1. Place slice in plating fixture and insert into silver plating bath.

2. Set power supply to specified readings and start timer.
Control and set plating current to proper value.
3. After specified time, rinse slice in D.I. water for 5 minutes.
4. Place slice in plating fixture and insert into tin-lead plating bath.
5. Set power supply to specified readings and start timer.
Control and set plating current to proper value.
6. After specified time, rinse slice in D.I. water.
7. Blow slice dry with nitrogen.
8. Inspect with metallurgical microscope (200X)
 - a) bump height, 30 ± 2 microns
 - b) imperfections, i. e. outgrowths, plating through pinholes in photoresist.

2.13 Wafer Cleaning:

A. Materials

1. J-100 photoresist stripper, concentrated.
2. Deionized water.

B. Equipment

1. Ventilated hood with acid sink.
2. Hot plate
3. Beaker
4. Fixture
5. Ultrasonic cleaner.

C. Procedure

1. Insert slice in hot J-100 for 10 minutes
2. Place beaker with J-100 and slice in ultrasonic cleaner and treat for 5 minutes.
3. Rinse slice in running water for 5 minutes.
4. Boil slice in hot D.I. water, treat in ultrasonic cleaner. Typical time 10 minutes.

5. Rinse in D. I. water, 5 minutes.
6. Blow dry with nitrogen.

2.14 Sputter Glass:

A. Material

1. Slice with plated bumps
2. Glass targets (Corning 1723)
3. Argon

B. Equipment

1. Sputtering module with RF generator, Mathis SP-210
2. Instruments for the control of temperature vacuum and argon gas pressure.

C. Procedure

1. Same as in Section 1.6.
Desired glass thickness on slices 5 - 6 microns.

2.15 Photoresist Apply:

A. Materials

1. Slices with sputtered glass
2. Photoresist (KTR)

B. Equipment

1. Photoresist spinner with speed control and timer.
2. Oven
3. Fixtures
4. Hypodermic needle.

C. Procedure

1. Place slice on photoresist spinner.
2. Apply photoresist on slice with hypodermic needle.
3. Spin at 1200 rpm for 20 seconds.
4. Dry photoresist for 15 minutes at room temperature.
5. Dry photoresist for 15 minutes at 65° C.

2.16 Glass Opening Mask Alignment and Expose:

A. Material

1. Glassed slice, coated with KTFR.
2. Glass-opening mask (see Figure 19).

B. Equipment

1. Mask alignment and exposure system.

C. Procedure

1. Select proper mask and place in alignment system.
2. Insert slice under mask and align to each other.
3. Expose for specified time.

2.17 Photoresist Develop:

A. Material

1. KMER developer
2. KTFR rinse
3. Exposed slice
4. Dry nitrogen

B. Equipment

1. Ventilated hood
2. Tray for KMER developer
3. Beaker for KTFR rinse
4. Fixture
5. Timer
6. Metallurgical microscope
7. Oven

C. Procedure

1. Immerse slice in KMER developer for 2 minutes.
2. Rinse in KTFR rinse, 5 seconds.
3. Blow dry with nitrogen
4. Inspect under microscope for complete development and definition of edges.
5. Bake in oven at 125° C for 20 minutes.

2.18 Glass Etch:

A. Material

1. Slice with developed pattern.
2. Hydrofluoric acid 1 : 1 diluted with D. I. Water.

B. Equipment

1. Ventilated hood with acid sink
2. Timer
3. Teflon fixture
4. Teflon beaker
5. Metallurgical microscope, 100X.

C. Procedure

1. Fill hydrofluoric acid solution in Teflon beaker.
2. Immerse slice for specified time in HF solution.
Typical etch rate, 10 microns per minute.
3. Rinse in running water.
4. Blow dry with nitrogen.

2.19 Substrate Cleaning:

A. Material

1. Etched slice
2. Photoresist stripper J-100 concentrated.
3. Deionized water
4. Dry nitrogen.

B. Equipment

1. Ventilated hood with acid sink.
2. Hot plate.
3. Beaker
4. Timer
5. Metallurgical microscope

C. Procedure

1. Immerse slice in hot J-100 (120° C) for 10 minutes.
2. Rinse in running water for 10 minutes.

3. Boil in D.I. water for 10 minutes.
4. Rinse in D.I. water for 5 minutes.
5. Blow dry with nitrogen.

2.20 Photoresist Apply:

A. Material

1. Clean slices
2. Photoresist KTFR, 100%

B. Equipment

1. Photoresist spinner with speed control and timer.
2. Hypodermic needle.
3. Oven
4. Fixture
5. Timer

C. Procedure

1. Place slice on spinner
2. Apply photoresist with hypodermic needle.
3. Spin at 1200 rpm for 20 seconds.
4. Dry for 15 minutes at room temperature
5. Dry in oven for 15 minutes at 65°C.

2.21 Crossover Mask Alignment and Expose:

A. Material

1. Photoresist coated slice
2. Crossover photomask (see Figure 5)

B. Equipment

1. Mask alignment and exposure system

C. Procedure

1. Select proper mask and place in alignment system.
2. Insert slice under photomask and align to each other.
3. Expose for specified time.

2.22 Photoresist Develop:

A. Material

1. Exposed slice
2. KMER developer
3. KTFR rinse
4. Dry nitrogen

B. Equipment

1. Ventilated hood
2. Tray for KMER developer
3. Beaker for KTFR rinse
4. Fixture
5. Timer
6. Metallurgical microscope.

C. Procedure

1. Immerse slice in KMER developer for 2 minutes.
2. Rinse in KTFR rinse, 5 seconds.
3. Blow dry with nitrogen.
4. Inspect under microscope for complete development and line definition.

2.23 Cr/Au/Cr-Evaporation:

A. Material

1. Powdered chromium, 99.99% Mallinckrodt Chemical Works.
2. Gold wire, .125 inch dia., 99.99%, Wilkinson.
3. Tungsten evaporation boats
4. Photoresist coated slice

B. Equipment

1. Evaporator with controls for temperature, vacuum and thickness of evaporated film.
2. Timer

C. Procedure

1. Load substrate holder with slices
2. Load evaporation boats with chromium and gold
3. Close vacuum chamber, exhaust to 1×10^{-6} torr
4. Refill chamber with argon to a pressure of 10 to 20 microns.
5. Glow discharge for 15 minutes
6. Exhaust to 1×10^{-6} torr
7. Evaporate chromium, 100 Ω /sq.
8. Evaporate gold, .08 Ω /sq.
9. Evaporate chromium, 100 Ω /sq.

2.24 Substrate Cleaning:

A. Material

1. Slice with evaporated crossovers
2. Photoresist stripper, J-100 concentrated.
3. Deionized water
4. Dry nitrogen

B. Equipment

1. Ventilated hood
2. Hot plate
3. Timer
4. Beaker

C. Procedure

1. Soak slice in hot J-100 (120°C) for 30 minutes
2. Swap with cotton
3. Rinse in running water for 10 minutes.
4. Boil in D.I. water for 10 minutes
5. Rinse in D.I. water
6. Blow dry with nitrogen.

2.25 Inspection:

A. Material

1. Cleaned slice

B. Equipment

1. Metallurgical microscope, 100X

C. Procedure

1. Inspect for remaining photoresist. If necessary, repeat step 2.24.

2.26 Dicing:

A. Material

1. Inspected slices
2. Steatite blocks
3. Shellac
4. Methyl ethyl Ketone

B. Equipment

1. Microscope
2. Diamond Saw, The DoAll Company.
3. Ventilated hood
4. Hot plate
5. Beaker

C. Procedure

1. Heat steatite blocks to 150°C and apply Shellac.
2. Place hot steatite blocks under microscope and mount slices to be cut on block. Align slices to grid lines cut into block surface.
3. Select proper spaces for specified distances of diamond blades and mount with diamond blades on arbor.
4. Mount steatite blocks on diamond saw.
5. Cut slices

6. Remove blocks from diamond saw, rinse in running water and blow dry.
7. Place blocks on hot plate. Remove dice as soon as shellac softens and immerse in methyl ethyl Ketone.
8. Rinse in clean methyl ethyl Ketone
9. Blow dry with nitrogen.

2.27 Testing:

A. Material

1. Diced substrates

B. Equipment

1. Microscope
2. Ohmmeter
3. Probing fixture

C. Procedure

1. Inspect visually all substrates for the following defects:
 - a. Continuity of all interconnections
 - b. Continuity of the seal frame
 - c. Residual metal between interconnections
 - d. Imperfections of bumps
 - e. Imperfections of the cross-over metallization.
2. Test each individual crossover for shorts against the undercrossing line.
3. Store mechanically and electrically good substrates in nitrogen-filled container.

3.0 Assembly of the Five-Stage Binary Counter

3.1 Mount Lead Frame to Substrate:

A. Material

1. Inspected substrates
2. Lead frames, Micro Science Ass. see drawing No. μ E-0011, Figure 24.

3. Rosin flux 611, Alpha Metals
4. Flux remover 563, Alpha Metals

B. Equipment

1. Fixture (see Figure 7)
2. Vacuum pump
3. Beaker

C. Procedure

1. Place substrate on vacuum chuck and clamp lead frame on mounting fixture with crossover and the longer contact tips on the same side.
2. Brush rosin flux on substrate
3. Align contact with each other
4. Raise chuck temperature to specified value
5. Press the lead-frame down on substrate and cool vacuum chuck to 160° C.
6. Release clamp and vacuum and insert substrate in flux remover.

3.2 Substrate Cleaning:

A. Material

1. Flux remover 563, Alpha Metals.
2. Acetone
3. Dry nitrogen

B. Equipment

1. Beaker
2. Microscope

C. Procedure

1. Immerse substrate in flux remover, 10 seconds
2. Immerse substrate in acetone, 5 seconds
3. Immerse substrate in clean acetone, 5 seconds
4. Blow dry with nitrogen
5. Inspect with microscope. Ensure that all lead tips are soldered to the pads.

3.3 Ultrasonic Chip Mounting:

A. Material

1. Sub-assembled substrates
2. AO-3 chips, tested.

B. Equipment

1. Ultrasonic flip chip mounter (Hughes Model 2906)
2. Pyrex dish

C. Procedure

1. Set the flip chip bonder to the approximate values:
Clamping force - 550 grams
Ultrasonic power - 6.0
Time - 5.0
2. Place substrate on vacuum chuck of bonder
3. Place AO-3 chips face down on alignment mirror.
4. Align one specified pad of AO-3 chip to the cross hair in microscope and pick up with vacuum nozzle.
5. Move substrate under microscope
6. Align specified bump to cross hair
7. Push button for bonding operation
8. Move alignment mirror under microscope and repeat steps 3 through 6 until all five chips are mounted.
9. Release vacuum. Store assembled module in pyrex dish.

3.4 Reflow Solder AO-3 Chips:

A. Material

1. Ultrasonically mounted modules

B. Equipment

1. Reflow soldering fixture (see Figure 20).
2. Timer
3. Tweezer

C. Procedure

1. Preheat fixture to 150° C
2. Set flow-meter for mixed gas (10% hydrogen, 90% nitrogen) on specified gas flow.
3. Insert sub-assembled module into fixture and locate first chip under gas nozzle.
4. Set timer to 10 seconds and initiate hot gas flow.
5. Repeat step 4 for all chips.
6. Take module out of fixture and store in nitrogen.

3.5 Test Module Electrically:

A. Material

1. Assembled unit

B. Equipment

1. Test fixture
2. Pulse generator, Data Pulse 106.
3. Power supply
4. Voltmeter, 0 to 5 volts.

C. Procedure (see Figure 14).

1. Place unit into jig
2. Define low state (1) .5 to 1.5 volts
Define high state (0) 4.5 to 5.5 volts

	Q	$\overline{Q}$
I	0	1
II	1	0

3. Plug meter into Q1 and the other meter into $\overline{Q}$ 1
Press the reset button. The meters indicate the I condition.
4. Apply single pulse from the generator and note that the conditions alternate.
5. Plug meter in Q 2 and $\overline{Q}$ 2. Press reset button.

6. Apply two pulses from the generator. Note that the conditions change every second pulse.
7. Repeat step 4 for Q 3 and $\overline{Q}3$ through Q 5 and $\overline{Q}5$.
Note that the conditions change with every 4th, 8th, and 16th pulse consecutively.

3.6 Final Package Seal:

A. Material

1. Lid, Micro Science Ass.
2. Assembled unit
3. Tin-lead preforms, 80% Au - 20% Sn

B. Equipment

1. Dix Flat Pack Sealer, Dix Engineering Division.
2. Tweezer

C. Procedure

1. Set Dix Sealer to the following settings:

Timer	0 - 105	Heat	32 - 70
Purge	4 - 20	Release	80 - 104
Pre-heat	10 - 30		
Vacuum	21 - 30	Set Heater at	13
Pressurize	31 - 104		

2. Load lid, solder preform and flat pack assembly (in that order) onto ceramic plate. Use vacuum arm on machine.
3. Press both machine buttons to start automatic sealing cycle.

3.7 Test Mechanically:

1. Temperature cycling, MIL-STD 750 A, Method 1051.
2. Mechanical shock of 300 g's, 1/2 sine wave, 3 milliseconds, MIL-STD-750 A, Method 2016.
3. Constant acceleration of 25,000 g's, MIL-STD-750 A, Method 2006.

3.8 Electrical Testing of Completed Unit (see Figure 14)

Repeat procedure in step 3.5.

Mark units with identification and serial number. (see Figure 23).

Five Bit Binary Counter HUE 0123

Lead Number Assignments:

1. Ground	8. Input, 0- +5V Pulse
2. $\overline{Q5}$	9. $\overline{Q5}$
3. $\overline{Q4}$	10. $\overline{Q4}$
4. $\overline{Q3}$	11. $\overline{Q3}$
5. $\overline{Q2}$	12. $\overline{Q2}$
6. $\overline{Q1}$	13. $\overline{Q1}$
7. Reset	14. V_{cc} , +5 Volts

FIGURE 23. Package Outline

HERMETIC LEAD FRAME - 14 LEADS

NOTE: GOLD PLATING ON ALL
KOVAR PARTS 100 μ inch.

- 4. UPPER GLASS 7059
- 3. BOTTOM GLASS 7059
- 2. LEAD FRAME Ni/Fe/Co .005
- 1. FLANGE Ni/Fe/Co .010

Hughes Aircraft Company
Microelectronics Laboratory
Drawing No. μ E-0011

FIGURE 24. Drawing of Lead Frame

FIGURE 25. CLEANING FIXTURE

MATERIALS & EQUIPMENT SOURCES

A. MATERIALS

<u>Item</u>	<u>Material</u>	<u>Manufacturer</u>
1	AO-3 Shift Register	Siliconix Inc., Los Angeles, Calif.
2	Al Si Mag 772 Substrates	American Lava, Corp. Chattanooga, Tenn.
3	Lead Frames and Lids	Micro Science Associates Mountain View, Calif.
4	Photoresist	Kodak, Rochester, N. Y.
5	Electroless Nickel Plating	Shipley Comp. Inc., Newton, Mass.
6	Electroless Gold Plating	SEL-REX Corp., Nutley, N. J.
7	99.99% Aluminum	A. D. Mackay, Inc., 198 Broadway New York, N. Y.
8	Chromium	Mallinckrodt Chem. Works, New York.
9	Gold	Materials Research Corp., Orangeburg, N. Y.
10	1723 Corning Glass	Corning Glass Works
11	Photoresist Stripper J-100	Indust-Ri-Chem. Laboratory Richardson, Tex.
12	Aurostrip	MacDermid Inc., Torrance, Calif.

B. EQUIPMENT

<u>Item</u>	<u>Equipment</u>	<u>Manufacturer</u>
1	Evaporators Mod. 3116	NRC, Newton, Mass.
2	RF Sputterer, Mod. SP-210	R. D. Mathis Co., Long Beach, Calif.
3	Photoresist spinner	Headway Research, Dallas, Tex.
4	Mask Alignment System Mod. 500	Electroglass, Van Nuys, Calif.
5	Ultrasonic Cleaner	Westinghouse
6	Flat Pack Sealer	Dix Engineering Div., Costa Mesa, Calif.
7	Flip Chip Mounter Mod. 2906	Hughes Aircraft Co., Newport Bch, Calif.
8	106A Pulse Generator	Data Pulse, Inglewood, Calif.
9	Diamond Saw	The DoAll Comp., Des Plaines, Ill.
10	Oven	National Appliance Corp., Portland Oregon
11	Metallurgical Microscope	Reichert, Austria.

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