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INFORMAL REPORT

EPICS Bifilar Helical Chamber Interface Electronics and Data Acquisition System

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UNITED STATES
ATOMIC ENERGY COMMISSION
CONTRACT W-7408-ENG. 36

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Printed in the United States of America. Available from
National Technical Information Service
U. S. Department of Commerce
5285 Port Royal Road
Springfield, Virginia 22151
Price: Printed Copy \$4.00; Microfiche \$0.95

LA-5310-MS
Informal Report
UC-37

ISSUED: July 1973

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by

J. D. Nickell

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EPICS BIFILAR HELICAL CHAMBER INTERFACE ELECTRONICS
AND DATA ACQUISITION SYSTEM

J. D. Nickell

ABSTRACT

This report describes a recently developed electronics system that will be used to read out data retrieved from a multiwire bifilar helical chamber. Information processed by the chamber interface electronics will be transmitted to a CAMAC data module where it will be retained until an FNA command demanding readout is received. A CAMAC test module is also included in the system to facilitate dynamic testing of the amplifiers, discriminators, and the chamber interface electronics coding. Each of the three units comprising the system is described separately herein.

<u>Section</u>	<u>Title</u>
I	EPICS Bifilar Helical Chamber Interface Electronics
II	EPICS Bifilar Helical Chamber CAMAC Data Encoder
III	EPICS Bifilar Helical Chamber CAMAC Test Module

EPICS BIFILAR HELICAL CHAMBER INTERFACE ELECTRONICS

I. INTRODUCTION

A. General Description

The EPICS Bifilar Helical Chambers consist of two insulated arrays of wire planes in close proximity to, but insulated from, each other. One plane forms a bifilar helical transmission line (cathode wires) tapped at 2-cm spacings and surrounds the second wire plane (anode). In this configuration, nearly equal charges of opposite polarity are induced in the cathode and anode wires.*

Each wire is assigned a preamplifier, adjustable threshold differential comparator, and a count rate meter. The output of the comparator is sent to (1) the count rate meter for rate measurements and (2) the Helical Chamber Interface Electronics for data processing.

The Helical Chamber Interface Electronics (see Fig. 1 for block diagram) will process data received from the preamplifiers and output digital information pertaining to the physical location of the event in the chamber. This digital information will be shipped to a Data CAMAC module (one for each chamber) for interface with the analysis software electronics. A separate CAMAC module is utilized for preamplifier testing and for collecting event fault information for up to four chambers.

The first Bifilar Helical Chamber will be constructed with 14 cathode taps and 62 anode wires. Subsequent chambers of larger arrays are planned; and with this in mind, the design of the Interface Electronics is such that expansion to handle the larger chamber may be accomplished with minimal changes, primarily addition of storage registers.

B. Electrical Operation (Interface Electronics)

The data from the preamplifiers responding to the event are stored in the appropriate EVENT REGISTER ('20 nsec setting time allowed) and held pending receipt of an External Accept (EXT ACPT) signal from the external EPICS fast logic. This signal signifies that the event has been deemed "good" by the EPICS logic. If no EXT ACPT is received within a predetermined time (~1 μ sec), a reset signal is automatically generated to clear all registers and prepare the electronics for new event data.

Assuming receipt of EXT ACPT, data will be clocked from the event holding registers and processed to yield information pertaining to: event location (wire and tap number), event magnitude (number of wires and taps effected), fault conditions detected (cathode event but no anode event, event magnitude too great, and/or multiple events detected), EPICS TAC stop, processor BUSY,

* "A Bifilar Helical Multiwire Proportional Counter for Positive Sensitive Detection of Minimum Ionizing Particles," D. M. Lee et al, LA-4968-MS.

and an event data ready for read out signal. This information will be interfaced with analysis peripherals via CAMAC control. Any additional data received subsequent to EXT ACPT will be locked out of the EVENT REGISTERS by the updated BUSY signal.

Software necessary to perform preamplifier and logic testing is incorporated in the chamber Interface Electronics and will be under the command of a separate Test CAMAC unit so that testing of the chamber electronics may be performed whenever event data are not being handled.

II. THEORY OF OPERATION

The following is a detailed description of the operation of the chamber Interface Electronics and will require reference to the detailed schematics of the unit (63Y-149594) or the block diagram, Figure 1.

A. Anode Event Data Handling (Sheets 1, 2, 3, 4 and 5)

1. Singles Event OR, SOR

Signals from the preamplifiers (W1 through W62) are buffered and ORed together (SOR1 through SOR8) to form a singles event OR signal, SORH*, the SOR signal is shaped to produce 80 nsec SORDH and SORDL signals. (This width is adjustable from 40 nsec to 500 nsec.) These shaped signals are used for several primary functions:

a. SORDH

If the chamber electronics is not busy processing data from a previous event, SORDH produces GATE 1 through GATE 4 enabling the transfer gates. The data that occurs on the anode wires during this 80 nsec window are directly set into storage registers (parallel entry).

The SORDH signal is also buffered with a TTL to NIM level translator which is capable of driving 250 feet of RG-213 coaxial cable and presenting a signal with a 5-nsec rise time to the EPICS logic for dead time measurements and count rate information. A schematic of this level translator is shown in Fig. 2.

b. SORDL

Initiate a timing cycle used to generate BUSY which inhibits entry of subsequent data into the EVENT REGISTERS.

Signals involved in producing BUSY and the master reset signal RSTDH (and RSTDH) are: ACPTL, SORDL, SORDLR, SORD2LR, UPDTH, UPDTL, and UPDT2L. These signals are generated by one-shots and determine the time necessary to wait for the external EPICS logic to

* Signal names generally indicate the "true" state of the dynamic signal i.e., SOR H is high true and SOR L is low true - either is related to SOR.

return an EXT ACPT signal. If no EXT ACPT signal is received within approximately 1000 nsec, RSTDH and RSTDH are generated and all data are cleared from memory. Figure 3, BUSY and RSTD Timing Relationship, shows the timing relationship of these signals with respect to SOR.

As indicated in Figure 3, if the EXT ACPT is received within the 1000-nsec time interval, BUSY is extended until all data have been processed, read out to the Data CAMAC, and the External Reset (EXT RST) received.

2. External Accept and Data Collection

The EPICS fast logic system will receive data from the Interface Electronics (SORD), scintillators, and Cherenkov counters in order to determine the validity of any particular event. Upon accepting an event for complete analysis, an external accept (EXACPT) trigger will be generated by the EPICS fast logic and will be transmitted to the chamber Interface Electronics to initiate data analysis of the event that produced the related SORD signal. Any subsequent events will be locked out by BUSY while the Interface Electronics is waiting for the EXT ACPT or the 1000-nsec timeout reset signal as described previously.

The EXT ACPT signal (Sheet 1) is buffered and used to produce ACPH and ACPTL signals. ACPH is used to synchronously enable the 20-MHz clock (to insure gating a full clock width into the system) via AENBL and produce the anode data clock CT (Sheet 2). Clock CT is buffered to produce SHFCL1 through SHFCL4 which clock the data serially from the anode event holding registers (Sheets 4 and 5). Clock CT is also counted by a divide-by-128 scaler to determine the wire location (WLⁿ) of the anode event and also counted by a divide-by-16 scaler to determine the number of (parallel) wires involved in the event (WWⁿ). (In both cases above, "n" represents $2^0, 2^1, \dots, 2^n$, where "n"=4 for the WW scaler and "n"=7 for the WL scaler.)

By examining the data outputted from the anode event holding registers' bit 1 and bit 2 lines (Z1Q and Z2QL), the readout control flip-flop is directly set (AHITL) at the end of an event group producing ROA (read out anode) and ENDL. The CT clock is momentarily stopped by ENDL and the accumulated data are held awaiting readout upon command from the Data CAMAC (to be discussed more fully later).

The WWⁿ scaler has the capability to recognize an event involving up to eight wires wide. Upon scaling to the count of eight, the WWFLT (wire width fault) line goes true and inhibits any further counting by the WWⁿ scaler. The WWFLT bit is ORed with TWFLT and used to directly set the FAULTL flip-flop (Sheet 6). The FAULTL bit is routed to the Test CAMAC module where fault data for up to four chambers is accumulated. Note that the WLⁿ scaler is reset only by the master reset signal RSTDH, whereas the WWⁿ scaler is reset by the intermediate reset ARSTH and/or RSTDH (except where a fault has been detected in which case only the master reset,

RSTDH, can reset the scaler). This reset scheme is used in order to preserve WL information in the advent of additional event data readout while WW must be reset for each and every readout.

The ROA signal that occurred at the conclusion of the anode event analysis period is ANDed with its cathode counterpart, ROC, to generate a readout data signal (ROD) which initiates a data readout cycle to the chamber Data CAMAC. Upon receipt of the Read Accept signal (RACPTH) from the Data CAMAC module indicating that all data has been received, the CT clock is again enabled and a search is initiated for any other event data received from the chamber. (See paragraph B.5 for a detailed description of the re-start technique.)

The output of the WL scaler is decoded; and at a predetermined count (64 or 128 depending on the number of cathode wires in the helical chamber), the CT clock is stopped and ROA set high to initiate a final readout cycle as described above.

3. Output Multiplexer, Data Transfer to CAMAC

The data communicated between the Data CAMAC and the computer used to analyze Helical Chamber data consist of two words, each containing 16 bits of information. In order to communicate the Helical Chamber event data to the Data CAMAC module in the most efficient manner, i.e., number of physical lines re transmission time, a two-word, 11-bits per word format was chosen. Figure 4 shows the format of the CAMAC and the Interface Electronics event data words.

In order to accomplish this encoding scheme, the 11-bit data multiplexer (Sheet 8) in the Interface Electronics is first loaded with anode event data (assuming reception of an EXT ACPT signal from EPICS). The reception of ROD (readout data) by the Data CAMAC causes the anode data on the Data CAMAC input lines to be entered into the first word holding registers located in the Data CAMAC. Simultaneously, the Data CAMAC sends a READ ACPT handshake signal back to the Helical Chamber Interface Electronics. This READ ACPT signal is buffered and used (THCL) to enter data into the cathode event temporary storage registers and hence to the data multiplexer. This data will be sent to the Data CAMAC after the extra bit information has been extracted from the next analysis period. The Data CAMAC operation is explained in more detail in Paragraph II.B.4, Cathode Event Data Holding Registers and in the Data CAMAC report, MP-1-3302.

B. Cathode Event Data Handling (Sheets 6, 7, 8 and 12)

1. Cathode Event Data Multiplexer (Sheet 7)

Data from the helical wire tap preamps are handled in a different manner than data from the anode preamps. In order to prevent multiple bit detection in the cathode array, data are clocked into holding registers (SETA, SETB or SETC) within 20 nsec of the leading

edge of SOR. The cathode signals are then ORed in a similar manner to the anode except that the preamplifier signals are "combed" so that the signals from every third preamplifier (tap) are grouped to form the cathode singles event OR (AORL, BORL, and CORL which produce TACA, TACB, and TACC, respectively). This technique is used in order to make use of the delay characteristics of the helical line (25 nsec per cm) to determine the location of the event by time of flight measurements. The measurement is initiated by the EPICS equivalent of the anode SOR and stopped by the cathode singles OR, TACA, TACB, or TACC. Figure 5 is a simplified schematic of one of the three storage registers and its control signals. Figure 6 contains timing relationships of the cathode signals concerning event identification, timing, and storage register control.

2. MUX "Combed" Clock Generation (Sheet 6 and 7)

The ACPH signal from the EPICS logic is used to synchronously enable the 20-MHz clock as described previously and the cathode data master clock (COUNTL) is produced. This master clock is ANDed with the outputs of a Johnson counter (which provides enabling signals CTA, CTB, and CTC) to produce the "combed" multiplexer clocks CLKA, CLKB, and CLKC, which are used to shift the data from the cathode storage registers. Register output data are buffered for time coherence, ANDed with CT n+1 and COUNT, and the result ORed with the same type resultant from the other two registers. The ORed signal (TWCL) is digitized event data and therefore can be counted by the width scalars to produce event width information directly.

3. Cathode Event Identification

The method of identifying an event on the cathode plane is similar to that used in the anode section except that since data result from a multiplexed register output it must be handled in a different manner. The digitized event data (TWCL) is exclusively ORed with a delayed master clock signal (COUNTD) to produce HITEND which directly sets the ROC flip-flop generating TENDL to momentarily stop the COUNT clock and produce the readout cathode signal (ROC). Because of this detection scheme, two more COUNT pulses are derived for the first event than is really indicative of the tap number.

In order to subtract these extra clock pulses that occurred after the end of the event group and maintain the correct count in the tap location register (TL"n"), a toggle flip-flop controls the state of the first TL"n" register by using the CTC enable pulse to parallel enter zeros into the register before allowing the successive clocks to be counted. This technique maintains the correct count by effectively subtracting two counts.

The operation of the tap location scaler and the tap event width scaler (TAPW"n") is otherwise the same as described in Paragraph II.A.2 for the anode event logic. The location scaler can accumulate up to 256 counts with a predetermined STOP at any

intermediate count and the TAPW scaler can accumulate up to eight counts before being paralyzed by a fault (TWFLT) condition (>8 taps involved in the event group).

4. Cathode Event Data Temporary Holding Registers (Sheet 8)

Because of the possibility of occurrence of multiple events and the disclosure of such made available in the second data word to the Data CAMAC, a holding register is incorporated which is used to temporarily hold the cathode n^{th} event data while searching for the $n+1^{\text{st}}$ event. Upon transmitting a readout data (ROD) signal to the Data CAMAC and receiving a READ ACPT back, cathode data accumulated from an event are toggled into holding registers and held while the anode and cathode primary scalers are being used for the next data search. If additional data are detected, an extra hit bit (EXHIT A and/or EXHIT C) is set and directly sent to the data multiplexer, cathode word bits 11 and 12, respectively.

Upon conclusion of the "next data search," a ROD signal is generated; sent to the Data CAMAC, and used by the CAMAC module to strobe in the second word containing the cathode event data and extra hit notification bits just obtained.

Figure 7, System Timing, shows the timing relationship of signals communicating between the Interface Electronics and the Data CAMAC during the first event data readout, the READ ACPT handshake, and the second event analysis and readout. A description of major activities and logical states of major controls is also included to aid in clarification of the events occurring at this time.

Figure 8, System Timing-Action, Reaction; contains the same basic information as does Figure 7 except presented in a different manner. Figure 8 shows the reaction of control signals involved in transmitting data to and from the Data CAMAC module.

5. Data Clock Re-Start

Upon receipt of the Read Accept signal (RACPTH) from the Data CAMAC module indicating that all data have been received, the CT clock (anode logic) and the COUNT clock (cathode logic) are synchronously re-started re., the 20-MHz master clock. This will ensure gating a full clock width pulse into the system eliminating any possibility of partial clock pulses toggling 75Sxx logic while standard speed logic might not respond to the same clock pulse.

Figure 9 shows the logic and timing relative to the anode re-start logic and Figure 10 the cathode re-start logic and timing.

C. Auto-Testing Capability (Sheets 13 and 14)

In order to test efficiently the 62 wire anode and the 24 tap cathode preamplifiers, data handling registers, output registers and controls, and Data CAMAC operation, a Test Pulse will be generated within the Inter-

face Electronics unit. This Test Pulse will be in the order of 100-nsec wide and occurrence will be controlled by a special Test CAMAC module. This test module is described in detail in Section III of this report entitled "EPICS Bifilar Helical Chamber CAMAC Test Module."

A special NIM to TTL level translator is required to receive the Test Pulse from the Test CAMAC module. This level translator is shown in Figure 11 NIM to TTL Level Translator.

Briefly, the Test CAMAC will issue (by command) Test Enable, Test Pulse, and Test Increment signals. The Test Pulse signal is transmitted from the Test CAMAC module to a particular Helical Chamber Interface Electronics unit over type RG-213/U coaxial cable, whose length has been adjusted such that test pulses will arrive at each chamber unit within a very few nanoseconds of each other (TAC calibration). The Test Enable signal enables the Test Pulse reshaping one-shot in the Interface Electronics that distributes the actual Test Pulse to be used to the wire or tap pre-amplifier steering (decoding) logic. The Test Increment signal selects the wire or tap preamplifier to be tested by incrementing a divide-by-128 scaler to the anode wire preamplifier number or the cathode tap preamplifier number.

Figure 12, System Test and Fault Data Collection - Block Diagram, illustrates the scheme of interconnecting the Test CAMAC module to four Helical Chamber Interface Electronic units.

III. Summary

A. General

The Helical Chamber Interface Electronics is designed to receive positive going, 100 nsec, TTL level signals from the preamplifier/discriminator units which amplify and shape signals received from a Bifilar Helical Chamber. These signals signify that an ion-pair occurring within the chamber has induced a charge in an anode and/or cathode wire. In order to physically locate the position of this occurrence in the chamber, each anode and cathode signal is independently amplified and processed to yield information describing:

1. Linear Location - anode and cathode plane
2. Width (spread) of Event - number of adjacent wires - anode and cathode plane
3. Fault Condition - anode/cathode width >8 wide, anode but no cathode data retrieved, multiple event recorded.

Upon receiving signals from the preamplifiers, an anode event singles OR (SOR) signal, a BUSY signal, three independent TAC stop signals are generated from the cathode singles ORs, and all data relative to the anode event SOR timing will be stored. The logic will now await reception of an External Accept signal from the EPICS fast logic signifying a good event was detected (concurrent with the anode SOR). If no accept signal is received within 1000 nsec (electrical time from chamber to EPICS logic and back to

chamber) an automatic reset is accomplished and all data destroyed. If the accept pulse is received within the allotted time, data processing starts.

Two new CAMAC modules were developed for interface between the Helical Chamber Interface Electronics and analysis software. The purpose of these CAMAC modules is data handling and auto-testing.

B. Physical Dimensions

The Helical Chamber Interface Electronics is contained on four CASH cards, two each 24 socket and two each 96 socket arranged about the chamber as shown in Figure 11, Physical Layout - Helical Chamber and Interface Electronics. Overall dimensions are also indicated on Figure 13 for a 62-wire chamber, support frame and input/output connector panel.

C. Electrical Requirements

Electrical power requirement for one Helical Chamber Interface Electronics unit (excluding preamplifiers and CAMAC modules) is:

+5.0 $\pm$.25 Vdc at 4 A*

-5.0 $\pm$.25 Vdc at 1 A

* NOTE: Power for approximately 200 each 74Sxx integrated circuits at 100 MW per integrated circuit.

# Cables	R1	R2
1	91 Ω	110 Ω
2	47 Ω	56 Ω

Fig. 2. TTL/NIM Level Translator.

Fig. 3. BUSY and RSTD Timing Relationship.

Fig. 4. Data Word Format.

Fig. 5. Simplified Schematic--Cathode Storage Registers.

Fig. 6. Cathode Event Data Control Signals--Timing.

Fig. 7. System Timing.

A = Anode

C = Cathode

F/F = Flip-flop ("Q" state)

▶ = Signal transmission to CAMAC module

◀ = Signal transmission from CAMAC module

Fig. 8. System Timing--Action/Reaction.

Fig. 9. Clock Restart--Anode.

Fig. 10. Clock Restart--Cathode.

Fig. 11. NIM/TTL Level Translator.

Fig. 12. System Test and Fault Data Collection.

J1 thru J5: Type "N" UG-58 A/U

J6 : Burndy MS 3126E-12-3P (3 pin)

J7 : Burndy MS 3127E-24-61S (61 pin)

Fig. 13. Physical Layout--Helical Chamber and Interface Electronics.

EPICS BIFILAR HELICAL CHAMBER CAMAC DATA ENCODER

1.0. PURPOSE

This CAMAC module is intended to accept two each 11-bit words from the EPICS Bifilar Helical Chamber Interface Electronics and place the data on the Dataway R-lines upon command. Handshake signals communicate the module status to the Interface Electronics in order to accomplish a synchronous data exchange.

2.0. DESCRIPTION

The module is a two-wide unit utilizing a special printed-circuit card for Dataway interface (63Y-149530) and CASH hardware mounting. TTL logic is used for circuit implementation.

2.1. Input and Output Signals

The input/output signals fall into three classifications:

2.1.1. Dataway R-lines

Up to 2 words, each consisting of 12 bits of data, are accepted by type DM8820 balanced receivers and stored in type SN7475 flip-flops. Upon receiving the appropriate FNA command, either word one or word two data bits are placed on the dataway R-lines. Figure 1 shows the data word format of input and output data.

2.1.2. Control Signals

Control signals sent to the Interface Electronics are:
1) External Reset and 2) External Accept.

The External Reset signal is generated by FNA commands [F(2) or F(9)] or front panel push button. The signal is transmitted over a twisted pair by a type DM8830 balanced driver (as are all signals going to the Interface Electronics).

The External Accept signal is received from the EPICS fast logic via front panel LEMO connector. The signal is received as a NIM level signal, converted to TTL level, and shipped to the Interface Electronics over a twisted pair line as described above.

2.1.3. Handshake Signals

In order to ensure that input data from the Interface Electronics is present on the input lines and has had sufficient settling time, a Read Out Data (ROD) signal is received by the CAMAC module along with the data. This ROD signal is delayed (~100nsec) and used to enter the data into the Word One storage registers. The trailing edge of the ROD signal changes the state of the LOAD steering flip-flop and returns READ ACCEPT signal to the Interface Electronics. This READ ACCEPT signal causes the Interface Electronics data multiplexer to place Word Two on the data lines (along with a new ROD) and hence entered into the CAMAC module Word Two registers as described above.

A more detailed description of the entire data handling technique is presented in Paragraph II.B.4. of Section I of this report.

3.0. USED WITH

This module was designed to operate as an integral part of the EPICS Bifilar Helical Chamber readout electronics. Figure 2 shows a block diagram of the readout electronics system and the position of the Data CAMAC in this system.

4.0. CONTROLS

4.1. Indicator Lights

Front panel indicator lights are provided for "N" (module selected), "READ" [F(1) or F(2)] and BUSY. (BUSY indicates that the Interface Electronics is busy analyzing event data.)

4.4. Controls

Front panel control is limited to a manual pushbutton switch that generates a master RESET signal sent to the Interface Electronics.

5.0. CONNECTORS

5.1. Front Panel

Front panel LEMO connectors provide for:

1. External RESET
2. EXTERNAL ACCEPT - NIM signal from EPICS fast logic
3. BUSY - NIM signal to EPICS fast logic
4. FAULT - Bit 12, Word 1 to TEST CAMAC module

5.2. Rear Panel

Printed circuit connectors provide for 1) I/O data to the Interface Electronics and 2) CAMAC Dataway interfacing.

6.0. COMMANDS

6.1. Input Commands (FNA)

6.1.1. $F(1)A(15)$, Read register one (Anode Data)

6.1.2. $F(1)A(13)$, Read register two (Cathode Data)

6.1.3. $F(2)A(n)$, Read and Clear $A(15)$ or $A(13)$

6.1.4. $F(9)A(0)$, Clear Interface Electronics data

6.2. Output Commands

Commands generated by the module and returned to the Dataway for housekeeping purposes are:

6.2.1. $Q, [F(1) + F(2) + F(9)] N$

6.2.2. $X, \left\{ [F(1) + F(2)] [A(15) + A(13)] + F(9) \right\} N$

7.0. DIMENSIONS

The Bifilar Helical Chamber Data CAMAC is a two-wide module using a special printed circuit card for command decoding and mounting of CASH hardware. Figure 3 is a detailed drawing of the module.

NOTE: This module is designed so that the Dataway connector is left registered with respect to the front panel.

8.0. POWER REQUIREMENTS

Power requirements for this module are:

+6.0 Vdc @ 1.2 Amps

9.0. ADDITIONAL INFORMATION

This module was developed for use with the EPICS Bifilar Helical Chamber Readout Electronics and will be used by H. A. Thiessen, D. Lee, J. Amann, and J. P. Egger, all presently associated with the Clinton P. Anderson Meson Physics Facility of the Los Alamos Scientific Laboratory.

Fig. 1. Data Word Format.

Fig. 2. Block Diagram--B.H.C. System.

Fig. 3. Bifilar Helical Chamber Data CAMAC.

EPICS BIFILAR HELICAL CHAMBER CAMAC TEST MODULE

1.0. PURPOSE

This CAMAC module utilizes TTL logic and is intended for use as a Helical Chamber Test Controller for the EPICS Helical Chamber Readout Electronics. Output signals include: (1) Test Enable, (2) Test Pulse, (3) Test (Channel) Increment. Input signals, for insertion in the Dataway Bus, are four fault indications from the four Helical Chamber readouts.

Outputs may be controlled via dataway commands or front panel switches.

2.0. DESCRIPTION2.1. Output Signals

The output signals are as follows:

2.1.1. Test Enable; Enable=F26, Disable=F24 or Z

A high true signal available at the rear I/O connector. Upon receiving N·F26 from the dataway, this output is set high. Upon receiving N·F24, this output is reset low. The signal source is a DM8830 capable of driving a balanced line with characteristic impedance of 50 ohms minimum.

A front panel switch (TEST-ENBL/DSBL) is provided for setting and resetting this output, and an indicator light (TE) is used to indicate the enable state.

2.1.2. Test Pulse, F27

A high true signal of 100 nsec duration available at LEMO type front panel connectors TP1, TP2, TP3, and TP4 when under manual control. When under dataway control, this signal is present whenever commanded by N·F27, the pulse width being determined by the dataway timing. The signal source is of a special design capable of driving up to 300 feet of RG213 cable at AEC NIM signal levels ("0" = -0.7 Vdc, "1" = 0.0 Vdc).

Front panel control is provided for either manual control via a push button switch (TST PL) or through a LEMO connector for external signal operation (switch closure or TTL signal). The front panel controls are operating only when the Test Enable signal has been set high. An indicator light (TP) flashes when a Test Pulse has been generated. (See Figure 1.)

2.1.3. Test Increment, F25

A high true signal available at the rear I/O connector. When under dataway control, this signal is present whenever commanded by N·F25 and the width is determined by the dataway timing. The signal source is a DM8830 capable of driving a balanced line with characteristic impedance of 50 ohms minimum.

Front panel control is provided for either manual control via a push button switch (TST INC) or through a LEMO connector for external signal operation (switch closure or TTL signal). The signal width is determined by the activating source.

2.2. Input Signals

Normal data input signals consist of Helical Chamber FAULT data. This signal is low true and is inserted at one of four front panel LEMO connectors. Upon receiving a F1 command, type N8881 transfer gates present the FAULT data received to the Dataway as bits R1, R2, R3, and R4. These inputs are designed so that no connection to an input will transfer a binary "0" to the Dataway.

3.0. USED WITH

This module is to be used to implement test control and collection of fault data when interfaced with the EPICS Helical Chamber Readout Electronics.

The Test Enable and Test Increment signals are of relatively long duration ($>1\mu\text{sec}$) and therefore are carried to the Readout Electronics via approximately 250 feet of twisted-pair transmission line. These two signals are used to enable a transmission gate and increment a decoder so that timing (rise, fall, or relationship to the Test Pulse) is not critical within the limits of the intended module usage.

The Test Pulse, however, is required to arrive at each Helical Chamber so as to simulate an event (particle) and must be transmitted over coaxial cable with good frequency characteristics in order to preserve the integrity of the pulse. Special drivers were designed for another project that translated TTL level pulses to AEC NIM levels with the capability of driving one or two 50-ohm (RG213) cables a distance of 250 feet and maintain a rise and fall time of $\leq 5\text{ nsec}$. These drivers were used in this module and provide the Test Pulse output signals present on the front panel LEMO connectors. One driver is provided for each output but a common signal source generates the Test Pulse for the driver inputs.

The Fault inputs are received from CAMAC modules which interface directly with the Helical Chamber Readout Electronics. The Fault signals received are from low true open collector sources and therefore have $1\text{ k}\Omega$ pull up resistors provided. Upon receipt of a readout command (NF1) the Fault data received is gated onto the Dataway for the duration of the read command.

A schematic of the TTL/NIM drivers is shown in Figure 2.

4.0. CONTROLS

4.1. Indicators

Front panel indicator lights are provided for "N" (module selected), "TP" (Test Pulse Generated) and "TE" (Test Enable true).

4.2. Controls

Front panel controls provide manual control of:

1. Test Enable, Enable and Disable
2. Test Pulse initiation
3. Test Increment generation

5.0. CONNECTORS

5.1. Front Panel

Front panel LEMO connectors provide for:

1. External source, Test Pulse initiation
2. External source, Test Increment generation
3. Test Pulse output (four each)
4. Fault Data input (four each)

5.2. Rear Panel

A rear I/O printed circuit connector containing the Test Increment and Test Enable signals and a Dataway printed circuit interface connector.

6.0. COMMANDS

6.1. Input Commands

The following commands from the Dataway are required for operation.

- 6.1.1. F1 , Fault Data Readout
- 6.1.2. F25 , Test Increment
- 6.1.3. F26 , Test Enable "Set"
- 6.1.4. F24 , Test Enable "Reset"
- 6.1.5. F27 , Test Pulse
- 6.1.6. Z , Initialize

All the above commands must be accompanied by "N," module station selected.

6.2. Output Commands

Commands generated by the module and returned to the Dataway for housekeeping purposes are:

- 6.2.1. Q , (TEST ENABLE·F27) + F1 + F24 + F25
- 6.2.2. X , Redundant Q
- 6.2.3. R1 , Chamber 1 Fault·F1
- 6.2.4. R2 , Chamber 2 Fault·F1
- 6.2.5. R3 , Chamber 3 Fault·F1
- 6.2.6. R4 , Chamber 4 Fault·F1

7.0. DIMENSIONS

The Helical Chamber Test Controller is a two-wide CAMAC module using a special in-house printed circuit card for the command decoding and house-keeping data IC's. Provisions are made for mounting CASH cards to this printed circuit card for implementation of the system logic. Figure 1 is a detailed drawing of the front panel of the module.

NOTE: This module is designed so that the Dataway connector is left registered with respect to the front panel.

8.0. POWER REQUIREMENTS

Power requirements for this module (from a standard CAMAC crate) are:

+6.0 Vdc @ 600 mA

-6.0 Vdc @ 150 mA

9.0. ADDITIONAL INFORMATION

This module was developed for use with the EPICS Helical Chamber Read-out Electronics and will be used by H. A. Thiessen, D. Lee, and J. P. Egger, all presently associated with the Clinton P. Anderson Meson Physics Facility of the Los Alamos Scientific Laboratory.

10.0. DETAILED DESCRIPTION

10.1. Command Decoding and Housekeeping Data

This portion of the module is straightforward and uses a pair of 74154 (4-line-to-16-line) decoders to decode the function commands and subaddresses. Housekeeping data (Q and X) are sent to the Dataway via N8881 open collector IC's.

10.2. Test Enable Generation

Integrated circuits 1-3 (7410, Sections 1 and 2) are arranged to form an R-S flip-flop. "Set" is accomplished by either F26 or the TEST, ENBL/DSBL switch through an R-C differentiating network. The "reset" is accomplished by F24, Z, or the TEST, ENBL/DSBL switch. The R-C network associated with the SET/RESET is unbalanced with a larger value of "C" in the RESET line. This is done so that when the TEST switch is in the DSBL position and power is applied the R-S flip-flop will come up in the reset state.

10.3. Test Pulse Generation

When the Test Enable is manually set high, the Test Pulse one-shot is enabled so that an external signal (via the LEMO connector) or the front panel TST PL switch will generate a Test Pulse. Both the external signal and the push button switch are buffered through a 7413 Schmidt Trigger to prevent multiple pulsing caused by switch contact bounce or noise. The F27 command will generate a Test Pulse directly regardless of the manual TEST-ENBL/DSBL switch position. Pulse width output resulting from the F27 command is determined by the Dataway timing.

Provisions are made for external signal input to initiate a Test Pulse. This signal is in parallel with the front panel switch and is provided with a 1 k Ω pullup resistor and takes advantage of the Schmidt Trigger noise protection effect.

10.4. Test Increment

Generation of the TEST INC is via a front panel switch, F25 command, or an external signal source. The front panel switch and external signals are buffered with a Schmidt Trigger as described above.

10.5. Fault Data Readout

The Helical Chamber Fault signals (low true) are received by front panel LEMO signals, supplied with 1 k Ω pullup resistors and buffered with 7404 type invertors. When command F1 is received, the Fault data is transferred to the Dataway via open collector N8881 transfer gates.

10.6. Indicator Lights

Indicator lights (N, TP, and TE) are HP 5082-4403 LED's. The "N" and "TP" indicators are driven by 74123 type one-shots with approximately 6-msec pulses. The TE indicator is driven directly from the Test Enable R-S flip-flop since the TE signal is of long duration.

Fig. 1. Helical Chamber Test CAMAC Panel.