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MAGNETIC CORE MEMORY FOR A
NUMERICAL CONTROL SYSTEM

T. L. Williams

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OAK RIDGE Y-12 PLANT
OAK RIDGE, TENNESSEE

prepared for the U.S. ATOMIC ENERGY COMMISSION
under U.S. GOVERNMENT Contract W-7405 eng 26

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Printed in the United States of America. Available from
National Technical Information Service
U.S. Department of Commerce
5285 Port Royal Road, Springfield, Virginia 22151
Price: Printed Copy \$4.00; Microfiche \$0.95

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**MAGNETIC CORE MEMORY FOR A
NUMERICAL CONTROL SYSTEM**

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Date Issued - July 11, 1973

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Prepared for the U.S. Atomic Energy Commission
Under U.S. Government Contract W-7405-eng-26

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ABSTRACT

A magnetic core memory system was developed for use on a continuous-path numerical-control system. The memory is used as a part description data source instead of punched tape. This modification was made in an effort to determine if problems associated with the controller are directly related to the tape reader. The memory is interfaced to the controller in a manner such that part description data can flow from numerical control to memory for storing data or from memory to numerical control for normal machine control. Memory systems were installed on a two-axis and a four-axis controller. These machines are in regular production and are functioning satisfactorily.

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SUMMARY

There is a consensus of opinion among some Y-12 Plant personnel that many problems associated with numerical control system failures are directly related to the punched tape reader that is used as an input medium for part description data. In an effort to minimize these problems, a magnetic core memory was interfaced to a numerical control (NC) system to replace all of the functions of the tape reader. Data are originally stored in the memory from the NC under tape-reader control. After this, the reader is disabled and all successive operations are programmed from the memory. The memory system is designed to operate from any Bendix 1000 series controller and has a maximum tape capacity of 1,092 feet. This capacity can be reduced by eliminating core modules with each of the eight modules having a capacity of 136.5 feet.

Memory systems were installed on a two-axis turning machine and a four-axis milling center. These machines are in production and are functioning satisfactorily.

INTRODUCTION

A large percentage of the production malfunctions associated with numerical control machine tool systems originate in the tape reader which transfers part description information from the punched tape to the NC electronics. These problems are due to the mechanical-optical characteristics of the tape reader. Clutches, brakes, and bearings undergo wear which results in mechanical breakdowns. Foreign particles, mainly dust and oil, cause reading errors. Some other problems associated with the reader are Mylar tape wear, critical optical alignment, and electrical interference produced by the reader's brakes and clutches.

In an effort to circumvent these difficulties, a magnetic core memory is being used at the Oak Ridge Y-12 Plant^(a) as the operational source of part-description data instead of a tape reader. Part-description information is stored in the memory using the NC's tape reader as its input. The reader is then disabled, and all subsequent operations originate from the memory. This mode of operation is continued until it is desired to machine a different part, which necessitates reloading the memory. Since the reader is only used to initially load the memory and is never used while machining, most problems associated with the reader are eliminated.

An interface unit (IU) controls memory functions and the flow of data from NC to core or core to NC. The IU presents the core in a manner such that it duplicates the tape reader. This action is accomplished by using the tape forward and reverse signals (tape movement commands) to control the state of an up/down counter which is used to address particular locations within the core. With this arrangement, the only NC modifications that need to be made are those needed to route the tape-reader data to the memory and memory data to the NC.

(a) Operated for the US Atomic Energy Commission by the Union Carbide Corporation's Nuclear Division.

NUMERICAL CONTROL - CORE MEMORY SYSTEM

BASIC PROBLEM

It is theorized that a large portion of machine-tool malfunctions occur because of data-input errors originating at the tape reader. A good indication of its problems can be obtained by observing the reader repair rate compared with the remainder of the machine-tool control system. Maintenance personnel have indicated that this requirement is more than 25 percent for several recently installed machine control units and even higher for some older-model controllers. This one repair rate indicates that the tape reader is the weakest link in the NC machine tool system. The reader's basic problem lies within its mechanical-optical nature. The brakes, clutches, and bearings associated with the tape movement wear with time and have to be periodically replaced. Brakes, clutches, and spooler motors are electrically operated and introduce electrical interferences which can cause malfunctions within the NC electronics. Alignment of the optics is critical and cannot be accomplished in a shop environment. The photodiodes used for detecting the tape information differ in electrical characteristics. Each time they or their associated amplifiers are changed, it is necessary to perform a calibration procedure to ensure proper tape operation. Their optical nature also leaves them vulnerable to dust particles and oil films in the optic path.

Any economical solution for minimizing these problems would add to the reliability of the NC machine tool systems while reducing the cost of maintenance. One such solution is the use of a magnetic core memory as the input device instead of the tape reader. This component eliminates all optics and mechanics except when initially loading a part description into the memory. The cost of the memory depends on the maximum tape length needed to be stored in the memory. The most involved case in the Y-12 Plant was found to require approximately 250 feet of tape (for two-axis machines only) which is equivalent to a memory capacity of 30,000 eight-bit words, or:

$$\begin{aligned}\text{Memory Capacity} &= \text{Tape Length} \times \text{Inches/Foot} \times \text{Characters/Inch} \\ &= 250 \times 12 \times 10 = 30,000 \text{ Characters.}\end{aligned}$$

The cost of this memory (32K x 8 bits is standard) plus interface is approximately \$6,000, compared to the tape reader cost of \$3,500. For shorter tapes (< 133 feet), a memory capacity of 8K x 8 bits can be used and reduce the cost to \$4,000. Even with the larger-sized system, core memories can be economically justified through less machine downtime, less maintenance cost, greater speed, and the fact that the memory is good for the life of the NC unit, which is not the case for the tape reader.

A system of this nature was designed using an Ampex 1885 core memory⁽¹⁾ interfaced to a Bendix 1800⁽²⁾ two or four-axis NC unit. Shown in Figures 1 and 2, the system can either operate from the tape reader or the memory, depending on the status of the tape-control switch. The interface allows information to pass either into the memory from the tape reader or from the memory to the NC input logic. When the tape control switch is in the "run" position, the machine receives information from the tape reader. In this mode, reader information is also fed to the memory where it is stored for later use. To operate the system from memory requires that the tape control switch be in the "load" position. Here, the reader is completely disabled and the memory is used as the part description source.

Figure 1. CORE MEMORY SYSTEM.

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SYSTEM COMPONENTS

Bendix 1000 Series Two and Four-Axis Controllers

A numerical control system, of which there are two types (point to point or continuous path), is a method of controlling the motions and operations of a machine tool. In a point-to-point system, the cutting tool is instructed to move from one point to another without regard to the route that the tool takes between these points. With the continuous-path system, as is the Bendix controllers in question, the path of the cutting tool

Figure 2. PRINCIPAL COMPONENTS OF THE CORE MEMORY SYSTEM.

is always under control. The basic 1000 series system provides velocity and displacement control simultaneously for all machine motions. The input data, normally read from a tape reader, contain incremental motion commands, feedrate numbers, and other commands that control such actions as coolant flow, spindle speed, tool compensation, and tool offset. Buffer storage is included to ensure a smooth flow of command as the interpolator concludes one motion segment and starts another. For linear motions, the controller has a standard pulse value of 100 microinches. Other pulse values are available; for example, 20 microinches as is the case for the two-axis system. The standard input medium is a one-inch-wide, eight-channel punched tape that is read by a photoelectric reader. The 300-character-per-second reader is of the latest design using a point light source and fiber optic light distributors for each photodiode light detector. In order to ensure proper data entry, the controller incorporates such features as electronic redundant sprocket, sprocket fault detection circuits, continuous parity check, and block overshoot detection. Detailed information can be found by referring to the manual entitled *Numerical Control System Service Manual Series 1800*.⁽²⁾

Ampex 1885 Magnetic-Core Memory System

The memory system (Figure 3) comprises up to eight 16 kilowords by 9-bit memory modules with power supplies, giving a maximum storage capacity of 131,072 9-bit words. Each basic core memory module is an all-electronic data storage unit using ferrite cores for data storage. Each module (Figure 4) has the capability for read-restore, clear-write, read-modify-write, read-only, and write-only operation. The system utilizes a three-wire coincident-current core array. All logic, addressing, control, and sensing functions are accomplished with silicon integrated circuits. Only the high-current circuitry (for driving the core matrix) uses discrete semiconductors.

Numerical Control-Core Memory Interface

Two main criteria were followed when the interface shown in Figure 5 and in Appendix A, Figures A-1 through A-14, was designed. These were: (1) that no modifications were to be

made to the NC's printed circuit boards, and (2) that the memory was to be completely slaved to the NC. A practical solution was to make the interface look like a tape reader and use the reader input NOR gates located in the NC as data entry points while using the reader control signals for addressing part description data that reside in memory. A block diagram of the resulting unit is presented in Figure 6. Detailed discussions of circuit operation along with schematics and mechanical drawings are contained in the Appendixes.

Address Register - A 17-bit up/down counter is used to address memory locations during both the "read" and "write" memory operations. The counter is controlled by tape-reader control signals generated within the NC and has the capability of addressing 131,072 words of memory.

Memory-to-NC Buffer and Sprocket Generator - Memory data are presented to the interface for 300 nanoseconds along with a data-available signal when a read cycle is requested. This information is stored in interface buffer registers which present the data to the NC for 1.2 milliseconds along with a sprocket signal that is generated within the interface.

NC-to-Memory Buffer and Parity Generator - Seven of the eight tape-reader channels are available from channel registers located in the NC electronics. The remaining channel

Figure 3. COMPONENTS OF THE MODEL 1885 MEMORY SYSTEM. (64K x 18, with Byte Control)

Figure 4. FUNCTIONS OF THE MEMORY MODULE.

Figure 5. NUMERICAL CONTROL/CORE MEMORY INTERFACE.

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(parity) is checked serially and is not conveniently available because of critical timing within the NC. This information is generated in the interface by monitoring the supplied channels with an odd-parity generator. The results along with the other data are fed to the memory through eight buffer gates that are enabled when data are stored in memory.

Memory and Address Register Controller - All functions pertaining to memory operation originate here. By monitoring the NC control parameters, the circuits generate properly timed address register signals along with SOC (read data out of the addressed memory location and then rewrite data back into the same location) and SIC (clear the addressed memory location and write data on the input lines in the same location).

Display System - The memory location that is addressed is displayed on six decades of light-emitting diode (LED) numeric indicators. These units are driven by a six-decade up/down counter that runs in tandem with the binary up/down counter used for addressing memory. Memory data are displayed on a 64-character alphanumeric LED display. Its control is derived from seven channels of memory information that is stored in the display circuits and converted from an EIA to binary code. The display circuits were added to assure the machine operator that the system is functioning, since there are no moving parts as in the tape reader, and to provide maintenance personnel with a troubleshooting aid.

Figure 6. COMPONENTS AND FUNCTIONS OF THE INTERFACE.

SYSTEM OPERATION

The system is designed to provide NC operation from either the tape reader or memory. The operating mode is controlled by the "run-load" switch located on the tape reader. When the switch is in the "run" position, the reader is enabled, the memory output circuits are disabled, and the memory input circuits are enabled. This mode is used to operate from tape or load the contents of the tape into the memory. The latter action is accomplished by depressing the NC's "clear all logic" (CAL) switch which presets the memory address to 512 or 0. Memory locations 0 - 510 were set aside for storage of maintenance programs with those from 512 up for storage of the part description. A switch is provided to enable the section of memory being used. After the CAL is depressed, the "tape forward" switch is energized, starting tape movement. As the NC reads the tape, the data are being stored into memory. This mode of operation continues until the operator observes the tape's last sequence number. At this time he again depresses the CAL switch which stops tape movement and resets the address register to 512. The contents of the tape should now be stored in memory. This action is verified by switching the "run-load" reader switch to "load", disabling the tape reader and memory input circuits while enabling the memory output circuits (in this mode the NC is under memory control), and again initiating a "tape forward" operation. By watching the NC's sequence number display and interface display, the operator can observe that the system is operating. If no NC input fault occurs during this operation, the tape was most likely loaded without error. One further check can be made by searching out each sequence number that is within the part description. If this step is successful, the operator can proceed with full assurance that the memory was loaded correctly.

Operation of the NC from memory is identical to that from the tape. The only difference is that the tape is disabled and the memory provides somewhat faster data retrieval.

CONCLUSIONS AND RECOMMENDATIONS

By replacing the NC's punched-tape reader with a magnetic-core memory for data input, most problems associated with the reader should be eliminated. Memory-versus-tape reader cost for most two-axis applications can be justified and will become easier because of the declining cost of core memory. The two systems that were installed are operating satisfactorily and no operational failures have occurred to date.

For applications requiring more than two memory modules, the core cost becomes a dominant factor. With this requirement, one memory module should be used in conjunction with a cassette magnetic tape recorder where data are read from the recorder into one half of the memory. While machining operations are being performed from the part description that resides in memory, the remaining memory is loaded from tape. After all operations are performed from the first half of memory, the second half is used as the data source and the first half reloaded with the next section of magnetic tape. Under these conditions, as much as 3,000 feet of punched tape can be stored on tape while machining from magnetic core memory.

REFERENCES

- (1) *Ampex 1885 Series Core Memory Systems 3265815-01 REV C3172*; Ampex Corporation, Computer Products Division, Marina del Ray, California.
- (2) *Numerical Control System Service Manual Series 1800*; Bendix Industrial Controls Division, Detroit, Michigan.

ACKNOWLEDGEMENTS

The author wishes to thank C. M. Lay of the Engineering Section, Fabrication Division, for technical assistance during design of the system and J. D. Chapman of the Electronic Systems Diagnostic Repair and Verification Shop, Maintenance Division, for supplying equipment and personnel that enhanced the system troubleshooting.

Figure A-3. NUMERICAL CONTROL MEMORY. (System 2 Printed Circuit's Component Layout)

Figure A-4. NUMERICAL CONTROL MEMORY. (Core Memory 2 Display Printed Circuit Layout - Sheet 1)

Figure A-5. NUMERICAL CONTROL MEMORY. (Core Memory 2 Display Printed Circuit Layout - Sheet 2)

Figure A-6. NUMERICAL CONTROL MEMORY. (Core Memory 2 Read-Write Buffer Printed Circuit Layout)

Figure A-7. NUMERICAL CONTROL MEMORY. (Core Memory 2 Controller Printed Circuit Layout)

NC CORE MEMORY CONTROLLER	NC CORE MEMORY READ/WRITE BUFFERS
NC CORE MEMORY	DISPLAY BOARD

CONNECTOR BLOCK (FRONT VIEW)

VIEW 1-1
W/ FRONT PNL OMITTED

N.C. CORE MEMORY
SYSTEM INTERFACE

Figure A-8. NUMERICAL CONTROL MEMORY. (Numerical Control Memory System 2)

- + NO. 25 (.1495) DRILL - 10 HOLES
- + NO. 30 (.1285) DRILL - 20 HOLES

NOTES:
 1- THIS PANEL SHALL BE PRODUCED
 BY THE PHOTO-METAL PROCESS
 USING $\frac{1}{8}$ " PHOTO SENSITIVE ALUM.

Figure A 0: NUMERICAL CONTROL MEMORY. (Numerical Control Memory System 2 Rear Panel)

Figure A-10. NUMERICAL CONTROL MEMORY. (Read-Write Buffer Schematic - Sheet 1)

Figure A-11. NUMERICAL CONTROL MEMORY. (Read-Write Buffer Schematic - Sheet 2)

Figure A-12. NUMERICAL CONTROL MEMORY. (Read-Write Buffer Schematic - Sheet 3)

BCD ADDRESS DISPLAY REGISTER

Figure A-13. NUMERICAL CONTROL MEMORY. (Core Memory 2 Display Board - Sheet 1)

Figure A-14. NUMERICAL CONTROL MEMORY. (Core Memory 2 Display Board - Sheet 2)

APPENDIX B

DETAILS OF THE NUMERICAL CONTROL/CORE MEMORY INTERFACE OPERATION

Address Register

Access to any memory location is controlled by the memory's address input where 17 bits of binary information are used to address up to 131,072 nine-bit words. The binary address is derived from a 17-bit up/down counter that is controlled by the NC's "tape fwd" (TF), "tape rev" (TR), and $IA \cdot \bar{IB}$ signals (Figure A-10). The TF and TR signals are used to enable either the up-count or down-count gates and $IA \cdot \bar{IB}$, which is generated when the NC finishes its read cycle and either increments or decrements the counter in preparation for the next memory cycle. From Figure B-1 it is seen that a high level at either TF or TR will enable either G1 or G2. After the NC has finished reading the previous character, it will output the $IA \cdot \bar{IB}$ signal that increments or decrements the address register for the next operation.

Figure B-1. ADDRESS REGISTER.

Memory-to-NC Buffer and Sprocket Generator

For proper operation, part description data must be presented to the NC for 1.2 milliseconds (500-characters-per-second input rate). Since memory information is present at the data outputs for very short time periods (Figure B-2), some storage medium must be used. A block diagram of the circuits is given in Figure B-3. Data are strobbcd into eight circuits similar to those shown in Figure B-4 on the fall of memory data available (DA) and allowed to reside there for 1.2 milliseconds by grounding the I2's input for this time duration. The Q output of the storage element is NORed with the NC's manual data. These two signals are then buffered by I3 and fed to the NC input that was previously driven by manual data.

Normally, the NC input circuits will look like either of those shown in Figure B-5. These circuits are modified by removing the + 5 volts from the two-axis controller or manual data from the four-axis controller, NORing with the memory data in the interface, and feeding the two back to the NC, as noted in Figure B-6.

Figure B-4 has two data-out lines coming from the memory. These lines are necessary because of the memory configuration of 18-bit words with byte control for reading either Bits 0 - 8 or 9 - 17. With the wiring configuration of Figure B-7 and the lowest address bit used to select the proper byte, the memory is converted to one of twice the original capacity and half the word length (from 8K by 18 to 16K by 9 for one memory module).

Figure B-2. READ-RESTORE TIMING.

Figure B-3. MEMORY-TO-NC BUFFER AND SPROCKET GENERATOR.

Along with the eight data channels, the tape reader also generates a sprocket signal each time a character is present. Under memory control, this signal is generated (circuit given in Figures B-8 and A-12) by enabling the SPK FF through Inverter I3 just prior to a memory DA. Approximately 60 nanoseconds later, I1 sets $\overline{Q}$ of the flip flop to ground which grounds the output of I4, giving the proper sprocket level. I4 remains in this state until I3's input rises to + 5 volts 1.2 milliseconds later which resets $\overline{Q}$ to + 5 volts and I4's output to + 5 volts. The output of the SPR FF is NORed with the tape-generated sprocket and fed back to the NC as were Channels 1 - 8.

Figure B-7. MEMORY INTERFACE WIRING FOR A NINE-BIT WORD LENGTH.

Figure B-8. SPROCKET GENERATOR.

NC-to-Memory Buffer and Parity Generator

Part description data are stored in memory by monitoring NC tape channel registers during normal tape operation. This work is performed by the circuit shown in Figure B-9 that consists of eight NAND gates and a parity generator (Figure A-11). These gates are enabled during normal tape operation and allow NC data through to the memory data inputs. Here, again, the selected memory inputs are ORed together as were the outputs to provide a nine-bit word.

For proper operation, the NC requires each data character to be eight bits (8 channels) in length with Channel 5 such that the sum of all channels is always odd. Because of the

Figure B-9. NC-TO-MEMORY BUFFER AND PARITY GENERATOR.

interface timing, NC Channel 5 is not conveniently available when storing data in the memory. This signal is derived from the parity generator shown in Figure A-11 by monitoring Channels 1, 2, 3, 4, 6, 7, and 8.

Memory and Address Register Controller

The block diagram for these circuits is presented in Figure B-10. These circuits control the state of the address register and supply properly timed clear-and-write (SIC) and read-restore (SOC) signals to the memory's control inputs.

Address and Data Output Control - These circuits supply the necessary signals that control the address register and cause the memory to initiate a read-restore (SOC) cycle. Operation of these circuits is initiated upon receiving a TF or TR from the memory. Assuming a TF was received, the rise to + 5 volts triggers OS1 (Figures B-11 and A-10) which outputs a 1.5-millisecond pulse. The fall of OS1 sets FF1-12 high which grounds the memory SOC input, starting a SOC cycle. Approximately 80 nanoseconds after the memory recognizes this signal, it generates a unit available (UA) which is used to reset FF1-12, removing the SOC signal at G3-1. Because of line and electronic delays, the resulting signal has a pulse width of 180 nanoseconds (Figure B-12 gives the timing diagram). Three-hundred nanoseconds after the SOC was recognized, memory data are presented at the output registers along with the DA which strobes the data into interface storage registers that were previously discussed. The NC reads these data and, after a delay of between 300 and 600 microseconds, generates an $1A \cdot \bar{1}B$ (dependent on the data bit pattern). This signal increments the address counter and retriggers OS1 which initiates another SOC after its 1.5-millisecond delay. This process continues until an end of block (EOB) is sensed (Bit 8 equal to "1" with all others "0"). At this time, TF immediately falls to ground and would

Figure B-10. MEMORY AND ADDRESS REGISTER CONTROLLER.

Figure B-11. DATA FROM MEMORY TIMING.

prevent the $IA \cdot \overline{IB}$ from incrementing the address counter if not for FF1-9, OS2, and G1-9. When TF originally went to +5 volts, FF1-9 was set to ground. This signal was fed to G1 (NOR gate) along with TF where either of these signals will keep G2-8 enabled for accepting the $IA \cdot \overline{IB}$. When TF falls to ground, FF1-9 keeps G2-8 enabled for 1.5

Figure B 12. TIMING DIAGRAM OF SOC.

milliseconds, providing ample time for acceptance of $IA \cdot \overline{IB}$. FF1-9 is reset to +5 volts by the fall of OS2-6 whose 1.5-millisecond pulse was started by the fall of TF. The address register is now set to read the next character when called by the NC's TF or TR rising to +5 volts.

Data Input Control - Information is stored in the memory with the NC operating under tape control. Each time a tape character is recognized, the NC generates a channel present (CP) which is used to generate a clear and write (SIC) in the interface (Figure A-11). Assuming the address was preset to the initial location where data are to reside and the NC's "tape forward" switch was depressed, TF goes to +5 volts (see Figure B-13 for the timing diagram) and the tape starts to move. When the first character moves by the reader photodetectors, a CP is generated. This action is used to trigger Interface OS3 (Figure A-11) which emits a 0.2-millisecond, +5-volt pulse. This delay ensures that all eight data channels are present when the write cycle is initiated. The fall of this signal initiates a SIC cycle by setting FF2-12 high and the G9-4 (SIC signal) low. Upon recognition by the memory, data at the inputs are stored in the addressed location, and a UA is generated that resets FF2-12 to its original state (as was with the SOC, delays cause the SIC signal to be approximately 180 nanoseconds wide). A short time later, an $IA \cdot \overline{IB}$ increments the address register for storing the next tape character. Operation of the address register is as was explained earlier, but now the SOC signals are disabled by a ground at G3-3 (Figure A-10).

Display System

An address and character display provides the operator with visual assurance that the system is operating satisfactorily. It also provides installation and maintenance personnel with a troubleshooting aid.

Memory Address Display - Memory address is displayed by six light-emitting diode (LED) numeric displays. The units are driven by a six-decade BCD up/down counter (Figure A-13) that runs in tandem with the 17-bit address counter previously discussed.

Character Display - The character that is read from memory is displayed by a 5 x 7 dot matrix alphanumeric LED display. The module contains a character generator capable of

Figure B-13. TIMING DIAGRAM FOR STORING DATA IN MEMORY.

displaying 64 ASCII characters. Character selection is achieved by presenting a six-bit binary word at the module input. This binary word is derived from the circuits shown in Figures B-14 and A-14. Any time a DA is generated by the memory, the contents of the addressed memory

Figure B-14. COMPONENTS OF THE CHARACTER DISPLAY.

locations are stored in SR1 and SR2. Their outputs are decoded to provide six bits of binary data suitable for driving the character display.

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