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The research program in computer systems architecture at Johns Hopkins continued its evaluations and analyses in computer organization; especially those of parallel processors and their associated program characteristics. Some of the interesting developments reported on over this year include:

1. Graph theoretic analyses of program structures: Concurrent processes may be represented by bilogic graphs called procedure graphs and the determinism of the programs they represent is expressed by structural properties of these graphs. Determinacy in a program insures that a program is decidable. It is well known that "all" of the parallelism in a program cannot be detected - detection is an undecidable issue. Determinacy insures decidability. As part of the research reported on this year, Dr. R. Regis has shown that the determinacy property is decidable for acyclic graphs. Further, it is suggested that the standard notion of the determinacy is too restrictive. Consequently, two less stringent properties have been developed - partial and terminal determinacy and easily implementable decision procedures have been proposed. Further, recursively defined concurrent processes have been considered as well as their determinacy. (JH 21)

2. Stochastic analysis of parallel processing systems: In another study performed by R. Regis the operational characteristics of concurrently operating systems (multiprocessors) were analyzed and modeled as networks of multiserver queues. General techniques were developed to study the underlying stochastic nature of the models and to derive closed form expressions of their performance under rather general assumptions. Special attention was paid to the effect of scheduling strategies on performance measures, assuming arbitrarily distributed service time. A sensitivity analysis

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of the well known exponential assumption clearly showed its very peculiar nature and stressed the need for more general assumptions. This was a particularly significant development since the bulk of the technical literature on stochastic models of operating systems rely on this assumption. The fact that when parameters are not so distributed, significant departures from traditional systems design notions on batch processing vs. time-sharing systems, for example, can be demonstrated. (R 1, JH 21)

3. Dynamic detection of concurrency: Dr. T. S. Tjaden in another major study undertaken as part of the program investigated techniques for transforming a series of ordered (i.e. serial) tasks into their maximum parallel form. The transformations studied were restricted to those which were done during execution of the instructions and is distinct from a priori detection of the concurrency done by, for example, a compiler. A series of sophisticated techniques to accomplish these transformations were developed. These techniques used a multi-state ordering matrix, which detected instruction independence both intra-cycle and inter-cycle instructions. This matrix was extended to dynamically detect opportunities for reassigning the resources specified by certain instruction to increase the amount of potential concurrency.

Experimental results using sample program streams were developed. The results of these simulations were largely negative - showing strong relation to the incidence of the branch type instruction. The potential concurrency developed - even using these quite elaborate techniques - was much less than those reported for the a priori detection techniques. Thus, we feel that dynamic detection may no longer be a promising avenue for improved performance through concurrency in computer organizations. (T 1, JH 16)

4. SIMD parallel processor organizations: Single instructions - multiple data stream organizations also received attention during the year. Mr. Charles Neuhauser reported on a series of studies on communications in parallel

processors - especially of the array type. These studies were done on sample problems: the FFT and matrix conversion. The ILLIAC IV interconnection pattern was compared against the ideal pattern for each of the problems studied.

The general class of SIMD processors include the array processor (such as ILLIAC IV) the pipelined processor and the associative processor. As such, they represent a growing and significant class of highspeed processors. It has been observed that in restructuring programs to suit the characteristics of these computers, performance is unexpectedly degraded. In fact, rather than achieving a hoped for n times performance improvement (n being the equivalent number of data streams processed per instruction stream) only $\log_2 n$ is observed for the broad class of problems. This broad class, of course, excludes certain problems well known for the intrinsic parallel characteristics. This observation was first made by M. Minsky and has been called Minsky's conjecture. We have been able to show plausible explanation for this based on the splitting of program streams which occur during the conditional branch instruction. Each time a conditional branch instruction is encountered, the single control unit - instruction stream can only control one leg of the program graph... the remaining resources go idle. If these branches are nested, resources are lost on an exponentially increasing rate. It can then be shown that the performance will go up only as the logarithm of the number of units. (JH 19, F 4, F 7)

5. Dr. S. P. Kartashev continued her work on relating automata theory to the design of integrated circuits. Dr. Kartashev produced a number of interesting results on universal modules - logic circuits which realize other arbitrary functions by feeding back some permutation of the variables from the input of the original array. This technique permits one to use several

copies of one integrated circuit mask in order to realize all possible logic functions. (K 1, JH 15, JH 17, JH 19)

6. Work continued in a variety of other areas, including the reliability of computer systems and computer arithmetic and microprogramming. (F 5, F 6, F 8)

Michael J. Flynn, the principal investigator, has, as of September 30, 1972, devoted approximately 36% of his time to this project and expects to devote 10% of his time for the remainder of the current contract term.

Recent (1971-72) publications and reports on
Computer Systems Architecture*

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PUBLICATIONS - Michael J. Flynn:

- F 1 (with S. Szygenda), "A perspective on Computer Reliability", 1972 Reliability and Maintainability Symposium, January 1972, San Francisco, California, Appears in Proceedings of 1972 Symposium of Reliability.
- F 2 "Multiprocessors with Shared Resources", IEEE International Convention Record, March 1972, New York, pp. 356-357.
- F 3 (with A. Podvin), "An Unconventional Computer Architecture: Shared Resource Multiprocessing", Computer, March/April 1972, Vol. 5, No. 2, pp. 20-29.
- F 4 "Towards More Efficient Computer Organizations", Presented at the Spring Joint Computer Conference, May 1972, Atlantic City, N. J., American Federation of Information Processing Societies (AFIPS) Conference Proceedings, Vol. 40, pp. 1211-1217.
- F 4 (with T. Hallin) "Pipelining of Arithmetic Functions" presented at the IEEE Computer Society's Workshop on Computer Arithmetic, May 1972, College Park, Md., appears in IEEE Transactions on Computers, August 1972, Vol. C-21, No. 8, pp. 880-886.
- F 5 (with T. Hallin), "Pipelining of Arithmetic Functions", (a version of the preceding paper) presented at the IEEE Computer Conference (COMPTCON) September 1972, San Francisco, California, appears in the COMPTCON Proceedings.
- F 6 "Some Computer Organizations and Their Effectiveness", IEEE Transactions on Computers, September 1972, Vol. C-21, No. 9, pp. 948-960.
- F 7 (with S. Szygenda), "Self-Diagnosis and Self-Repair in Memory: An Integrated System Approach", IEEE Transactions on Reliability, in press.
- F 8 "Computer Architecture at Johns Hopkins", Computer Architecture News (pub. ACM - SIGARCH) April 1972, Vol. 1, No. 2, pp. 21-33.
- S. P. Kartashev:
- K 1 "Integrated Circuit Realization of Sequential Machines (The Set of Algorithms)", Proceedings of the Sixth Annual Princeton Conference on Information Sciences and Systems, March 1972, pp. 245-432.

Renaud Regis:

- R 1 "Performance Evaluation and Resource Allocation Policies in Multiprocessing", Abstract Preprints, IEEE Workshop on Parallel Processor, Architecture and Programming, Seattle, Washington, June 1972.

Carold S. Tjaden:

- T 1 "Representation and Detection of Parallelism Using Ternary Matrices", Abstract Preprints, IEEE Workshop on Parallel Processor, Architecture and Programming, Seattle, Washington, June 1972.

REPORTS:

- JH 15 S. P. Kartashev, "A Mathematical Model of Assignment For Realizing Modular Sequential Logic Networks", JHCR Report #15.
- JH 16 G. S. Tjaden, "Computer Resources - A Preliminary Study", JHCR Report #16.
- JH 17 S. P. Kartashev, "Theory of P-Multiple Regular Sequential Networks and Its Application for Integrated Circuits, I.", JHCR Report #17.
- JH 18 S. P. Kartashev, "Theory of P-Multiple Regular Sequential Networks and Its Application to Integrated Circuits, II.", JHCR Report #18.
- JH 19 C. J. Neuhauser, "Communications in Parallel Processors (SIMD)", JHCR Report #19.
- JH 20 R. Regis, "Multi-Server Queueing Models of Multiprocessing Systems", JHCR Report #20.
- JH 21 R. Regis, "Structural Properties of Concurrent Processes", JHCR Report #21.
- JH 22 M. J. Flynn, "1971-72 Annual Progress Report", JHCR Report #22.