DEVELOPMENT OF SILICON NANOWIRE FIELD EFFECT TRANSISTORS

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Thesis Prepared for the Degree of

MASTER OF SCIENCE

UNIVERSITY OF NORTH TEXAS

December 2011

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Nukala, Prathyusha. Development of Silicon Nanowire Field Effect Transistors. Master of Science (Electrical Engineering), December 2011, 62 pages, 33 figures, 1 table, references, 58 titles.

An economically reliable technique for the synthesis of silicon nanowire was developed using silicon chloride as source material. The 30-40 micron long nanowires were found to have diameters ranging from 40 – 100 nm. An amorphous oxide shell covered the nanowires, post-growth. Raman spectroscopy confirmed the composition of the shell to be silicon-dioxide. Photoluminescence measurements of the as-grown nanowires showed green emission, attributed to the presence of the oxide shell. Etching of the oxide shell was found to decrease the intensity of green emission. n-type doping of the silicon nanowires was achieved using antimony as the dopant. The maximum dopant concentration was achieved by post-growth diffusion. Intrinsic nanowire parameters were determined by implementation of the as-grown and antimony doped silicon nanowires in field effect transistor configuration.

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to my thesis advisor Dr.Usha Philipose for her continuous support for my masters study and research at University of North Texas. The enthusiasm, inspiration, effort in making things simple and clear motivated me a lot during my research. It is a priceless experience working with Dr.Phillipose. Her continuous encouragement and rapport provided me an opportunity for attending an international conference. Her attitude towards teaching and research and deep devotion to career inspired me. Besides, she was always accessible, willing to help students in their research.

It is my pleasure to acknowledge professors Dr.Arup Neogi, Dr.Parthasarathy Guturu and Dr.Hualiang Zhang for serving on my masters advisory committee and providing valuable comments and suggestions on this work.

It is a great experience to work with my lab mates Gopal Sapkota, Pradeep Gali, Kiran Shresta, Mirza Tanweer Beig and Marzieh Zare. I am indebted for their constant source of encouragement and guidance. I would also like to thank Ben Urban for the photoluminescence measurements in Dr. Neogi's Raman Spectroscopy lab.

The Department of Physics has provided the support and equipment required to produce and complete my thesis. I am also thankful to the Department of Electrical Engineering faculty for giving me the opportunity to pursue thesis in my area of interest.

Finally I would like to express my appreciation to my parents and family members for their care and loving support.

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CHAPTER 1

INTRODUCTION

1.1. Motivation

Device miniaturization, reduced power consumption and high processing speed are major factors controlling growth of the current integrated circuit industry. There is a concentrated effort to develop strategies for device development addressing future technological demands. Conventional circuit scaling has physical and technological limitations in terms of low current, power dissipation and design complexity based on the limitations of lithography techniques. Hence, there is a need to advance research on developing strategies that have the potential to reach higher device densities and at the same time address the need for reduced power and higher speeds. Nanotechnology, which involves the engineering of functional systems at the molecular level, has made huge contributions to this effort and impacted science and technology especially in the fields of electronics, medicine and communications. Nanostructured materials have physical sizes in at least one dimension less than or equal to 100 nm. Three major scientific advancements have led to significant progress in the development of nanotechnology and contributed significantly to current scientific and industrial revolutions.

(i) Observation of novel physical phenomena as a consequence of size reduction. One example is the quantum size effect, where the electronic properties of a material are modified when material size is in the nanometer range.

(ii) Observation and manipulation of nanoscale objects (such as atoms and molecules) using tools like the scanning tunneling microscope.

(iii) Fabrication of single electron or photon nanodevices using nanostructures.

The first characteristic is due to quantum-size effects whereby the properties of a material change with its size in the nanometer regime. The second is made possible by the

invention of high resolution transmission electron microscopy (TEM) and scanning probe microscopy (SPM), including scanning tunneling microscopy (STM) and atomic force microscopy (AFM)). The third is the result of the developments of various nanofabrication techniques (such as nano-imprint lithography using electron beams or X-rays) as well as due to a physical phenomenon known as quantum confinement in the nanorealm [6]. Hence, combined with other well-developed characterization and measurement techniques such as transmission electron microscopy (TEM), it is possible to study and manipulate the nanostructures and nanomaterials to a great detail and often down to the atomic level.

One type of nanostructured material is the one-dimensional (1-D) nanowire, in which confinement in two dimensions allows for exploration of fundamental physical concepts and technological applications. In general, nanowires exhibit aspect ratios (length-to-width ratio) of 1000 or more. They are ideal systems for investigating the dependence of electrical transport, optical and mechanical properties on size and dimensionality. The transverse confinement of carriers leads to quantization of energy levels and results in a finite level spacing of energy levels. The unique fundamental physical, electrical, optical and magnetic properties of 1-D nanowires are attributed to size effects [30], quantum effects [32], and surface effects [10]. There are several established routes to synthesize nanostructures such as vapor phase methods, thermal evaporation and condensation [23], metalorganic chemical vapor deposition [56], laser ablation [31] and solution phase methods [16].

1-D nanowires have the unique advantage over other low dimensional structures. They can function as both interconnects and nanoscale electronic and optoelectronic devices. The semiconductor industry is traditionally based on Si and hence the efforts of this thesis are directed towards the development of one dimensional Si nanowires that can function as an active device.

1.2. Evolution of Nanotechnology

Nanotechnology is not new; study on materials in the nanometer scale can be traced back for centuries. It is the combination of existing technologies and our ability to observe

and manipulate matter at the atomic scale that makes nanotechnology compelling from scientific, business and commercial viewpoints. The semiconductor industry is currently driven by the need to achieve device miniaturization, achievable through developments in nanotechnology and is supported by the availability of characterization and manipulation techniques at the nanometer level. The continued decrease in device dimensions follows the Moore's law predicted in 1965 and is illustrated in Figure 1.1.

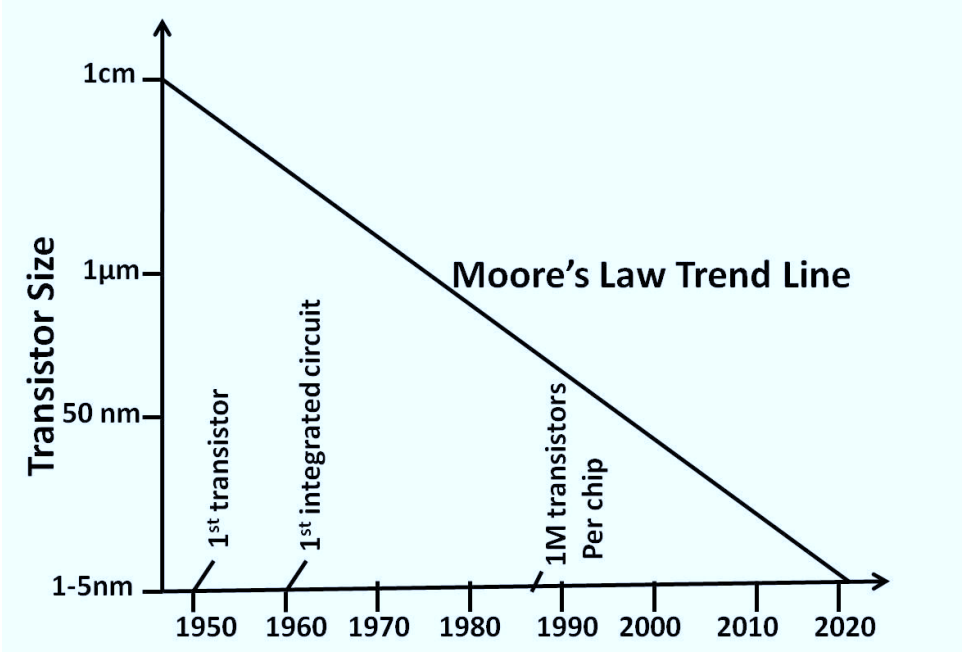

FIGURE 1.1. Moore's law of transistor size versus year.

Moore's law predicts that the dimensions of a device halves approximately every eighteen months. The above figure represents the scaling trend of Si devices described by Moore's law, which predicts that by year 2012 the size of a transistor should be below 20 nm. This is a challenge that needs to be addressed. Although current devices operate far below fundamental limits imposed by thermodynamics and quantum mechanics, a number of challenges in transistor design have already arisen from materials limitations and device physics. For example, the off-currents in a metal-oxide semiconductor field effect transistor (MOSFET) increase exponentially with device scaling. Power dissipation and overheating of chips have also become a serious issue in further reduction of device sizes. The continued size shrinkage

of transistors based on patterning and lithography techniques, the so called top-down approach imposes limitations based on resolution limits of optical or electron beam lithography as well as fundamental material limitations.

1.3. Promise of Bottom-Up Technology

The bottom-up approach is a technique that is used to synthesize materials from nanoscale building blocks. It is an inexpensive approach of self-assembly and uses chemical or physical forces operating at the nanoscale to assemble basic units such as atoms or molecules into larger structures. The inspiration for bottom-up approaches comes from biological systems, where chemical forces create complex systems and structures needed by life. Nanotechnology aims to replicate this ability to produce small clusters of specific atoms, which can then self-assemble into elaborate structures, such as nanowires (quantum wires) and quantum dots. The bottom-up approach is being exploited by researchers not to just achieve device miniaturization, but also to usher in an era of new device concepts and an exciting field of electronics that includes quantum computing and highly efficient surveillance and detection systems.

1.4. Semiconductor Nanowires

One dimensional semiconductor nanowires are the potential building blocks for electronic devices and have the potential of revolutionizing a broad area of nanotechnology including applications such as electronic devices, sensors, biological diagnostics, photovoltaics and thermoelectrics. It is well accepted that 1-D semiconductor nanostructures provide a good system to investigate the dependence of electrical transport and chemical properties on dimensionality and size reduction. More importantly, 1-D nanowires represent the smallest dimension that can effectively transport charge carriers and hence their role in nanoscale electronics is unique. In this respect carbon nanotubes and semiconductor nanowires have met with great success [50, 1, 35, 29] and have been used extensively to fabricate devices such as light emitting diodes, field effect transistors and lasers. Synthesis of 1-D nanostructures has been a major challenge, although several strategies have been pursued recently.

Nanometer sized structures are of prime interest for basic physical studies and are very challenging in terms of technological realization. Moreover, their high surface to volume ratio plays a prominent role in sensor applications. In this field of research, Si nanostructures are very fascinating objects since they open the way to low dimensional electronic effects and could offer full integration and technological compatibility with Si microelectronic circuits.

The successful functioning of all electronic circuits is based on controlled flow of electrons. The roots for the development of modern solid-state semiconductor electronics goes back to 1930's when it was realized that some solid-state semiconductors and their junctions offer the possibility of controlling the number and the direction of flow of charge carriers. Simple excitations like light, heat or small applied voltage can change the number of mobile charges in a semiconductor. The flow of charge carriers in the semiconductor devices are within the solid itself, while in the earlier vacuum tubes, the mobile electrons were obtained from a heated cathode and they were made to flow in an evacuated space or vacuum. No external heating or large evacuated space is required by current semiconductor devices. They are small in size, consume low power, operate at low voltages and have long life and high reliability. Semiconductors have resistivity or conductivity intermediate to metals and insulators. Engineering the properties of semiconductor materials through the process of doping allows for tuning of their intrinsic properties such as its band structure, carrier concentration, transport mechanisms, to name a few. In order to fabricate devices using semiconductor nanowires, an understanding of the effect of dopants on the morphology and properties of the nanowire is required. The efforts of this thesis is directed towards achieving this objective.

1.4.1. Significance of Si

Si belongs to group IV in the periodic table and it is the second most abundant element found in the earth crust. It also forms the backbone of the electronic industry and is the the most commercially popular microelectronic material covering about 99% of the electronic device market today. Si has diamond cubic lattice structure with lattice constant of 5.43Å.

Each Si atom has 14 electrons out of which 10 core electrons are tightly bound to the nucleus and the loosely bound four valence electrons are responsible for most of its electronic, optical and chemical properties. The atoms are tetrahedrally bonded and the sharing of the valence electrons forms covalent bonds. Figure 1.2 represents the crystalline structure of Si. The surface of Si can change its electronic behavior and hence requires detailed study. Mass production of electronic chips including solid state electronics such as in production of transistors, liquid crystal displays, diodes etc are almost entirely based on Si. Being an environmentally safe material, its processing techniques are reasonably safe; on account of its abundance in nature (Sand is SiO_2), it is also a relatively inexpensive material. On account of its indirect band gap, this material is not viable for use in opto-electronic applications, since it cannot emit light through a direct electron-hole recombination. However, in the form of nanostructures, Si nanowires have been reported to emit light in the visible region. This engineering of the optical properties of Si nanowires through a control of its crystal structure, electron energy levels and influencing its surface contributes to the significance of 1-D Si nanowires.

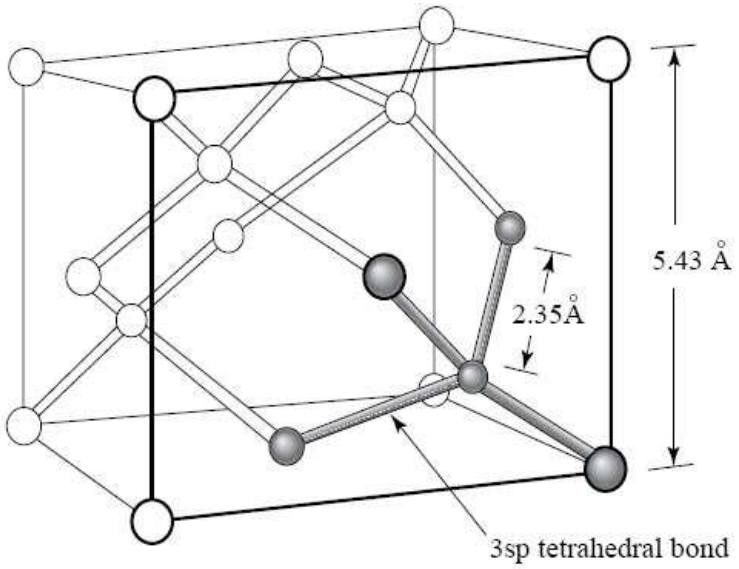

FIGURE 1.2. Crystalline structure of Si.

1.4.2. Si Nanowires

1-D Si nanowires can be grown by a relatively simple growth procedure with the potential of doping either n or p-type. Chemical functionalization, surface passivation and compatibility with conventional bulk Si technology will enable large scale commerical production. Thus Si nanowires hold promise as a component that has the potential to revolutionize the bottom-up assembly of nanoelectronic applications. Si nanowires achieved significant importance in wide variety of applications ranging from field effect transistors (FETs) [14, 10, 28, 17, 8], logic gates [21, 47], nonvolatile memories [27], solar cells [12, 20], thermoelectrics [4], waveguides [15] and other nanoelectronics to chemical and biological sensing [38, 58, 52, 25] in nano-regime. These multiple applications influenced an extensive research into the fabrication and characterization techniques of Si nanowires and their incorporation into functional devices. Si nanowires offer great opportunities to pursue high device density that the conventional semiconductor technologies cannot provide. Intense research is being carried on Si nanowires to make them compatible with the present complementary metal oxide semiconductor (CMOS) technology. During the growth, several parameters can be controlled for optimization to obtain high quality nanowires. Conductivity is one such parameter for the proper functioning of nanoscale structures. Doping is the key factor to control the conductivity. To-date, research has been primarily focused on p-type Si nanowires. n-type received little attention even though electron mobility is far larger than hole mobility in bulk Si. Generally doping is achieved by phosphine, trimethyl-antimonide dopants with silane as precursor in CVD growth for n-type. Doping with bismuth was also reported for n-type in previous works.However, there has been no work reported on doping with antimony.

1.5. Overview of Thesis

This thesis study is organized as follows:

Chapter 1 presents a brief introduction of evolution of nanotechnology and its benefits and applications. It also explains the emphasis on the choice of Si as source material for the synthesis of nanostructures and a overview of previous works on Si nanowires.

Chapter 2 describes the various approaches used in nanotechnology and in detail description of bottom-up approach for the synthesis of crystalline nanowires through vapor-liquid-solid (VLS) growth mechanism. Metal nanoparticles serves as catalyst and play a key-role in the VLS synthesis for crystalline growth. Hence the knowledge of metal-source material eutectic temperature is essential for the proper choice of catalyst. This chapter also focuses on the effect of growth parameters of Si nanowires. The morphology of these nanowires strongly depend on growth parameters such as choice of catalyst and precursor, flow rate of components in vapor phase, temperature and growth time. The effect of these parameters on morphology and defects of the as-grown nanowires are studied with various characterization techniques and the parameters to overcome these defects are explained.

Chapter 3 highlights the various approaches of doping Si nanowires and its effects on the chemical composition. Structural and compositional characteristics were also detailed in brief. This chapter also describes how the post-growth doping process will aid in the Sb diffusion into the crystal lattice.

Chapter 4 presents the results of characterization of electrical properties of undoped and doped Si nanowires using transport measurements. Electrical properties are usually analyzed by making contacts to a nanowires placed on a insulating substrate, usually an oxidized Si wafer. Gate-dependent two terminal measurements shows the evidence of these doped nanowires to be n- type, exploring the possibility of implementing these structures into nanoscale devices. Transport measurements will help in the estimation of transconductance, carrier mobilities and concentration of charge carriers.

Chapter 5 deals with the optical properties of Si nanowires. Photoluminescence (PL) is an important technique in determining the crystalline quality and morphology. Si is an indirect bandgap semiconductor with bandgap of 1.1 eV. Unlike bulk Si, a Si nanowire can become a direct band gap semiconductor at nanometer range due to quantum confinement effect. The quantum confinement effects are observed only when the dimensions becomes less than 5 nm (Bohr radius of exciton in Si). As the synthesized nanowires are greater than

5 nm, we do not expect to observe the effects of quantum confinement on the band gap in silicon nanowires. However, the PL measurements on the as-grown Si nanowires reveal a peak at energy higher than the band gap of Si, which is believed to have its origin in the oxide shell covering the Si nanowires. The reason for this increase in band gap will be discussed in this chapter. Raman spectra was also performed to confirm the structural characterization and chemical composition of the synthesized nanowires.

Based on these results, the work done in this thesis is summarized in Chapter 6 and future work and its applications are discussed.

1.6. Thesis Objectives

Research and development of nano-materials involves five key aspects : high yield, simplicity, economical, safety and application in real time. The evolution of nanoscale devices requires both the fabrication of nanoscale diameter wires and the integration with microelectronic processes. Semiconductor nanowires are potential alternatives to conventional planar MOSFETs. Si nanowires are important in nanotechnology because si-based nano-electronics could be a successor to microelectronics based on Si. Si nanowires in the nanosize regime exhibit quantum confinement effects and are expected to play a key role as interconnects and as functional components in future nanosized electronic and optical devices. Nanowire FETs (NWFETs) have a unique electronic structure which we can try and exploit. The ability to control the conductivity of the nanowires through intentional doping without unwanted changes in crystallinity is important for the realization of nanowire-based electronics. When the nanowire diameter is of the same order as the charge carrier wavelength, quantum confinement effects shift the energy states and, in Si, induce visible photoluminescence. Hence the properties of the nanowires strongly depend on the size, shape, and structure. It is tedious to measure the electrical properties of nanowires due to small dimensions. The primary focus of this thesis is to investigate a reliable and controlled approach for the bottom-up synthesis of silicon nanowires and achieve n-type doping with a detailed study of factors that affect growth. Though, silane precursors require low temperature, these are

self igniting gases that are potentially explosive if brought into contact with air. These gases requires complex experimental setup and more safety measures. On the other side, chlorinated silanes are nontoxic and requires less sophisticated instruments . This study also provides information on the optimization of the nanowire growth and doping parameters. Even though, these nanostructures function similar to the existing devices, it is expected that further work is warranted to modify their properties; one such being the reduction in diameter of the nanowire. The realization of these nanowires into real time devices has been a major challenge. To enable the successful integration into real time devices, a proper understanding of characterization is most essential. This thesis also highlight the results of characterization indicating the potential use of these nanowire devices. Optical properties of these nanowires will be helpful in the design of photovoltaics and liquid crystal displays. Hence the the study of optical properties will help in investigating the reasons behind the visible luminescence of these nanowires.

CHAPTER 2

SYNTHESIS OF SILICON NANOWIRES

2.1. Introduction

Si nanowires have been synthesized using various techniques such as vapor deposition, template-assisted, solution growth etc. Among these synthesis methods, vapor phase transport methods are often used to grow Si based nanostructures owing to their simple systems and fast growth rates as compared to other methods. The vapor deposition techniques in the synthesis of nanowires is divided into:

(i) Physical vapor deposition (PVD)

(ii) Chemical vapor deposition (CVD)

2.1.1. Physical Vapor Deposition

PVD is a process of transferring growth species from a source material and depositing them on a substrate. This process requires the system to be maintained in ultra-high vacuum and involves no chemical reactions. Various methods have been developed for the transfer of growth species from the source. These methods can be divided into two groups: Evaporation and Sputtering. In evaporation the source material is transferred from the source to the substrate by maintaining a thermal gradient between the source and the substrate. In sputtering, atoms are dislodged from a source material by means of gaseous ions. Depending on the specific technique used to activate the source atoms, each group is further categorized such as:

(i) Molecular beam epitaxy:

Molecular beam epitaxy is carried out in high vacuum or ultra high vacuum (10^{-8} Pa) with highly controlled evaporation of a variety of sources. The evaporated atoms or molecules from one or more sources do not interact with each other in

the vapor phase under very low pressure. Most molecular beams are generated by electrical heating of solid materials placed in source cells, which are referred to as effusion cells or knudsen cells. The source materials are most commonly raised to the desired temperatures by resistive heating.

(ii) Laser ablation:

Laser radiation when focused on the surface of a solid target, can be absorbed through various energy transfer mechanisms, leading to thermal and non-thermal heating, melting and finally ablation of the target. The ablation of the target yields to an ejection of its constituents and lead to the formation of nanostructures. When the target is ablated in vacuum or in a residual gas, the nanoclusters can be deposited on a substrate, placed at some distance from the target, leading to the formation of a thin nanostructured film.

(iii) Thermal evaporation:

The process of evaporation and condensation cycle to form thin films of any material that remains stable in a vapor state at high temperature in a high vacuum environment is known as thermal evaporation. The heat is provided either by Joule heating via a refractory metal element (resistive evaporation) or directly from a focused beam of high energy electrons (electron beam evaporation). Usually low pressures about 10^{-6} or 10^{-5} torr are used, to avoid reaction between the vapor and atmosphere.

Generally PVD systems requires both the source and the substrate located in a high pressure vacuum chamber. In addition, these are complex and sophisticated equipments that requires routine maintenance. Chemical vapor deposition (CVD) process is a more viable and economically versatile process.

2.1.2. Chemical Vapor Deposition

CVD is the process of chemically reacting a source material to be deposited, with other gases, to produce a nonvolatile solid that deposits on a suitably placed substrate. Because

of the versatile nature of CVD, the chemistry is very rich and various types of chemical reactions are involved. A number of CVD methods have been developed depending on the types of precursors used, the deposition conditions applied and the forms of energy introduced to the system to activate the chemical reactions desired. When metal organic compounds are used as precursors, the process is generally referred to as metal organic CVD (MOCVD) and when plasma is used to promote chemical reactions, it is referred as plasma enhanced CVD (PECVD). When the chemical reaction takes places at atmospheric pressure, the CVD is referred as atmospheric pressure CVD (APCVD). This thesis focuses on APCVD as the growth process of the Si nanowires discussed is carried out at atmospheric pressure and without the use of complex growth equipment. CVD systems are preferred over the MOCVD system because the metal-organics used in MOCVD are toxic and the waste gases released during the process are harmful to environment. Hence these need to be scrubbed before releasing into atmosphere.

2.2. Vapor-Liquid-Solid (VLS) Growth Mechanism

Many bottom-up synthetic strategies have been developed to produce bulk quantities of Si nanowires. To date, oxygen-assisted-growth (OAG), vapor-solid-solid (VSS) and electroless etching methods have been developed to synthesize large scale Si nanowires. Si nanowires grown by VLS or VSS techniques have an advantage over those grown by OAG and electroless etching techniques in terms of well-defined surface and well-controlled diameter. When etching is used to produce Si nanowires, these nanowires are embedded in the host and so their application becomes limited. On the other hand, Si nanowires synthesized by VLS mechanism can be grown on a substrate of choice and they can be released from the host substrate for single nanowire characterization and device development.

Most of the recent successful semiconducting nanowire growth is based on the VLS technique. This crystal synthesis method was first proposed by Wagner and Ellis in 1964 for the growth of Si whiskers with diameters from one hundred nanometers to hundreds of microns. Subsequently, E. I. Givargizov elucidated the growth mechanism of Si whiskers in

1975 [53, 13]. The need for systematic nanostructure synthesis and the progress in the formation technique of metal nanosized particles, renewed interest in the VLS technique. Since then, extensive research has been carried out on the synthesis, physical properties and device fabrication and applications of Si nanowires.

The name itself reflects the path way of Si for the synthesis of Si nanowires. Si in vapor phase diffuses into a liquid droplet and solidifies as Si nanowire [46]. The liquid droplet on the substrate is formed either by a metal (catalyst) or with the material supplied from the vapor phase. The stoichiometry will be in equilibrium at certain temperature. As more growth material is supplied at this equilibrium temperature, the alloyed particle becomes supersaturated, which results in nucleation and growth. As the purpose of the metal is to initiate the growth only, it is referred as catalyst. VLS growth mechanism works well for various catalysts and nanowire materials.

The metal particle acts as catalyst and determines the diameter of the nanostructures. Consequently, the choice of the metal, based on its physical and chemical properties, determines many of the nanowire properties. To be processed via the VLS growth mechanism, the metal has to be physically active, but chemically stable. The eligible metal is chosen from the phase diagram so that it forms a liquid alloy with the nanowire material of interest. The solid solubility of the catalyzing agent is low in the solid and liquid phases of the substrate material. This is possible if metal catalyst and source material forms a eutectic compound at certain temperature known as the eutectic temperature. At this temperature, the liquidus line will be minimum for a eutectic compound. The equilibrium vapor pressure of the catalyst over the liquid alloy should be small so that the droplet does not vaporize. The vapor-solid, vapor-liquid and liquid-solid interfacial energies play a key role in the shape of the droplets. A catalyst which has small contact angle between the droplet and solid is more suitable for large area growth, while large contacts angles result in smaller (decreased radius) whisker formations. Hence the equilibrium phase diagrams are particularly helpful for estimating the optimal composition and temperature for nanowire growth.

The VLS growth process can be described by the following:

(i) Formation of a liquid alloy droplet between the metal catalyst and the nanowire material on the substrate

(ii) The deposition of source from vapor directly onto the liquid alloy droplet in the vapor liquid system.

(iii) Precipitation of solid from the supersaturated liquid alloy at the liquid-solid interface.

Adsorption of the vapor phase reactants onto the metal catalyst leads to the formation of a liquid metal-semiconductor alloy (eutectic) at the surface. The sticking coefficient is higher on liquid than solid surfaces; so consequently the crystal growth occurs only where the liquid metal catalyst is present. When the liquid alloy becomes saturated, additional supply of source from the gas phase results in crystallizing solid source at the droplet or more specifically at the liquid-solid interface. Epitaxial growth of 1-D nanowires requires a direct contact of the droplet to the crystalline substrate. The solid-liquid interface must be well-defined crystallographically in order to produce highly directional growth of nanowires.

2.3. VLS Growth Applied to Si Nanowires

The VLS mechanism can be best explained on the basis of gold (Au) catalyzed Si nanowire growth on Si substrate by means of CVD. The melting point of Au-Si alloy primarily depends on composition. Figure 2.1 shows a binary phase diagram of alloy suitable for VLS assisted growth of Si nanowires. The composition of Au-Si significantly lowers the melting point when compared to the individual elements. When the ratio of Au-Si alloy is 4:1, the alloy readily melts at a eutectic temperature of 363°C which is about 700K lower than the melting point of pure Au and 1000K lower than the melting point of pure Si. Au/Si alloy has the lowest eutectic temperature among the usually used metal catalysts, thus allowing a lower reaction temperature to obtain thinner Si nanowires. Hence this thesis focuses on use of Au as the metal catalyst to synthesize the Si nanowires. At a specific temperature that corresponds to the growth temperature (higher than the eutectic temperature), the incoming vapors

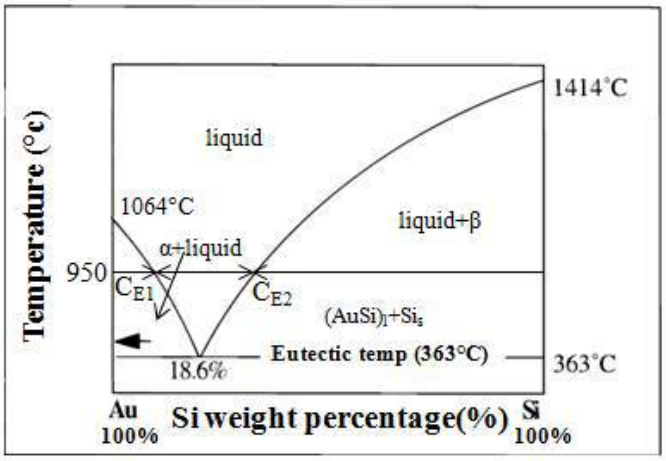

FIGURE 2.1. Binary phase diagram of Au-Si alloy suitable for VLS mechanism.

of Si forms a film of composition C_{E1}, a Au-Si alloy, on the surface of the Si substrate (Figure 2.2). When the Au-Si alloy droplets are exposed to more vapor containing Si, the precursor molecules diffuse through a concentration gradient ΔC of the alloy droplets of thickness L. The equilibrium concentration of the liquid alloy is C_{E2}. The liquid layer thickens with further deposition of Si. From C_{E1}, the concentration of Si increases and becomes saturated at C_{E2} with continuous flow of Si vapors at constant temperature. The liquid composition at supersaturation will be similar to equilibrium value of C_{E2}. Surface tension results in the liquid catalyst formation atop the growing nanowire. A Si nanowire, then precipitate from the melt, as it grows in length with further deposition of Si. For steady state VLS growth, the composition of liquid near the vapor interface is C_L and at solid-liquid interface is C_S . The schematic of the VLS process is depicted in the Figure 2.2

The concentration gradient Δ in the liquid droplet is given by the equation

$$\frac{C}{L} = \frac{V}{D} \tag{1}$$

where V is the advancement of the solid-liquid interface, D is the diffusion coefficient of Si in the liquid alloy and $\Delta C = C_{E1}$-C_{E2} corresponds to liquidus supercooling. Due to concentration difference, the liquid alloy is always supercooled during VLS growth. Si vapors were continuously produced until the gas flow and the temperature are maintained. Si

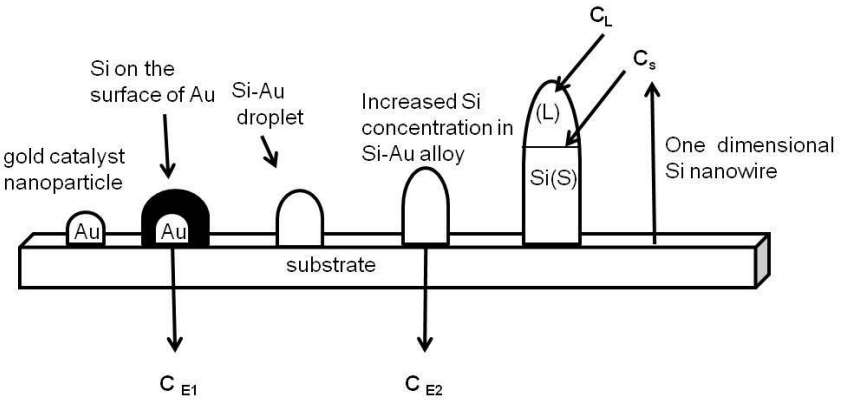

FIGURE 2.2. VLS growth of Si nanowires.

nanowires of high purity are obtained except at tip which contains solidified metal catalyst. According to Wagner and Ellis, stability of the liquid alloy particle is another requirement for VLS mechanism. According to Gibbs-Thompson law, the stability of liquid droplet of curvature r depends on the degree of supersaturation (partial pressure of growth material $\alpha = \frac{\mathrm{p}}{\mathrm{p}_0}$ where p_0 is the vapor phase of growth material in thermal equilibrium) which places a lower limit on nanowire diameter that can be grown under a given set of conditions.

$$\mathrm{r}_{\min} = \frac{2\Omega_{\mathrm{l}}\sigma_{\mathrm{lv}}}{\mathrm{kTln}(\alpha)} \tag{2}$$

where Ω_{l} is the volume of an average atom of growth material in the liquid, σ_{lv} is the liquid-vapor surface energy density, k is Boltzman constant and T is absolute temperature. Hence there is a limitation on minimum diameter of nanowires grown by VLS and therefore determined by the diameter of the catalyst liquid particle.

Once a nanowire has begun growing, there are actually two surfaces exposed to the vapor: the metal-semiconductor liquid and the solid-semiconductor. To achieve one-dimensional axial growth, vapor adsorption should occur preferentially at the surface of the catalyst particle rather than on the surface of the semiconductor nanowire.

2.3.1. Synthesis of Si nanowires by CVD

CVD is one among several different methods of Si nanowire synthesis. The choice of growth method depends on the application as well as on the advantages and limitations of the technique. A chemical reaction has to take place at the catalyst particle to initiate wire growth when a Si compound is used as a source. Generally for a CVD growth process, an oxygen free Si precursor is used as a source, as Si is sensitive to oxidation. The most frequently used Si precursors are silane (SiH_4) [55, 44], disilane (Si_2H_6), siicon dichloride (SiH_2Cl_2) and silicon tetrachloride ($SiCl_4$) [24, 54]. Chlorinated silanes are more stable than nonchlorinated silanes. As a result, higher temperatures are required to thermally crack the precursor. The homoepitaxial growth of Si wires on Si substrate is facilitated by the use of $SiCl_4$ used in combination with H_2. The developed hydrochloric acid HCl can etch away any unwanted oxide coverage of the substrate.

2.4. Experimental Details

Si nanowires were synthesized on Si substrates by VLS mechanism using a CVD. A single zone furnace is used in this experiment. The maximum working temperature of the furnace is 1200°C. A quartz tube placed inside the furnace acts as a growth chamber. The furnace is controlled by a microprocessor based self tuning PID to minimize the overshoot and maintain a optimum set temperature. A substrate is kept on a alumina boat and placed in a quartz tube. Prior to heating, the system which was at room temperature was flushed with a flow of Ar+H_2 gas flow rate in standard cubic centimeters per minute (sccm = 100) for almost 1 hour to eliminate contamination with O_2. The purpose of this setup is to maintain a uniform environment favorable for the reaction to take place. The above described experimental procedure is illustrated as shown in the Figure 2.3.

2.4.1. Synthesis of Si nanowires using $SiCl_4$ as source

The n-type Si (111) wafer is immersed in acetone and heated for few seconds to remove any contaminants from the surface followed by ethanol and deionized water. A thin layer of Au film is deposited on a Si (111) wafer by thermal evaporation. The substrate was

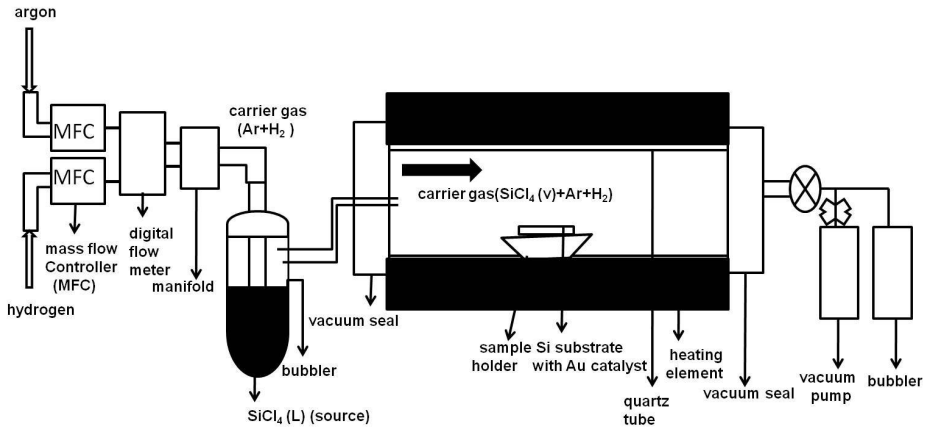

FIGURE 2.3. Schematic for the setup of synthesis of Si nanowires using a single zone temperature controlled furnace.

placed on an alumina boat and then loaded into the quartz tube maintained at atmospheric pressure. Silicon tetrachloride ($SiCl_4$, AlfaAesar, 99.99%) was used as Si precursor and the vapor was delivered into the growth chamber by bubbling a carrier gas mixture (Ar and H_2) through one end of the bubbler filled with source $SiCl_4$, with the other end connected to the the growth tube. The gases produced as a result of the chemcial reaction were taken out of the growth chamber and flushed into a bubbler. The furnace was rapidly heated at a rate of 60°C per minute to the desired growth temperature of 950°C.

2.4.2. Stages of Growth

During the synthesis of crystalline Si nanowires by VLS mechanism, the substrate is enclosed by vapors containing Si. At these high temperatures, $SiCl_4$ reacts with H_2 and decomposes into Si and HCl. The hydrogen reduction of $SiCl_4$ is highly endothermic and thus becomes more favorable at high temperatures. The simplified thermodynamic equation which describes the Si deposition is described as

$$SiCl_4(v) + 2H_2(v) \rightleftharpoons Si(s) + 4HCl(v) \tag{3}$$

As per the above equation, Si vapors produced inside the growth tube diffuse into liquid Au droplets to form Si-Au alloy nanoclusters as shown in Figure 2.4.

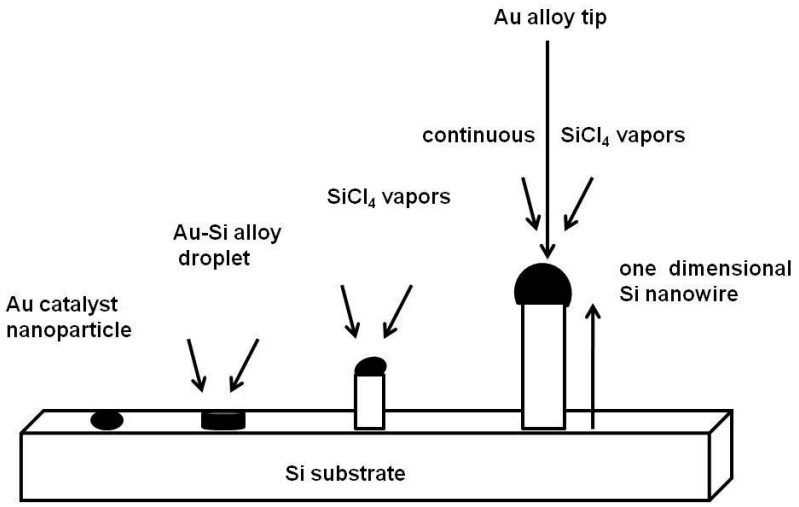

FIGURE 2.4. Schematic of Si nanowire growth process using $SiCl_4$ as Si source.

These vapors will be absorbed into Au alloy nanoclusters. Further deposition of Si vapors results in super-saturation of the Au-Si alloy droplet. Nucleation of liquid alloy droplets yield to crystalline Si nanowire growth. Growth will continue as long as there is sufficient supply of source $SiCl_4$ and the temperature is high enough to facilitate VLS growth. When the furnace temperature is turned down, Au-Si nanoclusters solidifies and growth terminates.

After the growth time, the furnace was cooled to room temperature. The Si substrates were found covered with light yellowish layer. The synthesized nanowires were characterized to determine their structural and compositional characteristics using FEI Nova 200 dual beam scanning electron microscopy (SEM) with energy dispersive x-ray spectroscopy (EDX). A systematic study of the as-grown nanowires confirms that their morphology and composition are sensitive to various factors.

2.5. Factors affecting the Morphology and Composition

(i) Temperature

(ii) Gas flow rate

(iii) Thickness of Au catalyst

(iv) Gas mixture composition

2.5.1. Temperature

Temperature plays an important role in the synthesis and growth mechanism of Si nanowires. At temperatures above 1000°C, in addition to vertical 1-D growth, there is lateral epitaxial growth on the surface of the nanowire. Also at higher temperatures, as a consequence of Ostwald ripening of the catalyst droplets, it becomes more difficult to grow nanowires with well defined diameters. Figure 2.5 shows the effect of higher temperatures on the growth of Si nanowires.

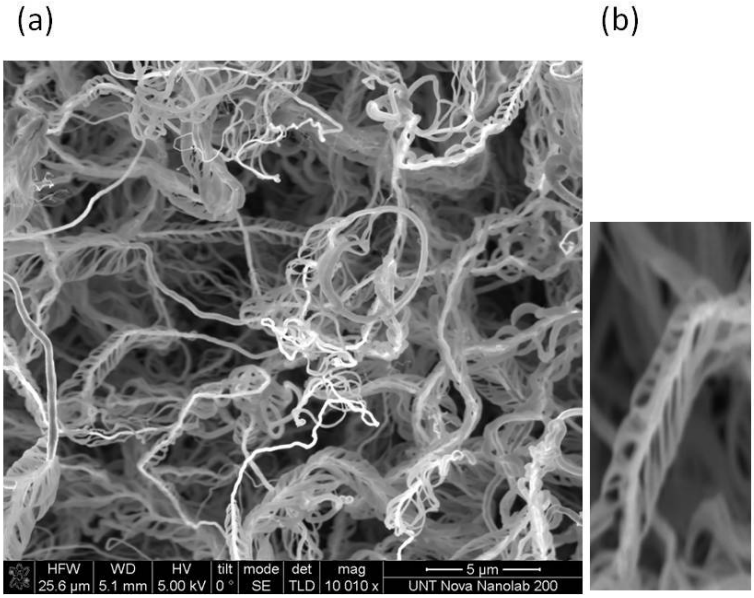

FIGURE 2.5. (a) Effect of higher temperatures on the growth of undoped Si nanowires. (b) Magnified image of the lateral growth of single nanowire.

2.5.2. Gas Flow Rate

When the gas flowrate is high, more vapors of $SiCl_4$ flows into the growth tube. Figure 2.6 shows the SEM images of the as grown nanowires with higher gas flowrate. A high uncontrolled growth can be observed from a single nodal point as shown in the figure. In some cases, these branched nanowires bundle together to form rope-like structures. Hence the flow of vapor flux should be optimized to prevent the lateral growth.

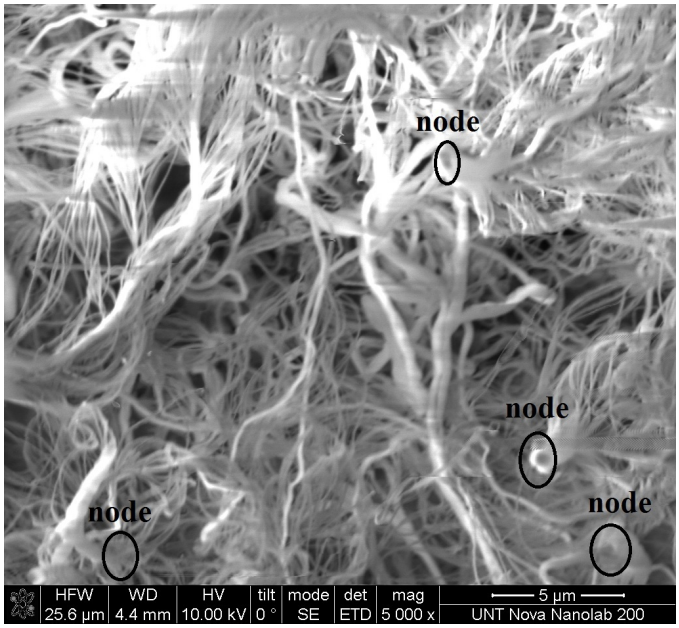

FIGURE 2.6. Effect of high gas flow rate on the growth of Si nanowires.

2.5.3. Thickness of Au Catalyst

If a very thick layer of Au (thickness $>$ 20 nm) is used as the catalyst, the size of the alloyed droplets or islands is very large. The droplets can also coalesce into each other forming even bigger alloyed droplets. When the size of the droplet is very large, there are several energetically favorable sites where incoming vapors of the source material can diffuse to initiate the nanowire growth. In such a case, there will be a collection of thick and thin nanowires, all of which can entangle together to form a highly disordered array of nanowires. Figure 2.7 reveals that the nanostructures are composed of thick and thin nanowire bundles.

2.5.4. Gas Mixture Composition

$SiCl_4$ is hygroscopic in nature and so contains a significant amount of water in it. In the absence of a reducing environment, the water molecules will provide oxygen that will oxidize the growing Si nanowire at high temperatures. This is why growth of Si nanowires by this technique is done in hydrogen environment. H_2 will react with the O_2 and will be driven out of the growth chamber in vapor form. Thus H_2 provides a reducing environment, eliminating the O_2 content in the growth chamber and it also adsorbs on the growing nanowire surface

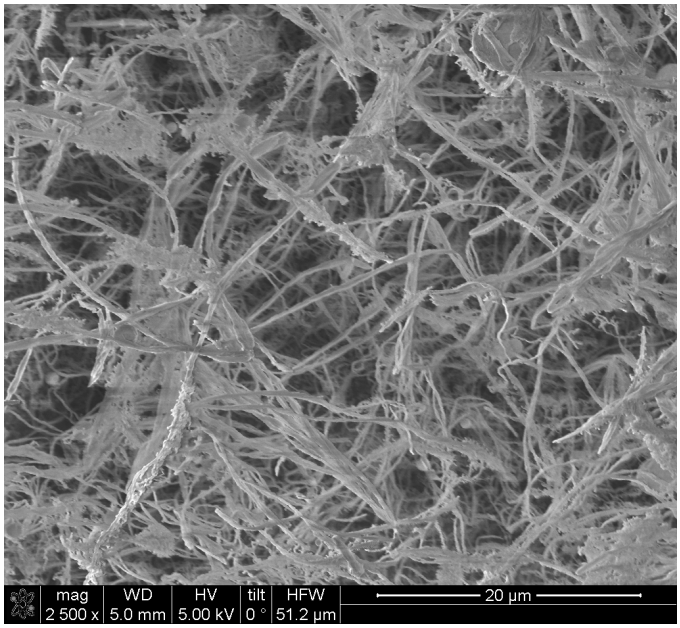

FIGURE 2.7. Effect of Au catalyst on the growth of Si nanowires composed of thick and thin nanowire bundles.

providing a temporary passivating layer.

The factors were optimized which contribute to the growth of Si nanowires. A controlled flow of carrier gas (80% Ar and 20% H_2) is passed through one end of the bubbler filled with source ($SiCl_4$) at a growth temperature of 950°C. Figure 2.8 represents the SEM and stoichiometric EDX (Figure 2.9) images of the nanowires after the optimized growth parameters. The image shows the high yield of straight nanowires formed on the substrate. Nanowires of length 30-40 μm and diameter 40-100 nm were observed. The composition of these nanowires when analyzed by EDX shows that the nanowires are mainly composed of Si. When the sample of nanowires is taken out from the growth chamber, it is exposed to atmosphere and the nanowires gets quickly oxidized and forms an amorphous layer over the nanowire surface. This is verified through EDX analysis which shows the presence of an O_2 peak. The surface and structural properties are studied through high resolution imaging and diffraction techniques respectively which will be discussed in the next sections.

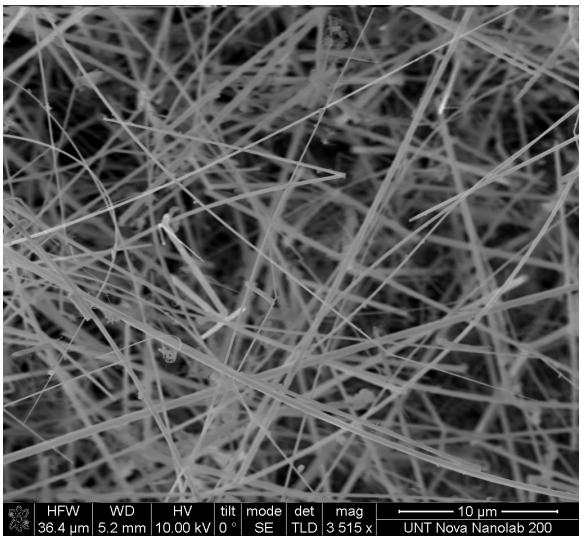

FIGURE 2.8. SEM image of Si nanowires grown on Si substrate at optimized growth conditions.

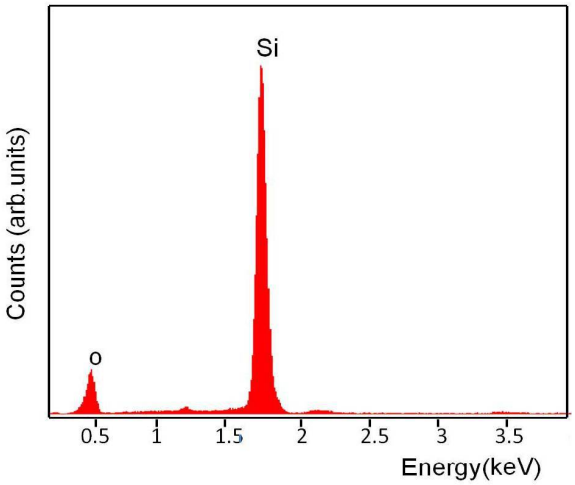

FIGURE 2.9. Stochiometric EDX spectrum of chemical composition of Si nanowires

2.6. Transmission Electron Microscopy Characterization

High resolution analytical capabilities provided by FEI Co. Tecnai G2 F20 S-Twin 200 keV transmission electron microscope (TEM) was used to observe the lattice structure and growth direction of the Si nanowires. The direct observation under high resolution transmission electron microscopy (HRTEM) of the cross-sections of nanowires is critical in the determination of the orientation and behavior of the growth of these nanowires as well as their internal structures and atomic arrangements. This information is important in

analyzing the properties in the nano-realm and ultimately, in the construction of nanodevices. Si nanowires were dispersed on a 3 mm copper grid by powder sample preparation technique which was performed at an accelerating voltage of 200 kV. HRTEM image of Si nanowires (Figure 2.10) shows that the nanowires are crystalline covered with surface of an amorphous oxide layer.

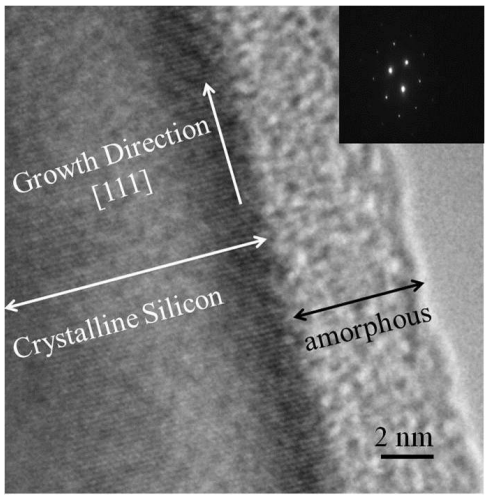

FIGURE 2.10. High resolution TEM image of a crystalline Si nanowire grown along [111] direction with amorphous shell of SiO_2 on the surface.Inset shows the SAED pattern.

The growth direction of Si nanowires is characterized by selected area electron diffraction (SAED). The electron beam was incident normal to the nanowire axis. Most of the long nanowires grown in [111] direction suggest that VLS growth mechanism favor this growth mode. The structure of the nanowire consisting of Si core and oxide shell is confirmed by high resolution TEM. An amorophus-oxide layer of 3-4 nm thickness was found on all the nanowires.

2.7. X-ray Diffraction Characterization

The Si nanowires were further characterized by using X-ray diffraction technique. X-ray diffraction (XRD) is a versatile, non-destructive technique that provides information about the chemical composition and crystallographic structure of various materials. The properties of a single crystal are not only a function of the type and quality of the crystal,

but strongly dependent on its orientation. The determination of orientation thus represents an essential step for using single crystals in technological applications. XRD has become the universal method for determining crystal orientation. High resolution XRD was performed with Rigaku Ultima III. Figure 2.11 shows the XRD spectrum of Si nanowires at room temperature. The characteristic of the sample is studied by plotting the angular positions and intensities of the resultant diffracted peaks of radiation pattern. Sample of as-grown Si nanowires shows clearly visible peaks of Si (111), (220) and (311) indicating the structure of crystalline lattice Si [34, 19] and a single peak corresponding to Si oxide [19].

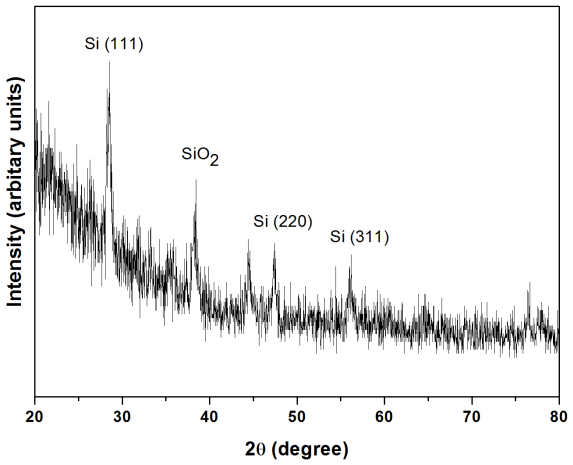

FIGURE 2.11. XRD spectrum of Si nanowires at room temperature. The peaks confirms the nanowires are crystalline Si.

2.8. Conclusion

Si nanowires are synthesized using CVD technique. The VLS mechanism involved in the growth of Si nanowires is discussed. Si nanowires are synthesized by vapor phase transport using $SiCl_4$ as precursor in $Ar+H_2$ environment. Synthesis of Si nanowires are sensitive to growth conditions and the factors effecting the growth were discussed. SEM observations showed that the nanowires have lengths of 30–40 μm and diameters of 40–100 nm. EDX spectrum reveals that the Si nanowires are crystalline and mainly composed of Si. HRTEM imaging with SAED analysis show that the nanowires grow along the [111] direction with

a thin layer of amorphous shell covering the surface. X-ray diffraction also confirms the crystalline structure of Si and the presence of SiO_2, which grows as an amorphous shell on the Si nanowire surface post growth. Based on our experiments, the optimum growth temperature of Si nanowires is determined to be 950°C, under a gas flow rate of 100 sccm. The Si nanowires were grown on a 20 nm thick Au seed layer.

CHAPTER 3

DOPING OF SILICON NANOWIRES WITH ANTIMONY

3.1. Introduction

Doping is the key for controlling the conductivity of semiconductor materials. Dopants are foreign atoms (impurities), which when added to a pure semiconductor alters its electrical properties. These impurities can be unintentional, or they can be added on purpose to provide free carriers in the semiconductor. These dopants can occupy substitutional positions and contribute free electrons or holes in to the Si lattice. The fifth group elements of the periodic table such as phosphorus (P) and antimony (Sb) have five valence electrons. A phosphorous (P) atom displaces a Si atom and the four valence electrons contribute to bond and there will be an excess electron. As the fifth valence electron is not bonded, the energy required to liberate this electron will be lower than the energy required to break the valence bond electron. Group V elements from the periodic table contribute electrons to group IV elements like Si, and hence they are commonly referred to as Donors. On the other hand, group III elements such as boron (B) or aluminium (Al) have three valence electrons. When substituted in Si lattice, the boron atoms form a bond with three neighboring Si atoms and one atom is left unbonded. An electron from the neighbouring atom will move into this hole and leave a hole behind. These dopants contribute holes and are referred to as Acceptors. Figure 3.1 represents the n-doped and p-doped Si lattice structures.

Doping of bulk materials is typically done during its growth, when dopant atoms are added to the melt from which bulk semiconductors are grown. However, doping of nanostructures is a complex process on account of its size and hence requires detailed study. If Si nanowires are to be reliable materials for nanoscale electronic devices, there has to be an

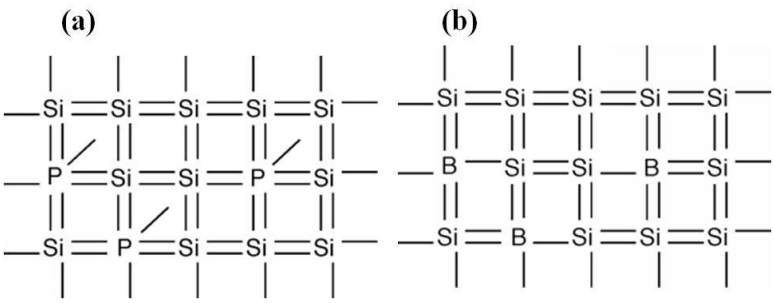

FIGURE 3.1. Lattice structure of (a) n-doped and (b) p-doped Si.

efficient control of the dopant type and concentration. Numerous strategies have been developed to dope Si nanowires; these include using the metal catalyst (seed layer in VLS growth) such as In, Ga or Al to cause doping in the Si nanowire [3]. Another way of doping is to add some dopant to a catalyst such as Au so that the dopant atoms would be diffused during growth [45]. But the feasibility of all these methods seems to be inefficient. The most reliable way to dope semiconductors during growth is to introduce the dopant during the growth so that control over the dopant type and density can be achieved. This can be accomplished either by the co-evaporation or co-ablation of dopant and Si in case of molecular beam epitaxy (MBE) and laser ablation respectively. In the CVD growth process, an easier doping route is to use gaseous sources of Si and the dopant. There have been reports on p-type doping of Si, using metalorganics such as diborane (B_2H_6), trimethylborane ($B(CH_3)_3$) [26]. Similarly, use of phosphine (PH_3) [58, 43] and trimethyl antimonide [41] have been reported for n-type doping of Si nanowires in a CVD growth process. Recently, post-growth bismuth doping has been reported for n- type doping [5]. In spite of these successful attempts, the process is not viable due to the toxicity of materials used and the need for sophisticated equipment.

In this chapter, the results of a novel technique to achieve doping of Si with Sb to form n-type Si nanowires is presented. The dopant atoms need to be diffused into the Si lattice to become electrically active. If the dopant atoms occupy interstitial sites or become trapped on the nanowire surface, though their presence will be detected during compositional analysis using EDX, the dopant atoms will be electrically inactive. Such inactive dopant atoms will not contribute to the electrical conduction process. The presence of doping impurities

displace the fermi level close to the band edges. Since, Sb is an n-type dopant in Si, this implies that Sb will introduce energy states closer to the edge of the conduction band in the energy band structure of Si. This is represented in Figure 3.2.

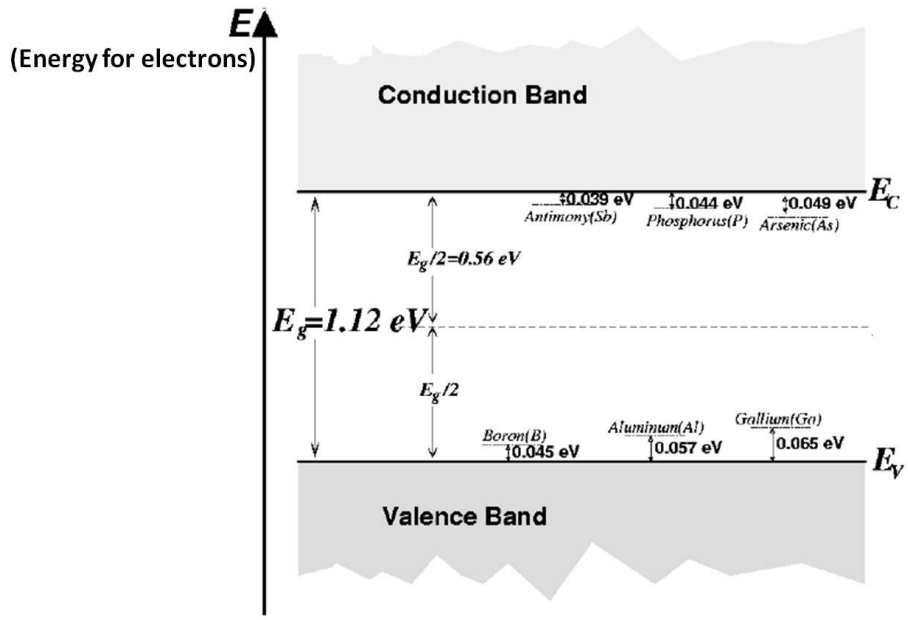

FIGURE 3.2. Donor and acceptor ionization energy levels in Si.

The growth procedure of Sb doped Si nanowires and optimization procedure are discussed in the following sections.

3.2. Synthesis of Sb-doped Si Nanowires

n- type doping of Si nanowires was achieved by using Sb as the dopant, following two strategies:

(i) Doping during growth

(ii) Doping after growth (post-growth)

3.2.1. Doping During Growth

To fabricate n-type Si nanowires, vapor phase doping was performed using Sb vapor. Sb has relatively high vapor pressure and hence Sb doping was achieved by incorporating Sb atoms into the growing Si nanowire during growth. For Sb doping during growth, pure

Sb was heated at 900°C at atmospheric pressure in a quartz tube with the substrate at the same temperature in the Ar+H_2 gas mixture. $SiCl_4$ was bubbled into the growth tube similar to the procedure described for the synthesis of undoped Si nanowires. Following the doped growth process of Si nanowires, the substrate was taken out and studied using EDX analysis; the results are shown in Figure 3.3.

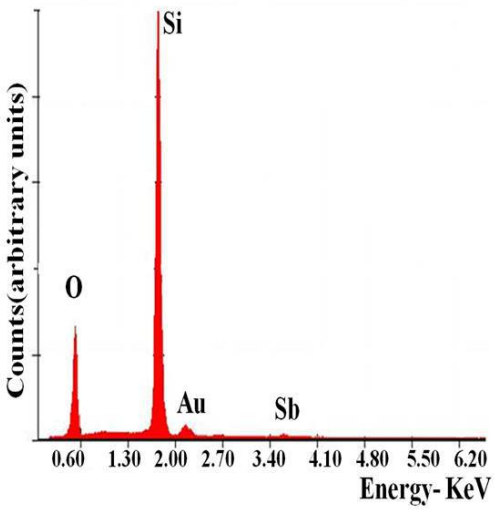

FIGURE 3.3. EDX image of Sb doped Si nanowires; Sb atoms added during growth. The Sb content is estimated to be about 1 wt%.

EDX analysis confirms the presence of Si, O and trace amounts of Sb. The Sb concentration is found to be $\approx$ 1 wt% under these growth conditions. This was considered relatively light doping and not significant enough to modify the conduction mechanisms in the Si nanowire.

Hence, an alternate technique that involved post-growth doping of Si nanowires was designed. The experimental procedure and the results are discussed in the next section.

3.2.2. Doping After Growth (Post-Growth)

Due to the low levels of Sb doping achieved in doping during growth, the nanowires were annealed in Sb vapor at temperatures ranging from 450°C to 900°C, to enable post-growth vapor diffusion of Sb into the Si nanowires. In this technique, Sb was diffused into the Si nanowires using a post-growth diffusion process, at various temperatures. This process was

done for 30 min in Ar environment. This was done to study the dependence of temperature on the doping content of Sb. The Sb content was found to change with temperature. The as-grown Si nanowires were returned to the growth chamber post-growth. This was done almost immediately to prevent the growth of a thick oxide shell. A solid source of Sb was also placed in the furnace, along with the as-grown Si nanowires; as shown in Figure 3.4. The temperature is maintained at 900°C for 30 min. From the EDX analysis, the Sb concentration is found to be $\approx$ 2 wt%. Postgrowth doping at 900°C and doping during the growth yielded approximately same amount of Sb content. As the post-growth doping temperature was reduced, the Sb content in the Si nanwoires was found to increase and finally at 450°C, we observed an increase in the Sb concentration upto $\approx$ 4 wt% (Results shown in EDX analysis as shown in Figure 3.5).

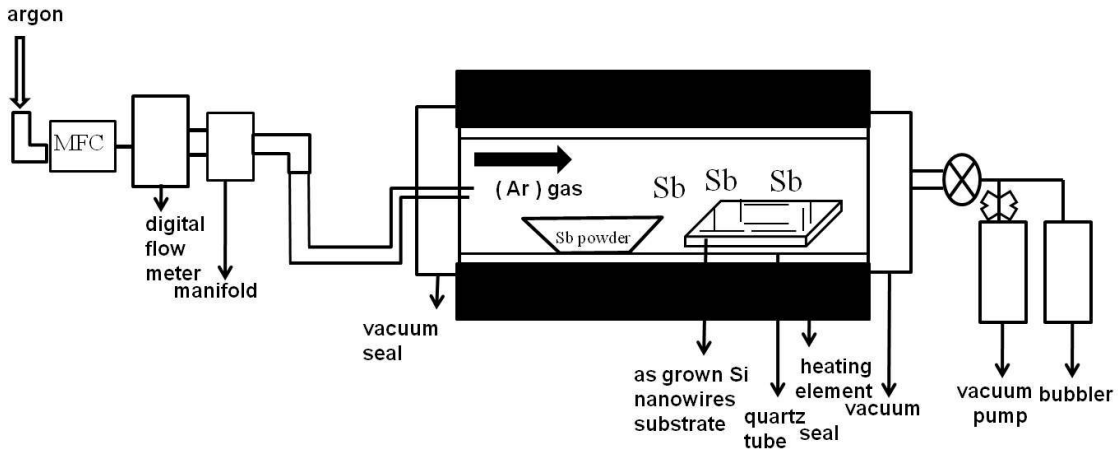

FIGURE 3.4. Schematic of postgrowth diffusion of Sb as dopant.

The decrease in concentration of Sb with increase in temperature is attributed to the re-evaporation of Sb from the growing nanowire because of its higher vapor pressure [39]. Sb doping of Si nanowires post-growth was done immediately after growth of the Si nanowire, which ensures that the amorphous oxide shell (if any exists) is too thin and does not significantly effect the diffusivity of Sb into the Si core. The process of diffusion that enables doping of Sb is discussed in the following section.

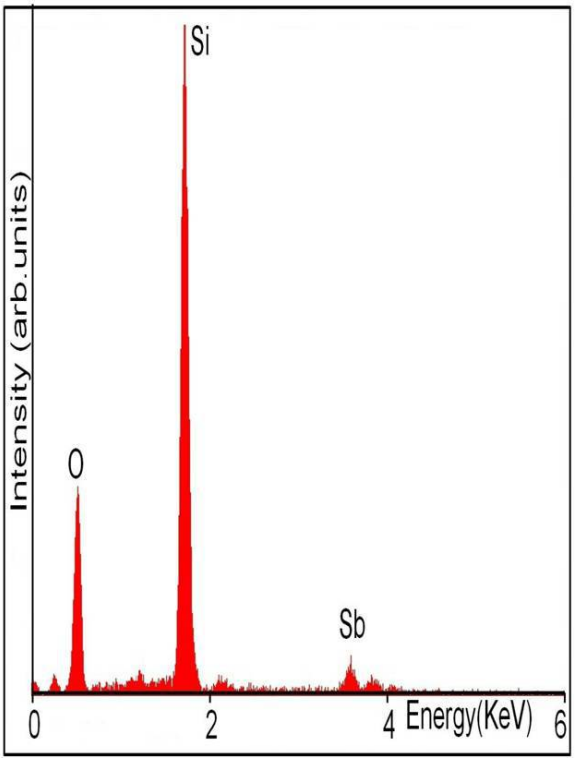

FIGURE 3.5. EDX of the Sb doped Si nanowires. Sb atoms added during postgrowth. The Sb content is estimated to be about 3–4 wt%.

3.2.3. Diffusion

Diffusion is the process of spreading a localized substance through out the medium due to random thermal motion. The diffusion of impurity occurs through the host material (Si), when the impurity either move around Si atoms or displace Si atoms. Diffusion in Si is directly associated with native point-defects and impurity-related defects. Impurity related defects arise from the introduction of group-III elements or group-V elements into the Si lattice. The diffusion of impurities takes place through vacancy, interstitial or a combination mechanism known as interstitialcy. The exchange of lattice positions by substitutional atoms with a vacancy, is known as vacancy diffusion. Interstitial diffusion takes place when an interstitial atom jumps to another interstitial position. Interstitialcy diffusion results from Si self interstitials displacing substitutional impurities to an interstitial position, which may then knock a Si lattice atom into a self-interstitial position. Any substitutional dopant in Si should diffuse through either a pure vacancy or pure interstitialcy mechanism. Figure 3.6

shows the vacancy, interstitial and interstitialcy mechanisms of diffusion.

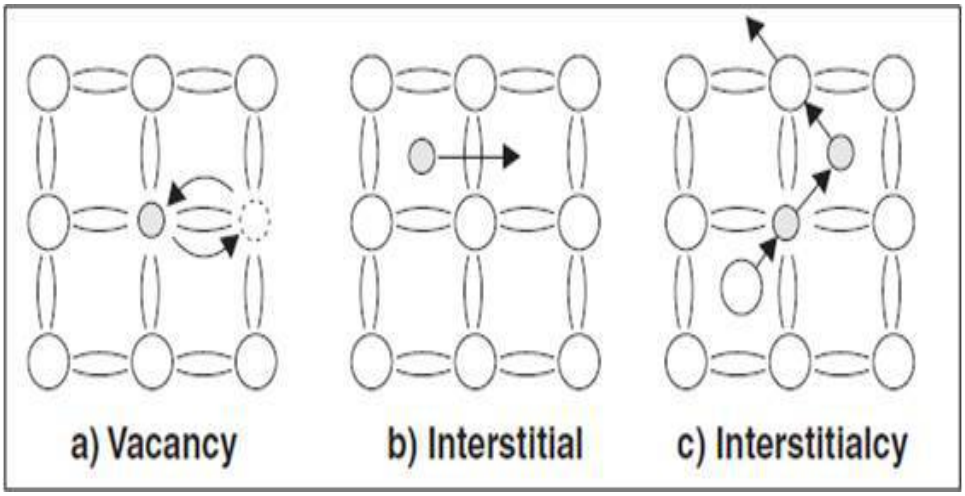

FIGURE 3.6. Vacancy, Interstitial and Interstitialcy diffusion mechanisms.

Breaking bonds of the lattice is a relatively high energy process and substitutional atoms tend to diffuse at much lower rate than interstitial atoms. The diffusion process is characterized by a barrier with activation energy E_a, where E_a is the energy required to jump from one site to next site. The temperature dependence of diffusivity will take the Arrhenius form as:

$$D = D_0 \times e^{-Ea/(kT)} \tag{4}$$

where D_0 is pre-exponential constant, T is absolute temperature in kelvin and k is Boltzman constant.

3.2.4. Diffusion of Sb in Si

Diffusion of Sb in Si is purely through vacancy mechanism. The intrinsic diffusivity of Sb is given by

$$D_i = 0.214 \times e^{-3.65/(kT)} cm^2/s \tag{5}$$

Sb has a large tetrahedral radius of 0.136 nm and a lower activation energy. From the Figure 3.7, the diffusivity of Sb in Si is found to be $1 \times 10^{-28} cm^2 s^{-1}$ at 450°C and increases

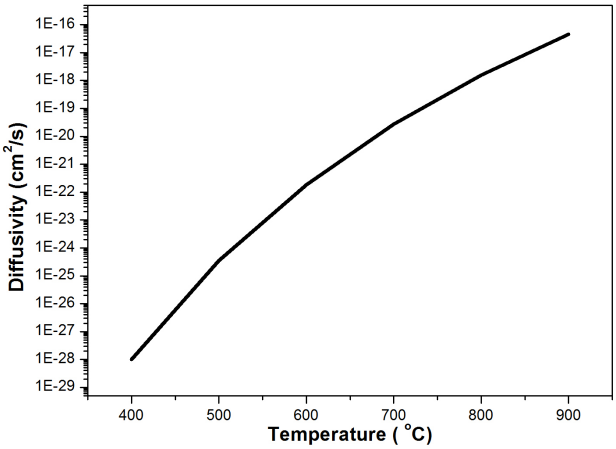

FIGURE 3.7. Diffusivity of Sb in Si versus temperature.

up to $1 \times 10^{-17}\text{cm}^2\text{s}^{-1}$ at 900°C. Thus, we expect that at high temperature, more Sb atoms should diffuse into the Si nanowire. However, at high temperatures, there is a competing mechanism, whereby Sb atoms that have diffused into the Si nanowire re-evaporate from the growing crystal. This occurs due to increased vapor pressure of Sb at high temperatures, leading to a decrease in the Sb content. At lower temperatures, the diffusivity is lower, but the re-evaporation of Sb from Si is minimized. This leads to most of the sb that have diffused into Si remaining in the crystal.

The Sb (wt%) content is determined in terms of donor concentration as follows:

From the diamond cubic lattice structure of Si, the number of atoms in unit cell can be determined. The lattice consists of 4 atoms inside the cell and the 8 atoms on the corner are shared among the cells contribute 1 atom inside the cell and the 6 atoms among the faces are shared among 2 cells counts for 3 atoms inside the cell,comprising of total 8 atoms inside the cell. The cell volume V is determined by

$$\text{V} = \text{a}^3 \tag{6}$$

Where a = 0.543 nm is the lattice constant and the volume of the cubic cell is found to be $1.6 \times 10^{-22}\text{cm}^{-3}$.

The density of Si atoms (n) is given by

$$\text{n} = \frac{\text{number of atoms in the cubic cell}}{\text{V}} \tag{7}$$

where no.of atoms in unit cell is 8. The density of the atoms is found to be $5 \times 10^{22}\text{cm}^{-3}$.

The Sb doping content in Si determined by EDX (4 wt%) in terms of Sb donor concentration is determined as follows:

$$\text{Sb concentration corresponding to 4 wt\%} = \frac{\text{No.of Si atoms} \times \text{amu of si} \times 0.04}{\text{amu of Sb}} \tag{8}$$

Where (amu) is atomic mass unit. amu of Si is 28 , amu of Sb is 121.8 and no.of Si atoms is $5 \times 10^{22}\text{cm}^{-3}$. The donor concentration is found to be $4.6 \times 10^{20}\text{cm}^{-3}$.

Even though the donor concentration indicates the number of Sb atoms in the Si, all these atoms would not contribute to the conductivity. Some of these atoms become trapped at the Si-SiO_2 interface or occupy interstitial sites and hence and would be inactive. Therefore, an indirect way of to calculate the number of active dopants is through electrical transport measurements which will be discussed in the next chapter.

3.3. Conclusion

In summary, n-doped Si nanowires were synthesized by vapor phase transport using $SiCl_4$ as source and Sb as dopant. The concentration of Sb in the Si nanowire was found to be highly dependent on the doping temperature. Post-growth diffusion of Sb into the Si lattice was considered a more effective route to achieve n-type doping of Si. The decrease in Sb with increase in temperature is attributed to the re-evaporation of Sb from the Si nanowires. The doping conditions were optimized to obtain an optimum doping content of 3–4 wt%, achieved by post-growth diffusion of Sb at 450°C into the Si nanowires, corresponding to an Sb concentration of $4.6 \times 10^{20}\text{cm}^{-3}$.

CHAPTER 4

ELECTRICAL CHARACTERIZATION OF SILICON NANOWIRES

4.1. Introduction

Electrical transport measurements provides information about the electronic structure and behavior of charged carriers in an electric field. The large surface to volume ratio of Si nanowires could potentially be important in influencing their transport properties. This phenomena could be exploited through Si nanowire functionalization. The conductivity of majority carriers in Si nanowires is dependent on the overall charges trapped in its crystalline core. One powerful configuration for studying electrical transport is the field effect transistor (FET). FET is the most important and basic device structure widely used in microprocessors and memory devices.

A gate electrode is used to vary the electrostatic potential of the Si nanowire while measuring current versus voltage of nanowire. The change in the conductance as a function of gate voltage can be used to distinguish whether a given nanowire is n or p type. The conductance will vary oppositely for positive and negative gate voltages. Effects of doping have been investigated by electrical transport measurements.

A p-type and n-type Si nanowire are connected to the both ends of the metal electrodes as shown in the Figure 4.1. As for conventional metal semiconductor interface, the Si nanowires bend above for p-type and down for n-type to align Fermi levels with respect to metal contacts. When the gate voltage is greater than zero volts, the bands are lowered, depleting holes in p-type doped and suppresses conductivity, whereas it leads to accumulation of electrons in n-type Si nanowires and enhances conductivity. Contrary, when the gate voltage is less than zero i.e at negative gate voltages, the band level is raised, increasing the conductivity in p-type and decrease of conductivity in n-type.

The observed gate dependence can be understood by referring to the schematics as shown in Figure 4.1 which shows the effect of gate voltage on Si nanowire bands [9].

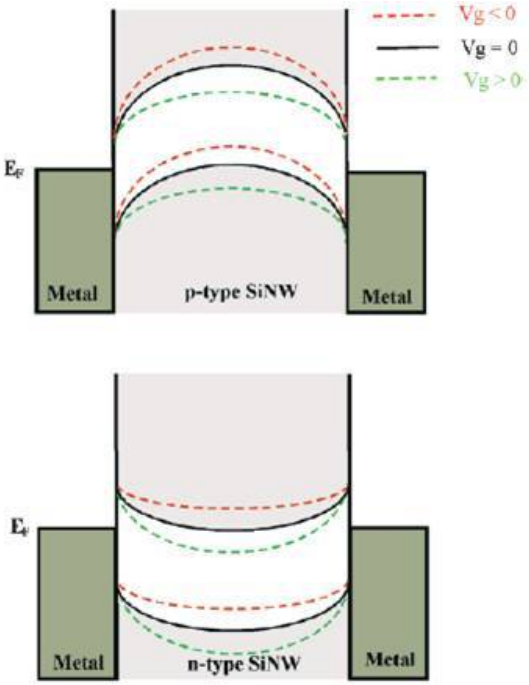

FIGURE 4.1. Energy band diagrams for p-type and n-type Si nanowires.

4.2. Design of FET

The electrical behavior of undoped Si nanowires is determined by the FET configuration using nanowires as active regions as shown in Figure 4.2. A thin layer of 200 nm SiO_2 grown on Si (110) wafer acts as dielectric. The underlying conducting Si functions as global back gate electrode to vary the electrostatic potential of nanowire. Prior to making source and drain contacts, these substrates were cleaned with acetone followed by alcohol and rinsed with deionized water to eliminate any contaminants on the surface. As grown Si nanowires from the growth substrate are transferred to the FET substrate by gentling pressing each other. Source and drain contacts were established to the nanowire by using Au contacts, as shown in Figure 4.3. The nanowire acts as a channel between source and drain. Transport measurements were performed on the undoped and doped nanowires having an amorphous

oxide layer on the surface. Electrical measurements are performed with Agilent B1500 semiconductor device analyzer at room temperature.

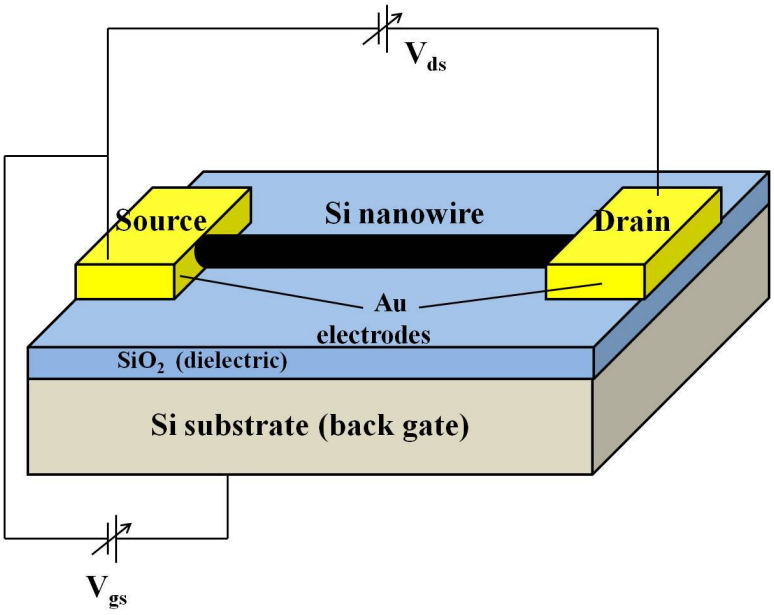

FIGURE 4.2. Schematic of a nanowire FET with a Au source and drain contacts on a SiO_2 surface.

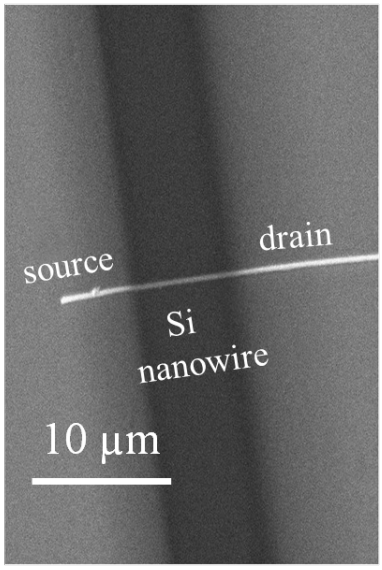

FIGURE 4.3. SEM image of the Si nanowire FET.

4.3. Transport Measurements of Undoped Si Nanowires

The current voltage characteristics are obtained by applying a range of voltages, varying from -250 mV to +250 mV, across the source and drain terminals (V_{ds}) and measuring current through the nanowire. Initial I-V measurements showed a Schottky behavior, arising due to the metal-semiconductor barrier. A Schottky contact to the Si nanowire would produce a nonlinear relationship between I and V, and the current I through the nanowire at zero bias would exhibit thermally activated behavior. In particular, a large mismatch between the Fermi energy level of the metal and semiconductor can result in a high-resistance rectifying contact. Most metal-semiconductor contacts are annealed or alloyed after the initial deposition of the metal in an effort to further improve the contact resistivity. Annealing is the process of creating ohmic contacts at higher temperatures, in an ambient environment, which reduces the unintentional barrier at the metal-semiconductor interface. The effect of annealing on the nature of contacts made to Si nanowires has been reported by several groups [10, 37]. The device was subsequently annealed in Ar environment at 300°C for ≈ 5 min to create ohmic contacts. After annealing, the I-V curves are linear which indicates that the contacts are very nearly ohmic and the contact resistance is assumed to be negligible compared to the nanowire resistance. The resistivity is measured to be 0.23 Ω-cm from the I-V characteristics (i.e $V_{gs} = 0$) for the Si nanowire of radius 45 nm and length 10 μm.

The electrical characteristics were further assessed with back gate geometry for the same undoped Si nanowire. Transport measurements of undoped Si nanowire in Figure 4.4, shows the dependence of drain-source current (I_{ds}) on drain-source voltage (V_{ds}) at zero gate bias ($V_{gs} = 0V$). Figure 4.5 shows the gate dependence on I_{ds} at fixed drain voltage of $V_{ds} = 0.25$ mV. This dependence shows that the conductance of the undoped Si nanowire decreases as V_{gs} becomes more positive, indicating a p-channel FET behavior. The weak gating characteristics results in negligible changes in current even with significant change in gate voltage (V_{gs}) due to unintentional doping of Si nanowire. We thus conclude that the undoped Si nanowire exhibit a p- type behavior, the origin of which is attributed to the presence of

native defects. Schottky defects (vacancies) and interstitial defects in bulk Si has been established by numerous studies and have been reported to co-exist at high temperatures [36], with defect concentrations of the order of $2 \times 10^{16}\text{cm}^{-3}$ in bulk Si. There is also the possibility that the undoped sample showed p-type conduction, which could be attributed to the nucleating metal itself, i.e. Au, which is known to be a p-type dopant in Si. Au in Si acts as a scattering center and the effect of acceptor levels induced the p-type behavior in the undoped Si nanowires [18].

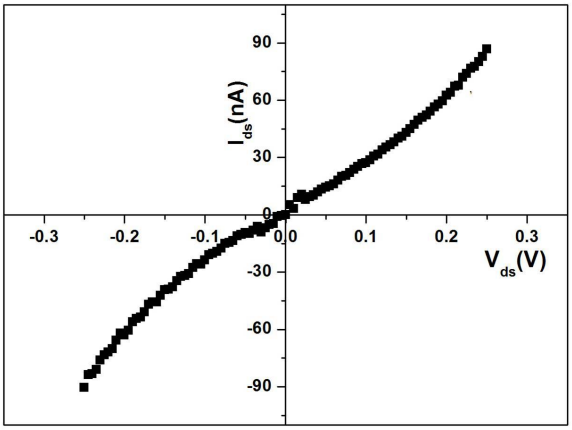

FIGURE 4.4. I_{ds}-V_{ds} data of as-grown Si nanowire FET at zero gate bias.

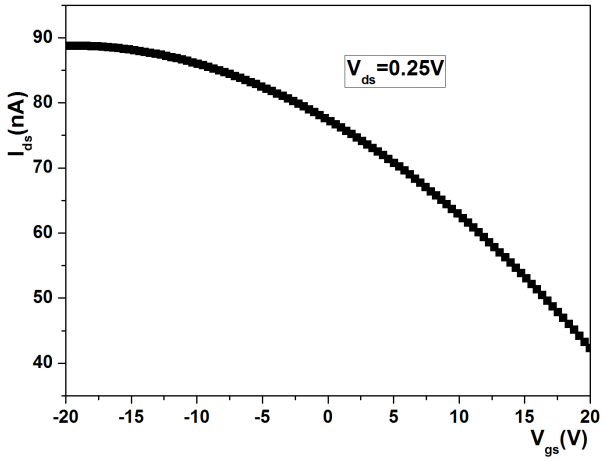

FIGURE 4.5. I_{ds}-V_{gs} graph at fixed $V_{ds} = 0.25$V.

4.4. Transport Measurements of Sb Doped Si Nanowires

Transport measurements were also performed on a single Sb doped Si nanowire and the results in Figure 4.6, shows the dependence of current (I_{ds}) on voltage (V_{ds}) at three different gate bias voltages (V_{gs}).

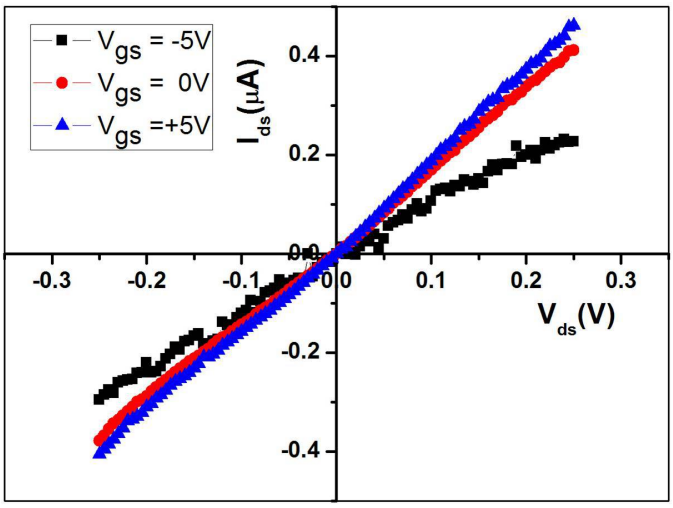

FIGURE 4.6. I_{ds}-V_{ds} data plotted for an Sb doped Si nanowire FET for different gate voltages shows n-type behavior.

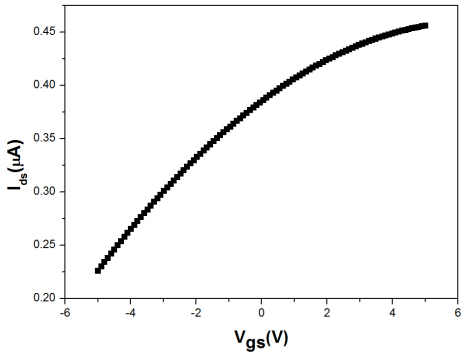

FIGURE 4.7. I_{ds}-V_{gs} data plotted for an Sb doped Si nanowire FET for a fixed gate voltage V_{ds} = 0.25V.

The variation in current I_{ds} was studied for V_{gs} varying from -5 V to + 5 V is shown in Figure 4.7 and it was found that the conductance increases with increase in positive gate voltage V_{gs}. This characteristic is typical of n-channel FET. These results confirm that Sb was incorporated as an active dopant into the Si nanowire. In addition, the magnitude of

the current in the Sb doped Si nanowire is approximately 10 times higher than that of the undoped Si nanowire of approximately the same diameter. Transconductance from the slope of I_{ds}-V_{gs} graph plotted in Figure 4.7 is estimated to be 37 nS for the Sb doped Si nanowire.

4.5. Determination of Intrinsic Parameters for Undoped and Sb-doped Si Nanowires

Intrinsic parameters such as transconductance (g_m), field effect mobility (μ_{FE}) and carrier concentration (n) are the crucial parameters in determining the electrical characteristics which will aid in device design.

The field effect mobility [51] was estimated using the following equation:

$$\mu_{FE} = \frac{(\delta I/\delta V_g)L^2}{CV_{ds}} \tag{9}$$

where $\delta I/\delta V_g$ is the measured transconductance from the experimental values, C is the gate capacitance and L is the channel length. An analytical estimate for the capacitance is found by means of finite element method. The traditional metallic cylinder on an infinite metal plate model [2] assumes that nanowires are completely embedded in the dielectric and posses a circular cross section. The absence of the dielectric material on the top surface of the non embedded nanowire, yields only the upper limit of the gate capacitance using the infinite metal plate model. Hence an alternate approach which takes all these conditions into account is the finite element method [57].

$$C = \frac{2\pi\epsilon_{eff}\epsilon_0 L}{\text{arccosh}((t_{ox} + R)/R)} \tag{10}$$

The effective dielectric constant of $\epsilon_{eff} \approx 2.2$ is considered for the SiO_2 back-gate dielectric instead of the relative dielectric ($\epsilon_r \approx 3.9$) of SiO_2 considering the theory of finite element method, ϵ_0 is the permitivity of the free space, $t_{ox} = 200$ nm is the dielectric thickness, $L = 10$ μm is the distance between the electrode contacts and $R = 45$ nm is the radius of nanowire. The gate capacitance is found to be 51.37×10^{-17} F. Transconductance of the undoped single Si nanowire was estimated from the slope of I_{ds}- V_{gs} graph plotted in

the Figure 4.5 and is calculated to be 5.23 nS. The weak gating translates into a field effect mobility of 40 $cm^2V^{-1}s^{-1}$. The carrier concentration n of undoped Si nanowire is determined by

$$n = \frac{1}{q\rho\mu} \tag{11}$$

Where $q = 1.6\times10^{-19}$ coulombs is the charge of the carrier, $\rho = 0.23$ Ω-cm is the resistivity and $\mu = 40$ $cm^2V^{-1}s^{-1}$ is the mobility of undoped Si nanowire. The carrier concentration is found to be $7 \times 10^{17}cm^{-3}$. Using the same equations, the mobility of the Sb doped Si nanowire is found to be 288 $cm^2V^{-1}s^{-1}$ from the equation (9) with the transconductance of 37 nS. Hence the carrier concentration is found to be $5.3 \times 10^{18}cm^{-3}$ from equation (11) with resistivity $\rho = 0.0041$ Ω-cm. This carrier concentration will indicate the active number of Sb atoms contributing to the conductivity. Comparing the Sb doping content (4 wt% by EDXS) to the electrically determined carrier concentration ($5.3 \times 10^{18}cm^{-3}$), we estimate the degree of impurity ionization to be of the order of 1–2 %.

4.6. Conclusion

Si nanowire FET device was fabricated using a single Si nanowire contacted by Au electrodes, to determine the electrical characteristics of the nanowires. We show that the as-grown Si nanowires were intrinsically p-type. This p-type behavior is ascribed to the presence of native defects. There is also the possibility of unintentional Au doping which could be attributed to the nucleating metal itself, i.e. Au, known to be a p-type dopant in Si. The as-grown Si nanowires were subsequently doped with Sb. The n-type behavior of Sb doped Si nanowires was also confirmed through transport measurements. We thus show that the majority carriers in the as-grown nanowires can be compensated by the Sb dopant species.Table 4.1 is a summary of intrinsic parameters from our experimental findings, using Au as the metal catalyst.

TABLE 4.1. Intrinsic parameters of undoped and doped Si nanowires

Intrinsic parameters	Undoped Si nanowires	Sb doped Si nanowires
Type	p-type	n-type
Resistivity (ρ)	0.23 Ω-cm	0.0041 Ω-cm
Transconductance (g_m)	5.23 nS	37 nS
Field Effect Mobility (μ)	40 $cm^2V^{-1}s^{-1}$	288 $cm^2V^{-1}s^{-1}$
Carrier concentration (n)	$7 \times 10^{17} cm^{-3}$	$5.5 \times 10^{18} cm^{-3}$

CHAPTER 5

OPTICAL CHARACTERIZATION OF SILICON NANOWIRES

5.1. Photoluminiscence Measurements on Si Nanowires

5.1.1. Introduction

The optical properties of Si nanowires were investigated by photoluminescence (PL) spectroscopy measurements. The emission of light by a substance through any process other than blackbody radiation is referred to luminescence. The emission of light can result from variety of stimulations. For example, the light emission resulted from electronic stimulation, is referred to as cathodoluminescence (CL). In X-ray fluorescence, high-energy photons, i.e. X-rays, are used to excite the sample. In PL spectroscopy, the intensity of emitted light is measured as a function of wavelength. Light is emitted from a semiconductor as a result of radiative recombination of electron-hole pairs that have been optically excited. The carriers are first optically excited by light (photons) with energy greater than or equal to the band gap of the semiconductor. The excited electrons return to a lower energy state and if they do so by radiative means, the process emits a photon whose energy is the difference between the energies of the two states, which corresponds to the near band edge luminescence. The spectral distribution of the emitted photons shows an emission peak at the energy (or wavelength) corresponding to each excited level. PL spectroscopy is a useful tool to determine the optical quality of semiconductors. In these measurements, light is used as a source of excitation, and the emitted luminescence is collected by a lens and passed through an optical spectrometer on to a photon detector. The spectral distribution and time dependence of the emission are related to electronic transition probabilities within the sample. Spectral distribution provides information about chemical composition, structure,

impurities, kinetic process and energy transfer.

The two pre-requisites for luminescence are:

(i) The luminescent material should have a semiconductor structure with non-zero band gap (E_g).

(ii) The semiconductor must absorb the light for the luminescence to take place.

When a free electron from the conduction band recombines radiatively with a free hole from the valence band, this recombination process is a band-to-band recombination. Most semiconductors have impurity or defect states that introduce energy levels close to the band edges. Energy levels that lie close to and below the conduction band edge are referred to as donor levels and those close to and above the valence band edge are referred to as acceptor levels. These levels in the band gap provide alternate paths for recombination. When both the excited electron and hole are captured by different impurity centers and then the trapped electron and hole recombine radiatively, the process is a donor-acceptor pair (DAP) recombination. Emission bands thus appear in the low energy region of the spectrum resulting from recombination of electron and hole pairs captured at acceptor and donor sites respectively. Recombination of this type reflects the energy difference between the donor and acceptor levels involved in the recombination process.

5.1.2. Energy Levels in Si

Si is an important semiconductor material and has an indirect band gap with low light emission efficiency. The electron band gap structure of Si is shown in the Figure 5.1 where energy (E) versus wave vector (k) is plotted [33]. For the Si energy band structure, the maximum in the valence band occur at k = 0 and minimum in the conduction band does not occur at the same value of k = 0. A semiconductor whose maximum valence band and minimum conduction band does not occur at the same value of k is defined as indirect band gap semiconductor. Bulk crystalline Si has relatively small and indirect energy band gap which normally hinders the efficient inter band radiative recombination and emissions are

restricted to infrared part of the spectrum. Si near-band-gap luminescence consists of a single weak band at 1.1 eV at room temperature.

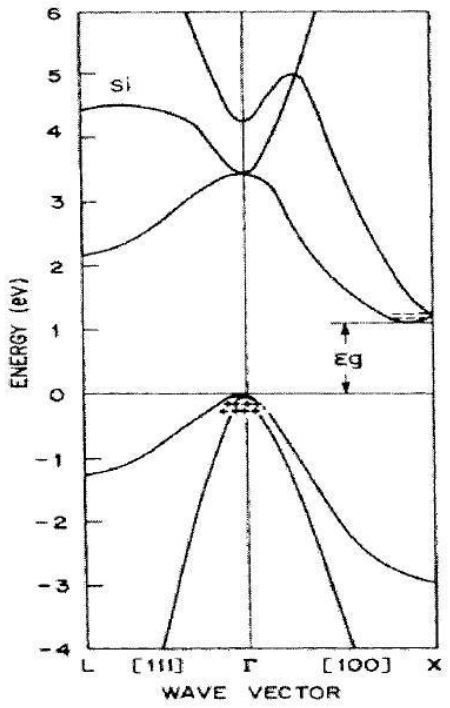

FIGURE 5.1. Electron band gap structure of Si.

5.1.3. PL in Si Nanowires

Semiconductor nanowires offer many interesting opportunities for the assembly of optoelectronic devices. Si nanowires are emerging as a powerful class of materials through controlled growth and organization, which opens up ample opportunities for novel nanoscale photonics. Numerous studies have been performed in order to understand the physical mechanism involved in PL phenomenon in Si for promising optoelectronic and photovoltaic applications. Si at nanoscale dimensions becomes a direct-band gap semiconductor due to quantum confinement effects. This property enables Si nanowires to exhibit visible PL at room temperature.

The PL measurements performed on our Si nanowires have two constraints:

(i) The radius of the as-grown Si nanowires were greater than Bohr's radius of Si,hence effects of quantum confinement were not observed. It is possible to grow these nanowires thinner by using Au colloids as the metal catalyst or by etching the nanowires to make them thinner.

(ii) The PL facilities available at the University of North Texas are limited to detection below 1000 nm.

We do not observe near band edge emission for Si nanowires of diameters (80-100 nm) because of these constraints. Hence we expect the visible PL spectra to originate from amorphous oxide layer and defects residing on the nanowire surface. To investigate the effect of amorphous oxide on the optical properties, PL measurements were done with and without the amorphous oxide layer on the surface of the nanowire. The amorphous oxide layer was subsequently removed by etching for 10-20 seconds in diluted liquid HF solution (1 HF (49%):20 de-ionized H_2O) [22]. A He-Cd (325 nm) laser at room temperature was used as the excitation source to characterize the PL properties of the sample. Figure 5.2 shows the experimental setup for measuring the PL spectrum.

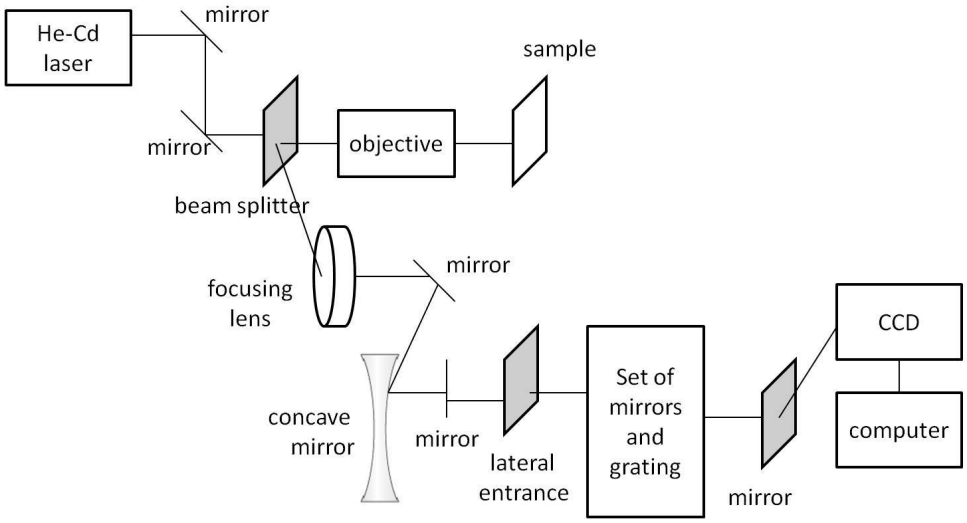

FIGURE 5.2. Experimental setup for the PL measurements.

The laser is passed through a set of mirrors before hitting the sample and the emitted spectrum is passed through a set of mirrors and lenses and collected through a CCD connected

to a computer for data analysis. Figure 5.3 shows the PL spectra of Si nanowires at room temperature before and after etching with HF.

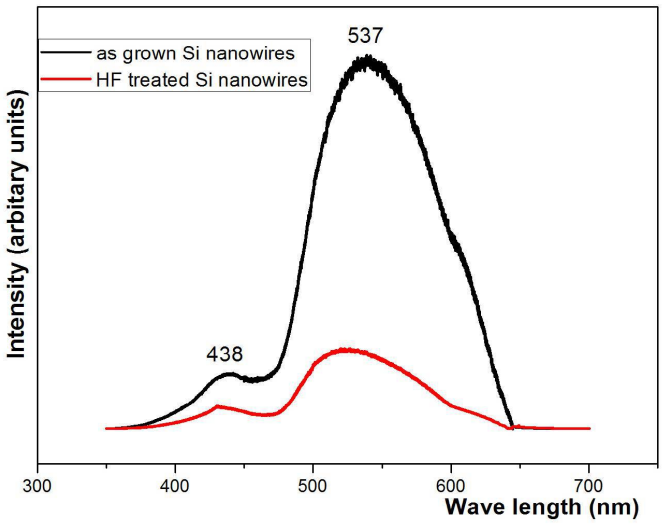

FIGURE 5.3. Green emission of the PL spectrum of Si nanowires before and after HF etch.

Two strong broad emission peaks were observed at 438 and 537 nm. Comparison of the emission spectra before and after the HF acid etch shows that there was no significant change in the emission wavelength of the two peaks; however a huge reduction in the intensity of both peaks were observed. We attribute the peaks observed at 438 nm and 537 nm to the presence of the oxide shell and to defects residing on this shell. This is the reason why, when the amorphous shell is etched or its thickness considerably reduced, we observe a decrease in the intensity of these peaks. According to the theoretical prediction, the near band edge emission due to size confinement can occur only when the mean size of the Si crystalline is less than that of free exciton or Bohr radius of Si. The observed green and near blue band peaks in Figure 5.3 are related to the radiative recombination of defect centers that occur in the outer oxide shell and to the formation of siloxenes and their derivatives [49]. Defects such as oxygen vacancies [42] existing at the interface between the Si crystalline core and the amorphous oxide layer is believed to be the source of these blue-green emission.

5.1.4. Conclusion

Photoluminescence measurements on Si nanowires were performed and a visible green emission is observed. This visible emission is not attributed to near band edge emission from crystalline Si. This is confirmed by a comparison of the PL spectrum on the as-grown nanowires and the spectrum obtained after the amorphous oxide on the nanowire surface has been etched off. This comparison shows that there was a huge reduction in the intensity of the emitted light from the etched Si nanowires, as compared to that of the as-grown ones, which indicates that these peaks arises from the amorphous oxide on the Si nanowire.

5.2. Raman Spectroscopy on Si Nanowires

5.2.1. Introduction

When a beam of light is incident on a material, a part of it is transmitted, a part of it is reflected and a part of it is scattered. Classic concept of Raman scattering is shown in Figure 5.4. Raman spectroscopy is based on inelastic scattering of monochromatic light in the visible or near visible ranges.

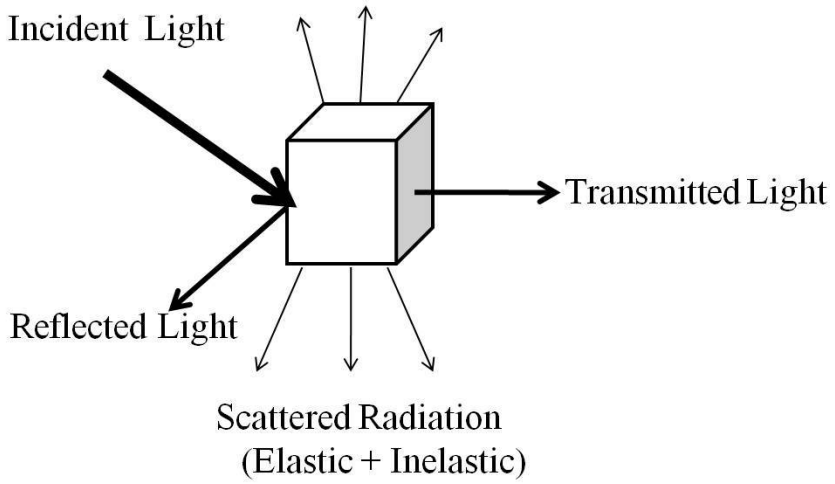

FIGURE 5.4. Classic concept of Raman scattering.

Commonly, a laser is used as a source of monochromatic light to stimulate the molecules to a higher energy virtual state of excitation. When this light interacts with the sample, photons are absorbed by the sample and remitted, resulting in a change of frequency. The

shift in the frequency of re-emitted photons, when compared to the original frequency of monochromatic light is called Raman Effect. Normally, a sample is illuminated with a laser beam and the scattered light is collected with a lens and is sent through interference filter or spectrophotometer to obtain Raman spectrum of a sample. Raman spectrum is used to study micro structure of materials using their vibrational properties. Molecular vibrations alter the wavelength and intensity of the scattered light, providing information about the material. Raman spectroscopy can be used to examine solid, liquid and gaseous samples. Raman spectroscopy is a versatile and non-destructive technique for characterizing semiconductor materials, enabling assessment of crystalline quality of a material, lattice structure. Hence Raman spectra of Si nanowires assist in further understanding of the composition of Si nanowires.

5.2.2. Raman Spectra of Si Nanowires

The Si nanowires grown in our experiment are covered with amorphous surface as observed in the HRTEM images described in Chapter 2. In order to ascertain the composition of the amorphous shell, Raman measurements were made on the Si nanowires with Nicolet Almega XR Raman Spectrometer at room temperature using a green laser with an excitation wavelength of 532 nm. To eliminate contributions from the Si substrate, the Si nanowires were transferred onto a quartz substrate. Figure 5.5 shows the first-order optical phonon mode of single-crystalline Si peak with a slight red shifted peak at 519 cm^{-1}. The characteristic Raman peak at 519 cm^{-1}, which indicates size confinement effects has no effect on the frequency downshift. The slight shift in the frequency is due to the heating of the laser used for Raman measurements [40]. Additional peaks at 465 cm^{-1} and 481 cm^{-1} are attributed to the amorphous Si oxide shell [48], which has Raman scattering between 400 cm^{-1} and 550 cm^{-1}. The amorphous oxide layer was subsequently removed by etching for 40-60 seconds in diluted liquid HF solution [22] (1 HF (49%):20 de-ionized H_2O which was enough to remove amorphous oxide of ≈ 3 nm. Figure 5.6 reveals a single peak at 516 cm^{-1}, arising from the crystalline core of the Si nanowires. This shift could be due to the size effect

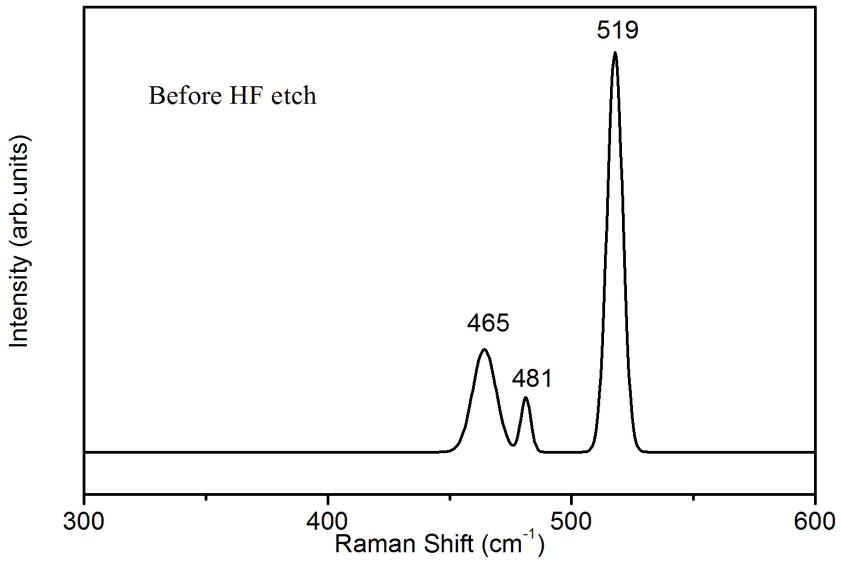

FIGURE 5.5. Raman spectra of as-grown Si nanowires at room temperature with Raman peaks corresponding to crystalline Si and amorphous oxide.

of Si surface defects, observed by HRTEM. There is no obvious Raman frequency down-shift caused by the size confinement effect in the etched nanowires also. It is known that the size confinement effect will not significantly affect the electron and phonon properties of crystals unless their size is less than the Bohr radius of Si, i.e 5 nm at room temperature. As the average diameter of Si nanowires in our sample is greater than 10 nm, we donot observe any significant frequency down-shift caused by the size confinement effects. The absence of amorphous oxide peak, in the Raman spectra of Si nanowires after etch reveals that the nanowires are pure crystalline. Post-etching, the diameters of the Si nanowires are reduced which accounts for the higher red shift and an asymmetric broadening of the line width which is attributed to phonon spatial confinement effects and lattice stress effects [40, 7]. As the crystal decreases to nanosize, the spatial wave function of optical phonon is confined which indicate that the Raman scattering is not confined to Brillouin zone center. The optical phonon vibrational frequency ω at the point Γ decreases with increase in wave vector and the Raman peak downshifts. The different coordination of atoms on the surface of a

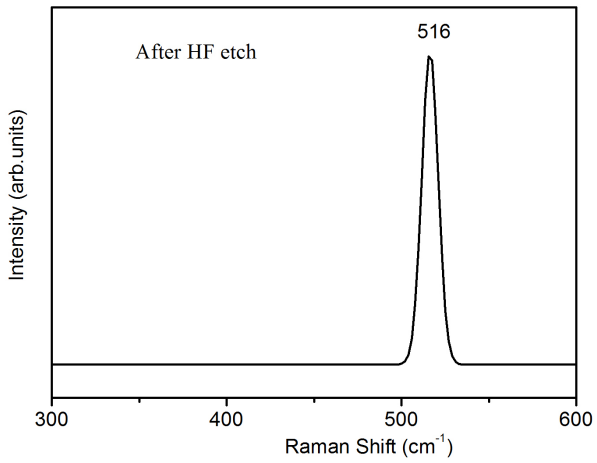

FIGURE 5.6. Raman spectra of Si nanowires after etching with HF, the peak due to crystalline Si is present but the peak due to the oxide shell is disappeared.

material with those inside it leads to distributed charge density below the surface. As the charges rearrange in response to missing atoms, the resulting net forces on the surface atoms induce surface stress. The stress depends on the electronic structure of the material and the crystallographic orientation of its surface. This stress in the lattice also accounts for the shift in the frequency. Raman spectrum of the Sb doped Si nanowires were also studied, but no significant change in the spectra was observed.

5.2.3. Conclusion

The composition of amorphous shell was confirmed by Raman spectroscopy measurements. Raman measurements indicate that the amorphous shell is composed of SiO_2. Subsequent treatment with HF, the amorphous oxide is etched off leading to crystalline Si nanowire. The shift in the optical phonon peak of Si nanowires is not attributed to quantum confinement effects, since the as-grown nanowires exhibit diameters greater than the Bohr's radius of Si. The shift in the optical phonon peak of Si nanowires is attributed to the spatial confinement effect and lattice stress effects.

CHAPTER 6

CONCLUSION AND FUTURE PROSPECTS

6.1. Achievement of Objectives

The commercial implementation of Si nanowires in nanoscale devices is based on reliable synthesis techniques, doping procedures and compatible device design. The objective of this thesis was to develop a safe and cost-effective approach in the synthesis of n-doped Si nanowires. We have successfully achieved our objective of optimizing the growth parameters and analyzing the effect of each of these parameters on the morphology and composition of the as-grown nanowires. The implementation of the as-grown and Sb doped Si nanowires in an FET type device configuration enabled determination of several intrinsic parameters associated with the semiconductor material.

VLS mechanism, the basis for bottom-up approach in the synthesis of nanowires is discussed. This thesis presents the detailed study on the synthesis of Si nanowires in Chapter 2. Crystalline Si nanowires were synthesized and their structural and compositional characteristics were studied. n-doped Si nanowires are synthesized by CVD growth using Sb as dopant.

6.2. Conclusions Based on Experimental Results

The following conclusions are drawn from the experimental work detailed in Chapter 1-5 and from detailed analysis of results:

Doping conditions are optimized for typical n-type behavior. n-doped Si nanowires were synthesized by vapor phase transport using $SiCl_4$ as source and Sb as dopant. Due to low levels of doping (1–2 wt%) achieved during growth, we approached an alternate post-growth doping procedure. The post-growth doping process yielded the optimum doping content of 3–4 wt%, of Sb into the Si nanowires at 450°C. This corresponds to an Sb concnetration of

4.6×10^{20}cm^{-3}. The concentration of Sb in the Si nanowire was found to be highly dependent on the doping temperature. This is explained on the basis of the high vapor pressure of Sb, which causes Sb to re-evaporate from the Si nanowire at higher temperatures.

Field Effect Transistor devices were fabricated to determine the electrical characteristics of the undoped and doped Si nanowires. This involved establishing a drain and source contacts to a single Si nanowire. Gating was accomplished through a thin SiO_2 layer. The effect of metal contacts to Si nanowires was also observed. The Au contacts to Si nanowire initially showed a Schottky behavior. Subsequent annealing in Ar environment at 300°C for ≈ 5 min to create ohmic contacts. The as-grown Si nanowires exhibited p-type behavior and following Sb doping they exhibited n-type behavior. We thus show that the majority carriers in the as-grown nanowires can be compensated by the Sb dopant species. One possibility for the p-type behavior of the undoped Si nanowires could be the nucleating metal Au used to initiate the growth of Si nanowires. Au in Si is known to be an acceptor impurity that induces p-type behavior by introducing acceptor levels in Si. The other possibility is the presence of point defects such as Si vacancies. The hole concentration in the undoped Si nanowires is estimated to be about 7×10^{17}cm^{-3}. n-type doping achieved through Sb incorporation into the Si lattice changes the intrinsic behavior of the Si nanowire. The transconductance, field effect mobility and carrier concentration of the Sb doped Si nanowires were determined to be 37 nS, 288 cm^{2}V^{-1}s^{-1} and 5.5×10^{18}cm^{-3} respectively. Though an Sb concentration of 4.6×10^{20}cm^{-3} was incorporated in to the Si nanowire by the doping process, transport measurements enabled us to realize that the number of active dopants in the Si nanowire was of the order of 5.5×10^{18}cm^{-3}. This decrease in the Sb concentration is due to the fact that some of the Sb atoms are believed to be trapped at the interface of the Si-SiO_2 structure and so they do not contribute to the conduction process.

Structural characterization analysis revealed the existence of amorphous layer on the surface of the nanowires. The composition of amorphous layer is confirmed through Raman

and PL measurements. The peaks at 465cm^{-1} and 481cm^{-1} in the Raman spectra confirms that the amorphous shell grown over the surface of Si nanowires is SiO_2. Subsequent treatment with HF, etches away this amorphous oxide which is confirmed through Raman spectroscopy measurements. PL spectra also confirms the presence of the shell with the decrease in the intensity with HF etching. The observed green and near blue band peaks in PL spectrum are related to the radiative recombination of defect centers that occur in the outer oxide shell layer of the Si nanowires. Defects such as oxygen vacancies [42] existing at the interface between the Si crystalline core and the amorphous oxide layer is believed to be the source of the blue-green emission. Si at nanoscale dimensions becomes a direct-band gap semiconductor due to quantum confinement effects. The quantum confinement effects will not significantly affect the electron and phonon properties of crystals unless their size is less than the Bohr radius of Si, (i.e 5 nm) at room temperature. As the synthesized Si nanowires have diameters of $\approx$ 40–100 nm, we did not observe the direct-band gap effects on PL spectrum of Si nanowires.

The experiments described in this thesis established a reliable way of realizing n-type FET'S based on post-growth doping. To the best of our knowledge there are no existing reports of n-type doping achieved through this technique. The only other report on Sb doping of Si nanowires reported in 2009 [41], used tri-methyl antimonide, which requires the use of complex processing techniques. In comparison, our technique can easily be commercialized for the synthesis of Sb doped Si nanowires. Progress in the research of high quality n-type Si nanowires ensures the design of nanoscale devices for the assembly of sensors, logic gates, inverters and diodes, which will lead to exciting opportunities in the field of nanotechnology.

6.3. Future Perspectives

There exists several important questions that need to be addressed and applications to be implemented for the doped Si nanowires to translate further into device development. One such strategy that could be developed is the fabrication of p- and n-type regions in the

same Si nanowire. If successful, a single nanowire will contain the p and n junctions required for the realization of diodes, transistors and logic gates.

Oriented and patterned growth is in demand for future applications of bottom up materials. This can be achieved through template assisted growth. Further improvement in the performance of FET can be achieved by using advanced gate structures such as the trench back gate and surrounding gate [11]. Transport measurements with respect to temperature will be useful in determining the temperature coefficient resistance (TCR) which is a crucial factor in the bolometer device design.

The essential parameters such as transconductance and mobility can be improved through surface treatment techniques. Even though the amorphous oxide layer serves to passivate the Si core, defects that exist at the Si-SiO_2 oxide interface could compensate the applied gate voltage, trap and scatter carriers and lead to a decrease in mobility. Hence, an approach that involves treatment of the nanowire to passivate its surface will improve electrical transport through the surface amorphous layer of the Si nanowires [10]. The improved conductivity will be useful in the application of chemical and biological sensors and thermoelectrics.

The effect of oxide shell around the crystalline core also plays a prominent role in the optical properties of Si nanowires. This is because the quality of the oxide that forms on the surface is poor, thereby inducing a high number of unwanted, uncontrolled interface states in the band gap of Si. The origin of optically stimulated emission of nanoscale Si is not concrete since multiple bands have been observed from near-infrared to ultraviolet wavelengths, and conditionally assigned to contaminated or defective Si oxide, dangling bonds, and quantum confinement effects which needs further study. Passivating the surface of Si nanowires and synthesizing very thin nanowires can improve the optical characteristics which will aid in further research into the development of photovoltaics and optoelectronic devices.

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