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A Multimode Interface Between a PDP-9 Computer and a Geoscience ADC/Processor

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A MULTIMODE INTERFACE BETWEEN A PDP-9 COMPUTER
AND A GEOSCIENCE ADC/PROCESSOR

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ABSTRACT

The hardware design of an interface used for general-purpose data acquisition and analysis and some examples of the software necessary to operate it are described. The interface permits the computer to accept data from nuclear counting experiments with an average deadtime of 2 to 3 μ sec (not including ADC deadtime), to digitize and store analog signals from nondestructive tests, and to use an external memory as a type of random access mass storage. Wiring and logic diagrams are included, as well as the software listings, of typical operating subroutines. Two computer-initiated pulses are also available at the front panel of the interface and may be used by the experimenter to control external devices.

1. INTRODUCTION

With the acquisition of various nuclear counting systems and the increased involvement of LASL Group GMX-1 in x-ray, fluorescent, and activation analysis, it was mandatory that our present PDP-9 computer play a greater part in data acquisition and analysis. This report describes an interface that permits the computer to interact on-line with nuclear data-acquisition experiments, nondestructive tests producing analog signals, or share data with an external memory device. The output signals and levels are designed for a Geoscience Model 8050 ADC and Model 7000 Processor, but any ADC and external memory can be used if the signal levels are modified accordingly.

The interface, a single input data-acquisition system, is illustrated schematically in Figs. 1 through 3. Each figure represents one of the three operating modes: (1) pulse-height analysis,

(2) DC sampling, and (3) memory-to-memory transfer.

When operating in the pulse-height analysis mode, the interface accepts digital data from the ADC at the ADC's rate and interprets that data as an address within the computer memory, the contents of which are incremented by one.

Fig. 1. PHA mode.

Fig. 2. DC sampling mode.

Fig. 3. Memory-to-memory transfer.

This data-acquisition mode (one-cycle data break) is very fast (average latency about 2 to 3 μ sec) and, by bypassing the accumulator, permits the computer to perform data analysis and data acquisition at the same time. Because the data are interpreted as addresses and are not stored explicitly, this mode is only useful in pulse-height analysis.

When operating in the DC-sampling mode, the interface accepts the digital data from the ADC and delivers the data to the computer through the accumulator with a program interrupt transfer. The computer can then

perform manipulations with the data. This mode of transfer is considerably slower than the one-cycle data break (20 to 30 μ sec) but permits the data to be stored explicitly. Reference 1 illustrates an application of this mode of operation.

The last data-transfer mode is memory-to-memory transfer where data from the external processor memory may be read into the PDP-9 memory or data written into the external memory from the PDP-9. The memory addresses within the PDP-9 involved with the transfer are specified by the software, whereas the starting address and number of data words in the external memory are transmitted to the interface from the computer. Because the two memories may have incompatible cycle times, the faster data break I/O transfer was discarded in favor of the simpler but slower program interrupt transfer. By optimizing the software for this particular mode, a transfer rate of 100,000 18-bit data words per second can be realized.

The PDP-9 computer used in this system has 8192 words of memory with hardware multiply and divide (integer). The I/O devices include a high-speed paper-tape reader and punch, 30-character/sec data terminal, 200-card/min card reader, Model 601 Tektronix storage scope and three DEC tape transports. The logic levels and signals at the detector side of the interface were designed to accommodate a Geoscience Model 7000 Processor and a Model 8050 ADC. Any other ADC and processor could be used if the logic levels and signals were transformed to look like those from a Geoscience.

II. SOFTWARE

Because of the existing three modes of operation and the relatively large number of functions that must be performed within the operating modes, the I/O commands issued by the computer to the interface

TABLE I
INPUT/OUTPUT COMMANDS AND USES

<u>Mnemonic</u>	<u>Octal</u>	<u>Use</u>
MADT	703404	<ol style="list-style-type: none"> 1. Load address and direction bits into interface buffer from the AC. 2. Set status flag and appropriate error bit if the processor is in any mode but stop. 3. Start processor memory cycle if I/O direction is toward the computer and if the mode is memory-to-memory.
MADZ	703401	<ol style="list-style-type: none"> 1. Generate address reset in processor. (May be microcoded with MADT.) 2. Generates a 1-μsec-wide pulse that is brought to the front panel for external use as a control pulse (see DCST).
MDSF	703501	<ol style="list-style-type: none"> 1. Skip the next instruction if buffer flag is set.
MDRD	703512	<ol style="list-style-type: none"> 1. Strobe data onto I/O bus from buffer after clearing the accumulator. 2. Clear buffer flag. 3. Start a processor memory cycle only if the direction bit has been previously set as a transfer to the computer and if the mode is memory-to-memory.
MDWT	703504	<ol style="list-style-type: none"> 1. Strobe data from I/O bus into buffer register. 2. Clear data flag. 3. Start processor memory cycle if the direction bit has been previously set as a transfer to the processor and if the mode is memory-to-memory.
DCST	703601	<ol style="list-style-type: none"> 1. Generates a 1-μsec-wide pulse that is brought to the front panel for external use as a control pulse (see MADZ).
ABCD	703602	<ol style="list-style-type: none"> 1. Disables ADC
ADCE	703604	<ol style="list-style-type: none"> 1. Enables ADC
CLAF	703402	<ol style="list-style-type: none"> 1. Clear all flags (Status and Data).
STSF	703701	<ol style="list-style-type: none"> 1. Skip next instruction if status flag is set.
STRD	703712	<ol style="list-style-type: none"> 1. Clear accumulator. 2. Read status register.
STCL	703704	<ol style="list-style-type: none"> 1. Clear status flag and zero status register.

may perform different functions depending on their operating mode. Table I lists the various I/O commands and their functions. As an example of the multiple uses of some I/O commands, MDRD and MDWT are used in both the DC-sampling and the memory-to-memory transfer modes. The actual effect issuing one of these commands will have depends on the operating mode.

There are two registers, data and status, within the interface and both may be read by the computer. However, only the data register may be written into. The status register may only be zeroed from the computer. Associated with each register, there is a flag that may be interrogated by the computer. Both the data and status flags are interfaced to the computer's interrupt system.

Subroutines have been written to operate the buffer and are entered from a FORTRAN main program by a CALL statement. We used this method rather than using the READ and WRITE statement because the argument list in a CALL statement is much more flexible and general. Subroutines have been written that utilize the interrupt system and the advanced system monitor in the PDP-9 as well as some that operate with the interrupt system disabled. Figure 4 illustrates a short routine used to handle any error flags that may come up.

```

/ SUBROUTINE-----MIDAS
/
/ CALLING SEQUENCE
/   CALL MIDAS
/
/   .GLOBL MIDAS
CLAF=703402
STSF=703701
STRD=703712
STCL=703704
/
/ ENTER ROUTINE. INSERT SKIP IOT
/ AND SUBROUTINE ENTRY POINT,INT,
/ INTO SYSTEM SKIP CHAIN.
/
MIDAS 0
      CAL
      16
      STSF
      INT
      LAC (JMP+MIDAS+7
      DAC MIDAS+1
/
/ CLEAR ALL FLAGS,CLEAR STATUS
/ REGISTER AND RETURN TO MAIN
/ PROGRAM.
/
      CLAF
      STCL
      IOV
      JMP* MIDAS
/
/ ENTRY POINT AFTER ANY STATUS
/ ERROR CONDITION.
INT    DAC ACSAVE#
      LAC* (0
      DAC OUT#
      IOF
/
/ READ STATUS REGISTER INTO AC
/ AND HALT
/
      STRD
      HLT
/
/ RESTORE AC AND RETURN TO MAIN
/ PROGRAM
/
      LAC ACSAVE

```

```

LAC ACSAVE
IOV
JMP* OUT
HLT
•END

```

Fig. 4. MIDAS - An error handling subroutine.

The subroutine is entered at MIDAS by the sequence CALL MIDAS.

Whenever an error condition exists and the error flag is set with the interrupt system on, the routine is entered at INT, the status register is read into the accumulator, and the processor is halted. (Figure 7 describes the status register.) If this should happen during a data-acquisition program run, the operator would note which status bits were set, correct the appropriate error condition if possible, and continue the program by depressing CONTINUE.

The first portion of MIDAS is typical of the coding needed to insert the skip IOT and the interrupt entry point (INT) in the skip chain maintained by the system.

Figure 5 illustrates a short subroutine used to read data from an ADC in the pulse-height analysis mode for a specified number of minutes and seconds.

```

/ SUBROUTINE-----DCOLL
/
/ CALLING SEQUENCE
/   CALL DCOLL(MIN,ISEC,IOFF)
/   MIN-NO. OF MINUTES TO COLLECT DATA
/   ISEC-NO. OF SEC. TO COLLECT DATA
/   IOFF-UNDERWAY FLAG
/
/   .GLOBL .DA,.AD,DCOLL,DEVD
ADCE=703604
ADCD=703602
/
/ ENTER ROUTINE AND LOAD
/ ARGUMENTS.
/
DCOLL 0
      JMS* .DA
      JMP .+4
/
MIN    .DSA 0
SEC    .DSA 0
IOFF   .DSA 0

```

```

/ CONVERT MIN AND SEC TO A BINARY
/ NUMBER REPRESENTING THE EQUIV-
/ ALENT NUMBER OF 60 CYCLE CLOCK
/ PULSES.
/
    LAC* MIN
    JMS* .AD
    LAC (74
    TAD* SEC
    JMS* .AD
    LAC (74
    CMA
    TAD (1
    DAC .+4
/
/ START INTERNAL CLOCK. AFTER IT HAS
/ RUN OUT, REENTER ROUTINE AT INT.
/
    CAL
    14
    .DSA INT
    .DSA 0
/
/ START ADC AND SET UNDERWAY FLAG
/ TO -1. REENTER MAIN PROGRAM.
/
    ADCE
    CLA
    CMA
    DAC* IOFF
    IOV
    JMP* DCOLL
/
/ ENTRY POINT AFTER THE PRESET DATA
/ COLLECTION TIME HAS RUN OUT. STOP
/ ADC. SET UNDERWAY FLAG TO 1 AND
/ REENTER MAIN PROGRAM.
/
INT    0
    DAC ACSAVE#
    LAC INT
    DAC OUT#
    ADCD
    DZM* IOFF
    LAC OUT
    RAL
    LAC ACSAVE
    JMP* OUT
/
/ ENTRY POINT FOR A SOFTWARE TERM-
/ INATION OF DATA AQUISITION.
/
DEVD    0
    LAC DEVD
    JMP DEVD-7
    HLT
    .EVD
END OF FILE REACHED BY:
P 50
>

```

Fig. 5. DCOLL - A data collection sub-routine operating in the PHA mode.

The calling sequence for data collection is
CALL DCOLL (IMIN, ISEC, IFLAG) .

The integer arguments, IMIN and ISEC, contain the number of minutes and seconds to collect the data. IFLAG is an integer flag with the following meanings

IFLAG = -1 if data are being collected, and

IFLAG = 0 if data collection has stopped.

Another entry point, DEND, from the main program is used to stop the data collection before the time has run out. The calling sequence is

CALL DEND

IFLAG = 0 after a call to DEND.

These are examples of typical data-acquisition Subroutines that we used. The user may write his own to be as general or specific as he pleases. A very specific subroutine, DCSI, is used to acquire data in the DC-sampling mode but it is so specialized that it probably could not be adapted to any other problem.¹ DCSI does, however, illustrate the use of the two I/O commands, 703401 and 703601, to control an external device; in this case, an electronic pulser and the ADC are used. One command, 703401, initiates a pulse in the interface that is led directly to the pulser to start an eddy current pulse. The other, 703601, is connected to the coincidence gate in the ADC. With these two pulses, the subroutine DCSI can control to within a microsecond the time the electronic pulse will start and when the coincidence gate on the ADC will open to permit digitizing the input wave form.

Figure 6 illustrates a short routine that might be used to transfer blocks of data from the PDP-9 memory to an external memory.


```

OVERFLOWING-----TRAN
CALLING SEQUENCE
CALL TRAN (IDATA, JDATA, IWC, IDIR)
IDATA--INTEGER ADDRESS OF EXTERNAL
MEMORY.
JDATA--INTEGER ARRAY WITHIN PDP-9
MEMORY.
IWC---WORD COUNT
IDIR---DIRECTION
      =0--READ
      =1--WRITE
DATA IS TRANSFERRED TO OR FROM
JDATA(1) THROUGH JDATA(IWC) FROM
OR TO THE EXTERNAL MEMORY STARTING
AT IDATA AND ENDING AT IDATA+IWC.

```

```

MART=703400
MDIF=703501
MOPD=703512
MDMT=703504
CLAF=703402

```

```

GLOBAL TRAN, DA
TRAN
    JMC ← DA
    JMC ← +5
ENT ← DCA 0
CMP ← DCA 0
WC ← DCA 0
DIR ← DCA 0

```

```

/ SET UP REGISTERS AND COUNTERS.
/ CALCULATE -32'S COMPLEMENT OF
/ THE WORD COUNT, WC1.

```

```

IDF
LAC ← WC
CMA
TAD ← 1
DRC WC1 ←

```

```

/ LOAD PDP-9 MEMORY POINTER.

```

```

LAC ← CMP
DRC CMP ←

```

```

/ SET DIRECTION BIT AND ADDRESS
AND LOAD INTO EXTERNAL MEMORY.

```

```

LAC ← DIR
PTRCLL
AND ← 400000
TAP ← ENT
MART
LAC ← DIR
DCA
JMP MART

```

```

/ READ DATA INTO THE COMPUTER.

```

```

PED MDIF
JMP ← 1

```

```

/ DATA IS IN BUFFER. READ IT INTO
THE AC AND STORE.

```

```

MDPD
DRC ← CMP
ISZ CMP
ISZ WC1
JMP PED

```

```

/ WORD COUNT OVERFLOW. STOP DATA
TRANSFER AND RETURN TO MAIN
PROGRAM.

```

```

STP CLAF
IDM
JMP ← TRAN

```

```

/ WRITE DATA INTO EXTERNAL MEMORY.

```

```

MRT LAC ← CMP
ISZ CMP
MDMT
ISZ WC1
SKP
JMP STP
MDCF
JMP ← 1
JMP MRT
END

```

```

END OF FILE REACHED BY:
P 50

```

Fig. 6. TRAN2 - A memory-to-memory data transfer subroutine.

The calling sequence is

```
CALL TRAN (IDATA, JDATA, IWC,
IDIR) .
```

The arguments in the call to TRAN are

IDATA - Starting address in the external memory,
JDATA - Starting address in the PDP-9 memory,
IWC - The number of 18-bit words to be transferred, and
IDIR - Direction of transfer.

The starting address in the external memory is an integer variable that varies from 1 to 4096 in the case of the Geoscience Model 7000 Processor. The starting address in the PDP-9 memory is represented by an integer array. The word count may be any number between one and the smallest capacity of either memory, but the user is responsible for ensuring that overflow does not occur. Note that single-word transfers to and from random locations may be made with this subroutine although the overhead is high. The transfer direction variable is an integer 0 for transfers away

from the computer and on integer 1 for transfers toward the computer.

III. HARDWARE

The interface hardware for all three modes of operation of this acquisition system appears as a single peripheral unit on the PDP-9 I/O bus. From the software point of view, the acquisition system appears as a single peripheral device with three mutually exclusive modes of operation. The appendix contains all of the logic diagrams.

A. Pulse-Height Analysis (PHA) Mode

That portion of the interface devoted to the PHA operation mode consists of a multiplexer (W104), I/O bus address line drivers, and start/stop control logic. The W104 multiplexer provides control and synchronization between PHA events in the acquisition system and the PDP-9 memory.

Upon receipt, at the acquisition system, of a digital address from the Model 8050 ADC (digitized nuclear pulse), the W104 multiplexer halts the PDP-9 processor operations and presents the address information to the PDP-9 memory address lines during the next memory cycle. An INCMB signal is then supplied to the PDP-9 memory that effects an increment by one to the addressed memory location. Thus, the nuclear event is recorded in the PDP-9 memory in a location relative to its energy.

Facilities are provided at the interface operator's panel (15-binary switches) for adding any base address between 0 and 7777₈ to all incoming PHA events. Thus, the user can define spectra to any base address within memory limitations. The user is also provided with upper-level discrimination, selectable at the operator's panel. Four ranges are available, 1K, 2K, 4K, and 8K. The range selected represents the maximum digital

number that will be accepted before base address addition, thereby allowing the user to discriminate against unwanted data. Hardware PHA start/stop control facilities include manual start/stop at the operator's panel, software start/stop and start/stop lines available for control by external equipment (minimum 50 nsec pulse from +5 V to ground potential).

B. DC-Sampling Mode

DC sampling operates under program interrupt control. The sequence of events are as follows.

1. DC sampling start.
2. Coincidence pulse to the ADC.
3. ADC digitizes the analog level at its input and strobes the digital number into the acquisition system buffer register.
4. A program interrupt flag is set.

DC-sampling logic consists of control logic, I/O bus data line drivers, and an 18-bit binary buffer register that is shared with the memory-to-memory transfer mode. Start/stop control logic includes manual control at the operator's panel and start/stop lines available for control by an external device (minimum 50 nsec pulse from +5 V to ground). Start/stop control relative to the DC-sampling operation mode is merely an enable or disable to the model 8050 ADC. In this mode, the ADC converts only when enabled and supplied with a coincidence pulse. Available at the operator's panel are two BNC connectors that provide two software pulses (device 34 IOT1 and device 36 IOT1) to synchronize external analog events to system software. Typically, device 34 IOT1 is used as a trigger or an initiator of the analog event to be sampled. Device 36 IOT1's can then be issued as coincidence inputs to the ADC on a software time base relative to the initiate pulse (device 34 IOT1).

C. Memory-to-Memory Transfer Mode

The memory-to-memory transfer mode was designed for bidirectional data transfer between the PDP-9 memory and the memory of a Geoscience 7000 analyzer. Data are transferred under program interrupt control because of different memory cycle times and the respective memories. The interface logic consists of control and synchronization logic, address line gates, and the common 18-bit buffer register.

The basic control signals necessary to control the analyzer memory are

1. CMPST (Computer Start Pulse),
2. ART (Address Reset),
3. CDIR (Computer Direction),
4. DATA STROBE, and
5. MBSY (Memory Busy) $\sim 3.5 \mu\text{sec}$ duration.

Random access of the analyzer memory is accomplished through analyzer option -03. This option makes available all of the analyzer memory address lines to the interface. A logic 1, gated on any of these lines, sets the respective F/F in the analyzer memory address register.

A read or write to the analyzer memory from the PDP-9 begins by execution of a microprogrammed I/O instruction to device no. 34. This I/O instruction is microprogrammed to issue IOP1 and IOP4 pulses to the interface. The IOP1 pulse generates an address reset signal (ART) to the analyzer. The IOP4 loads the interface buffer register with a micro-coded data word from the PDP-9 accumulator. The most significant bit of the 18-bit word specifies a read or write operation and the least significant 12 bits represent the address to be accessed. The interface then generates a delayed IOP4 ($\sim 1 \mu\text{sec}$ after the IOP4) that gates the logical 1's from the address stored in the buffer register onto the analyzer

memory address lines and also generates a computer start pulse (CMPST) if a read operation is specified. If a write were specified, CMPST would not be generated until later. Another instruction must be issued that will load the interface buffer register with the data word to be written in the analyzer memory. The IOP4 pulse issued by this instruction strobes the data word into the buffer register and the interface generates another pulse delayed by $\sim 1 \mu\text{sec}$, which, when 'ANDED' with the write bit, generates a CMPST pulse and strobes the data word from the buffer register onto the analyzer memory data input lines. As soon as the CMPST signal is issued, the analyzer generates a memory busy signal (MBSY). When this signal drops, indicating a completed memory cycle, a program interrupt flag is set in the interface which indicates that the data word has been written into the analyzer memory or, in a read operation, indicates that the read operation is complete and the data word is available in the interface buffer register. At this point, the interrupting device must be serviced.

Servicing the device for a write operation consists of sending another data word if an additional sequential location is to be written. If writing in random locations, the write procedure as described above must be repeated each time. That is, a new address must precede each new data word to be written. Essentially the same procedure applies to the read operation. Servicing the device consists of reading the interface buffer register into the PDP-9 accumulator.

When reading data from the analyzer memory into the PDP-9 memory another analyzer memory cycle is initiated each time the buffer register is read into the PDP-9 accumulator. The IOP2 pulse, which strobes the data onto the PDP-9 I/O bus

data lines, is delayed by $\sim 1 \mu\text{sec}$ and this delayed pulse generates a computer start pulse (CMPST), which initiates a new memory cycle. The analyzer automatically increments its address register by one after each cycle; therefore, the next read cycle accesses the next sequential location. This automatic recycle was incorporated for faster block data transfer into the PDP-9 memory. It must be noted that to stop reading or to read from a new location the flag set by the next automatic read must be cleared by a clear all flags instruction (CAF). The CAF instruction will halt activity at the interface in preparation for a new address or a complete halt of read operations. When writing to the analyzer memory, the same situation applies. At the end of a write cycle, the program interrupt flag is set indicating that the analyzer memory is ready for another sequential data word. This flag must be cleared in the same manner.

are reset by an IOP4 pulse issued during an I/O instruction to device No. 37. Those bits in the status register that represent fatal errors at the interface are wired to the program interrupt flag such that if any of those error bits are present, the program interrupt flag is set, thereby requesting service. The bit assignments are illustrated in Fig. 7.

Fig. 7. Status register.

An 18-bit status register is included in the interface. This register is software accessible. An IOP2 pulse from an I/O instruction issued to device No. 37 reads the contents of the status register into the PDP-9 accumulator. Error bits

REFERENCE

1. R. A. Morris and R. M. Ford, "PEC: A Pulsed Eddy Current Data Acquisition and Analysis Program," Los Alamos Scientific Laboratory Report LA-4915 (March 1972).

LOGIC DIAGRAMS

DEVICE SELECTORS

P. I. INTERFACE

P.1. INTERFACE

P.N.A.

ADC (DC SAMPLING) CONTROL

INTERFACE REGISTER ($2^0 - 2^8$)

INTERFACE REGISTER ($2^9 - 2^{17}$)

INTERFACE REGISTER ($2^9 - 2^{17}$)

I/O BUS DRIVERS (BUFFER REGISTER)

6632
GATED INPUTS = GND OUT

I/O BUS DRIVERS (BUFFER REGISTER)

STATUS REGISTER

STATUS REGISTER

I/O BUS DRIVERS (STATUS REGISTER)

I/O BUS DRIVERS (STATUS REGISTER)

• I BUS DRIVER
CONNECTIONS

I/O BUS CONNECTOR (DATA LINES)

I = END

I/O BUS CONNECTOR (DATA LINES)

PNA DATA INTERFACE

ADDRESS LINE GATES