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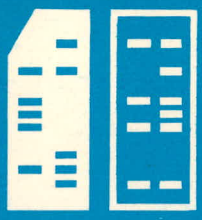
A SYNCHRONIZATION SYSTEM FOR A TELEVISION BANDWIDTH COMPRESSION SCHEME

by

EDWARD ELLIS CARR

October, 1971



DEPARTMENT OF COMPUTER SCIENCE
UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN · URBANA, ILLINOIS

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1. INTRODUCTION

This paper describes a synchronization system for a real time television bandwidth compression scheme called ORBIT [1] (ONLINE REDUCED BANDWIDTH INFORMATION TRANSFER). The ORBIT system is designed to transmit black-on-white drawings with an average bandwidth compression of twenty-five to one. It consists of a transmitting section, fed by a standard TV camera, and a receiving section, coupled to a conventional monitor. The system was proposed by Professor W. J. Poppelbaum and designed by Peter Oberbeck.

The transmitting section contains a standard TV camera and encoding circuitry. Its operation is as follows. Assume the TV camera is scanning a line drawing, as shown in Figure 1. Then the video signal for the horizontal line labeled A will be as shown in Figure 2. The ORBIT transmitter circuitry encodes the times from the beginning of the line of video to each of the video pulses on the line and places the results in digital storage registers. Then, as the next line is being scanned, the transmitter circuitry retrieves, at equal time intervals, the information about the previously scanned line and converts it to an analog signal: the times t_1, t_2, t_3 and t_4 of Figure 2 being converted proportionately into the voltages v_1, v_2, v_3 and v_4 of Figure 3. Bandwidth compression is obtained because the transmitter redistributes the video information equally spaced in time during the scanning of the next line, since a lower bandwidth signal is required to resolve points spread out than points which occur at closely spaced intervals. The last step in the transmitter circuitry is filtering the analog voltage to remove the high frequency components. The resultant signal, as shown in Figure 4, is transmitted via a wire to the receiver.

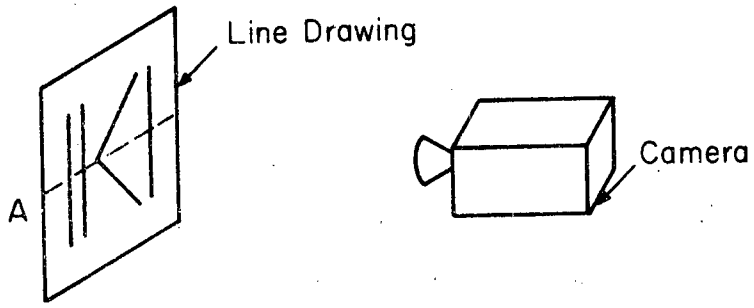

Figure 1
TV Camera Scanning
A Line Drawing

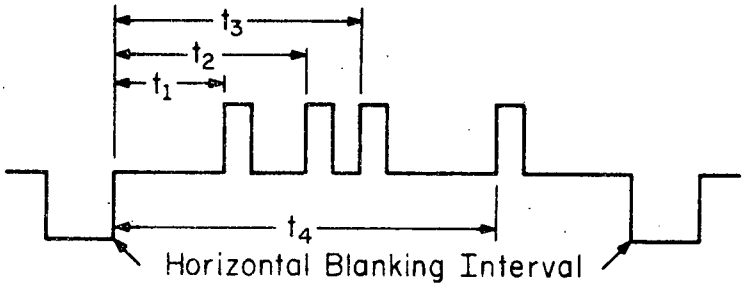

Figure 2
Video Signal For Line A

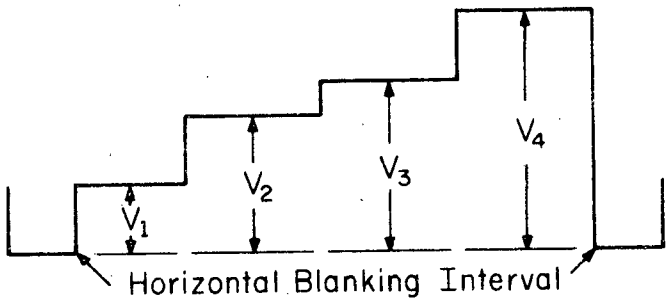

Figure 3
Analog Equivalent Of The
Video Line A

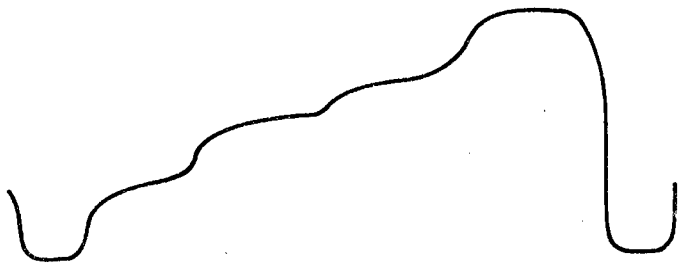

Figure 4
Transmitted Signal

The ORBIT receiver consists of decoding circuitry and a standard TV monitor for displaying the picture. The decoding circuitry contains an A/D converter, storage registers and a comparator circuit which drives the monitor. The incoming video signal is sampled at the correct intervals and converted to digital information. This information, which represents the time intervals for the video pulses on a line, is stored in registers. As the next line is received, the digital counts for the first line are compared sequentially by a digital comparator with a counter which is being driven by the receiver clock. When a comparison between the contents of a register and the counter is detected, the comparator drives the monitor which displays a point of the line.

The ORBIT system, as presently designed, can handle line drawings with up to 32 intersections per horizontal line.

2. THE NATURE OF THE SYNCHRONIZATION PROBLEM

As mentioned in the Introduction, the average video signal bandwidth for ORBIT is compressed about twenty-five to one. However, until this project was completed the receiver monitor was driven by using the RETMA sync waveform output of the transmitter camera, and the receiver circuitry was driven by the transmitter 9.45MHz clock, which is used to sample and digitize the camera video. Obviously, it does no good to reduce video signal bandwidth in the information channel if the 9.45MHz synchronization signal bandwidth cannot also be reduced.

One can see that the sync problem has two parts. One is the problem of driving the receiver monitor in synchronization with the television camera in the transmitter section. The second is the establishment of the correct interrelation between the information encoded in the transmitter and decoded in the receiver.

In order to synchronize the receiver monitor, the incoming line frequency must be detected. In addition information indicating the end of an even and odd field is necessary. The incoming video line frequency is obtained from the fundamental period of Figure 4 by circuitry diagramatically illustrated in the top left corner of Figure 5. The output of the VIDEO TO SQUARE WAVE CONVERTER is used to generate a pulse which indicates the start of each line. A detailed description of this operation will be given later. The information indicating the end of an odd or even field, which is necessary for interlacing, is encoded in the video signal. The scheme used is for the transmitter to hold the last line of an odd field and the last line

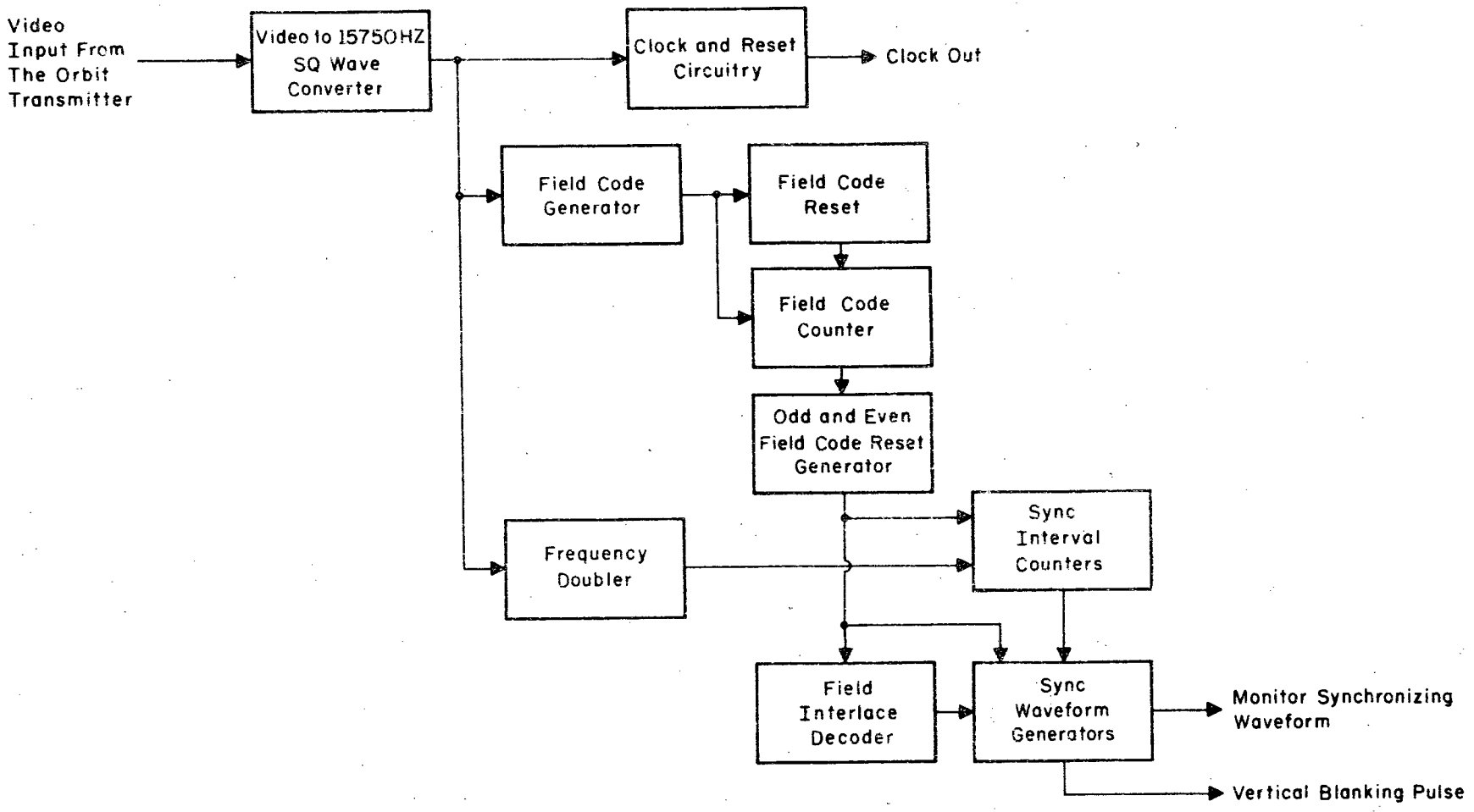

Figure 5. Block Diagram Of The Orbit Synchronizing System

and a half of an even field at ground. This code is detected by the circuitry of the central regions of Figure 5.

The circuitry remaining in the lower right corner of the figure serves to generate the required monitor signals.

The transmitting section of ORBIT uses a 9.45MHz clock which produces a 600 count line (9.45MHz/600 = 15.75kHz - the line frequency). The first 512 counts are used to digitize the video, i.e. to determine the positions of the intersections in the line being transmitted, and the remaining counts are used to define the horizontal synchronization interval. Since the receiver must determine the positions of the intersections from the encoded signal, it was initially thought that there should be a 9.45MHz clock to digitize this encoded signal. Thus, considerable effort was initially directed in this area. However, the sampling frequency for digitizing the video signal only needs to be approximately the same as the corresponding frequency in the transmitter, owing to the relative flatness of the video signal at the sampling points. Therefore, a clock which has an accuracy of about 1%, but is quite stable and capable of being restarted in the same phase at the beginning of each line, is all that is necessary.

3. A SOLUTION TO THE SYNCHRONIZATION PROBLEM

The understanding of the requirements for the receiver led to the design of the clock circuit shown in Figure 6. The circuit comprises an SN74122 retriggerable monostable multivibrator with clear and four inverters. The inverters, together with the internal delays of the monostable, provide for the logical "0" state of the clock. The theoretical timing diagram for the clock circuit is shown in Figure 7. Clear is initiated by the negative edge of the $\overline{\text{Clear and Trigger}}$ signal from the VIDEO TO SQUARE WAVE CONVERTER. The first clock pulse of a line is generated by the positive edge of the $\overline{\text{Clear and Trigger}}$ signal. Subsequent clock pulses are formed by Retrigger which is merely $\overline{Q}$ delayed by 40ns. The delay times shown in Figure 7 are the average delay times for the devices found in integrated circuit data sheets. In actual operation this clock has a period of 106ns and provides the receiver with a 600 count line.

The solution to the problem of synchronizing the receiver monitor was accomplished by designing a sync waveform generator; its components occupy two printed circuit boards. The first board contains a circuit which produces a 15,750Hz reference square wave for controlling the receiver clock and, in addition, detects the odd or even field code for the monitor sync system. This circuit is shown in Figure 8. Its operation is best described by referring to the waveforms in Figure 9. Waveform 2 in Figure 9 shows the last five lines of video of an even field from the ORBIT transmitter. Consider this waveform to be applied to the input pin 3 on the circuit in Figure 8. The

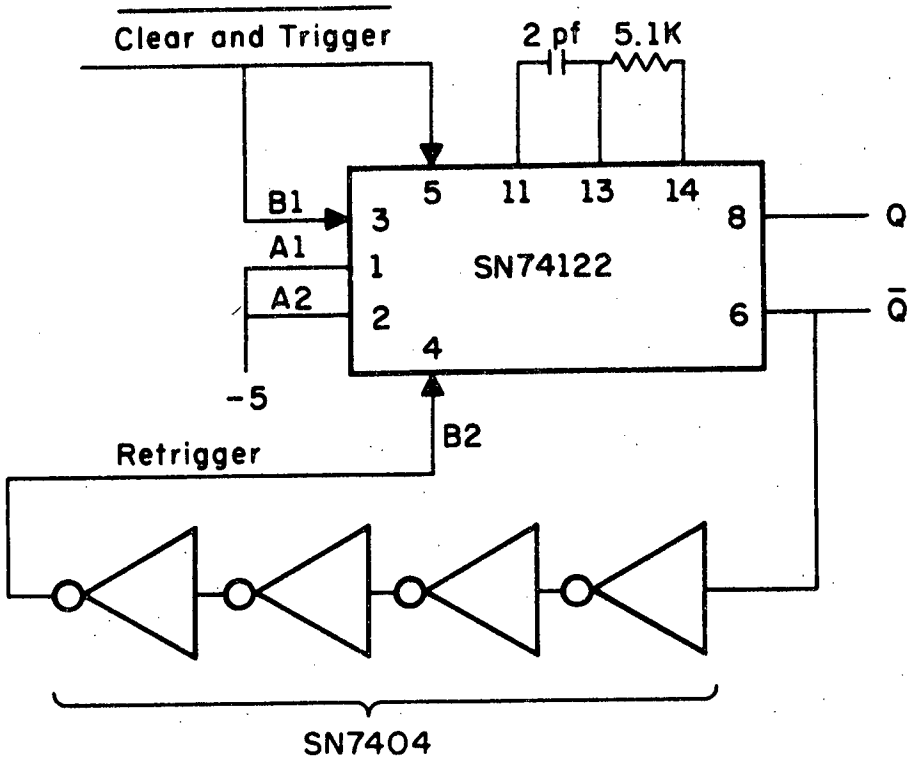

Figure 6. Orbit Receiver Clock

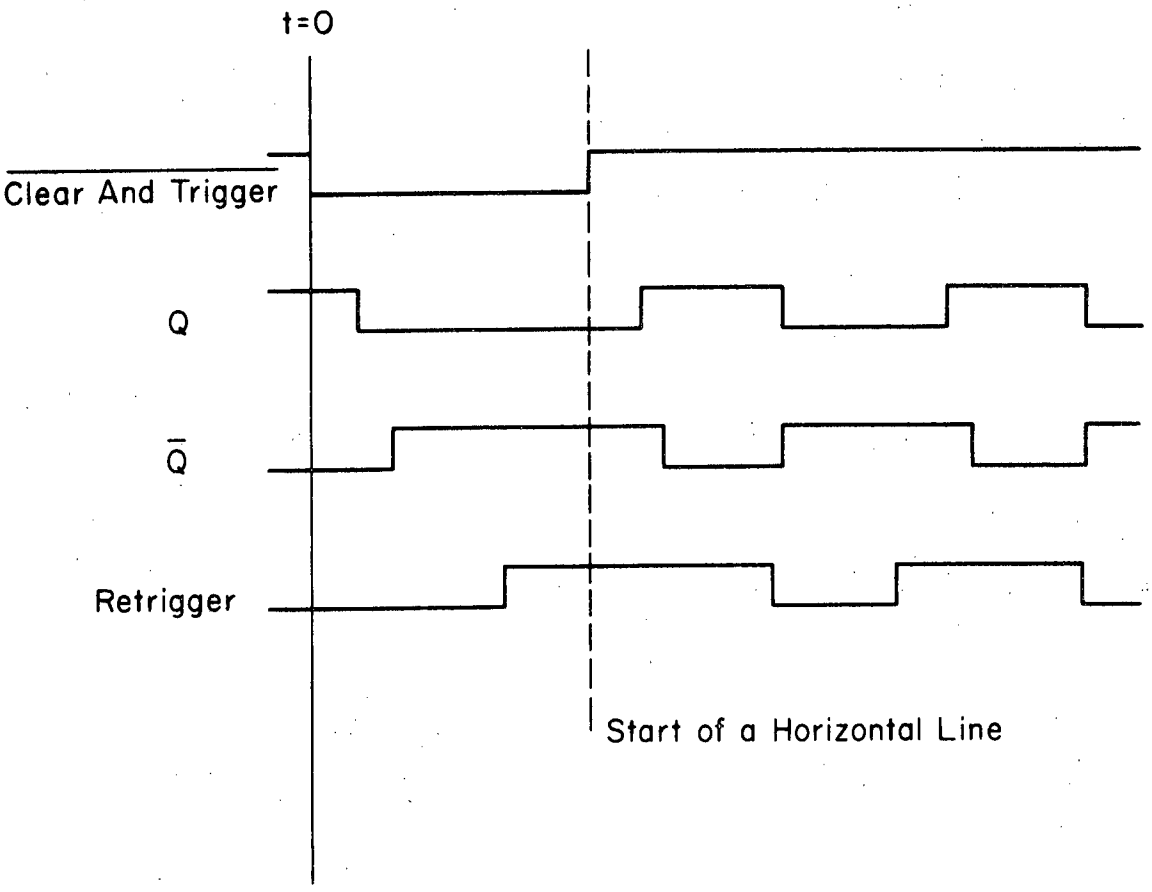

Figure 7. Orbit Receiver Clock Theoretical Timing Diagram

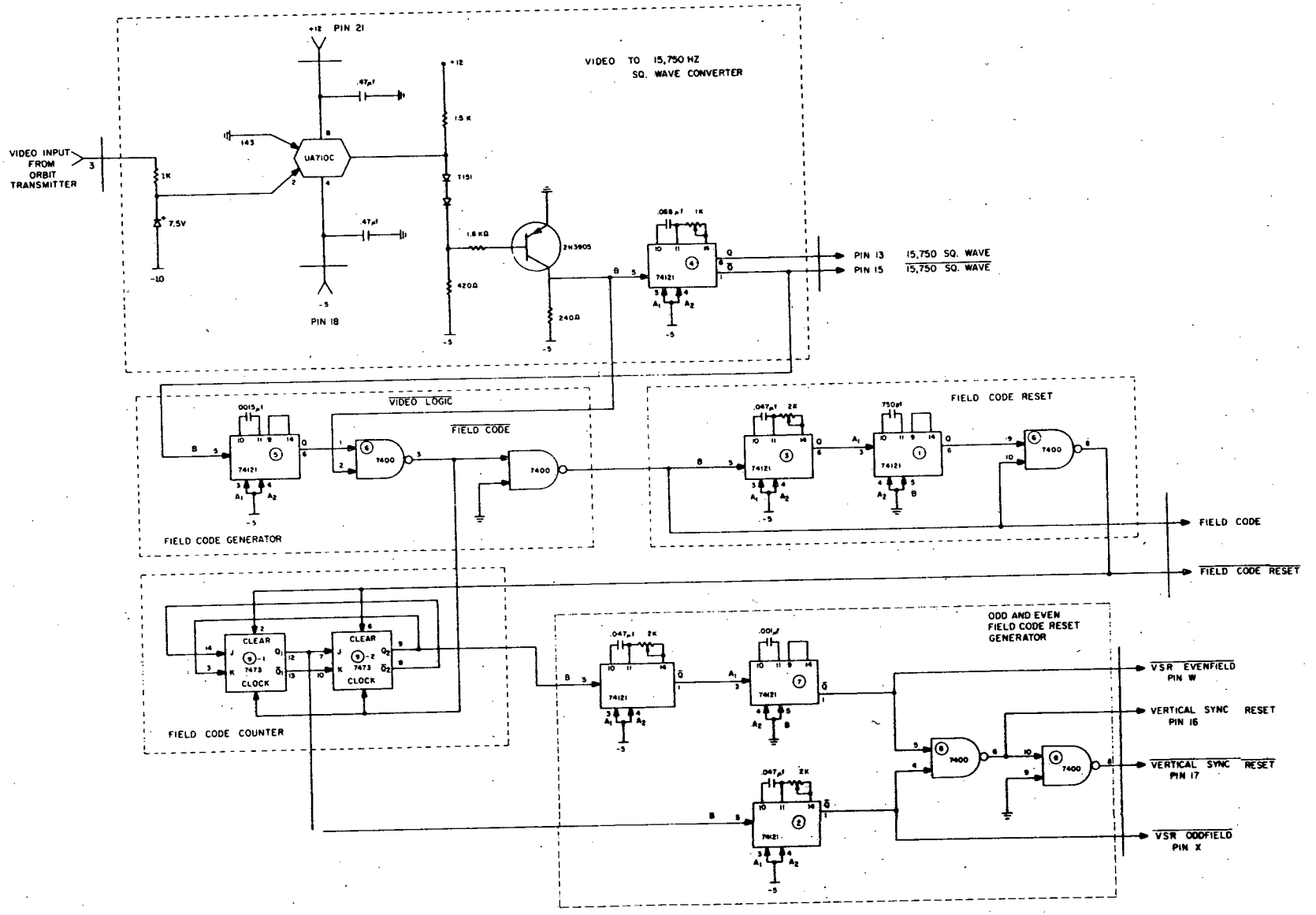

Figure 8. Orbit Sync Waveform

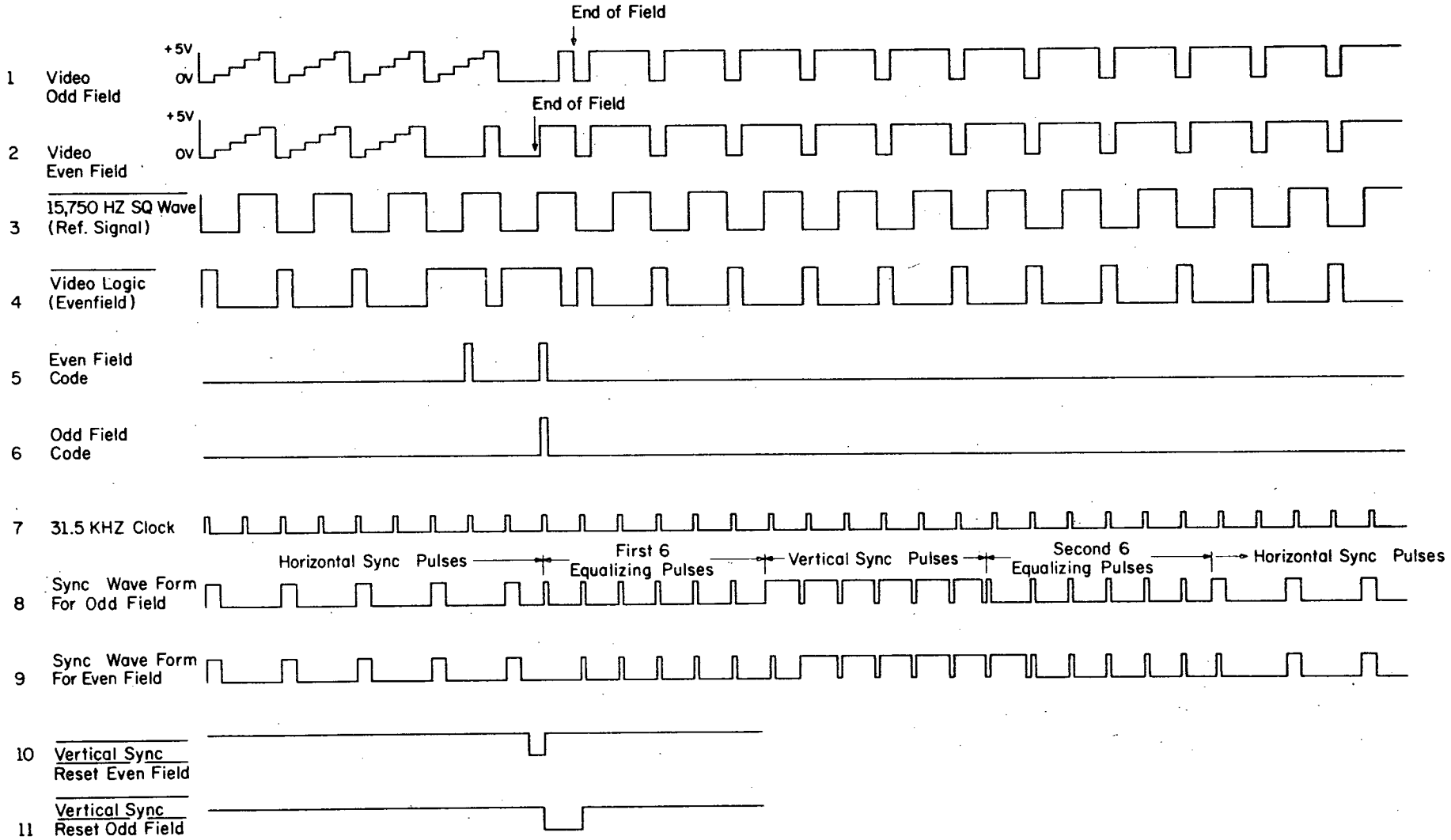

Figure 9. ORBIT Sync Waveforms

μA710C comparator outputs a "1" or "0" according as the video input is above or below ground. This logic signal is inverted and level-shifted to conform to the ORBIT receiver logic levels (ground = "1", -5V = "0") by the 2N3905 transistor. The inverted logic triggers an SN74121 monostable multivibrator which produces a 15,750Hz square wave (Figure 9, waveform 3). This, in turn, is used to produce the $\overline{\text{Clear and Trigger}}$ pulse for the receiver clock and to generate the odd or even field code pulse. Odd or even field information is necessary for interlacing, as mentioned previously.

The logic level output, from the collector of the 2N3905, resulting from the application of waveform 2 to the comparator is shown by waveform 4. This signal, called $\overline{\text{Video Logic}}$, is applied to a NAND gate together with a 1 μs pulse which is triggered from the rising edge of waveform 3. The resultant output is $\overline{\text{Even Field Code}}$ for input waveform 2. In a similiar manner the resultant output is $\overline{\text{Odd Field Code}}$ for input waveform 1. Even field code and odd field code waveforms are shown by waveforms 5 and 6 respectively.

After the field code is generated, it drives a counter and a reset circuit. The counter is composed of an SN7473 dual J-K flip-flop; its clock input is driven by $\overline{\text{Field Code}}$. A reset pulse, when the field code indicates the end of an even field, is produced by using two SN74121 monostables in series followed by a NAND gate. The latter has as its output $\overline{\text{Field Code Reset}}$. The way the reset circuit works is by causing the first pulse of the even field pulse code to be delayed by exactly one horizontal line time plus 1 μs. Due to a property of the monostable, this delay causes the second pulse to be ignored by the first monostable. After the first monostable has timed out,

it fires a second monostable which reaches its logical "1" state before the first monostable times out, the two inputs to the NAND gate are both "1", and the resultant signal is the desired counter reset pulse.

The time at which reset occurs and the resulting states of the counter are shown in Figure 10, waveforms 2 and 3. The positive edges of the counter outputs, Q_1 and Q_2, are used to generate the appropriately timed sync reset pulses shown as outputs in Figure 8. The timing and distribution of the reset pulses are best explained by first understanding the operation of the second circuit board of the sync waveform generator.

Figure 11 shows the circuits on the second circuit board. These generate the RETMA standard sync signal. The signals shown in Figure 9 (waveforms 8 and 9) detail the sync waveform for odd and even fields respectively. The sync waveform is divided into four intervals, as labeled on Figure 9, waveform 8. It is formed by generating signals which define the four intervals and using them to gate the required signals from the appropriate monostable multivibrator. Since the equalizing and vertical sync pulses are required to occur at a 31.5kHz rate, a clock having this frequency was needed to trigger these monostables. The simplest way to do this was to use the 15,750Hz reference signal to trigger two SN74121 monostables and gate their outputs. One monostable is triggered on the positive edge, and the other is triggered on the negative edge of the 15,750Hz reference square wave. The 31.5kHz clock signal is shown in Figure 9, waveform 7. The sync intervals are determined by modulo 6 and modulo 4 counters comprising negative edge triggered SN7473 and SN7476 J-K flip-flops. The sync waveform

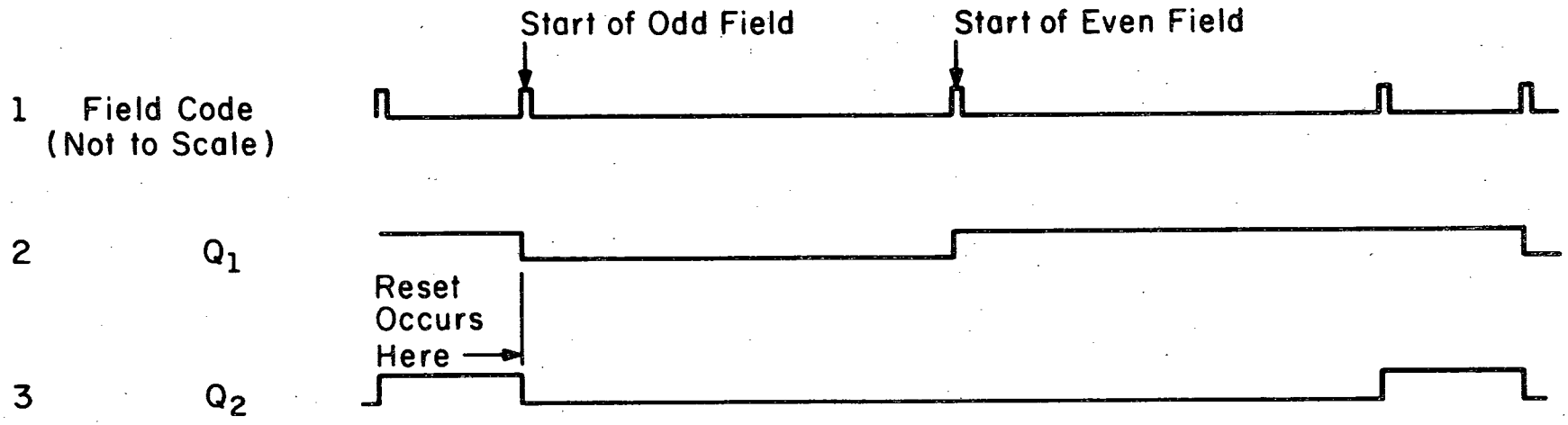

Figure 10. Field Code Waveforms

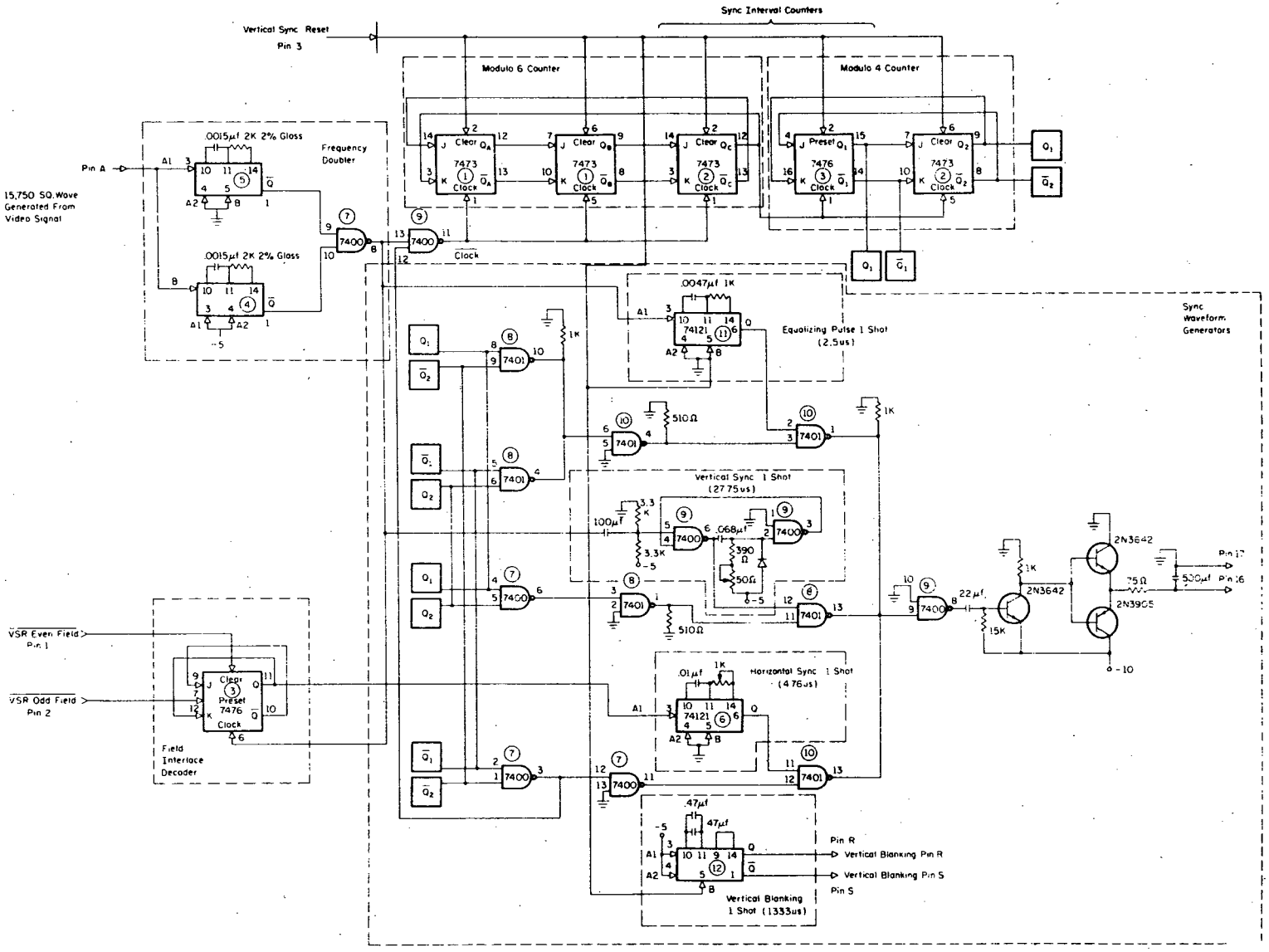

Figure 11. ORBIT Monitor Sync Waveform Generator

counters are started by $\overline{\text{Vertical Sync Reset}}$. This signal clears the modulo 6 counter and presets the modulo 4 counter to the $Q_1\overline{Q}_2$ state; this causes the gating of the equalizing pulse multivibrator. After a count of 6, the modulo 4 counter changes to the Q_1Q_2 state and gates the vertical sync multivibrator. Similarly the state $\overline{Q}_1Q_2$ occurs and causes the gating of the second six equalizing pulses from the equalizing pulse monostable. After the gating of the second six equalizing pulses, the modulo 4 counter changes to the state $\overline{Q}_1\overline{Q}_2$, which causes the horizontal sync monostable to be gated and cuts off the clock pulses driving the counters. The system then continues to generate horizontal sync pulses until the counters receive the $\overline{\text{Vertical Sync Reset}}$ signal. The outputs of the multivibrators are ORed using SN7401 open collector NAND gates in a "wired OR" configuration. As shown in Figure 11, the ORed output is inverted, amplified and matched to drive a 75Ω cable by the transistor network shown as the output stage. One point of interest is that, since the counters and the monostable multivibrator are negative edge triggered, the clock signal is inverted to drive the logic circuits, so as to provide a 2 μs lead over the triggering of the monostables. This procedure insures that the gate signals occur before the monostables are triggered. However, due to this procedure, only five equalizing pulses are generated for the first equalizing pulse interval. The reason for this is due to the way the modulo 6 counter is set up. The reset signal sets the modulo 6 counter to zero and gates the equalizing pulse monostable. The first clock pulse places a count of one in the modulo 6 counter and triggers the equalizing pulse monostable. But, on the sixth clock pulse the modulo 4 counter is triggered and the equalizing pulse monostable gate is closed; hence only five equalizing pulses are gated. This

problem does not occur during the subsequent intervals because the appropriate monostable is triggered by the clock pulse, which causes the modulo 6 counter to return to its starting state.

One could have avoided this problem by using a different counter configuration, but this would have meant the addition of another monostable in the odd field reset pulse circuitry.

It was however, sidestepped by appropriately timing the components of the $\overline{\text{Vertical Sync Reset}}$ signal. This consists of the OR of $\overline{\text{Vertical Sync Reset Even Field}}$ and $\overline{\text{Vertical Sync Reset Odd Field}}$. The timing of these signals causes the modulo 6 counter to ignore the first clock pulse at the start of the equalizing pulse interval which gates the first six equalizing pulses. The $\overline{\text{Vertical Sync Reset}}$ is also used to drive the B input of the equalizing pulse monostable; this inhibits the triggering of the latter, during reset, until the proper time. The $\overline{\text{Vertical Sync Reset Even Field}}$ and $\overline{\text{Odd Field}}$ signals are shown in Figure 9, waveforms 10 and 11 respectively. Observe that the positive edges of the two waveforms occur between two edges of a clock pulse.

The task of interlacing the odd and even fields is accomplished by controlling the clear and preset inputs to the SN7476 flip-flop which triggers the horizontal sync monostable. If the flip-flop is preset at the start of the vertical sync interval, the negative edge of the signal from the flip-flop will trigger the horizontal sync monostable one full line after the end of the vertical sync interval. If the flip-flop is cleared, triggering will occur one half line after the end of the vertical sync interval. This control of the horizontal blanking monostable causes the correct interlace.

Vertical blanking is provided by a monostable which is triggered by the positive edge of $\overline{\text{Vertical Sync Reset}}$.

4. CONCLUSION

A synchronizing system has been designed to provide the ORBIT system with its full capability for bandwidth compression unimpaired by any high frequency synchronization channel. The understanding of the clock synchronizing circuitry, in particular, led to the design of a very simple circuit to provide the ORBIT receiver with a proper time base.

The system described in this thesis has been built and is functioning correctly.

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