A 10 NSEC RESOLUTION COUNTER FOR MULTIPARTICLE.
ATOM PROBE TIME-OF-FLIGHT MEASUREMENTS

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ABSTRACT

The atom probe field ion microscope allows single atom identification by combining a field ion microscope with a time-of-flight mass spectrometer. A circuit is described which provides time resolution of ± 10 nsec in an interval of 100 μ sec for up to 8 particles arriving at the detector in any one field evaporation pulse cycle. The duty cycle of the instrument is limited only by the data recording system. The ± 10 nsec resolution allows identification of species separated by one mass unit under the worst case conditions of high atomic weight and high accelerating voltage.

I. INTRODUCTION

The atom probe field ion microscope, developed by Müller, Panitz and McLane¹, is the first time-of-flight micro-mass analyzer which combines the single atom resolution of the conventional field ion microscope with the mass analysis capability of a time-of-flight spectrometer. This instrument provides an extremely powerful tool for the investigation of many phenomena on a single atom scale. A short (5-50 nsec) high voltage pulse, when applied to the specimen, causes the field evaporation of one or more atoms from the surface of the specimen. These ions pass through a small probe hole in the viewing screen of the field ion microscope and travel down a drift tube to a detector. If Δt is the time interval between the evaporation (start) pulse and the arrival signal from the detector (stop) pulse, then the mass to charge ratio of the evaporated species, m/n , is given by

$$\frac{m}{n} = \frac{2eV(\Delta t)^2}{d^2}, \quad (1)$$

where m is the mass of the ion, ne is its charge, d is the specimen to detector distance, and V is the total accelerating voltage (D.C. imaging voltage plus pulse field evaporation voltage).

The time interval, Δt , contains not only the transit time of the field evaporated ion but also the associated propagation delays through the electronic detection system. This delay time, t_{pd} , can be deduced from calibration runs involving the field evaporation of known single isotope species and is not a problem as long as electronic jitter is small.

Very good results can be obtained using a fast storage oscilloscope². This technique gives a directly observable indication of the detector output and a time resolution, with careful calibration, of ± 20 nsec. It is obvious, however, that this is a tedious technique for any study involving more than

a few tens of observations.

The first digital timing device specifically designed for the atom probe microscope was reported by Johnson³. His very elegant circuitry had a resolution of ± 40 nsec and the ability to record the arrival time of up to 5 particles in sequence or to fill accumulators set with pre-set time intervals.

While this circuitry was a major step towards high speed data acquisition, it did not have the resolution required for the most critical types of experiments. Consider, for example, the problem of adjacent mass units, i.e., ^{196}Pt and ^{197}Au . For $V = 20\text{kV}$, $d = 2\text{m}$, and $n = 2$, $\Delta t_{^{196}\text{Pt}} = 10.08 \mu\text{sec}$, and $\Delta t_{^{197}\text{Au}} = 10.10 \mu\text{sec}$, a difference of only 20 nsec.

The present paper describes a ± 10 nsec resolution digital timing circuit designed specifically to be used with the atom probe FIM built in our laboratory. It has the ability to record the arrival times of up to 8 independently arriving particles per pulse sequence and display these times, as 4 decade decimal numbers. All the control and data output lines are paired for either "front panel" operator control or complete computer control. Under computer control the recorded time intervals together with D. C. and pulse voltages can be analyzed "on-line" and the immediate identification of the species can be made. The resolution of the timer can be easily increased to ~ 7.5 nsec by a simple change of the clock oscillator.

II. PRINCIPLES OF OPERATION

The circuit consists of a 100 MHz, .001% accuracy crystal oscillator which supplies the timing pulses to the decade counting registers through a master shift board. The clock pulses are fanned-out to 8 independent clock

drivers which can be started synchronously and stopped in sequence. The clock pulses are sent over twisted pair transmission lines to the first counting board. This board consists of 8 high speed (> 125 MHz) Motorola MC10137L binary coded decimal (BCD) counters, 4 Fairchild 9581, 8-bit multiplexers, and associated carry outputs and reset gates. The carry outputs and 4 BCD lines of the least significant decade go to a converter board where they are translated from the $-1.7V$ and $-0.8V$ logic levels of the high speed emitter-coupled logic (ECL) circuits to the $0V$ and $+5V$ levels of the transistor-transistor logic (TTL) levels. This basic scheme is repeated for 3 more decades with the exception that the BCD and carry outputs are now simply routed through the edge card connectors; thus giving a total timing range of $99.99 \mu\text{sec}$. Additional gating circuits provide the select codes for the 1 of 8 multiplexer in either a direct address mode or a sequential address mode. This dual mode select capability is provided since the computer addresses each register directly by putting its device code on the select lines while an operator would be more inclined to simply push an advance button to read the next register.

III. CIRCUIT DESCRIPTION

The timer circuitry (without power supply) is built on $4 \times 6 \frac{1}{2}$ " cards which fit into a Vero card frame. The clock oscillator occupies the first card, the high speed shift circuitry the second, and so forth. This modular construction technique allows easy circuit access for debugging and repair. The circuit boards are standard prototype designs and are available from a variety of sources. All boards have power and ground busses already "printed on" to permit easy layout. Sockets were used for all the integrated circuits and all wiring was either soldered or wire-wrapped to the socket.

The crystal oscillator consists of an International Crystal 100 MHZ commercial standard crystal with a Fairchild 9582 line driver/receiver as the active element.* The shift board circuitry is shown symbolically in Fig. 1. The sequence of operation is as follows:

A master reset pulse clocks all shift register outputs low (L) and also clocks a high (H) into the 3 input nor gate (MC10111L). This prevents the clock pulses from passing to the outputs. A start pulse clocks a L into the MC10111L from the MC10131L "D" flip-flop thus allowing the outputs to be toggled. This effectively "locks out" the start line from having any further effect upon the counting or shift circuitry. The arrival of a stop pulse clocks the shift register from the nor gate and moves the H input into each successive output. The filling of the last register, or the termination of the counting, causes a pulse to be returned to the shift board which clocks a H into the nor gate, thus terminating the count. This also initiates the "done" flag for the computer interface.

The shift register is composed of 4 MC10131L dual "D" flip-flops. At higher speeds (>150 MHZ) the MC10231L is an exact replacement. Since the start and stop pulses in our system are derived from a LeCroy Research Model 161 discriminator, which provides current source outputs, the inputs to the shift board are designed to provide a D.C. termination followed by an adjustable bias level gate input.

The counting boards are shown in Fig. 2. The 4 decades are identical in concept with the exception that the least significant decade requires;

* Crystal oscillator described in the Fairchild Semiconductor 9500 Series, High Speed Logic Handbook, May 1971..

(1) additional driver and receiver gates for twisted pair data transmission, and (2) reset gating circuits, since the MC10137L's do not have asynchronous reset inputs. The other 3 decade boards consist of National Semiconductor DM8530 decade counters and Texas Instruments SN74151 8 line multiplexers. The DM8530 were chosen over standard SN7490 decade counters because the minimum clock pulse of the DM8530 (15 nsec max.) insures accurate clocking by the 20 nsec wide carry pulses from the first decade.

The converter board consists of Fairchild 9595 ECL to TTL converter circuits. This provides logic level conversion for the 8 carry lines and the LSD BCD output. The BCD outputs go to the computer interface and to the SN7447 BCD to 7 segment decoder/display drivers. The SN7447 directly drives the light emitting diode readouts displays.

The circuit requires +5V at 6A and -5.2V at 5A. The circuit runs quite warm so that a blower is recommended to insure proper operation.

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FIGURE CAPTIONS

Figure 1. Schematic logic diagram for the clock pulse distribution circuitry.

Figure 2. Decade counting board. The wiring pattern for 1/2 of the board is omitted for clarity. Direct (asynchronous) reset is provided for in the 3 most significant decades. Additional gates (not shown) are need to provide the reset function for the least significant decade.

Figure 1.

Figure 2.