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COMPUTER AIDED CIRCUIT RELIABILITY ANALYSIS

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by

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COMPUTER AIDED CIRCUIT RELIABILITY ANALYSIS

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Summary

~~The time allotted for the design of various manual and automated types of system testers at Sandia Corporation is often quite short. To overcome these short design time scales and to help insure the necessary tester reliability, a Reliability Program was put into effect which parallels the test equipment design phase. A brief review of the Reliability Program is presented.~~

It has been found that considerable analysis and design time savings can be achieved by using computers and programs such as the general purpose circuit analysis program, NET-1. This user-oriented program was written by Messrs. A. F. Malmberg and F. L. Cornwell of the Los Alamos Scientific Laboratory (LASL).

Schematic diagrams of two circuits analyzed by the NET-1 program are presented. The necessary input data and plots of the observed and NET-1 predicted output waveforms are also included.

Some of the limitations and problems in using the NET-1 program are discussed.

Plans in process are presented which upon completion will make the NET-1 program even more useful and universal.

Thus far the LASL NET-1 program has enabled the reliability engineers to save a significant amount of analysis time and achieve a more thorough reliability review. The specific in-house programs have also been useful for analysis work.

Computer circuit analysis programs, properly utilized, have proven to be an effective and powerful tool and can be used as both an analysis and design aid for the engineer.

Introduction

A paper describing the reliability program in effect for Sandia Corporation test equipment design was presented by Mr. A. C. Littleford at the Tenth Annual Reliability Symposium in Washington, D.C. Mr. Littleford mentioned the use of computer circuit analysis programs as a tool to decrease the time required for design reviews. During the past year, the test equip-

ment reliability analysts at Sandia Corporation have been using the Los Alamos Scientific Laboratory NET-1 circuit analysis program quite extensively. It is the purpose of this paper to briefly review the reliability program, show how computer circuit analysis programs can be used as a technique to decrease analysis time, cover the usage and effectiveness of the general purpose NET-1 program plus two specific in-house programs as applied to the time problem and indicate some of the plans for making these programs more effective and universal in the future as analysis tools.

Reliability Program

The design time allotted to the various Sandia Test Equipment Design Groups is affected by the continuous changing of test requirements and other design responsibilities. To overcome the design time barrier and its effect upon system reliability, a tester reliability program was initiated at Sandia which is independent of, and runs concurrently with the test equipment design. In order to furnish maximum support to the design engineer, the reliability analyst must work from the designers' rough sketches rather than the formal drawings which are available after the design is firmed up. The purpose of the reliability program is to:

1. assure design reliability, and
2. educate the designer to make reliability an intrinsic characteristic of his design.

The techniques used to implement the reliability program are:

1. Human Factors study of over-all design
2. Electrical Study
  - a. Detailed analysis of every circuit, sub-system and system from a worst case standpoint
  - b. Circuit simplification
  - c. Determining and minimizing the electrical stresses on components
  - d. Check for proper application of individual parts
  - e. Use of quality parts

The results of the analysis, recommendations, etc., are discussed with the designer as the review progresses and the report issued is merely for record purposes.

The minimum analysis time will be achieved by parallelling the above techniques wherever possible.

The logic and control circuitry configuration used in many of the test systems is quite similar. Computers can be used to perform the necessary calculations with a resulting decrease in analysis time if programs are available which are easy-to-use. An easy-to-use program is defined as one which is user-oriented, i.e., requiring no special knowledge of computer programming and very little input data preparation.

The time required to obtain the computer analysis data can be used by the engineer to perform other reliability assignments.

Computer Programs

For several years the Reliability Review Group of the Systems Test Equipment Development Department at Sandia Corporation has been searching for easy-to-use computer programs which could be used as both analysis and design tools. Most of the work in time domain circuit analysis by computer programs has consisted of writing a special program for each circuit configuration of interest. The number of circuit configurations of interest is extremely large requiring a massive library of specific analysis programs. Consequently a general program capable of analyzing any arbitrary circuit in the time domain would seem highly desirable. To be effective in reducing analysis time the preparation of the program input data should require a minimum amount of mathematical manipulation.

The technical literature examined during 1963 contained articles about several analysis and simulation programs which were investigated.^{3, 4} One of these, the general purpose NET-1 Program, written by Messrs. A. F. Malmberg and F. L. Cornwell of the Los Alamos Scientific Laboratory (LASL) has been a very useful analysis tool.

NET-1 Network Analysis Program

NET-1 is a user-oriented program for the Maniac II computer at LASL which simulates both the DC steady state and the transient behavior of a large class of electrical circuits containing passive and solid state components. It has taken approximately five man years to develop the NET-1 program which is currently being converted for use on the IBM 7090 and 7094 computers.⁵

The circuit performance calculations are based upon nodal and mesh analysis techniques.

A circuit described to NET-1 for analysis may include the following elements connected in any manner provided the connections remain fixed: transistors, diodes, signal sources, fixed voltage sources, fixed value resistors, capacitors, inductors, and mutual inductive couplings.

The circuit configuration determines the exact quantity of elements and nodes which NET-1 can handle at one time. The circuit elements and quantities are indicated in Table I.

Table I

<u>Circuit Element</u>	<u>Max. Qty.</u>
C- Capacitor	300
D- Diode	75
K- Coefficient of Coupling	11,500
L- Inductor (If Ckt. contains K)	250
L- Inductor (If Ckt. contains no K)	300
P- Signal Source	63
R- Resistor	300
T- Transistor	40
V- Fixed Voltage Source	63

Total number of nodes equal to or less than 150.

Obviously a fairly complex circuit can be analyzed. The units for both input and output of NET-1 are listed in Table II:

Table II

<u>Quantity</u>	<u>Unit</u>
Time	Nanosecond (10 ⁻⁹ second)
EMF	Volt
Current	Milliampere
Power	Milliwatt
Resistance	Kilohm
Capacitance	Picofarad (UUF)
Inductance	Microhenry

The circuits of Figures 1 and 4 represent typical problems run on NET-1. Programming for NET-1 is very simple and starts with the circuit schematic.

The necessary steps are as follows:

1. Label the circuit elements
  - a. R1, etc., for resistors
  - b. C1, etc., for capacitors
  - c. D1, etc., for diodes
  - d. T1, etc., for transistors
  - e. L1, etc., for inductors
  - f. V1, etc., for fixed voltage sources
  - g. P1, etc., for signal sources

2. Label the circuit nodes (connection points where two or more elements tie together)
  - a. Voltage and signal sources do not require a node number

b. The common or ground connection is always node zero

c. Nodes may be numbered in any order but must be sequential: i.e., 1, 2, 3, etc., and not 1, 3, 7, etc.

3. Name the circuit (title)

4. Make a wire running list of the circuit (see figures 2 and 5)

The program list (3 and 4 above) is then typed on a special Mark II typewriter which prepares a punched paper tape. The punched paper tape is the input control for the NET-1 program.

The data output from the NET-1 program (including the title for identification) is a listing of the node voltages, transistor, diode and inductor currents for the DC steady state conditions and as a function of time for the transient analysis. (See figure 8.) Plots of the wave forms are available using peripheral routines. (See figure 9.)

The time required to analyze the circuits of Figures 1 and 4 manually (develop equivalent circuits and solve equations) versus NET-1 is given in the table below. The manual transient characteristics will usually be obtained from oscilloscope studies of the breadboard models.

ANALYSIS TIME-HOURS

	<u>Manual Methods</u>		
	<u>DC.</u>	<u>Transient (Breadboard)</u>	
Ckt. of Fig. 1	12	10	
Ckt. of Fig. 2	20	14	
	<u>NET-1</u>		
	<u>Program</u>	<u>DC.</u>	<u>Transient</u>
Ckt. of Fig. 1	.25	.08	1.5
Ckt. of Fig. 2	.25	.08	1.5

The illustrated circuits, fabricated on printed circuit boards, belong to a family of preferred circuits. They must operate reliably and have well defined operating specifications. Not all of the circuits reviewed are subjected to such a detailed analysis.

There have been approximately 40 circuits analyzed on NET-1 to date representing over 100 different programs. An analysis time savings of at least 30 percent has been effected. This represents approximately 360 man hours or 12 extra circuits which could have been examined at an average of 30 hours per circuit.

The NET-1 data have enabled the reliability engineers to perform a more detailed analysis in less time for the circuits run on the Maniac II computer than would have been possible using manual methods only.

Comparisons of the NET-1 predicted versus observed output waveforms have been made and the correlation has been good. (See figures 3, 6, and 7.) Any strange circuit performance characteristic as predicted by NET-1 is carefully examined and verified before the data is accepted as accurate. One of the major discrepancies thus far has been due to differences between the actual signal input to the circuit and that described to NET-1.

Limitations. Some of the limitations experienced in using the NET-1 program will now be reviewed.

1. To obtain a worst case analysis the engineer must determine and use the worst case circuit conditions. NET-1 at the present time does not have the capability of varying circuit values to determine these conditions. This has not been a serious problem since it is possible to run several programs with different component values for the circuits being studied.

2. The present diode and transistor library tape for NET-1 contains parameter information for only 40 transistors and 13 diodes. (See figure 10.) If the transistor or diode appearing in the circuit is not on the NET-1 library tape it is still possible to run the circuit by using a parameter substitution routine. After a new transistor or diode has been used in a circuit it can be added to the library tape provided there is agreement between the observed and NET-1 predicted waveforms. It is thus possible to expand the library tape in this manner.

3. Circuits containing unijunction transistors, tunnel diodes, etc. cannot be analyzed at the present time.

4. Some circuits such as a low frequency oscillator (10KC or less) require many hours of computer time on the Maniac II.

5. Until the NET-1 program is converted for the IBM 7090 and 7094 computers the Maniac II at LASL must be used for analysis.

Future Planning. The following work is now in process to overcome the above limitations.

1. Mr. Malmberg is writing a NET-II program which will allow component variations to be included without having to run a variety of programs to obtain the worst case analyses.

2. A development contract is being negotiated for the purpose of:

a. Developing a methodology for obtaining diode and transistor parameter information for the modified Ebers-Moll models. (See figures 11 and 12.)

b. Developing models, defining equations, parameters and the method for obtaining parameter values for:

1. unijunction transistors
2. tunnel diodes
3. zener diodes
4. silicon controlled rectifiers
5. silicon controlled switches

This will provide an easy method for expanding the semiconductor library tape and allow circuits containing unijunction transistors, tunnel diodes, etc., to be analyzed with the NET-1 program.

3. The conversion of NET-1 for use on other computers will broaden the potential usage of the program and the use of high speed computers will make low frequency oscillator circuit analysis less time-consuming.

SPECIFIC IN-HOUSE PROGRAMS

Two in-house programs, UNOC-1 and NPN-1 written in Fortran, are also being used to provide analysis data for the engineers. (See figures 13 and 16.) These programs merely mechanize the manual DC state analysis steps and make it possible for the analyst to use a computer to perform the calculations. (See Appendix A.) The input data for these programs is a deck of cards with the component values, voltages, etc., located in specific fields and arranged in the order shown in figures 14, 15, and 16. The output data are shown in figures 17 and 18.

These programs as written can only be used for the specific indicated circuit configurations..

Conclusions

The analysis and design time required for many circuits can often be greatly reduced by using computers provided the necessary easy-to-use analysis programs are available to the engineer.

Computers should not be used indiscriminately for analysis work particularly if the circuits are relatively simple and the desired information can be obtained easily by manual methods.

There may be no particular advantage in using computer analysis programs if the preparation time of the input data for a given circuit approaches the manual analysis time required.

The general purpose NET-1 program at LASL has been a useful tool in helping to decrease the circuit analysis time for reliability reviews. The degree of the analysis using NET-1 has been much greater than would have been possible using manual methods.

Models and parameter information for unijunction transistors, zener diodes, tunnel diodes, silicon controlled rectifiers, and switches, and other special devices will be included in the

NET-1 program when they are available. This will further increase the usefulness of the program.

Circuit design can usually be improved by using the analysis data from the NET-1 program as a guide for optimizing the circuit elements to achieve the desired performance characteristics.

The computer can thus be used in lieu of a breadboard until the circuit is firmed up at which time a breadboard model can be built as the final check.

Circuit analysis computer programs, such as NET-1, have proven to be valuable reliability analysis tools, particularly when analysis time is severely limited.

References

1. Design Analysis: An Effective Reliability Tool by Mr. A. C. Littleford, Sandia Corporation, Albuquerque, New Mexico, Proceedings Tenth National Symposium on Reliability and Quality Control.
2. NET-1 Network Analysis Program by Messrs. A. F. Malmberg and F. L. Cornwell, Los Alamos Report No. LA-2853.
3. Circuit Simulation: A Potent Tool Takes Shape by Mr. Gregory Comstock, Electronic Design, April 26, 1963.
4. Computer Programs for Circuit Design by Mr. Howard Falk, Electro-Technology, March 1964.
5. NET-1 Network Analysis Program by Mr. A. F. Malmberg, Proceedings Eleventh National Symposium on Reliability and Quality Control.

FIGURE 2

"NET-1 #1158 AE-3153 3 INPUT DIODE-TRANSISTOR GATE CIRCUIT JULY 30, 1964"

R1	0	1	1	D2	0	4	IN270 (2)
R2	2	0	1	D3	P1	7	IN270
R3	3	0	1	D5	6	7	IN270 (2)
R5	V1	4	1.8 (2)	D6	9	10	IN270 (5)
R6	4	5	1.5 (2)	T2	0	5	2N404 (2)
R7	V3	5	7.5 (2)	T3	0	8	2N404
R8	V1	6	1.8 (2)	T4	0	11	2N404 (5)
R9	V1	7	1.8	V1	-12		
R10	7	8	1.5	V2	12		
R11	V2	8	7.5	V3	11.8		
R12	V1	9	1.8	P1	PULSE - .5 -12 0 50 20+3 50 40+3		
R13	V1	10	1.8 (5)	RESOLUTION	20		
R14	10	11	1.5 (5)	INTERRUPT	2+03		
R15	V2	11	7.5 (5)	END			
R16	V1	12	1.8 (5)				

Figure 3 (Node 9 of Figure 1)

R1	V1	2	24	D20	P1	11		1N270
R2	2	3	10	D1	1	2		1N270
R3	V1	4	1.8	D2	10	2		1N270
R4	V2	3	51	D5	6	7		1N270
R5	V1	6	1.8	D6	6	12		1N270 (4)
R6	4	5	1.5	T4	0	13	1	2N404
R7	V1	9	.3	T1	0	3	4	2N598
R8	V2	5	7.5	T2	0	5	6	2N404
R9	V1	7	1.62	T3	0	8	9	2N404
R10	7	8	1.35	T5	0	14	10	2N404
R11	V2	8	8.25	T8	0	15	16	2N404 (4)
R12	V1	1	1.8	V1	-12			
R13	11	13	1.5	V2	12			
R14	0	14	.5	P1	PULSE -.5 -12 0 50 20+03 50 30+03			
R15	V2	14	2.5	RESOLUTION	10			
R16	V1	10	.6	PRINT	100			
R23	V2	13	7.5	INTERRUPT	6+03			
R24	V1	12	1.8 (4)	END				
R25	12	15	1.5 (4)	PARAMETER SUBS				
R26	V2	15	7.5 (4)	T0				
R27	V1	16	1.8 (4)	BN 40				
R50	V1	11	1.8	T1				
				BN 70				

Figure 6 (Nude 1 of Figure 4)

Figure 7 (Nude 6 of Figure 4)

```

TIME 0.00000+00      CYCLE 0
      P1
      0.00000+00
              1          2          3          4          5          6
              -1.07726-15 -1.07726-15 -1.90818-15 -1.26011-03 -1.26011-03 -3.13184-01
      L1
      0.00000-35
              IE          IB          IC
T1  1.07726-15  1.90818-16 -1.26808-15
T2  8.46080-01 -8.58682-01  1.26011-02
T1 SWITCHED FROM OFF TO ACTIVE AT TIME = 0.00000+00
T1 SWITCHED FROM ACTIVE TO SATURATION AT TIME = 5.00000+00
TIME 1.00000+02      CYCLE 20
      P1
      -8.20000+00
              1          2          3          4          5          6
              -5.55508-01 -2.92873-02 -5.02346-03 -6.09283-03 -1.26028-03 -3.13184-01
      L1
      -5.35341-02
              IE          IB          IC
T1  -7.59096+00  1.81981-01  7.40898+00
T2  8.46562-01 -8.58682-01  1.21195-02
T1 SWITCHED FROM SATURATION TO ACTIVE AT TIME = 1.20000+02
T1 SWITCHED FROM ACTIVE TO SATURATION AT TIME = 1.25000+02
T1 SWITCHED FROM SATURATION TO ACTIVE AT TIME = 1.30000+02
T1 SWITCHED FROM ACTIVE TO SATURATION AT TIME = 1.35000+02
T1 SWITCHED FROM SATURATION TO ACTIVE AT TIME = 1.40000+02

```

Figure 8 Typical NET-1 Data Print Out

FIGURE 10
TRANSISTOR AND DIODE LIBRARY TAPE #111:15 JANUARY 1964

1N914	2N1483	1N995
1N661	PT1867	2N705
1N279	2N2048	1N2199
2N393	2N457	2N706A
2N1307	2N1613	2N2188
2N1306	SD500	2N976
2N398	2N356	2N414
2N404	2N315	2N1308
2N711A	2N964	1N100
2N1037	2N797	2N1304
2N1039	TM12066	2N2369
1N63	2N385	2N2894
2N364	2N1301	2N174
2N1289	2N598	2N1132
2N2087	2N697	1N270
1N140	2N1499A	1N3605
2N597	1N191	FD700
2N645	2N1711	

1N100			
00		0.000000+00	
01	RB	1.700000-02	
02	RC	1.000000+03	
03	IS	2.500000-03	
04	TEMP	2.500000+01	
05	P	5.000000+01	
06	VR	8.000000+01	
07	IF	4.500000+01	
08	VZ	5.000000-01	CONT. POTEN.
09	N	5.000000-01	GRADING CONST.
0A	CM	5.000000-01	MEASURED CAP. FOR VM VOLTS
0B	VM	0.0	VOLTS FOR SPECIFIC CM
0C	F	1.000000-01	CONST.
0D	M	2.650000+00	CONST.
0E		0.0	
0F		0.0	
10		0.0	
11		0.0	
12		0.0	
13		0.0	
14		0.0	

FIGURE 12
TRANSISTOR AND DIODE LIBRARY
TAPE #106 3 JULY 1963

2N1306		NPN	
00		0.000000+00	
01	RBB	4.000000-02	
02	RC	4.000000+03	
03	RCC	1.000000-03	
04	REE	1.000000-04	
05	RE	1.500000+04	
06	A1	1.000000+00	
07	A2	0.0	
08	A3	0.0	
09	A4	0.0	
0A	A	1.000000+00	
0B		0.0	
0C	B1	1.000000+00	
0D	B2	0.0	
0E	B3	0.0	
0F	B4	0.0	
10		0.0	
11		0.0	
12	BN	1.000000+02	GAIN
13	BI	5.000000+00	INV. GAIN
14	ICS	3.500000-04	C TO B SAT. CURR.
15	P	1.500000+02	POWER
16	TEMP	2.500000+01	
17	VCE	1.500000+01	
18	VBE	2.500000+01	
19	VCB	2.500000+01	
1A	IC	3.000000+02	
1B	VZC	1.401000-00	C TO B JUNCT. CONT. POT.
1C	NC	4.073000-01	C TO B GRADING CONST.
1D	CMC	2.998000-01	
1E	VTC	-1.000000+00	
1F	VZE	1.400000+00	E TO B JUNCT. CONT. POT.

20	NE	4.000000-01	E TO B GRADING CONST.
21	CME	1.000000+01	
22	VTE	-5.000000+00	
23	FN	1.200000-02	PROP. CONST.
24	FI	2.000000-03	PROP. CONST.
25	IES	3.427000-04	E TO B SAT. CURR.
26	ME	1.517000+00	EMISSION CONST. - EMITTER
27	MC	1.500000+00	EMISSION CONST. - COLLECTOR
28		0.0	
29		0.0	
2A		0.0	
2B		0.0	
2C		0.0	
2D		0.0	
2E		0.0	
2F		0.0	
30		0.0	
31		0.0	

FIGURE 13
TYPICAL UNIJUNCTION OSCILLATOR CIRCUIT

DATA	DESCRIPTION	CARD NO.
1 2 3 4 5 6 7 8 9 10	15 ————— 72	74 75
1	NO. OF FIXED EM. RES. (5 MAX.)	1
	UNIJ. TRANS. CARD	2
2 .	DES. SPEC. V. P. CUR. SAFETY FACTOR	3
4 .	DES. SPEC. PEAK POINT SAFETY FACTOR	4
2 8 .	NOMINAL SUPPLY VOLTAGE	5
. 0 5	DECIMAL TOL. OF SUPPLY VOLTAGE (FOR 5%)	6
. 1	DECIMAL TOL. OF FIXED RES. (FOR 10%)	7
. 0 0 0 0 4 7	EMITTER TIMING CAP. (FARADS) [MIN. VALUE = $1\mu f$]	8
1 0 3 .	BASE 1 SERIES RES. (OHMS)	9
3 3 0 .	BASE 2 SERIES RES. (OHMS)	1 0
1 0 0 0 0 .	ADJ. EM. RES. (OHMS)	1 1
2 6 7 0 .	R (1) SMALLEST VALUE EM. RES. (OHMS)	1 2
3 3 2 0 0 .	R (5) LARGEST	1 6

FIGURE 14 CARD FIELDS

FIGURE 15
UNIUNCTION TRANSISTOR CHARACTERISTICS ON 1 CARD FOR UNOC 1 PROGRAM

FIELD LOCATION	LISTED AS	MAX. OR MIN. MAGNITUDE	DESCRIPTION
1 - 5	492B	5 CHARACTERS	NAME LESS 2N PREFIX
6 - 8	.56	3 CHARACTERS	n = MIN. INT. S. O. RATIO
9 - 11	.68	3 CHARACTERS	n = MAX. INT. S. O. RATIO
12 - 16	6800.	9999. OHMS	MIN. INTERBASE RESISTANCE
17 - 23	9100.	999,999. OHMS	MAX. INTERBASE RESISTANCE
24 - 27	3.0	999. VOLTS	MIN. VALLEY VOLTAGE
28 - 31	5.0	999. VOLTS	MAX. VALLEY VOLTAGE
32 - 38	.008	.000001 AMPS	MIN. VALLEY POINT CURRENT
39 - 45	.000006	.000001 AMPS	MAX. PEAK POINT EM. CURRENT
46 - 50	60.	6000. VOLTS	INTERBASE VOLTAGE
51 - 56	.07	.00001 AMPS	RMS EMITTER CURRENT
57 - 62	2.0	99,999. AMPS	MAX. PEAK EM. CURRENT
75	2	2	CARD NUMBER

FIGURE 16

CARD FIELDS	DESCRIPTION
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17	
SEE FORMAT FOR CARD 1	TRANSISTOR
1 N 2 7 0 0 . 3 1 0 . 4 5	DIODE
1 . 8 1 0 . 0	R1
2 . 4 1 0 . 0	R2
6 . 8 1 0 . 0	R3
. 9 3 0 . 0	R4 = RELAY COIL
1 2 . 0 1 . 0	V1 & VARIATION IN VOLTS
1 2 . 0 1 . 0	V2 & VARIATION IN VOLTS
2 8 . 0 1 . 0	V3 & VARIATION IN VOLTS

FOR RESISTORS: 10.0 = $\pm 5\%$; 20.0 = $\pm 5\%$; 30.0 = $\pm 10\%$ & TEMP. COEF.

FORMAT FOR CARD #1 - TRANSISTOR

FIELDS

- 1 - 7 = TYPE NUMBER 2N1613 ETC.
- 8 - 13 = MINIMUM EMITTER TO BASE VOLTAGE
- 14 - 19 = MAXIMUM EMITTER TO BASE VOLTAGE
- 20 - 23 = GAIN
- 1 - 7 = TYPE NUMBER 1N270 ETC.
- 8 - 13 = MINIMUM VOLTAGE DROP
- 14 - 17 = MAXIMUM VOLTAGE DROP

DIODE FORMAT

FIGURE 17
NPN GATE CIRCUIT ANALYSIS

TRANSISTOR - 2N1304
DIODE - 1N270

RESISTANCE IN KILOHMS - CURRENT IN MILLIAMPS

	MIN.	NOMINAL	MAX.
R1 =	1.53000	1.80000	1.89000
R2 =	2.04000	2.40000	2.52000
R3 =	5.78000	6.80000	7.14000
R4 =	.40500	.45000	.49500
R4C =	.36802		.56170
V1 =	11.00000	12.00000	13.00000
V2 =	11.00000	12.00000	13.00000
V3 =	11.00000	12.00000	13.00000
VEB =	.25000	#	.40000
VD =	.30000		.45000
REQUIRED BASE CURRENT IEB = .68303			
CURRENT I = 1.48459			
CURRENT II = .80157			
CURRENT I3 = 7.20285			
VNI = 1.33139			
VTH1 = 12 + RTH - (VNI - VDH)			
5.51989 + 6.40128 RTH = .88139			
VTH2 = 12P + RTH + VDL			
8.60065 + 8.30065 RTH + .30000			
FOR DIODE TO BE OFF			
VTH3 = 10.01850			
V1 CURRENT = 19.5000			
V2 CURRENT = 83.8196			

FIGURE 18
DESIGN ANALYSIS OF A UNIJUNCTION TRANSISTOR RELAXATION OSCILLATOR CIRCUIT WITH COMPONENT
AS INDICATED ON THE DRAWING. TYPE 2N 492B UNIJUNCTION

SPECIFIED INTRINSIC STAND OFF RATIO		SPECIFIED INTERBASE RESISTANCE IN OHMS		EMITTER TO BASE ONE VOLTAGE DROP IN VOLTS	
MIN	MAX	MIN	MAX	MIN	MAX
A1	A2	RBB1	RBB2	VEB1	VEB2
.58	.68	6200.	9100.	3.00	5.00

MINIMUM SPECIFIED VALLEY
POINT CURRENT IN AMPS
CIV = .0080

MAXIMUM PEAK FIRING
CURRENT IN AMPS
CP = .000006

18.00 = VBB-NOMINAL SUPPLY VOLTAGE
.020 = TOL. OF SUPPLY VOLTAGE
.100 = FIXED RESISTOR TOLERANCE

FIGURE 18 (CONTINUED)

SUPPLY VOLTAGE IN VOLTS		PEAK FIRING VOLTAGE IN VOLTS		OUTPUT VOLTAGE			
MIN	MAX	MIN	MAX	STATIC	DYNAMIC		
VBB1	VBB2	VPMIN	VPMAX	EO1	EO2	EOMIN	EOMAX
17.640	18.360	10.478	13.085	.086	.159	5.494	10.223

CIRCUIT CONSTANTS AS SPECIFIED ON DRAWING

EMITTER CIRCUIT COMPONENTS
RESISTORS ARE NOMINAL VALUES IN OHMS
RA = 1000000.
R (I) = 72500.
CAPACITOR NOMINAL FARADS
C1 = .000005000000

VOLTAGE RATING OF CAPACITOR C1
19.6 VOLTS

NOMINAL VALUES OF SERIES RESISTANCE IN OHMS
BASE ONE
PB1 = 51.00
BASE TWO
RB2 = 240.00

199. OHMS TO 368. OHMS = RANGE OF RB2.

CALCULATED TIME CONSTANTS OF THE EMITTER CIRCUIT USING NOMINAL COMPONENT VALUES
MIN I = C1 * R (M) = SECONDS
.362500
MAX I = C1 * (RA + R (M)) = SECONDS
5.362500

APPENDIX A

EQ. CKT. FOR
UNIJUNCTION

SAMPLE EQUATIONS FOR FIGURE 13

1. TIME CONSTANTS OF EMITTER CIRCUIT USING NOMINAL VALUES OF R (1) ETC.
  - a. $MIN = R(1) \cdot C1$
  - b. $MAX = (R(1) + RA) \cdot C1$
2. SUPPLY VOLTAGE VARIATION
  - a. $\overline{VBB} = VBB + (VBB \cdot TOLERANCE)$
  - b. $\underline{VBB} = VBB - (VBB \cdot TOLERANCE)$

SAMPLE EQUATIONS FOR FIGURE 13 (CONTINUED)

3. RB2 - BASE 2 FIXED SERIES RESISTOR
  - a. $\underline{RB2} = RB2 - (RB2 \cdot TOLERANCE)$
  - b. $\overline{RB2} = RB2 + (RB2 \cdot TOLERANCE)$
4. RB1 - BASE 1 FIXED SERIES RESISTOR OR EFFECTIVE IMPEDANCE.
  - a. $\underline{RB1} = RB1 - (RB1 \cdot TOLERANCE)$
  - b. $\overline{RB1} = RB1 + (RB1 \cdot TOLERANCE)$
5. PEAK FIRING POINT VOLTAGE
  - a. $VP_{MIN} = \eta \cdot \underline{VBB} + 0.6$
  - b. $VP_{MAX} = \bar{\eta} \cdot \overline{VBB} + 0.6$
6. OUTPUT VOLTAGE AT BASE 1
  - a. STATIC
    - 1) $MIN = EO1 = \frac{\underline{RB1} \cdot \underline{VBB}}{(\underline{RB1} + \underline{RB2})}$
    - 2) $MAX = EO2 = \frac{\overline{RB1} \cdot \overline{VBB}}{(\overline{RB1} + \overline{RB2})}$
  - b. DYNAMIC - ASSUMING IMMEDIATE SATURATION OF UNJ.
    - 1) $MIN = EOMIN = VP_{MIN} - VEB2 - (2.0 \cdot \frac{\underline{RB1} \cdot \underline{VBB}}{(\underline{RB1} + \underline{RB2})})$
    - 2) $MAX = EOMAX = VP_{MAX} - VEB1 - (2.0 \cdot \frac{\overline{RB1} \cdot \overline{VBB}}{(\overline{RB1} + \overline{RB2})})$

THE DATA OUTPUT FROM UNOC 1 IS A LISTING OF:

1. NAME OF CIRCUIT & UNJ. TYPE
2. MFR. SPECS FOR UNJ. USED: INTRINSIC, STAND-OFF RATIO, INTERBASE RESISTANCE, ETC.
3. SUPPLY VOLTAGE AND TOLERANCE
4. FIXED RESISTOR TOLERANCE
5. MAX. & MIN. VALUES OF SUPPLY VOLTAGE
6. MAX. & MIN. VALUES OF PEAK FIRING VOLTAGE
7. MAX. & MIN. VALUES OF BASE 1 OUTPUT VOLTAGE BOTH STATIC & DYNAMIC.
8. NOMINAL VALUES OF CAPACITOR AND RESISTORS USED
9. ALLOWABLE RANGE OF BASE 2 SERIES FIXED RESISTOR.
10. MAX. & MIN. EMITTER CIRCUIT TIME CONSTANTS.