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LAMPF Data Handling Workshop

Introduction to CAMAC

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MASTER

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LAMPF Data Handling Workshop

Introduction to CAMAC

by

J. P. Egger*

*Alien Guest. Permanent address: Institut de Physique,
Universite 2000 Neuchâtel, Switzerland.

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LAMPF DATA HANDLING WORKSHOP

Introduction to CAMAC

by

J. P. Egger

ABSTRACT

A typical on-line data-acquisition system for a LAMPF beam line consists of a PDP-11 computer interfaced to the CAMAC system with a microprogrammed branch driver (MBD). This part of the LAMPF data handling workshop describes the CAMAC system. The basic features and some programming examples of CAMAC modules are given.

I. INTRODUCTION

CAMAC is a general purpose electronic standard, particularly useful for data acquisition, process control, and digital information handling in connection with a computer.

The name CAMAC has no real meaning.

II. GENERAL DESCRIPTION

CAMAC is a system with up to seven crates, each of them offering space for up to 23 individual single-width modules (the two right most positions being reserved for control). The "Dataway" is the name given to all interconnections between the connectors of a CAMAC crate. In our case the CAMAC crates are connected to the PDP-11 computer through an MBD (microprogrammed branch driver) according to Fig. 1. All users modules are connected to the crate via a 86-pin connector (see Fig. 2 for pin allocation) in the back of the module. The following lines are connected:

---24 READ lines (R1 - R24):

Data are presented by the module when so demanded by the corresponding FCNA command (F = function, C = crate number, N = slot number, A = subaddress). The FCNA commands will be described below.

---24 WRITE lines (W1 - W24):

Data enters the module when so demanded by the corresponding FCNA command.

---5 Function lines (F):

Permits the use of up to 32 coded different functions, like F(0) → READ, F(9) → CLEAR, F(16) → WRITE, etc. These functions are given and explained below.

---1 Station address line (N):

This is an individual station address line to each slot in the crate coming from the control station.

---4 Subaddress lines (A):

Allows the use of up to 16 coded subaddresses in a given module. Examples of use of subaddresses will be given later.

---1 Individual LAM station demand line (LAM = look at me):

A LAM signal is produced when the users module wants to call the computer. This call may be due to: scaler's overflow, end of stepping motor controller countdown, etc. The specification sheet of a module tells you under what circumstances a LAM

Fig. 1. CAMAC multicrate systems.

Pin Allocation at Normal Station Viewed from Front of Crate

Individual Patch Point	P1	B	Busy	- Bus Line
" " "	P2	F16	Function	" "
" " "	P3	F8	"	" "
" " "	P4	F4	"	" "
" " "	P5	F2	"	" "
Bus Line - Response	X	F1	"	" "
" " with Patch Point - Inhibit	I	A8	Sub-Address	" "
" " " " " - Clear	C	A4	"	" "
Individual Lines - Station Number	N	A2	"	" "
with Patch Points - Look-at-Me	L	A1	"	" "
Bus Line - Strobe 1	S1	Z	Initialize	" "
Bus Line - Strobe 2	S2	Q	Response	" "
	W24	W23		
	W22	W21		
	W20	W19		
	W18	W17		
	W16	W15		
	W14	W13		
	W12	W11		
	W10	W9		
	W8	W7		
	W6	W5		
	W4	W3		
	W2	W1		
	R24	R23		
	R22	R21		
	R20	R19		
	R18	R17		
	R16	R15		
	R14	R13		
	R12	R11		
	R10	R9		
	R8	R7		
	R6	R5		
	R4	R3		
	R2	R1		
	-12	-24	-24 volts dc	
	+200	-6	-6 volts dc	
	ACL	ACN	Reserved for 117 volts ac Neutral	
	Y1	E	Reserved for Clean Earth	
	+12	+24	+24 volts dc	
	Y2	+6	+6 volts dc	
	0	0	0 volts (Power return)	

24 Write Bus Lines

W1 = least significant bit
W24 = most significant bit

24 Read Bus Lines

R1 = least significant bit
R24 = most significant bit

Reserved for -12 volts dc
Reserved for +200 volts dc
Reserved 117 volts ac Live
Reserved
Reserved for +12 volts dc
Reserved
0 volts (Power return)

-24 volts dc
-6 volts dc
Reserved for 117 volts ac Neutral
Reserved for Clean Earth
+24 volts dc
+6 volts dc
0 volts (Power return)

Fig. 2. 86-pin connector.

signal will be generated. Examples of use of LAM signals will be discussed later.

---1 Q-Response:

An FCNA command to a particular module, is usually acknowledged with a Q-response. Q may be 0 or 1. Q = 1 is returned for a FCNA command except in the three following cases.

- the command is not valid and has not been accepted by the module,
- Q = 0 is the result of a test, and
- the particular command has no Q-response (see specification sheet of module to find out if a Q-response is implemented for a particular FCNA command).

---1 X-line (command accepted):

X = 1 is returned for an accepted FCNA command (similar to Q). Note that some older CAMAC modules have no X-line implemented. Furthermore, for a module with an X-line, only the combination X = 0, Q = 1 indicates necessarily a malfunction.

---Various other lines, like I (inhibit), C (clear), S1 and S2 (timing strobes), Z (initialize), and B (busy), etc.

---Power supply lines

Most of the CAMAC modules have in the back a second connector called the 36-pin Input/Output connector. Examples of wiring of this I/O connector

will be shown later. Some modules may also have I/O connections on the front panel.

III. FCNA DATAWAY COMMANDS

Each CAMAC module has its specification sheet in which the possible FCNA commands are listed. The following commands are possible:

Command	No. of Bits	Possible Numbers
F(function code)	5	0 - 31
C(crate)	3	1 - 7 crate 1 - crate 7
N(slot)	5	1 - 31 station 1 - station 25
A(subaddress)	4	0 - 15
total	17	

As we know, the PDP-11 is a 16-bit computer. To get around the problem of the command requiring 17 bits, bit F8 is generally omitted from the command word and supplied separately depending on the type of F-command in which it appears:

Types of F-commands

F(0) - F(7):	read	bit F8 = 0
F(8) - F(15):	control/test	bit F8 = 1
F(16) - F(23):	write	bit F8 = 0
F(24) - F(31):	control/test	bit F8 = 1

Examples of F-commands

F(0) - F(3):	normal read
F(2)	: can be a read and clear
F(6)	: can be a read of module identification number
F(8)	: returns Q=1 if LAM request is true
F(9)	: clear
F(10)	: clear LAM
F(14)	: set LAM
F(16), F(17):	normal write
F(24)	: LAM disable
F(25)	: Increment
F(26)	: LAM enable

Examples of commands with N > 25 (we assume here C = 1):

		Octal No. without F8
F(24) C(1) N(30) A(9)	turn dataway inhibit off	101751
F(26) C(1) N(30) A(9)	set dataway inhibit	121751
F(24) C(1) N(30) A(10)	disable branch driver input	101752
F(26) C(1) N(30) A(10)	enable branch driver input	121752

IV. EXAMPLES OF SPECIFICATION SHEETS AND PROGRAMMING OF CAMAC MODULES

A. Kinetic Systems KS 3360 Stepping Motor Driver

Specification sheet:

Command	Action
F(0)·A(X) ¹	Gates sign bit and 15-bit countdown register onto Dataway.
F(1)·A(0)	Gates 8-bit status register onto Dataway.
F(6)·A(0)	Gates module identifying number onto Dataway.
F(8)·A(X)	Returns Q if LAM source is true.
F(16)·A(X)·S1	Latches sign bit, writes data into 15-bit countdown register, and initiates countdown at S2.
F(24)·A(X)·S1	Disables LAM status bit.
F(26)·A(X)·S1	Enables LAM status bit.
F(28)·A(X)·S1	Turns control transistor OFF.
F(30)·A(X)·S1	Turns control transistor ON.

NOTE:

¹The subaddress (X) may be 0 or 1.

This driver can drive two stepping motors. Stepping motor 1 is addressed with subaddress 0 and stepping motor 2 is addressed with subaddress A = 1.

F(16) A(X): This command clears LAM and writes into the lower 16-bits of the 24-bit dataway write lines. Bit 16 is the sign bit (bit 16 = 0 → up, CW rotation; bit 16 = 1 → down, CCW rotation). A number of pulses of 100 μsec each corresponding to the content of the lower 15 bits is generated. After the countdown of pulses reaching zero or the count stopping due to external inhibit, the LAM is set.

F(8) A(X): This command is used to test if the pulse countdown is completed:

- during pulse countdown: LAM cleared → Q = 0
- after pulse countdown: LAM set → Q = 1.

The waiting until the countdown is completed could be done in the following way in a FORTRAN program:

```

C   F,C,N,A = FCNA COMMAND
C   D = DATA, Q = Q-RESPONSE
      IMPLICIT INTEGER (A-Z)
      .
      .
      .
      C = 1
      N = 1
      A = 0
1    F = 8
      CALL MBDC(F,C,N,A,D,Q)
      IF(Q) 1, 1, 2
2    CONTINUE
      .
      .
      .

```

F(1) A(0): This command gates the 8-bit status register onto dataway. The meaning of the 8 bits is the following:

F(26) A(X) and F(24) A(X): Enables and disables LAM status bit. When the connected stepping motor is at rest, the corresponding LAM is always set. There is no way to clear this LAM. To avoid

interferences with other modules one can disable the LAM status bit (F(24) A(X)).

F(28) A(X) and F(30) A(X): Usually the motor power control is not wired into the KS 3360 modules we have here. So these commands will only modify bits 7 and 3 of the status register.

F(6) A(0): Gates the module identifying number (3360 decimal!) onto dataway.

F(0) A(X): It reads the dataway, that means that after an F(16) command the status of the pulse countdown is read. After the countdown is completed, the F(0) command will read zero and not the actual stepping motor position.

NOTE: Following is a general description of the 3360 stepping motor controller and a diagram (Fig. 3) showing the I/O connector in the back of the module.

CAMAC Dual Pulse and Stepping Motor Controller Model 3360

General Description

The model 3360 is a single-width module that contains two separate channels for producing trains of serial output pulses. Writing a 16-bit sign and magnitude word into a countdown register initiates a process that counts the register down to zero while generating an output pulse at each count.

Two transformer-coupled outputs are provided for each pulse train, and the pulse train is steered to one or the other by the sign bit. The countdown is halted at a count of zero or upon ground closure of one of two external inputs. The sign bit determines which of the external inputs is able to inhibit the counting process, and an attempt to restart the counting by writing a signed number while the related input is grounded will fail. The number will not be written and NO-Q will be returned.

A separate clock is provided for each channel, and the pulse rates are adjustable from 60 pps to 400 pps. Nominal pulse width is 100 microseconds. Means are provided to allow external control of the pulse rates.

The countdown registers are both readable and writeable.

Interrupt Capability

A LAM source bistable is provided for each channel. The bistable is cleared by write command

and is set by the count reaching zero or by the count stopping due to external inhibit. The LAM sources may be tested, or the 8-bit status register, which contains LAM source information, may be read. The LAM sources may be separately enabled and disabled.

Motor Controller Application

The 3360 is particularly useful as a dual-channel stepping motor controller. The pulses for clockwise (CW) rotation are available at one output, for counterclockwise (CCW) rotation at the other. A 1 in the sign bit designates CCW rotation. CW and CCW limit switches can be ground-connected to the external inputs. Operation of the CW limit switch, for example, will inhibit a CW pulse train, will not inhibit a CCW pulse train, and will cause any write commands with 0 in the sign bit to fail.

A transistor output for each channel is available to drive a relay to control power to the motor. An 8-bit status register may be read (four bits per channel) to ascertain the motor status. The four bits are LAM source, CCW limit, CW limit, and motor power.

Front Panel

A jack-screw is provided which functions both in insertion and in extraction of the module. The status indications on the front panel include an N light which flashes whenever the module is addressed and the following indicators for each channel:

- LE - ON whenever LAM is enabled
- L - ON whenever LAM source is true
- CW - ON whenever CW limit is present
- CCW - ON whenever CCW limit is present

Command	Action
F(0)·A(X) ¹	Gates sign bit and 15-bit countdown register onto Dataway.
F(1)·A(0)	Gates 8-bit status register onto Dataway.
F(6)·A(0)	Gates module identifying number onto Dataway.
F(8)·A(X)	Returns Q if LAM source is true.
F(16)·A(X)·S1	Latches sign bit, writes data into 15-bit countdown register, and initiates countdown at S2.
F(24)·A(X)·S1	Disables LAM status bit.
F(26)·A(X)·S1	Enables LAM status bit.
F(28)·A(X)·S1	Turns control transistor OFF.
F(30)·A(X)·S1	Turns control transistor ON.

NOTE:

¹The subaddress (X) may be 0 or 1.

B. 15-Channel Analog Read Relay Multiplexer (KS 3530)

Specification sheet:

Command	Action
F(0)·A(0)	Gates the address register onto the Dataway.
F(1)·A(15)	Gates the module number (3530 = 6712 ₈) on the Dataway.
F(16)·A(0)·S1	Writes the address register from the Dataway.
F(25)·A(0)·S1	Increments the address register.
(Z + C)·S2	Clears the address register.

This multiplexer contains 15 relays for switching one of 15 analog input signals onto an output. The indication which of the 15 inputs is connected with the output is given by a 4-bit address register that can be read, written and incremented by CAMAC command.

This module can be used for example for multiplexing analog signals into a DVM.

F(16)A(0): This command writes a number between 1 and 15 decimal into the address register. This is then the number of the connected input. As an example the write command is illustrated by the subroutine AMUL (see listing which follows Fig. 3).

F(25)A(0): Increments the address register. This is a practical command to sample all 15 inputs into the output. For example, a FORTRAN program to read 15 inputs in order into a DVM would look like this (same variables than before):

```

IMPLICIT INTEGER (A-Y)
.
.
.
N = 2
A = 0
D = 0
DO 1 J = 1,15
F = 25
CALL MBDC(F,C,N,A,D,Q)
C
SUBROUTINE DVM IS DVM READOUT
CALL DVM (Z)
1 CONTINUE
.
.
.

```

Kinetic Systems KS 3360
Stepping Motor Controller

Power Requirements

+6	1200	ma	- 6		ma
+12		ma	-12		ma
+24	30	ma	-24		ma

I/O Connector

1R	Chassis common	1	Chassis common
2R	CH-1, CW pulse out +	2	CH-1, CW pulse out -
3R	CH-1, CCW pulse out +	3	CH-1, CCW pulse out -
4R	CH-2, CW pulse out +	4	CH-2, CW pulse out -
5R	CH-2, CCW pulse out +	5	CH-2, CCW pulse out -
6R		6	
7R		7	
8R		8	
9R	CH-1, ext. clock	9	
10R	CH-1, ext. rate control	10	
11R	CH-2, ext. clock	11	
12R	CH-2, ext. rate control	12	
13R	CH-2, control out	13	
14R	CH-1, control out	14	
15R	CH-1, CW limit in	15	Chassis common
16R	CH-1, CCW limit in	16	
17R	CH-2, CW limit in	17	
18R	CH-2, CCW limit in	18	Chassis common

Pulse rates factory set
for 100 pps.

Pulse output, 5 volts
into 390 ohms
transformer coupled.

Fig. 3. Module 3360.

FORTRAN V003A		20-DEC-72	PAGE 1
C		'AMUL' : MULTIPLEXING INTO A DVM	
C			
C		F(1)=F COMMAND, C=1, N=SLOT, A=A COMMAND	
C		F(2)=Q RESPONSE, F(3)=DATA LOW 16 BITS, F(4)=DATA HIGH 8 BITS	
C			
0001		SUBROUTINE AMUL	
0002		IMPLICIT INTEGER(A-Y)	
0003		COMMON F(4),N,A	
C			
C		THIS IS THE WRITE COMMAND	
C			
0004		WRITE(6,1)	
0005	1	FORMAT(' TYPE IN NB. OF ANALOG MUL. (FORMAT 12)')//	
0006		READ(6,2)F(3)	
0007	2	FORMAT(12)	
0008		N=2	
0009		A=0	
0010		F(1)=16	
0011		CALL MBDFNA(F,N,A)	
0012		F(2)=0	
0013		F(3)=0	
0014		F(4)=0	
0015		RETURN	
0016		END	
BLOCK		LENGTH	
AMUL		00158	(000474)*
***.		00006	(000014)

F(0)A(0): This command reads the status of the address register (a number between 1 and 15). If the number is 0, the module is cleared.

Following is a general description of the 3530 Model CAMAC 15-Channel Relay Multiplexer with diagram (Fig. 4).

CAMAC 15-Channel Relay Multiplexer Model 3530

General Description

The model 3530 is a double-width module that contains 15 relays for switching one of the 15 differential signals onto an output. There is a 4-bit address register that can be read, written, and incremented by CAMAC command. The address register can also be incremented or decremented manually. Interlocking is provided to prevent two inputs from being selected at the same time and all switching is "break" before "make." The multiplexer can be expanded by bussing the outputs of a number of 3530's together. Two output connectors are provided to facilitate bussing. If the address "zero" is selected, all inputs are disconnected. A priority chain is provided for multiple 3530's to prevent more than one circuit in the system from being selected. The address of the selected channel is available on a printed circuit connector above the dataway connector as is a "busy" pulse which is high during switching.

Input

The maximum input current is 1A with the signal power limited to 10 watts. The resistance from input to output is less than 50 mohm. Switching is accomplished with mercury wetted relays selected for low thermal offsets. Circuitry is included to minimize coil dissipation and thus further reduce thermal offsets. Thermal offsets are typically less than 1 μ V and guaranteed less than 10 μ V.

Front Panel

A jack-screw is provided which functions both in insertion and in extraction of the module. There is an N light which flashes whenever this module is addressed. There are 17 LEMO, RA0302 connectors for the inputs and outputs. Four LED indicators are provided to indicate the address of the selected channel. The address register is incremented by depressing the "INC" push button and decremented by

depressing the "DEC" push button. Two LEMO "00" connectors are provided for the priority chain. An indicator is provided to indicate that this module is inhibited.

Command	Action
F(0)A(0)	Gates the address register onto the Dataway.
F(1)A(15)	Gates the module number (3530 = 6712 ₈) on the Dataway.
F(16)A(0)S1	Writes the address register from the Dataway.
F(25)A(0)S1	Increments the address register.
(Z + C)S2	Clears the address register.

The module returns X = 1 for all valid commands and 0 otherwise. The module returns Q = 1 for all valid commands except "write" and "increment" when the module is inhibited by the priority chain.

This units uses mercury wetted relays for signal switching. These relays, and therefore the module, must be operated in a vertical position. If the module has been out of the crate, contact bridging may occur. To avoid shorting inputs together, the module should be placed in the crate for a minimum of one minute and then cycled through all addresses prior to connecting the inputs.

C. Analog-to-Digital Converter (Jorway Model 30)

Specification sheet:

Data Command (all fully decoded)

NFOAO	Read, places data from the storage register onto Read lines, R1-R12. Inhibits updating of storage register. Generate Q response.
NFOAOS2	Resets LAM flip-flop.
NF8AO	Tests LAM flip-flop, generates response on Q line (can be disabled).
NF10AO	Same as F8 however at S2 it resets the LAM flip-flop.
NF24AOS2	Resets Enable-Disable flip-flop which disables L, and the Q response to F8 and F10.
NF26AOS2	Sets Enable-Disable flip-flop which enables L, and the Q response to F8 and F10.
NF28AOS1	Initiates a conversion cycle.

This analog-to-digital converter converts an analog signal of ± 5 V, ± 10 V, or 0 to 10V (internally selectable) into a 12-bit digital number:

Kinetic Systems KS 3530
15-Channel Relay Multiplexer

Power Requirements

+6	500	ma	-6		ma
+12		ma	-12		ma
+24	100	ma	-24		ma

I/O Connector

1R		1	
2R		2	
3R	Address 0	3	
4R	Address 1	4	
5R	Address 2	5	
6R	Address 4	6	
7R	Address 0	7	
8R	Address 1	8	
9R	Address 2	9	
10R	Address 4	10	
11R		11	
12R		12	
13R		13	
14R		14	
15R		15	
16R		16	
17R		17	
18R		18	

Viewed from the rear

Fig. 4. Module 3530.

$\pm 5V \rightarrow -2048$ to 2047 channels

$\pm 10V \rightarrow -2048$ to 2047 channels

0 to 10V $\rightarrow$ 0 to 4095 channels.

F(0)A(0): Gates the digital data onto the lower 12 bits of the read lines. (R1 - R12.) This command reads the 12-bit digital number.

F(8)A(0): Tests LAM if LAM is set $\rightarrow Q = 1$
if LAM is cleared $\rightarrow Q = 0$.

F(28)A(0): Initiates an analog-to-digital conversion. A simple way of using this A/D converter is the following:

---F(28)A(0): analog-to-digital conversion

---F(0)A(0): read digital data.

Following is a general description of the Jorway Model 30 Analog-to-Digital Converter and its specifications.

General Description

The Jorway Model 30 Analog-to-Digital Converter is a double-width CAMAC module conforming to EUR 4100e. This high performance 12-bit analog-to-digital converter features a 100 Mohm input

impedance, 20 μ sec conversion speed and high accuracy.

There is provision for three input voltage ranges which can be internally selected. A conversion may be initiated either internally with Dataway command F28, or externally. A status output signal is provided to indicate when a conversion is in process. A buffer storage is provided to simplify system operation. Normally, at the end of conversion the digital information is strobed into this storage register. Logic is provided, however, to inhibit this update of the register if a read operation is being performed. This will insure that only stable data is read onto the Dataway. In this case, when the read operation is complete, the register will be updated, the status output will go to zero and a complete pulse will be generated. Whenever data are strobed into the register, a LAM flip-flop is set to indicate this to the Dataway controller.

An N light is provided for visual indication of when the module is addressed.

Specifications

Inputs

Analog

Resolution 12 binary bits
Accuracy $\pm 1/2$ LSB
Conversion time 20 μ sec
Input Voltage Ranges $\pm 5V$, $\pm 10V$, 0 to $+10V$
Internally Selectable
Input Impedance 100 Mohms, min.

Initiate Command Logic "1" pulse 50 nsec wide will initiate an analog-to-digital conversion.

Outputs

Status

A logic "1" level indicates the time from the beginning of conversion to when the new data are placed in buffer storage.

Complete

A logic "1" pulse to indicate when the conversion is complete and the new data stored.

Data Commands (all fully decoded)

N·FO·AO Read, places data from the storage register onto Read lines, R1-R-12. Inhibits updating of storage register. Generate Q response.

N·FO·AO·S2 Resets LAM flip-flop.

N·F8·AO Tests LAM flip-flop, generates response on Q line (can be disabled).

N·F10·AO Same as F8 however at S2 it resets the LAM flip-flop.

N·F24·AO·S2 Resets Enable-Disable flip-flop which disables L, and the Q response to F8 and F10.

N·F26·AO·S2 Sets Enable-Disable flip-flop which enables L, and the Q response to F8 and F10.

N·F28·AO·S1 Initiates a conversion cycle.

Dataway Controls

Z·S2 Resets Enable-Disable flip-flop which disables L, and Q response to F8 and F10. Resets LAM flip-flop and 12-bit buffer register.

B Suppresses L signal.

L An L signal is generated whenever the LAM flip-flop is set and the module is enabled.

Q

A "Q" signal is always generated in response to a read function (FO). A "Q" signal will also be generated in response to commands F8 and F10 provided the LAM flip-flop is set and the module is enabled.

Indicators

An "N" light is provided to visually indicate the module is addressed. The N signal is integrated so that it will respond to a pulse.

Power Requirements

+6V 575 ma nominal
+24V 30 ma nominal
-24V 45 ma nominal.

Temperature Range

0°C to 60°C.

Size

Double CAMAC module with protective side shields. Analog connector LEMO RA0302 or equivalent all other connectors are LEMO RA00250 or equivalent.

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4. CAMAC Bulletin. Some issues of this journal include a CAMAC product guide.

APPENDIX A HOMEWORK

1. Please give the octal number (without F8) of the following CAMAC FCNA commands:

F(24) C(3) N(30) A(9)
F(26) C(2) N(30) A(10)
F(16) C(1) N(12) A(0)
F(24) C(1) N(11) A(1)
F(27) C(1) N(5) A(7)

2. You issue a F(1) A(0) command to a Kinetic Systems KS 3360 stepping motor driver and you get the response 231 octal. What does it mean?

3. You have a CAMAC crate (C = 1) with the following modules:

KS 3360 SMC	KS 3420 input gate	LRS 2550 Scaler	KS 3530 analog multi- plexer	LRS 2248 octal ADC	Jorway 30 A/D converter				
1	2	3	4	5	6	7	8	9	...

Please give the CAMAC commands for the following tasks:

- increment the scaler by 2
- read channel 33 of the 64-channel ADS (5-D system) connected with the KS 3420 input gate
- convert an analog signal and readout the result with the Jorway 30 A/D converter
- clear all 8 channels of the LRS 2248 ADC
- send 200 up pulses to stepping motor 2
- switch to input 13 in analog multiplexer

4. What is wrong with the following FCNA commands?

F(0) C(8) N(12) A(7)
F(16) C(3) N(0) A(0)
F(16) C(1) N(3) A(16)
F(32) C(1) N(13) A(3)
F(9) C(1) N(26) A(0)

5. You issue the command F(0) A(0) to a CAMAC 15-channel Reed Relay Multiplexer (Kinetic Systems KS 3530 or Yale). You get the answer 15 decimal. After that you give the command F(25) A(0). What is the status of the address register and what happened in general?

6. Homework on the EPICS PDP-11/45 (EPICS counting house, Area A)

- Login
- RU FCNA [6,27]
FCNA is a general purpose program to test CAMAC modules. An example of an output is given in Fig. A-1.
- Type in all possible commands for KS 3420 input gate, a KS 3530 analog multiplexer and a LRS 2550B scaler according to the following specifications. Try to understand what is going on.

Kinetic Systems KS 3420 Input Gate

Command	Action
F(0)·A(X) ¹	Gates external "group one" data onto Dataway and produces output strobe at S2.
F(1)·A(X)	Gates external "group two" data onto Dataway and produces output strobe at S2.
F(2)·A(X)	Gates external "group three" data onto Dataway and produces output strobe at S2.
F(3)·A(X)	Gates external "group four" data onto Dataway and produces output strobe at S2.
F(6)·A(0)	Gates module identifying number onto Dataway.
F(8)·A(0)	Returns Q if LAM is set.
F(10)·A(0)·S1	Clears LAM.
F(14)·A(0)·S1	Sets LAM.
F(24)·A(0)·S1	Prevents setting of the LAM flip-flop.
F(25)·A(0)·S1	Produces "Execute" output strobe.
F(26)·A(0)·S1	Allows setting of the LAM flip-flop.
F(27)·A(0)·S1	Produces "Test Status" output strobe.
C·S2	Clears LAM.
Z·S2	Clears LAM and prevents LAM from being set. ²

NOTES:

- The subaddress (X) may range from 0 through 15.
- May be changed via strapping option to allow LAM to be set.

LO 105.105

DATE: - 10-JUN-73

TIME: - 17:34:20

IRU FCN(6.27)

TYPE IN CRATE NO. (FORMAT I1)

1

TYPE IN FNA COMMAND PLEASE (FORMAT 312)

240701

CAMAC F COMMAND = F24

CAMAC N COMMAND = N 7

CAMAC A COMMAND = A 1

Q - RESPONSE = 1

DATA = 0 OCTAL 0 DECIMAL

TYPE IN FNA COMMAND PLEASE (FORMAT 312)

1615

TYPE IN DATA (IS DECIMAL), IF NO DATA TYPE

00255

ZERO

CAMAC F COMMAND = F16

CAMAC N COMMAND = N15

CAMAC A COMMAND = A 0

Q - RESPONSE = 1

DATA = 377 OCTAL 255 DECIMAL

TYPE IN FNA COMMAND PLEASE (FORMAT 312)

0015

CAMAC F COMMAND = F 0

CAMAC N COMMAND = N15

CAMAC A COMMAND = A 0

Q - RESPONSE = 1

DATA = 377 OCTAL 255 DECIMAL

TYPE IN FNA COMMAND PLEASE (FORMAT 312)

0915

CAMAC F COMMAND = F 9

CAMAC N COMMAND = N15

CAMAC A COMMAND = A 0

Q - RESPONSE = 1

DATA = 0 OCTAL 0 DECIMAL

TYPE IN FNA COMMAND PLEASE (FORMAT 312)

2502

CAMAC F COMMAND = F25

CAMAC N COMMAND = N 2

CAMAC A COMMAND = A 0

Q - RESPONSE = 1

DATA = 0 OCTAL 0 DECIMAL

TYPE IN FNA COMMAND PLEASE (FORMAT 312)

^C

.KI

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\$

LeCroy Research Systems Corporation Model 2550
Quad 100 MHz Scaler

The LRS Model 2550 Quad 100 MHz Scaler is a single-width CAMAC module containing four 24 (or 16) bit scalers. Front panel LEMO or BNC connectors are used for the signal and fast inhibit inputs. Also provided are a common "Clear" push button which resets all channels in parallel and a CAMAC "Inhibit Disable" switch which allows the CAMAC "1" command to be disregarded by all channels. IC sockets are used throughout. Requires approximately 6 W of ± 6 volt power.

Two bridged high impedance ($> 1K \Omega$) inputs on the front panel provide a common fast inhibit. An impedance of 50Ω may be obtained by simply terminating one of the inhibit inputs into 50Ω . This fast inhibit can be used as an overlap inhibit (Scaling Mode) or as a clock input when dc gating the signal inputs (Digitizing Mode).

The LRS Model 2550 responds to the CAMAC function codes F(0), F(9), and F(25). F(0) ("Read") and F(9) ("Clear") commands may be used to control individual scaler channels. F(25) is a test mode used to simultaneously test all counting registers in one module. Each counting register increments by 1 at the end of S2. The inputs are automatically inhibited by F(25), so that any input pulses are rejected during scaler testing. This feature is not affected by the "Inhibit Disable" switch.

The Model 2550 is a member of the LRS Series 2000, a line of nuclear-oriented instruments designed according to CAMAC standards.

Fig. A-1.

APPENDIX B
HOMEWORK ANSWERS

1. 103751
122752
101300
101261
131127

4. a. C(8) too big
b. N(0) is wrong, N should be ≥ 1
c. A(16) too big
d. F(32) too big
e. N(26) too big for a F(9) which is a clear

2. 231 octal = 1 0 0 1 1 0 0 1 binary

5. The status of the address register is zero;
the module has been cleared.

It means that the module is ready for a command.

3. a. F(25) C(1) N(3) A(0) twice
b. F(2) C(1) N(2) A(0) twice → start convert
→ readout
c. F(28) C(1) N(8) A(0)
F(0) C(1) N(8) A(0)
d. F(9) C(1) N(6) A(0) - A(3)
e. F(16) C(1) N(1) A(1) data 200 decimal
f. F(16) C(1) N(5) A(0) data 13 decimal